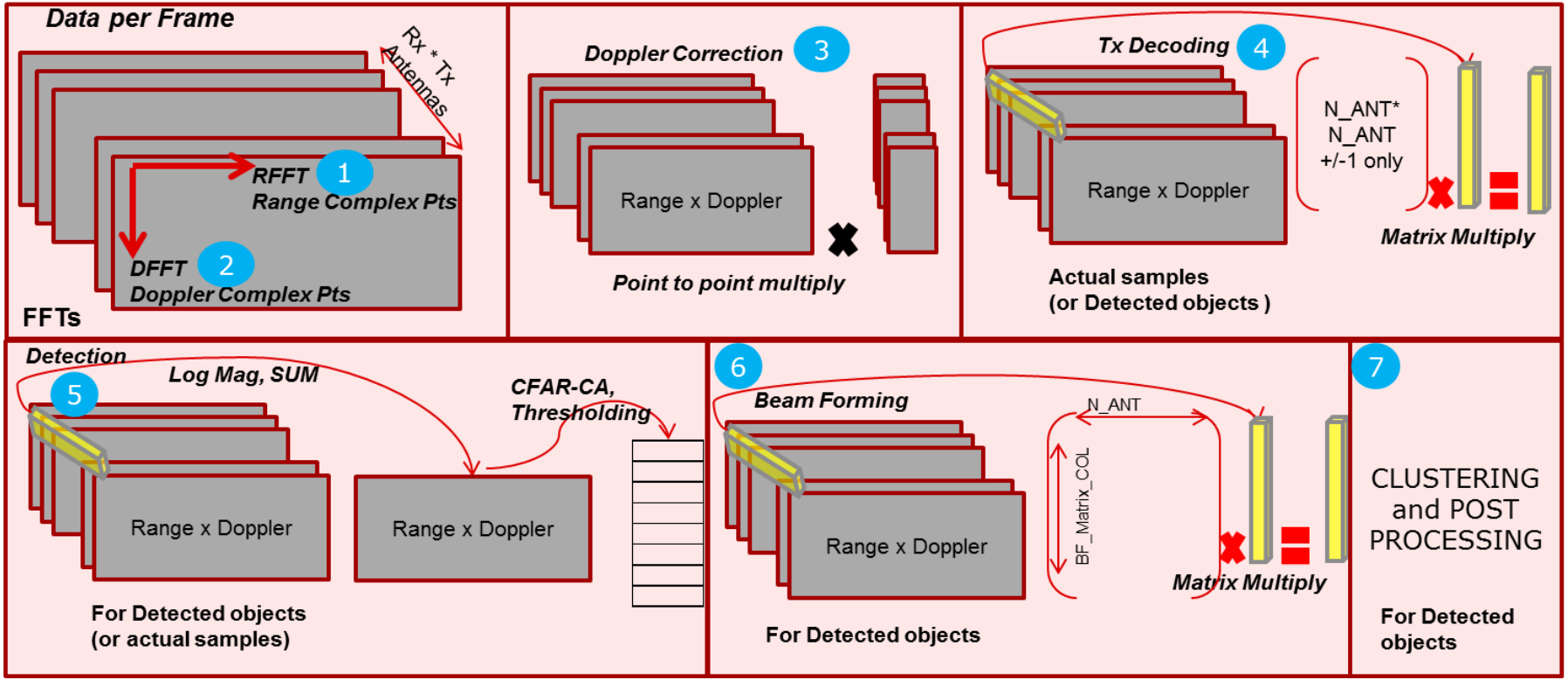
Introduction to
Processor SDK Radar – Part 2

Agenda

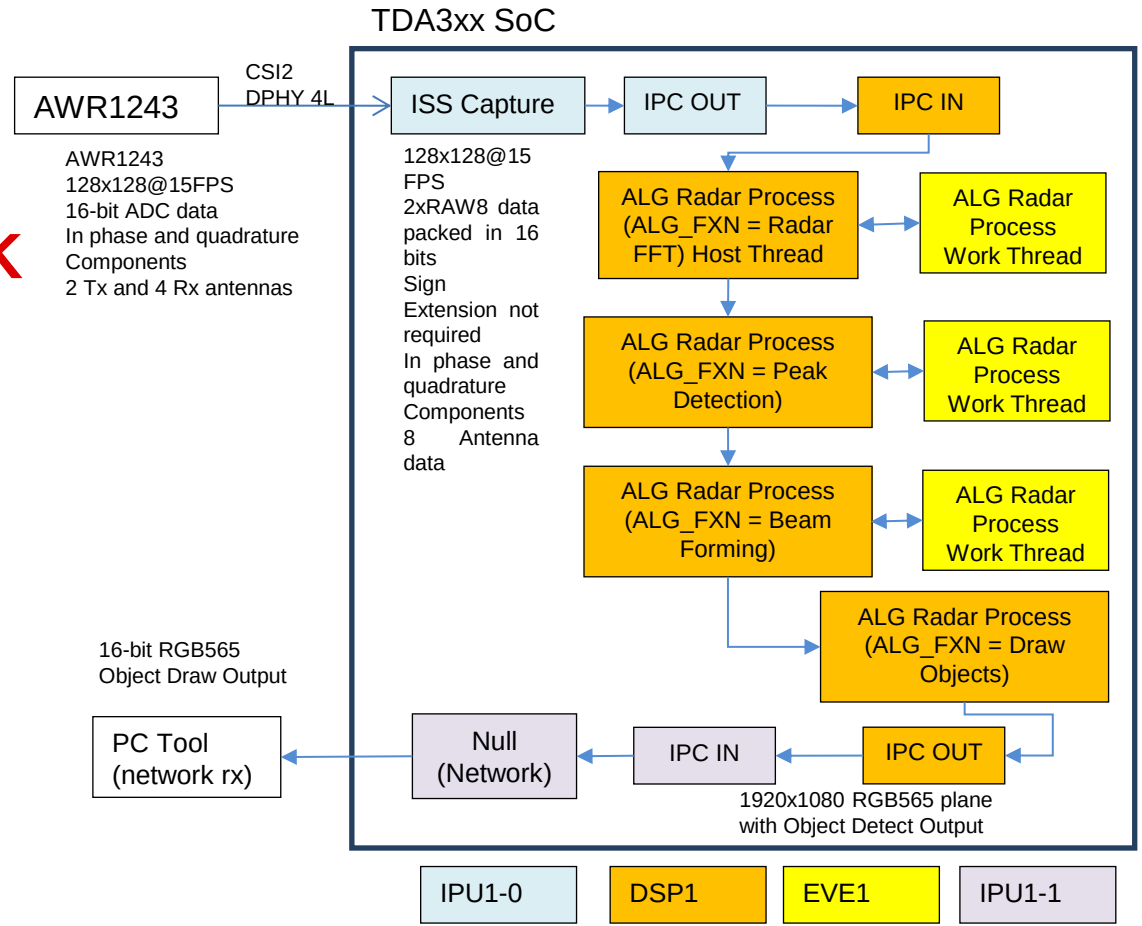
- What is Processor SDK Radar?
  - Radar SDK Software Stack
- Processor SDK Radar Processing Chain
  - Algorithm Blocks (FFT, Peak Detection, Beam Forming)
  - Cascade Radar Data Processing Chain
- Getting Started with Processor SDK Radar

Radar Data Processing flow

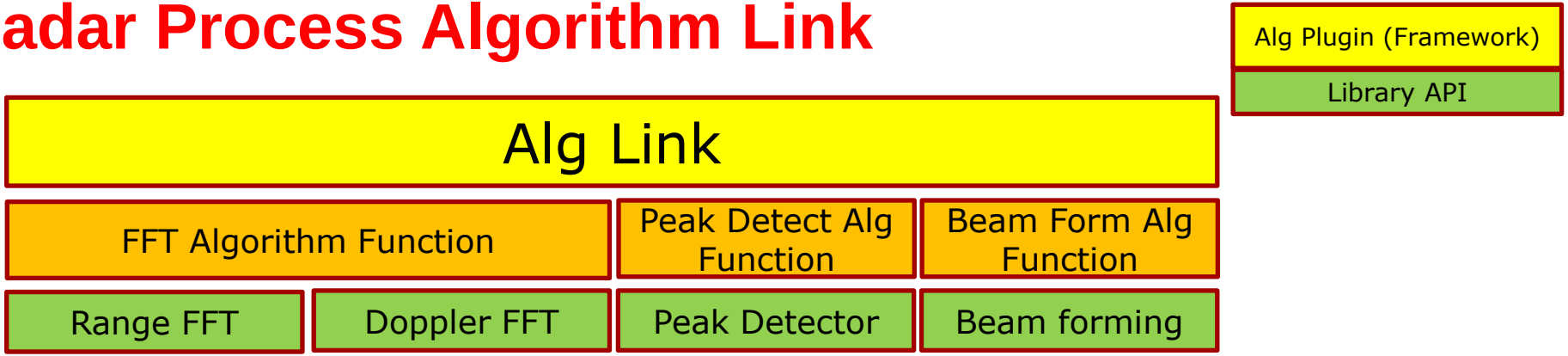


Single Chip AWR1243 based Object Detection using Processor SDK – Radar on TDA3xx

- This usecase demonstrates the EVE object detection computation.
- The data flow shows a radar data capture for a configuration of 128 samples per chirp and 128 chirps per frame @ 15 FPS for 4 Rx Antenna and 2 Tx Antenna.



Radar Process Algorithm Link



- A single radar algorithm link exposes the FFT, Peak Detection and Beam forming algorithm modules.
- This is achieved by the concept of “Algorithm Function”.
- The Algorithm link takes care of buffer management for single input and single output queue.
- Processor SDK Radar Users can develop their own Radar Processing algorithms and use the algorithm plugin and algorithm function infrastructure to create their own Radar processing

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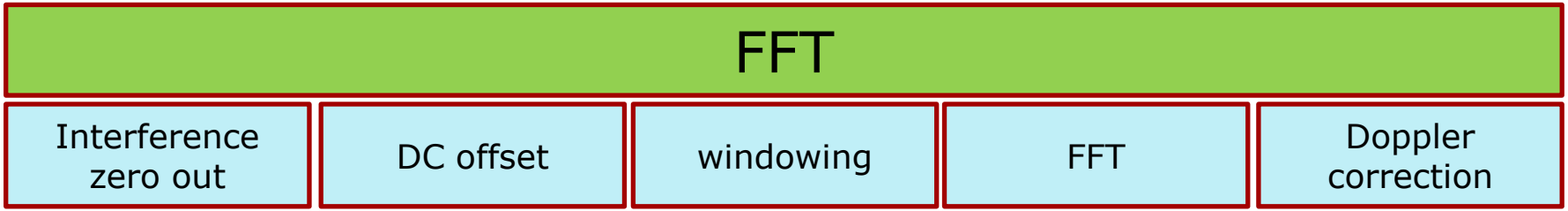
Algorithm Modules (FFT)

Library API

Sub-function within API



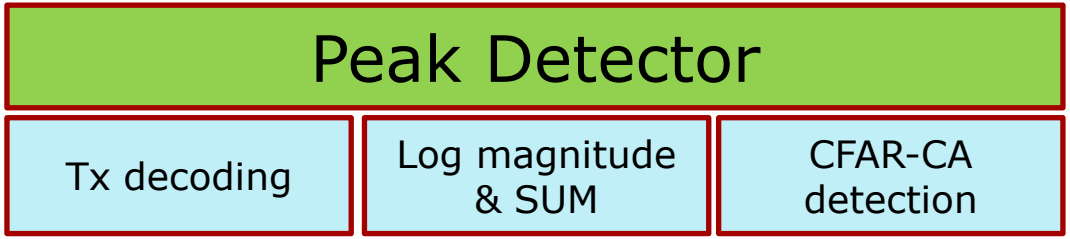
- **Kernels**
  - **FFT:** 64, 128, 256, 512, 1024 point FFT kernels (16-bit fixed point with shift control at each stage, overflow detection)
  - Interference zero out
  - DC offset
  - Windowing
  - Doppler correction

- **Applet**
  - XDAIS based interface
  - Control to enable/disable interference zero out, DC offset, windowing and Doppler correction
  - DMA based data flow using internal memories for data processing

Algorithm Modules (Peak Detector)

Library API

Sub-function within API



- **Kernels**
  - Tx decoding
  - Log magnitude, sum
  - CFAR-CA detection

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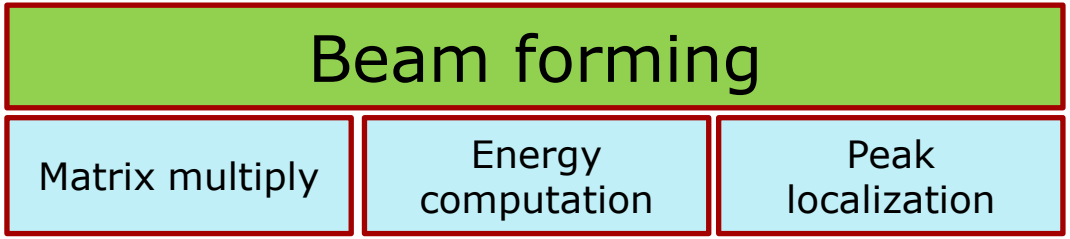
- **Applet**
  - XDAIS based interface
  - Control to enable/disable Tx decoding
  - Control for energy computation for detection to be sum of log magnitude vs direct energy sum
  - Control for cell sum direction (range vs doppler)
  - DMA based data flow using internal memories for data processing

Algorithm Modules (Beam forming)

Library API

Sub-function within API



- **Kernels**
  - Matrix multiply
  - Energy computation
  - Peak Localization

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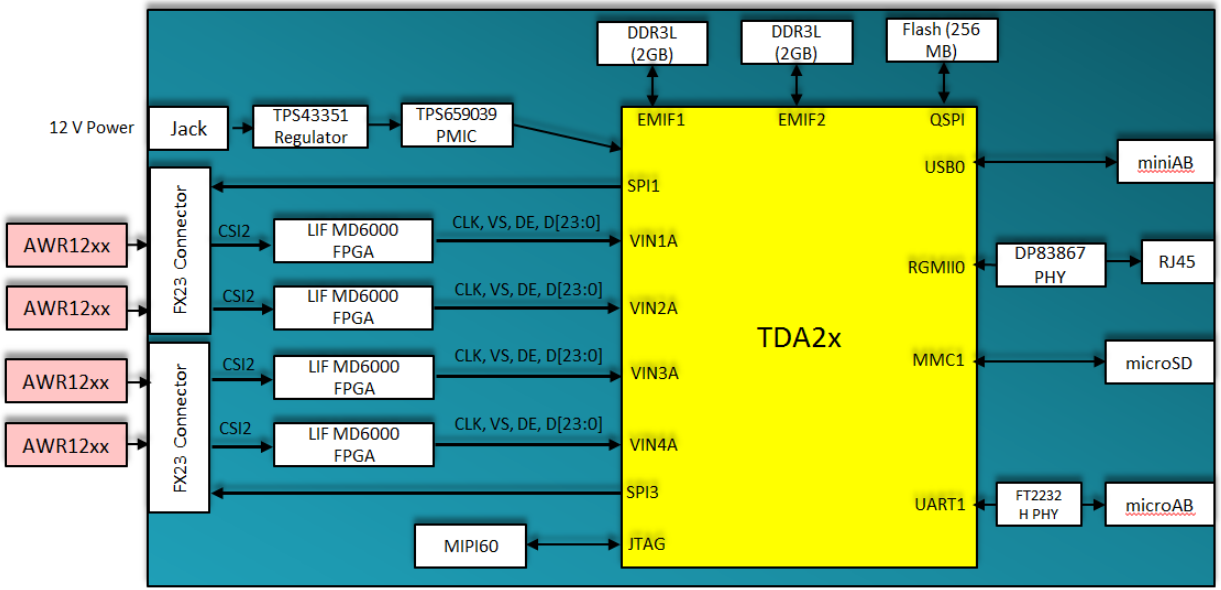
- **Applet**
  - XDAIS based interface
  - DMA based data flow using internal memories for data processing

System architecture: Cascade FMCW radars

MIMO cascade with synchronous radars

2 PCB system, Up-to 192 radar virtual array combinations
Radar front-end few inches from processors



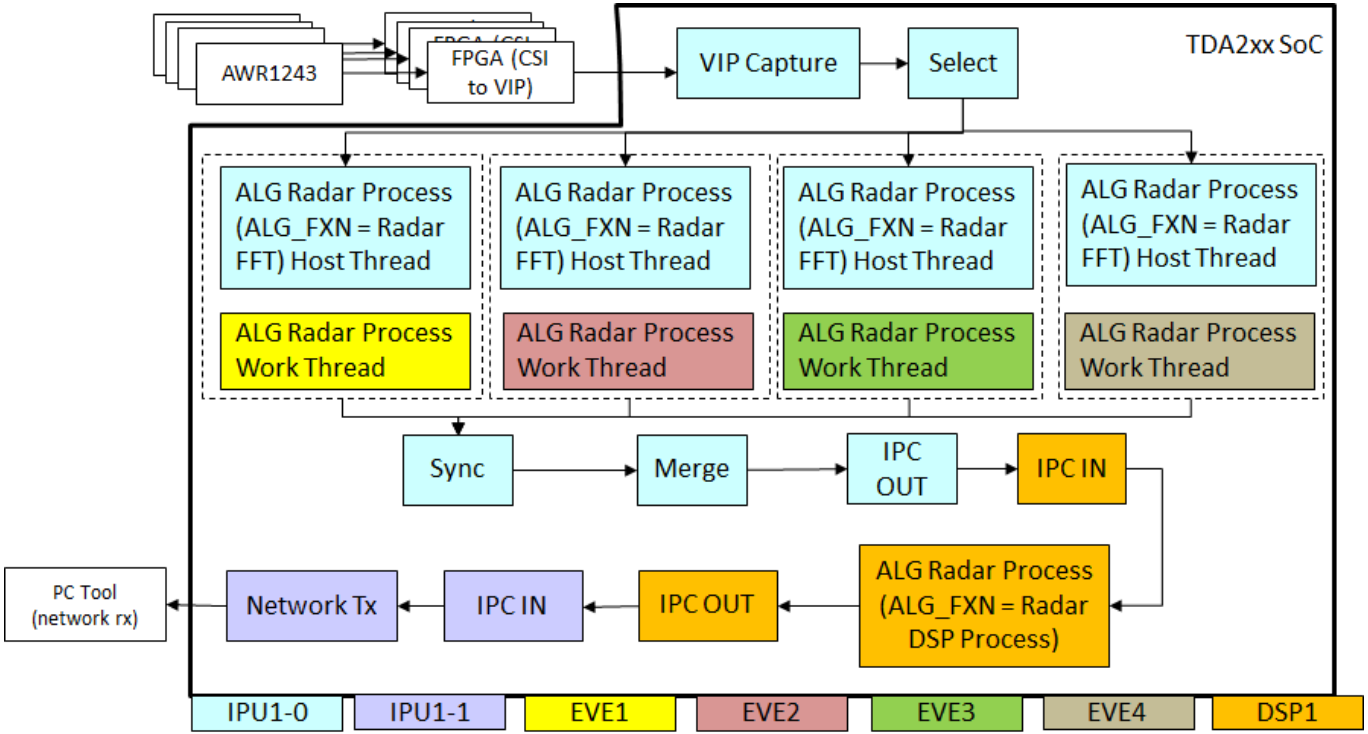
AWR1243 mmWave Sensors — Texas Instruments

Highly configurable frequency modulated continuous wave radio frequency transceivers with 76-81 GHz band which support up to 3 transmit (Tx) and 4 receive (Rx) chains

TDA2xx — Texas Instruments

Highly optimized and scalable family of TI ADAS devices.
Mix of TI's fixed and floating-point TMS320C66x digital signal processor (DSP), Vision/Vector AccelerationPac (EVE), ARM Cortex-A15 MPCore™ and dual-Cortex-M4 processors.

4-Chip Cascade Radar Data Flow



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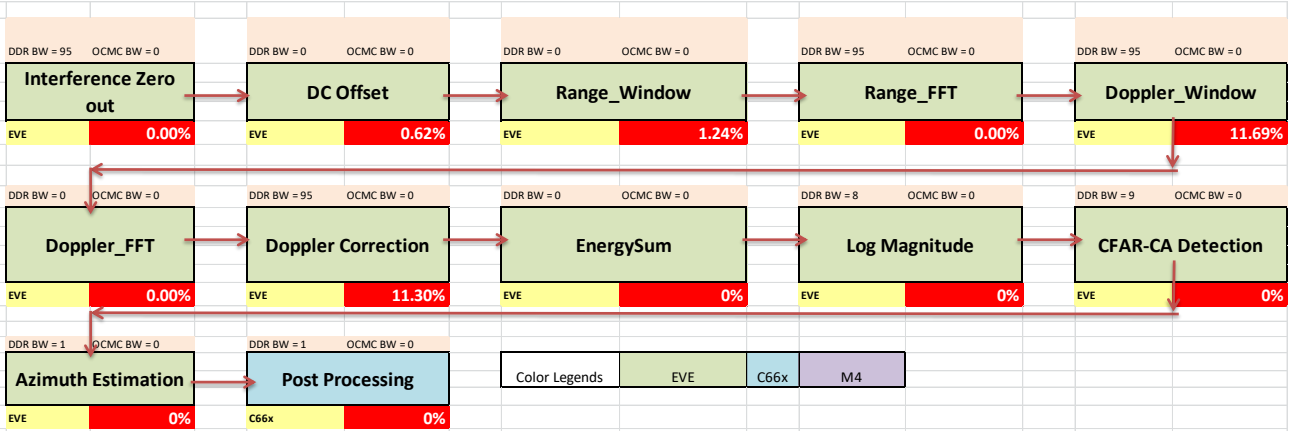
Radar System Planner

- Excel Based Utility to analyze the Radar processing requirements on TDA devices.

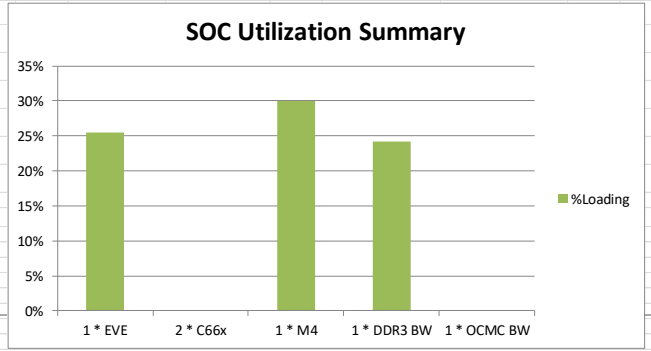
Configurations	
Range Dimension	1024
Doppler Dimension (per Tx)	128
Rx	4
Tx	3
Frames/sec	15
Multiplexing across Tx	Yes
Detection Method	CFAR-CA
Detection/dwells	20
Number of Angles (Angle resolution)	120
System Overhead	5%
Virtual Anteenas	12
#Raw samples/dwell (cube size)	1572864
Plane size (range * doppler)	131072
#Object samples/dwell	240
BeamForming Matrix Column	120
Sample size (in bytes)	4



SOC Utilization Summary			
Processing/Memory subsystem	Freq(MHz)	#cores	%Loading
EVE	500	1	25%
C66x	500	2	0%
M4	212	1	30%
DDR3 BW	532	1	24%
OCMC BW	266	1	0%

OCMC Memeory Size (KB)	0

Cells to control - user input
Derived (computed) information



Looking for Support?

- Use TI E2E forum to get additional support
- Kindly post queries/feedback on below forum
  - https://e2e.ti.com/support/arm/automotive_processors

Thank you