SN65DSI83/84/85- Single DSI Input to Single-Link LVDS

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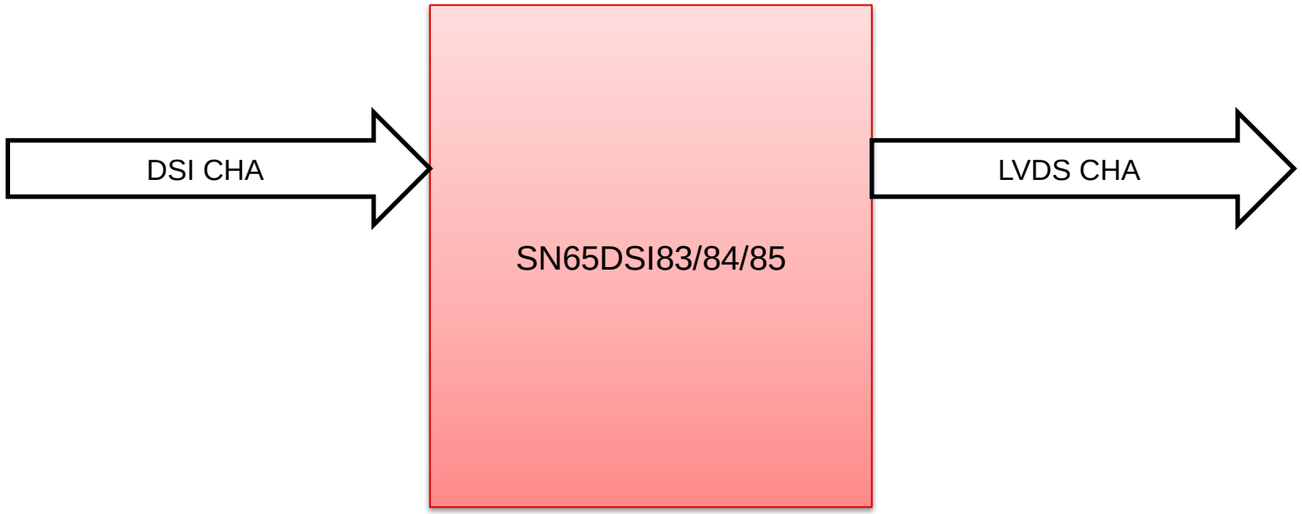
Single to single

- The SN65DSI83, DSI84, and DSI85 can all be used for single channel DSI to single channel LVDS, but we will use the SN65DSI83 for this demo



Single to single

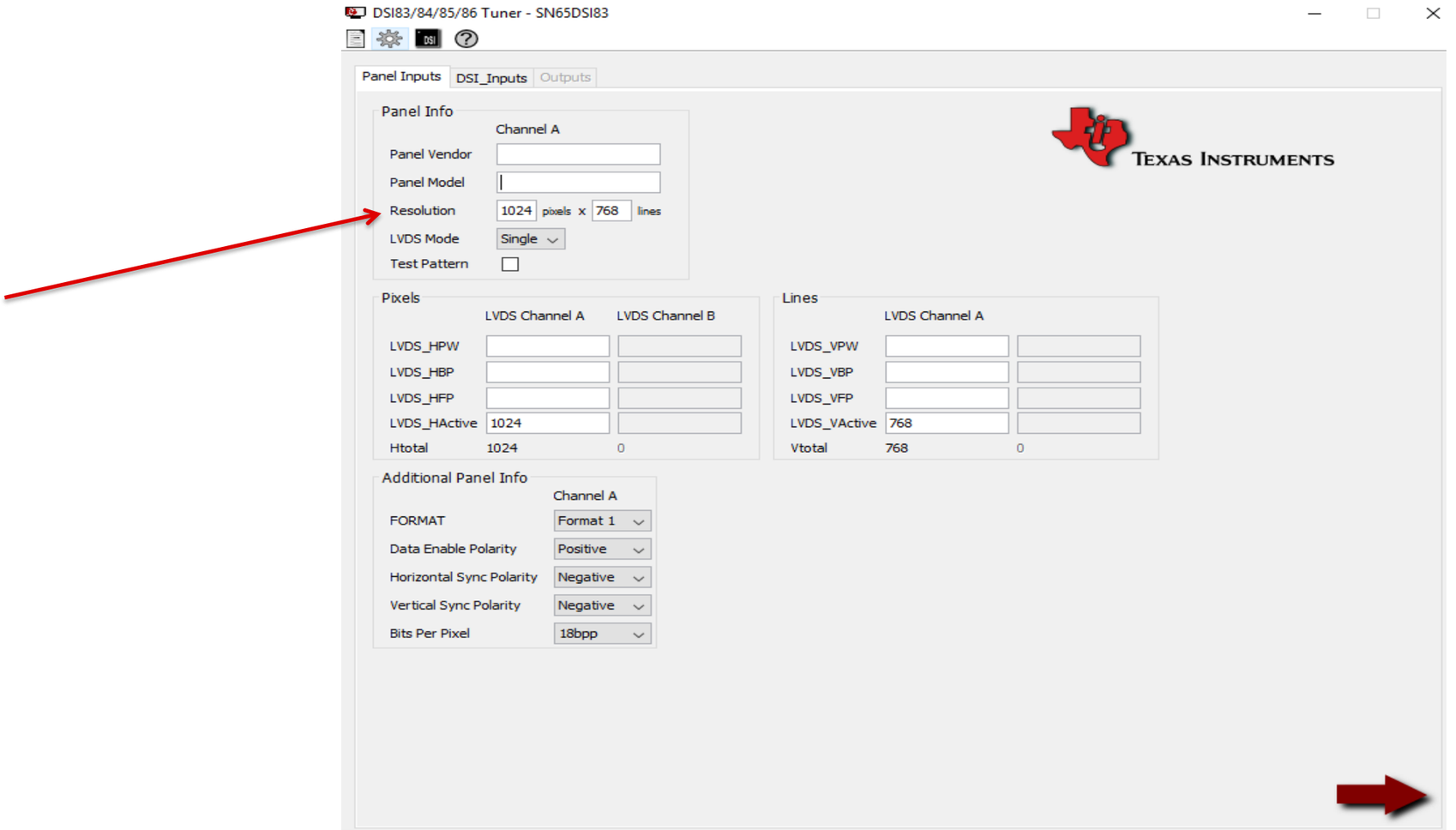
- From display datasheet, identify:
- Resolution:

Display area	210.432 (H) × 157.824 (V) mm
Diagonal size of display	26cm (10.4 inches)
Drive system	a-Si TFT active matrix
Display color	16,777,216 colors (At 8-bit input, FRC terminal= High) 262,144 colors (At 6-bit input, FRC terminal= Low or Open)
Pixel	1,024 (H) × 768 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe

- This is a 1024 x 768 panel

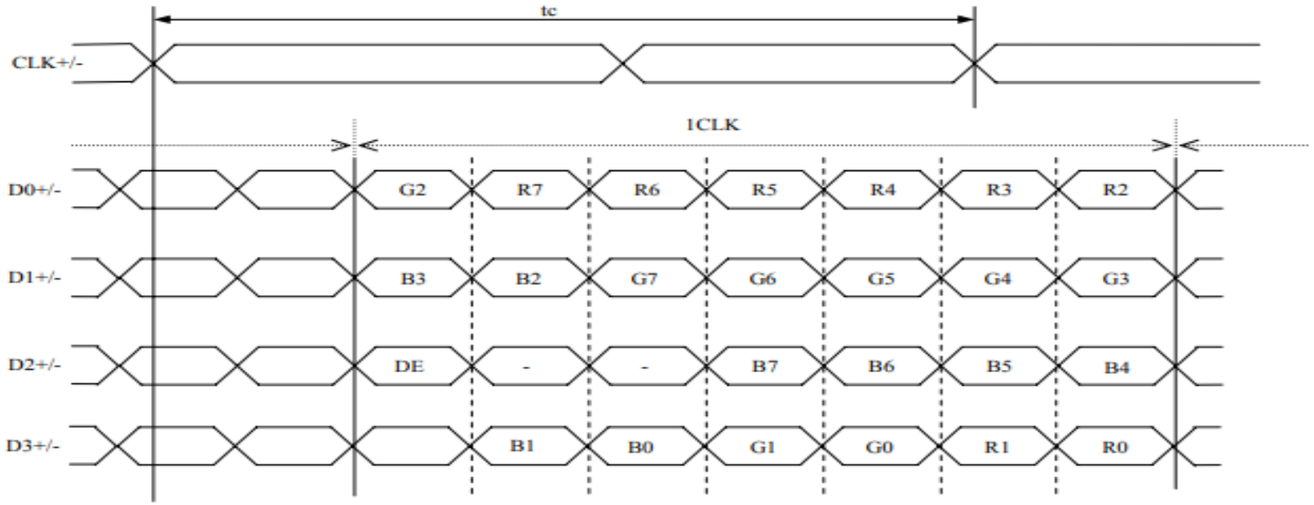
Single to single

- Fill out corresponding section in tool:



Single to single

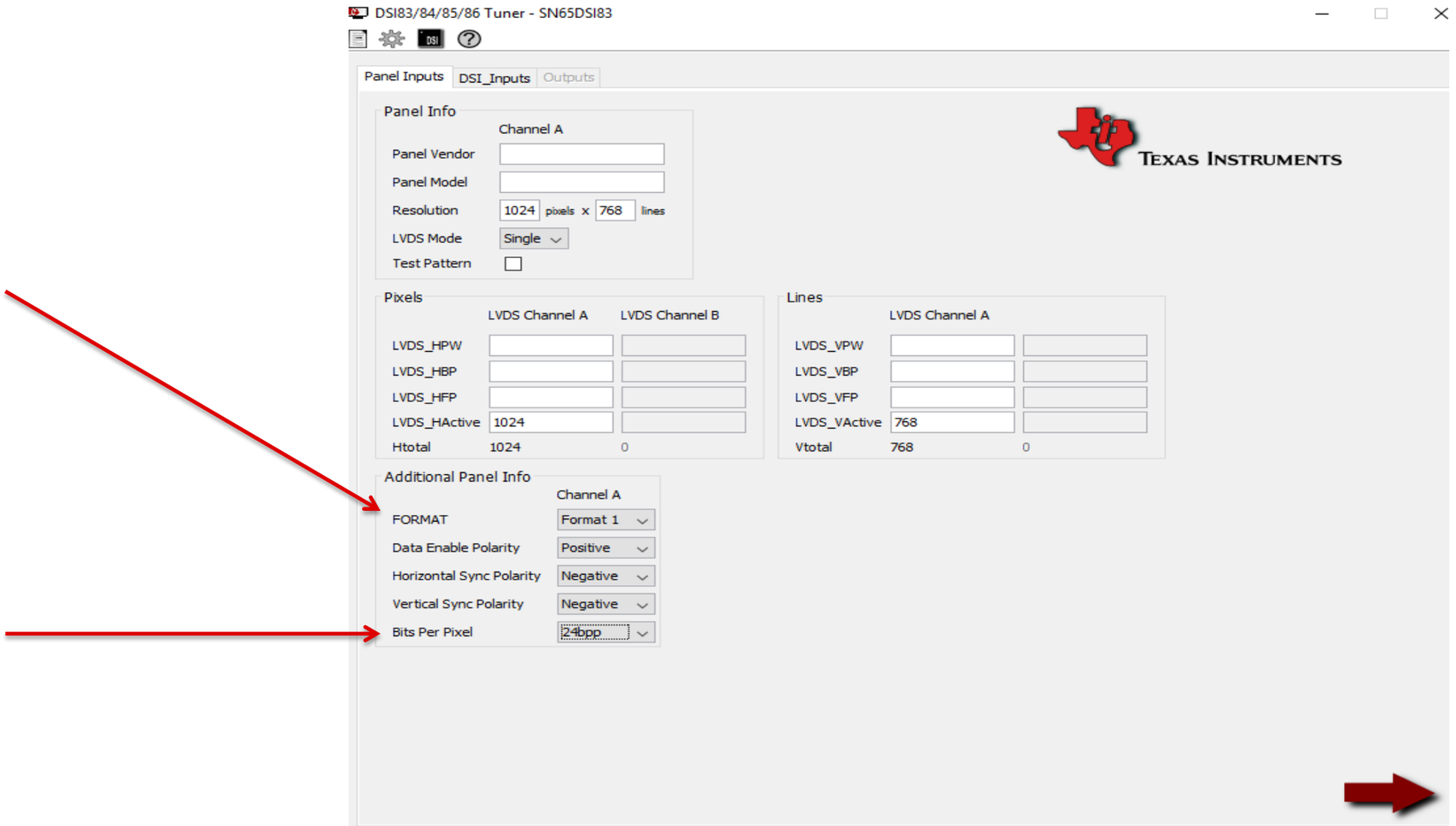
- From display datasheet, identify:
- Mapping format:



- This is Format 1 (JEIDA), 24bpp

Single to single

- Fill out corresponding section in tool:



Single to single

- From display datasheet, identify:
- Timing Parameters:

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	60.0	65.0	68.0	MHz	15.385ns (typ.)
	Duty		-	-			-	-
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-	-			ns	-
		Hold time					ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycle	th	19.67	20.676	22.4	µs	48.363kHz (typ.)
				-	1,344	-	CLK	
		Display period	thd	-	1,024	-	CLK	
	Vertical (One frame)	Cycle	tv	13.3	16.666	18.5	ms	60.0Hz (typ.)
				780	806	-	H	
		Display period	tvd	-	768	-	H	
	CLK-DE	Setup time	-	-			ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	

Total Horizontal Pixels

Active Horizontal Pixels

Total Vertical Pixels

Active Vertical Pixels

- This particular datasheet states the total display area and the active display area

Single to single

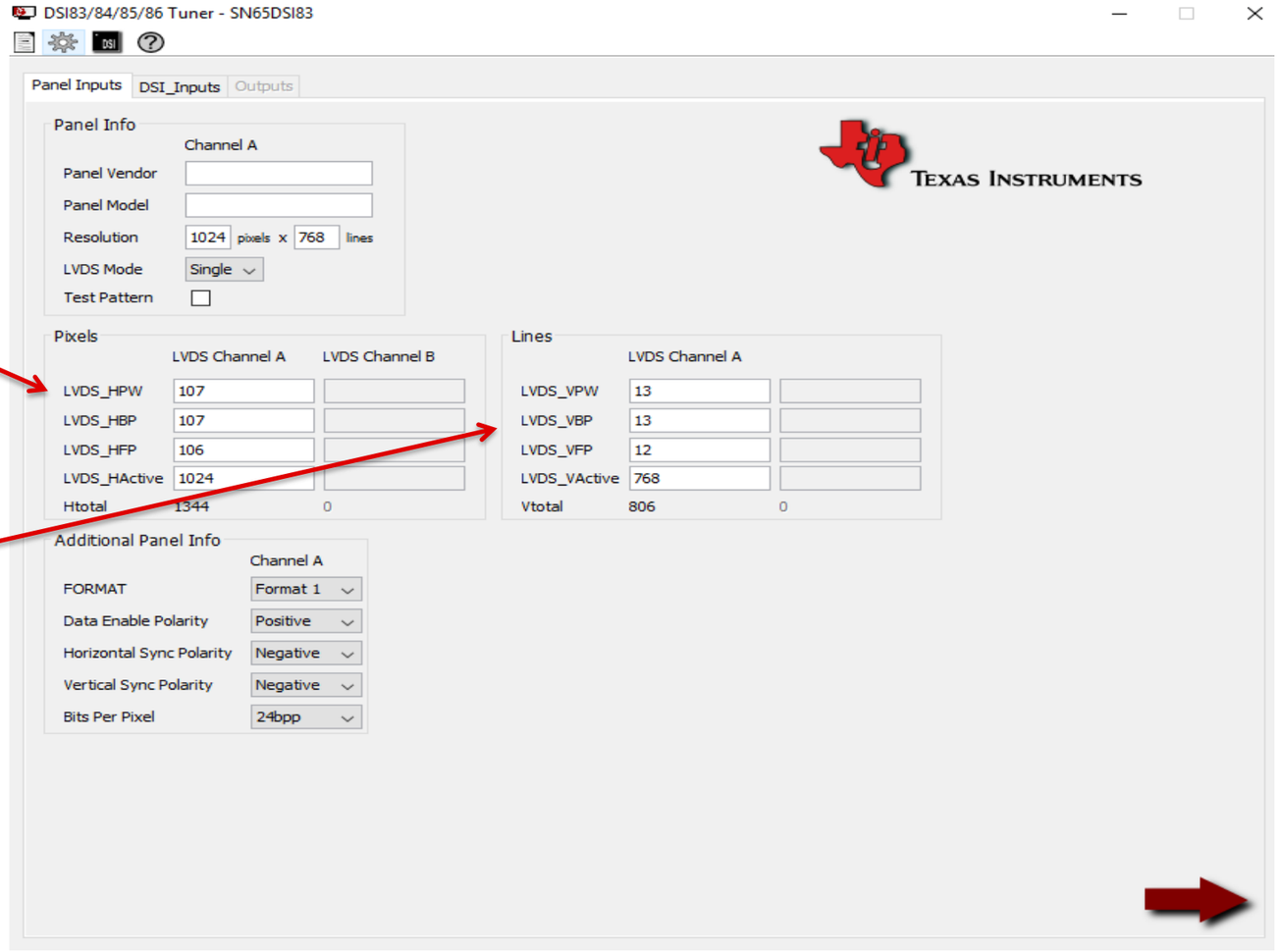
- From display datasheet, identify:
- Timing Parameters:

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	60.0	65.0	68.0	MHz	15.385ns (typ.)
	Duty		-	-			-	-
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-	-			ns	-
		Hold time					ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycle	th	19.67	20.676	22.4	µs	48.363kHz (typ.)
				-	1,344	-	CLK	
		Display period	thd	1,024			CLK	
	Vertical (One frame)	Cycle	tv	13.3	16.666	18.5	ms	60.0Hz (typ.)
				780	806	-	H	
		Display period	tvd	768			H	
	CLK-DE	Setup time	-	-			ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	

- Horizontal Blanking = 1344 - 1024 = 320
- Vertical Blanking = 806 – 768 = 38

Single to single

- Fill out corresponding section in tool:
- Horizontal blanking (320) is divided among HPW, HBP, and HFP
- Vertical blanking (38) is divided among VPW, VBP, and VFP

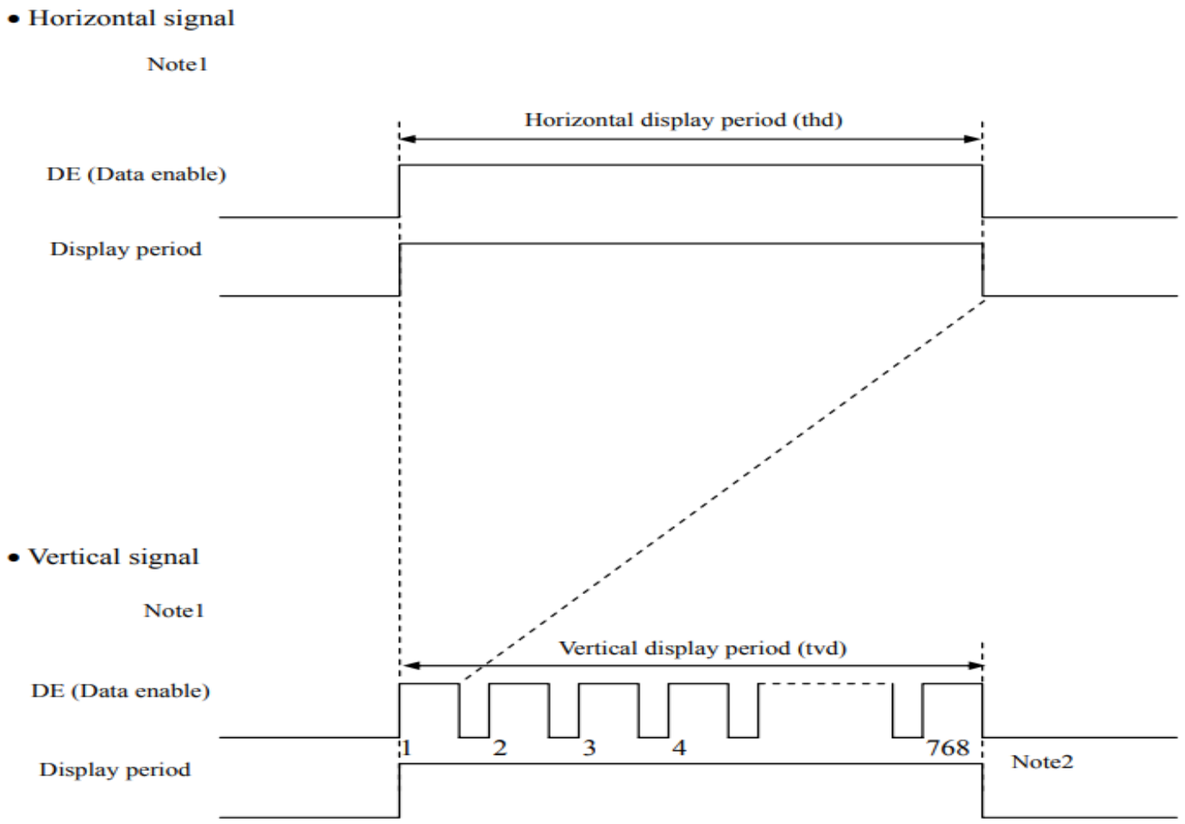


Single to single

- From display datasheet, identify HSYNC, VSYNC, and DE polarity

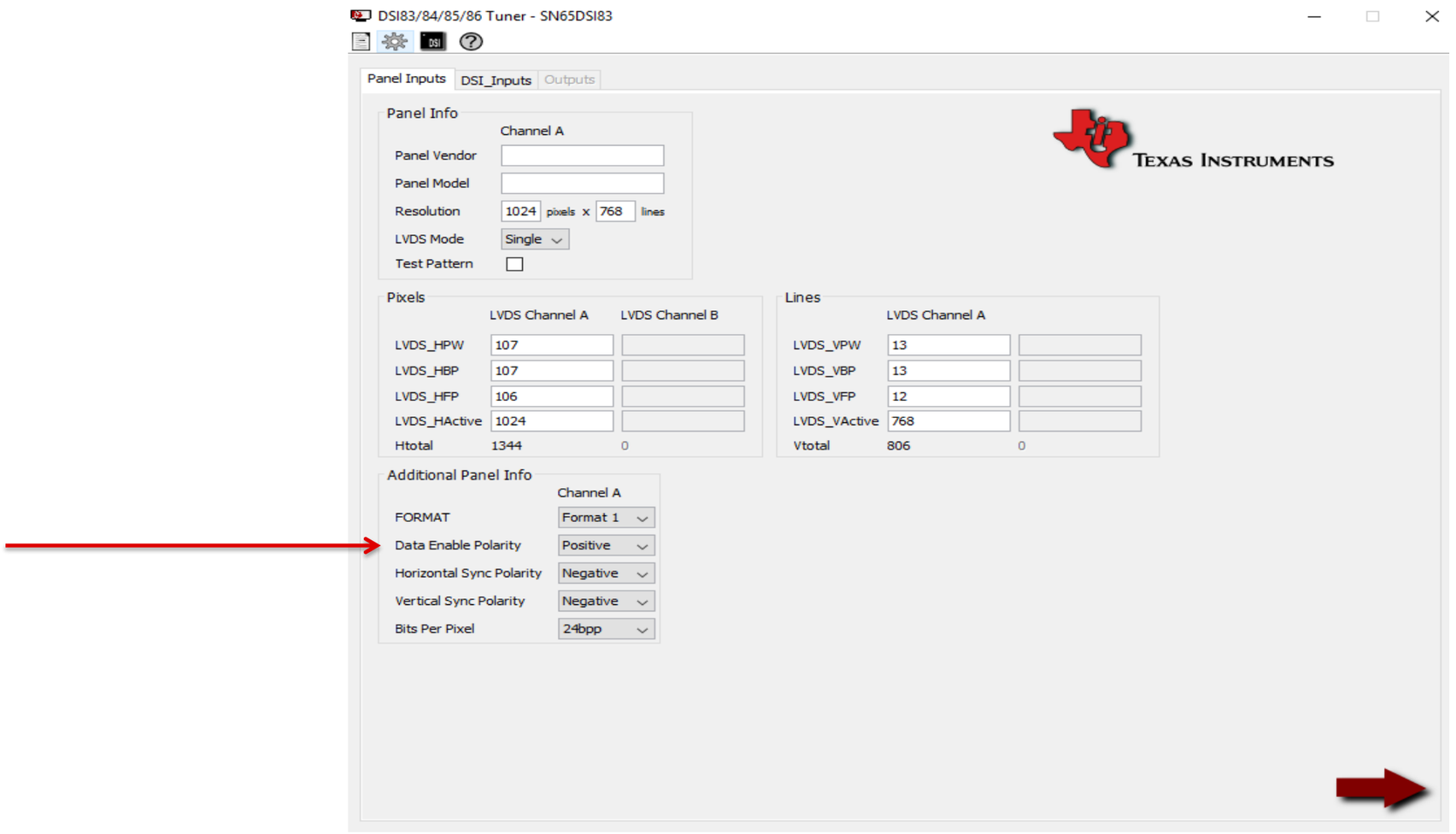
- This particular display operates in DE mode, so HSYNC/VSYNC Polarity don’t matter.

- DE is positive during active display, so DE polarity is positive



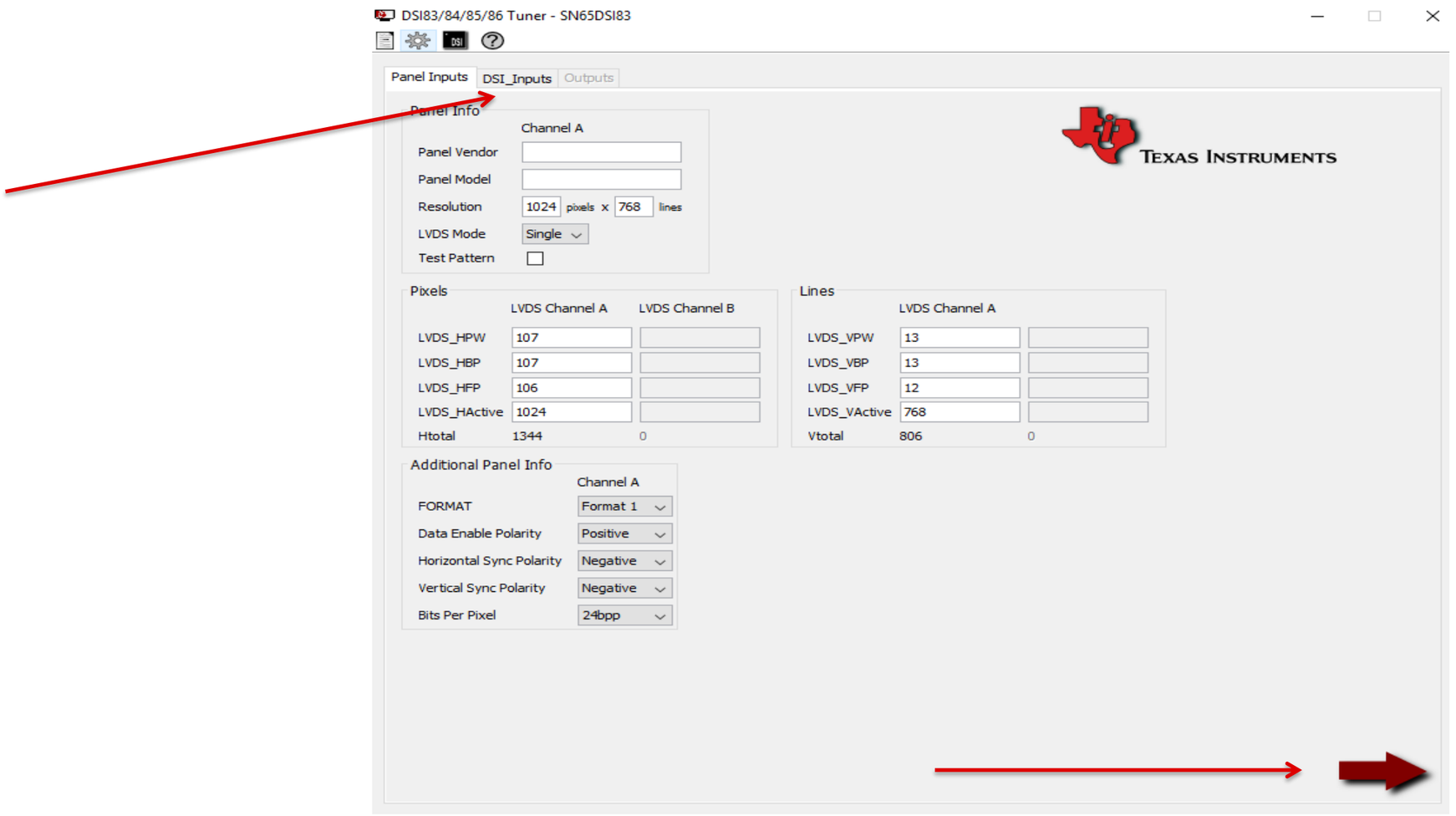
Single to single

- Fill out corresponding section in tool:



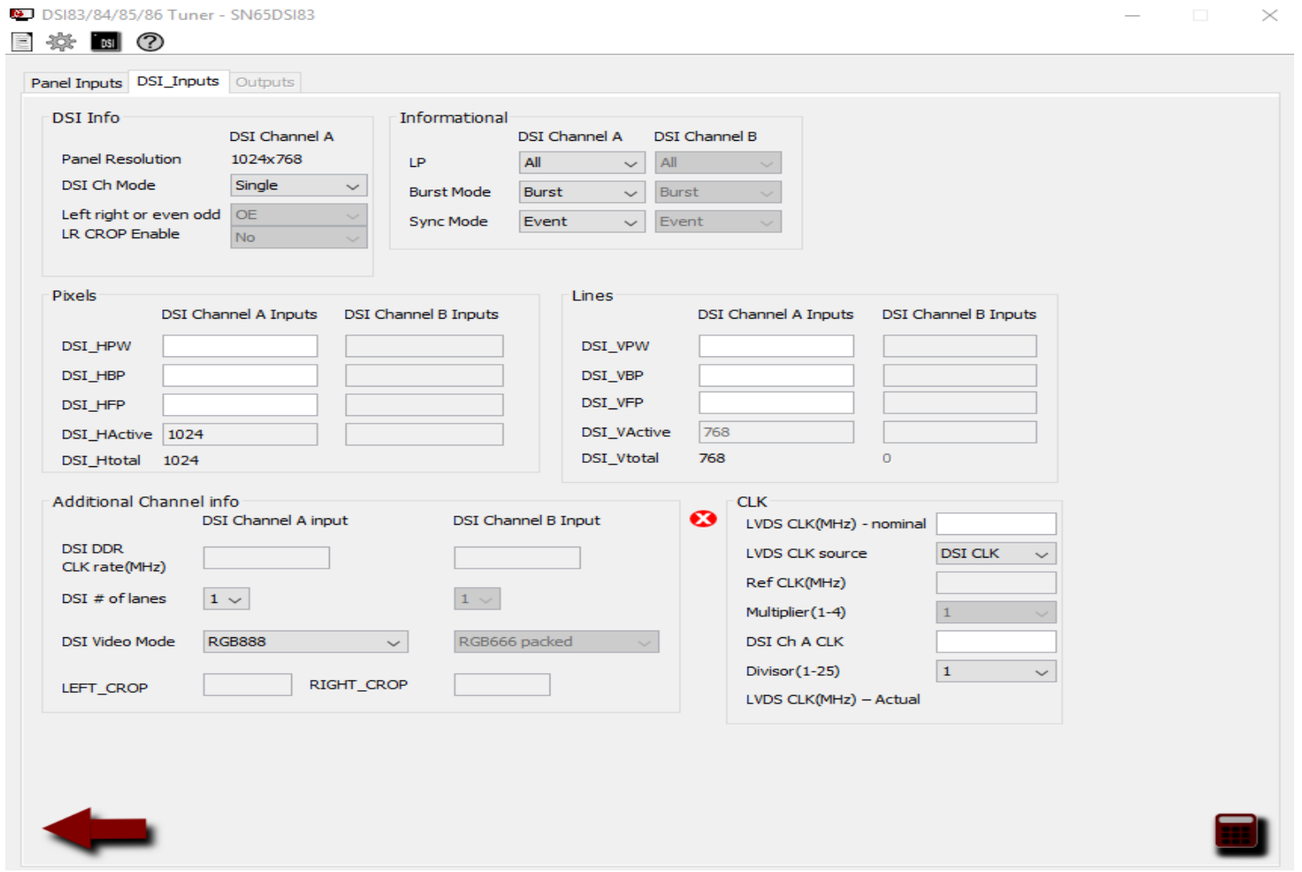
Single to single

- Switch to “DSI_Inputs” window by either clicking the tab or clicking the arrow:



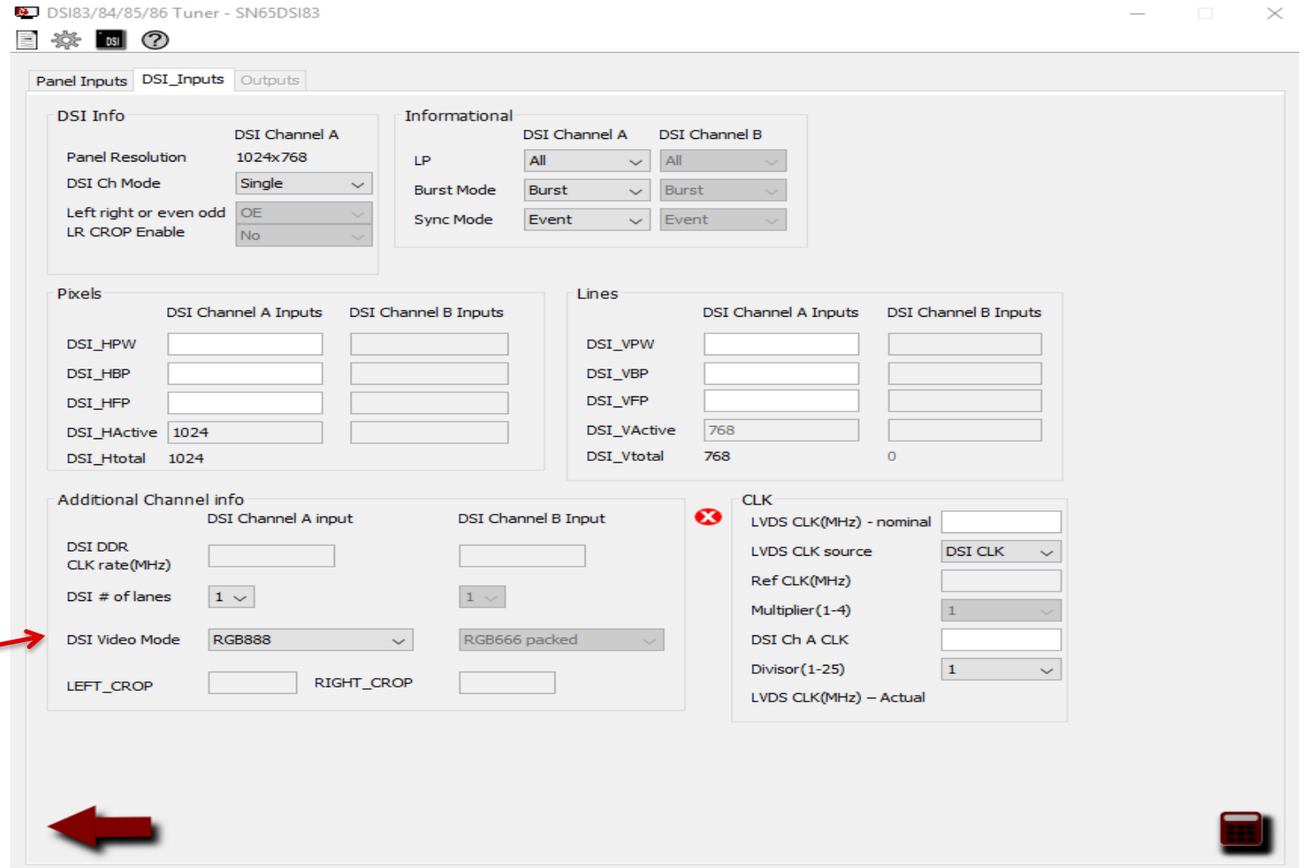
Single to single

- The inputs to this window mainly depend on the DSI source
- The parameters entered **must** match the actual DSI parameters transmitted by the DSI source



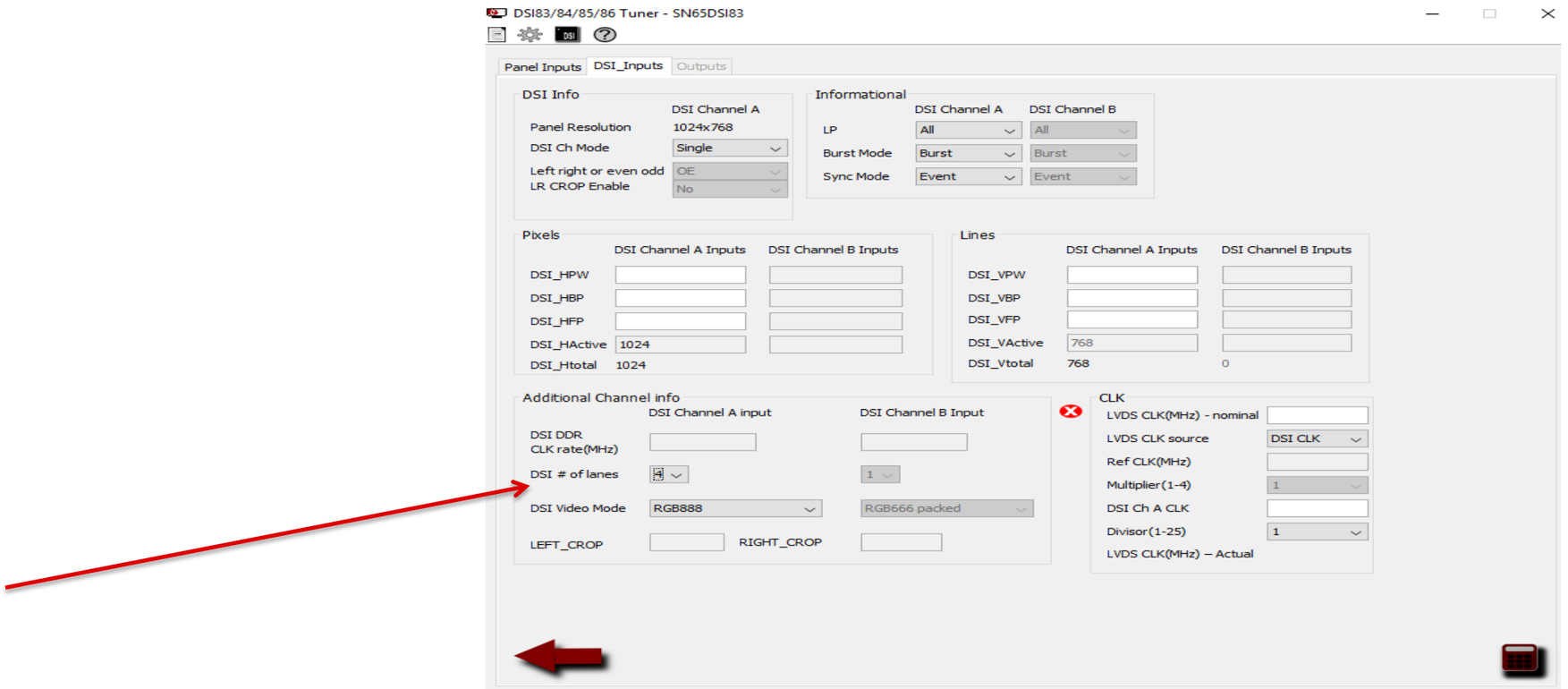
Single to single

- Since the display is 24bpp, select “RGB888” as the DSI Video Mode



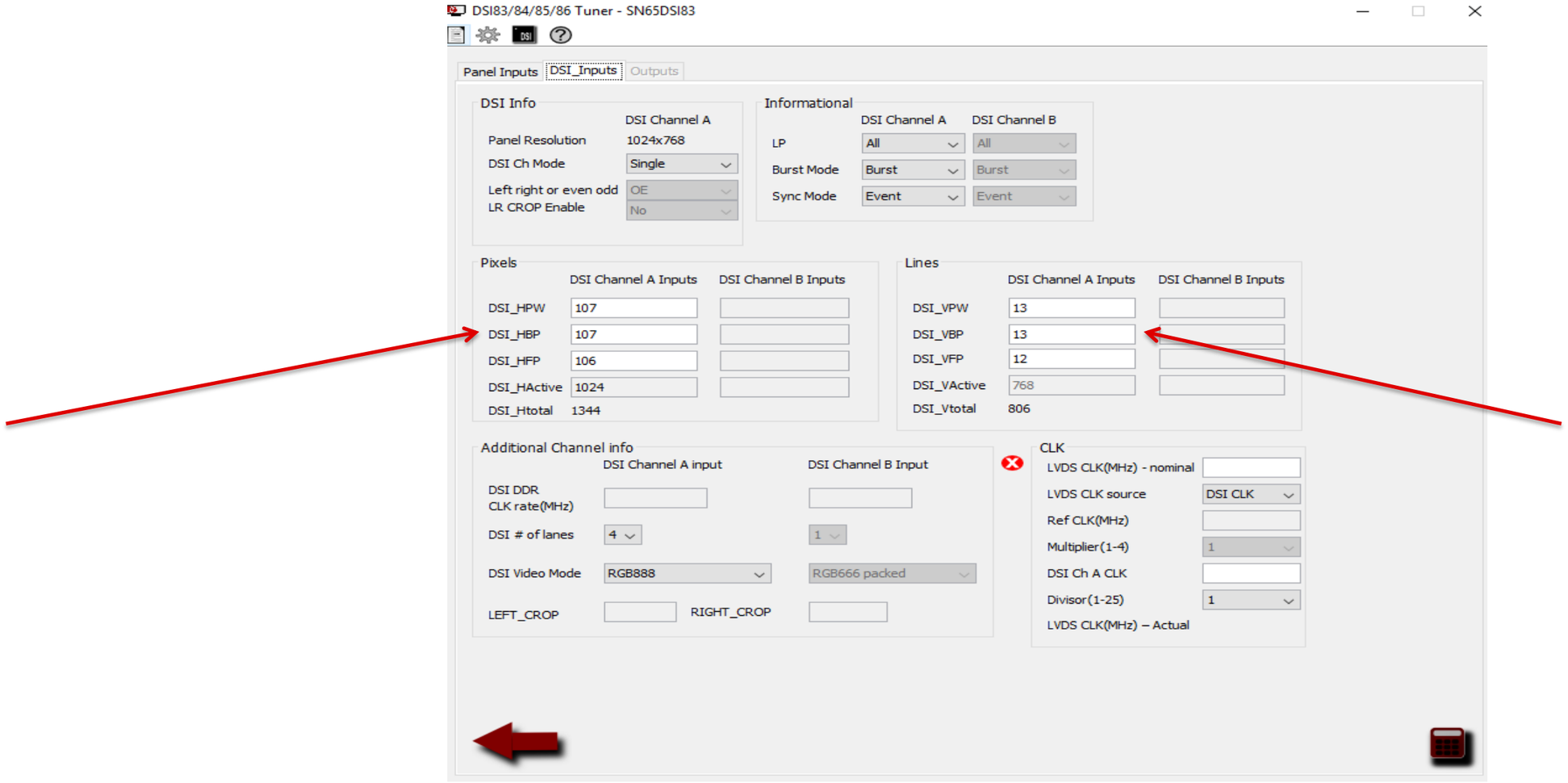
Single to single

- The “DSI # of lanes” depends on the required throughput to meet the display resolution
- Each lane can support up to 1 Gbps



Single to single

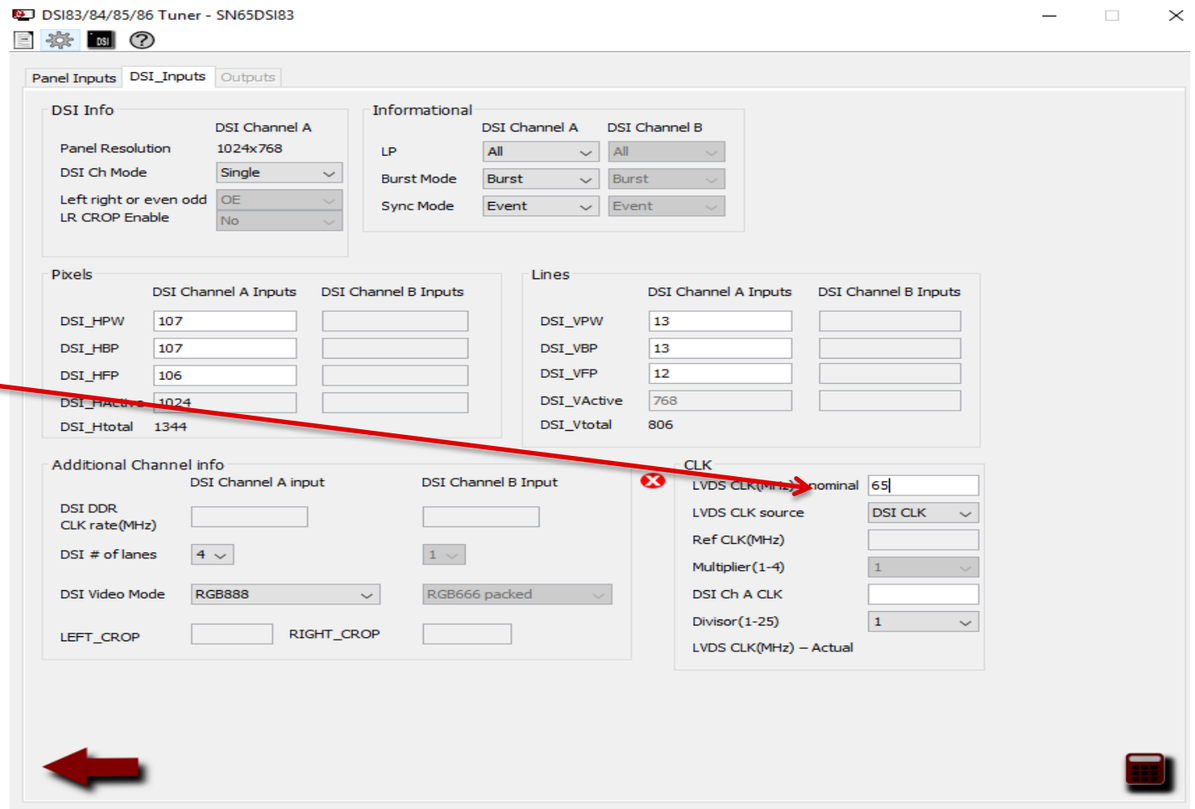
- Enter the pixel/line information. Typically this will match the display inputs:



Single to single

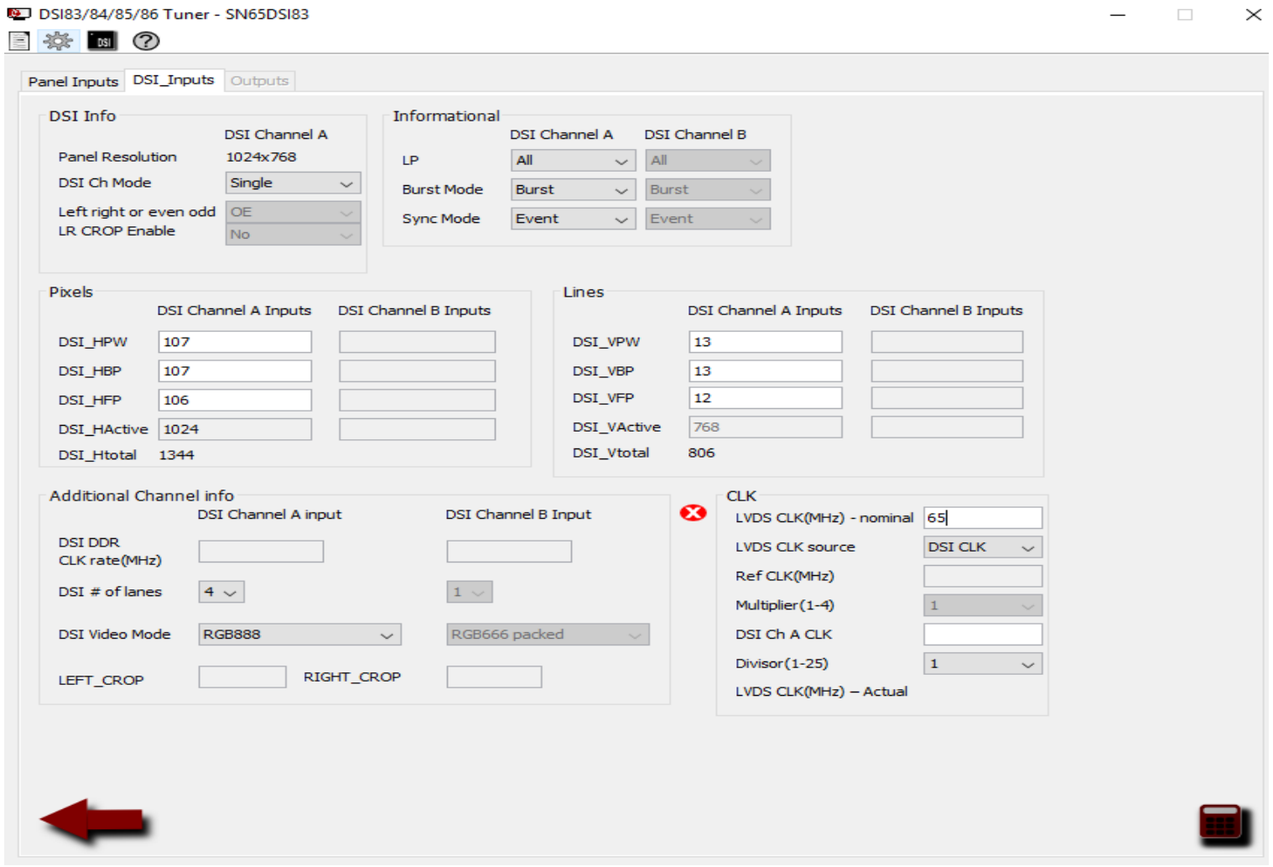
- Enter the “LVDS CLK(MHz) – nominal value from the frequency specified in the display datasheet
- The LVDS CLK range for the SN65DSI83/84/85 is 25 to 154MHz, so make sure you’re within this range

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	60.0	65.0	68.0	MHz	15.385ns (typ.)
	Duty		-		-		-	-
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-		-		ns	-
		Hold time					ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycle	th	19.67	20.676	22.4	μs	48.363kHz (typ.)
				-	1,344	-	CLK	
		Display period	thd		1,024		CLK	
	Vertical (One frame)	Cycle	tv	13.3	16.666	18.5	ms	60.0Hz (typ.)
				780	806	-	H	
		Display period	tvd		768		H	
	CLK-DE	Setup time	-		-		ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	



Single to single

- The LVDS CLK source can be derived from either the DSI Ch A CLK (DSI DDR CLK) or an external reference clock



Single to single

- To calculate the minimum required DSI CLK frequency, use the below equation:

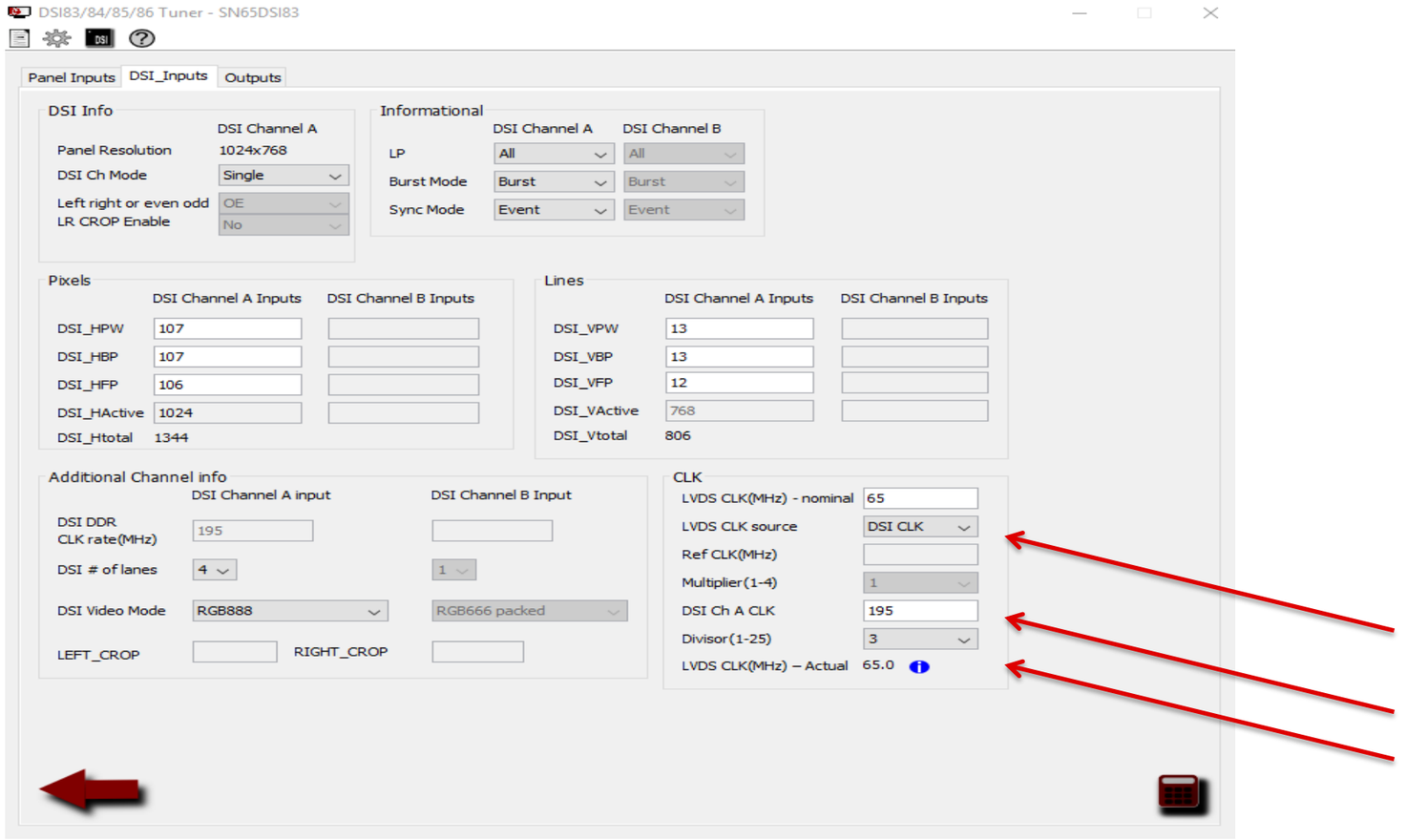
- $Minimum\ DSICLK\ frequency = \frac{Throughput}{2 \times \#\ of DSI\ Lanes} = \frac{LVDS\ CLK \times bpp}{2 \times \#\ of\ DSI\ Lanes}$

- For this example:

- $Minimum\ DSICLK\ frequency = \frac{65\ MHz \times 24\ bpp}{2 \times 4} = \frac{1560\ Mbps}{2 \times 4} = 195\ MHz$

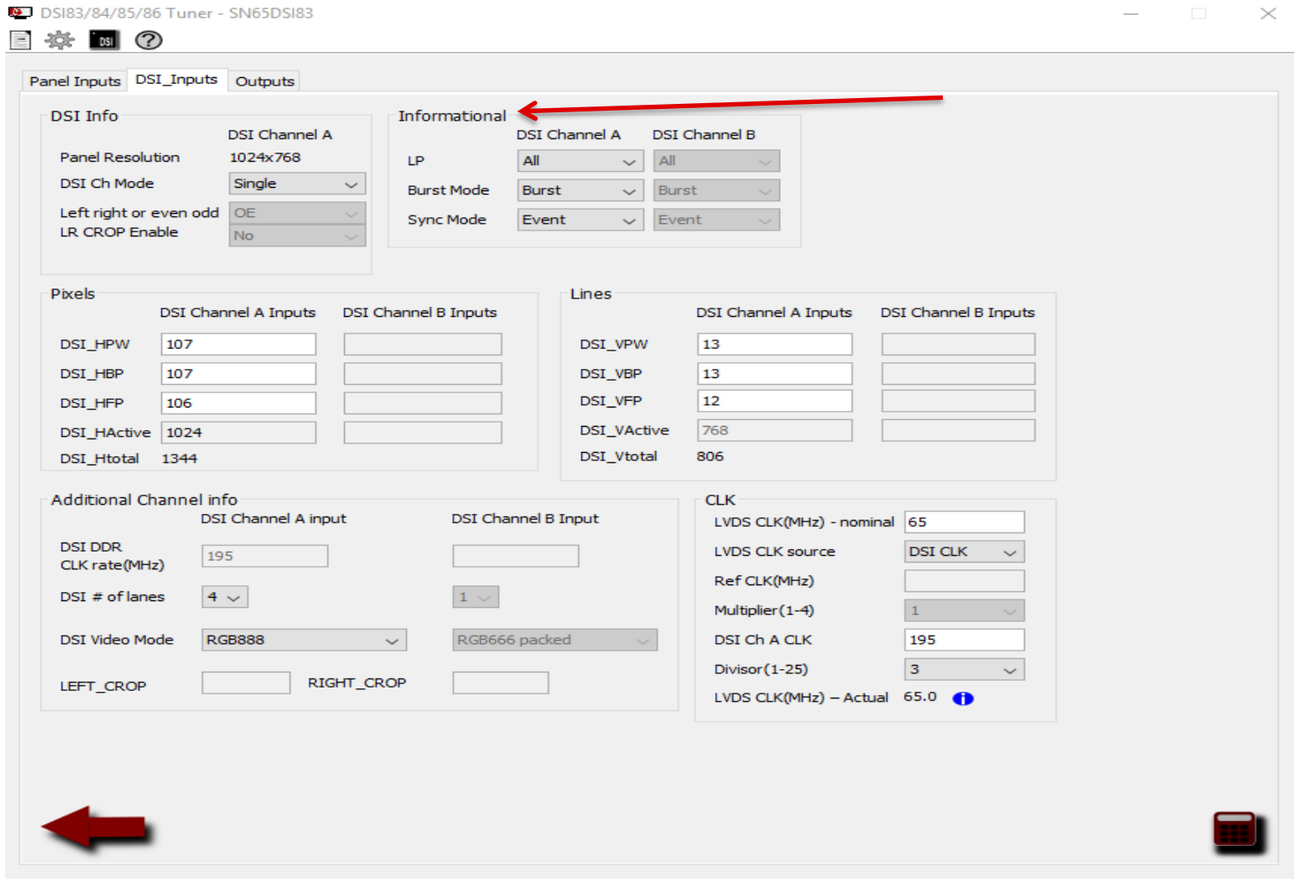
Single to single

- Fill out the corresponding section in the tool and select the correct divisor:



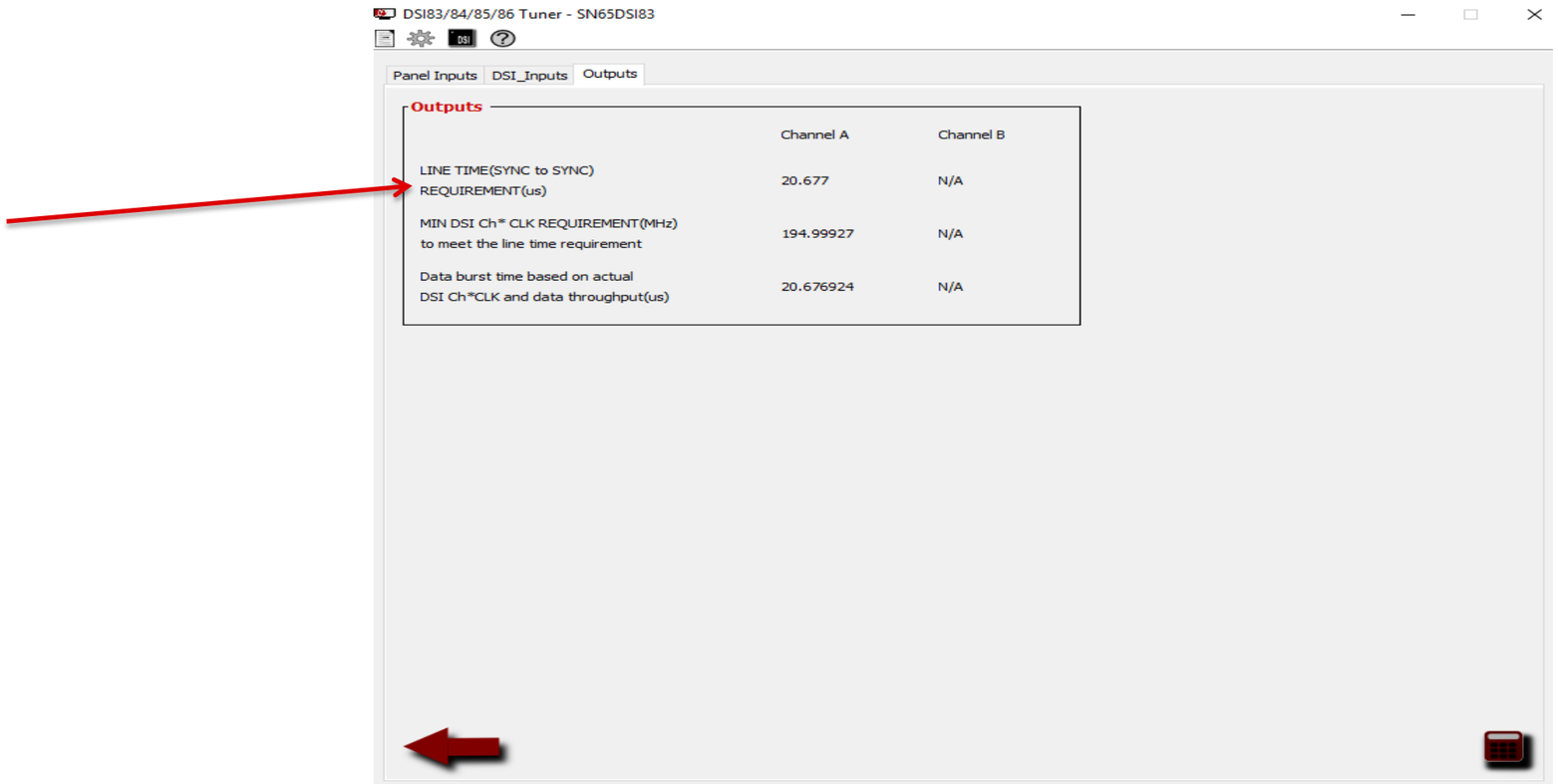
Single to single

- The “Informational” section depends on the DSI source:



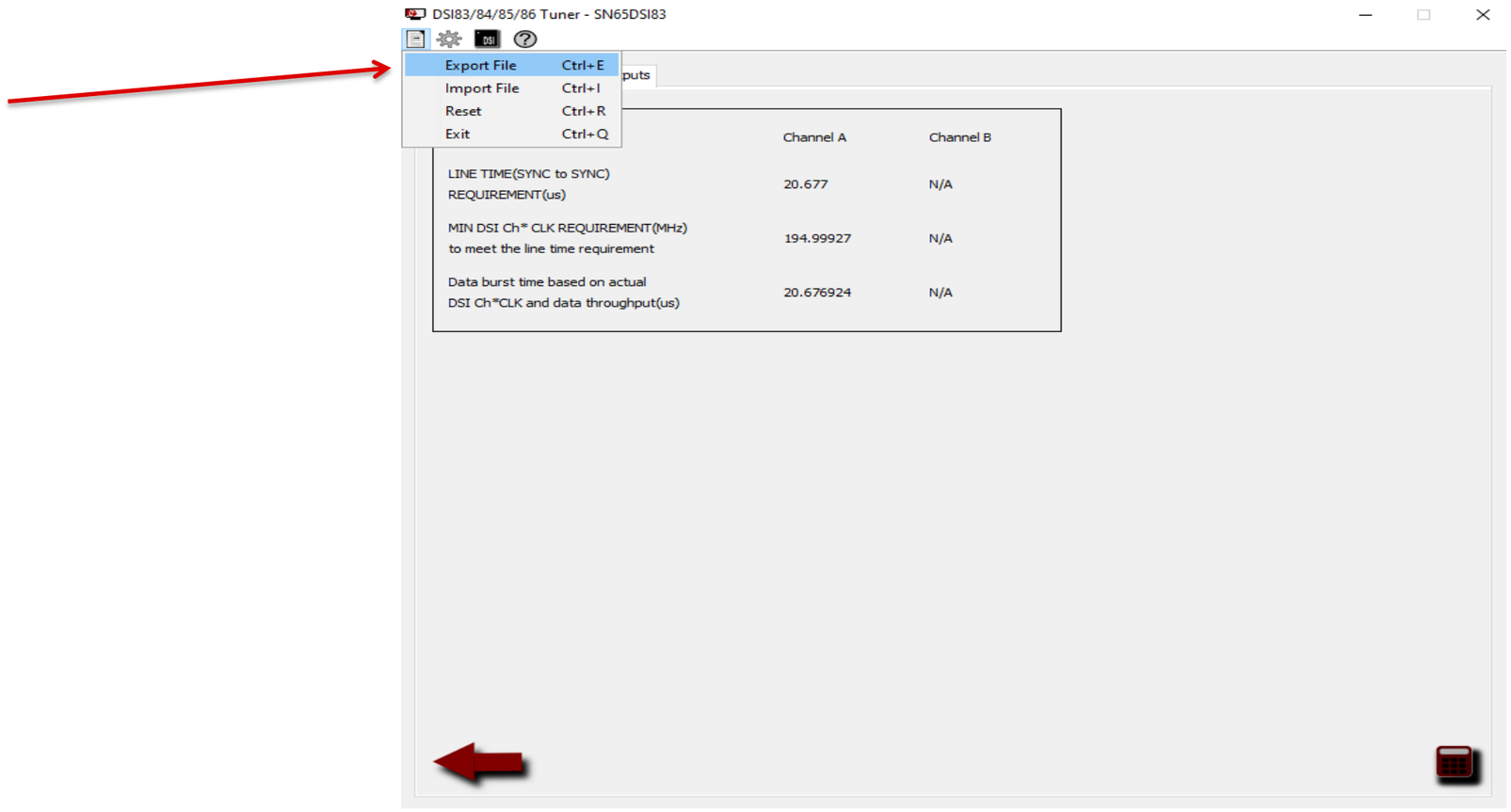
Single to single

- Click the calculator icon in the lower right to get to the “Outputs” window
- Make note of the LINE TIME requirement. The line time (horizontal sync to the next horizontal) on the input is preserved when outputting onto the LVDS interface.



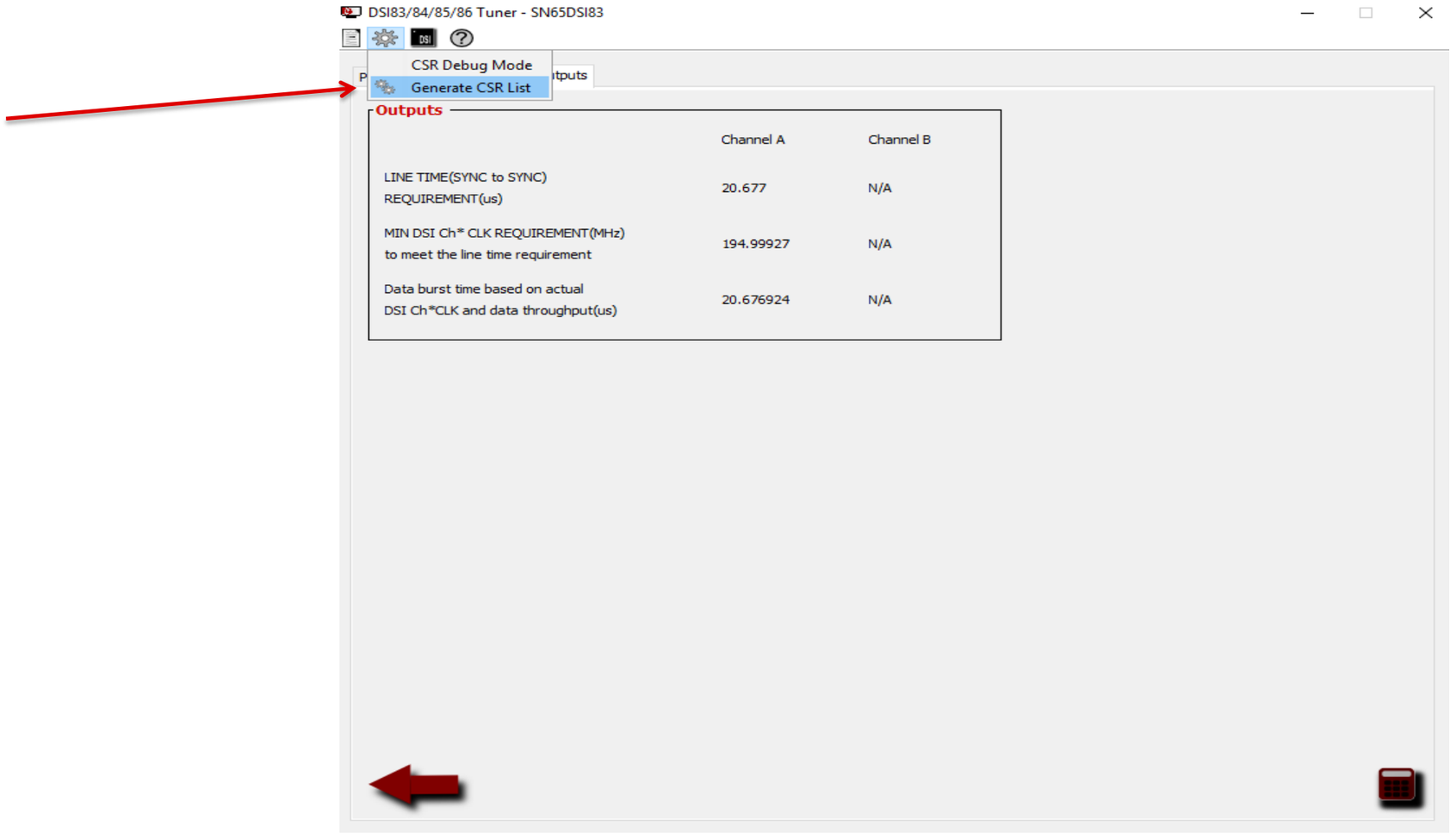
Single to single

- Click the icon in the upper left to export/save the .dsi file
- You can import it later without having to re-enter all the settings



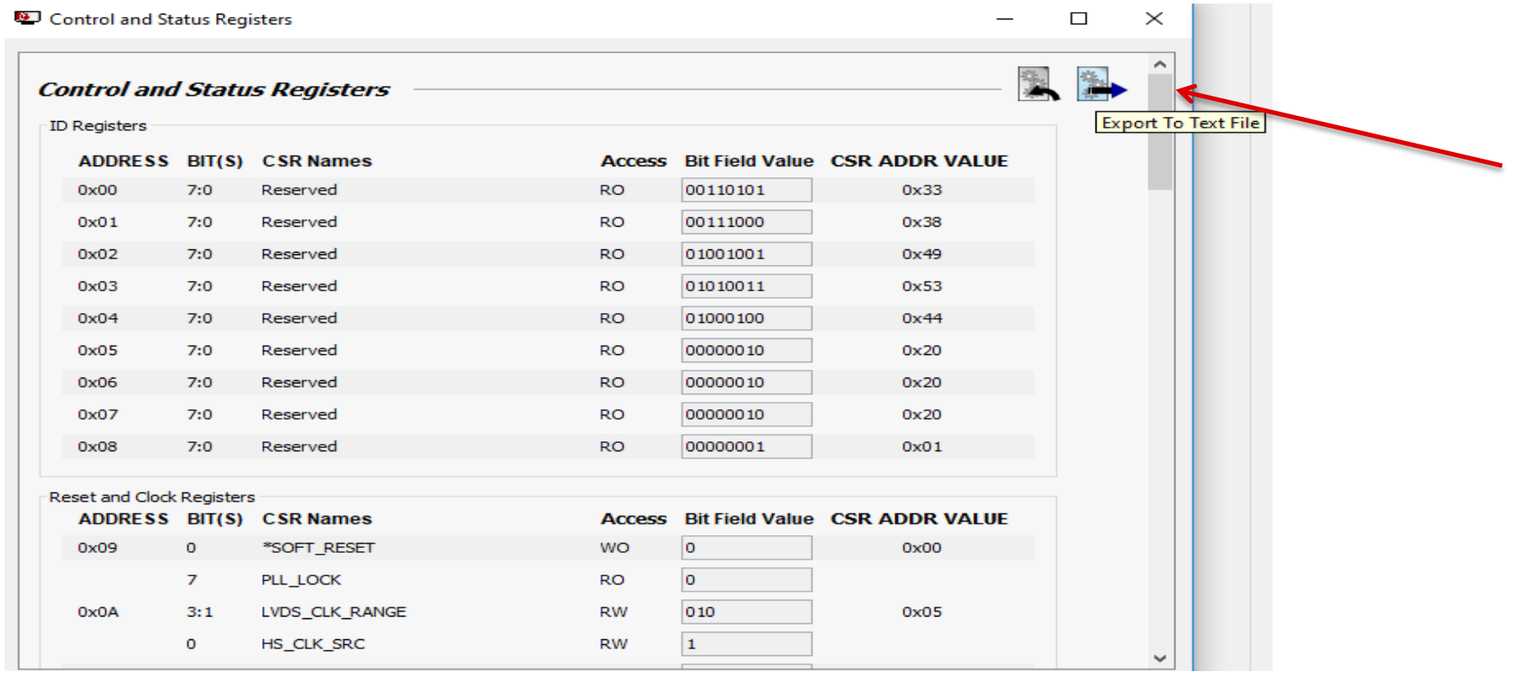
Single to single

- Click the icon in the upper left and Generate CSR list



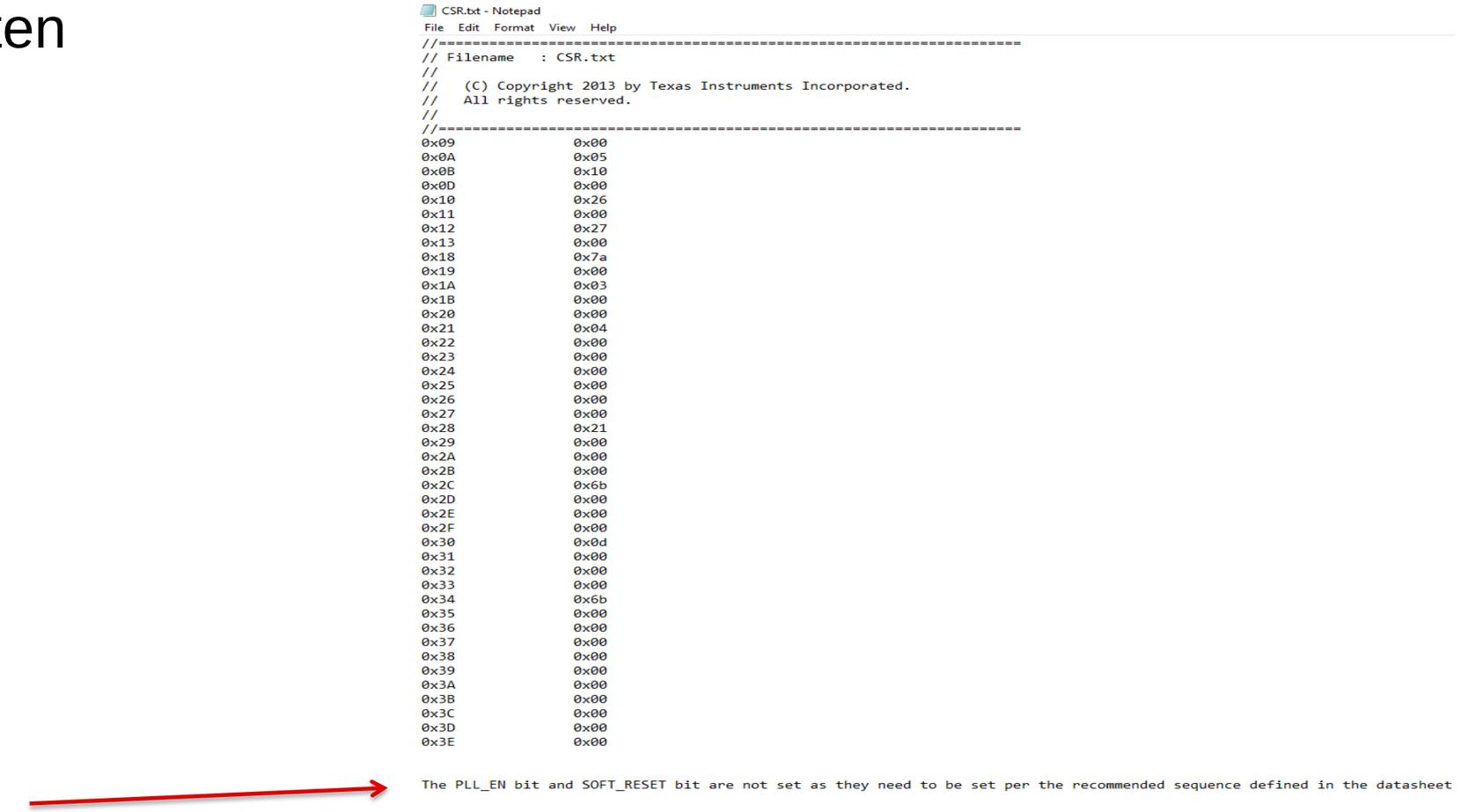
Single to single

- When the “Control and Status Registers” window pops up, click the  icon to export the settings to a .txt file



Single to single

- Open up the .txt file that was just generated. The column on the left contains the I2C register addresses, and the column on the right contains the values that need to be written



Thanks for your time!