## SN65DSI83/84/85- Single DSI Input to **Single-Link LVDS**

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• The SN65DSI83, DSI84, and DSI85 can all be used for single channel DSI to single channel LVDS, but we will use the SN65DSI83 for this demo





- From display datasheet, identify:
- Resolution:

Display area	210.432 (H) × 157.824 (V) mm
Diagonal size of display	26cm (10.4 inches)
Drive system	a-Si TFT active matrix
Display color	16,777,216 colors (At 8-bit input, FRC terminal= High) 262,144 colors (At 6-bit input, FRC terminal= Low or Open)
Pixel	1,024 (H) × 768 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe

• This is a 1024 x 768 panel



• Fill out corresponding section in tool:

Panel Inputs DSI_Inputs Outputs Panel Info Channel A	
Panel Vendor Panel Model Resolution 1024 pixels x 768 lines LVDS Mode Single  Test Pattern	TEXAS INSTRUMENTS
Pixels	Lines
LVDS Channel A LVDS Channel B	LVDS Channel A
LVDS_HPW	LVDS_VPW
LVDS_HBP	LVDS_VBP
LVDS_HFP	LVDS_VFP
LVDS_HActive 1024	LVDS_VActive 768
Additional Panel InfoChannel AFORMATFormat 1 ~Data Enable PolarityPositive ~Horizontal Sync PolarityNegative ~Vertical Sync PolarityNegative ~Bits Per Pixel18bpp ~	



- From display datasheet, identify:
- Mapping format:



• This is Format 1 (JEIDA), 24bpp



• Fill out corresponding section in tool:

Panel Inputs DSI_Inputs Outputs Panel Vendor Panel Model Resolution 1024 pixels x 768 lines LVDS Mode Single  Test Pattern	Texas Instruments
Pixels       LVDS Channel A       LVDS Channel B         LVDS_HPW	Lines LVDS_VPW LVDS_VBP LVDS_VFP LVDS_VActive 768 Vtotal 768 0



- From display datasheet, identify:
- Timing Parameters:



 This particular datasheet states the total display area and the active display area



Active Vertical Pixels

Total Vertical Pixels

- From display datasheet, identify:
- Timing Parameters:

Parameter			Symbol	min.	typ.	max.	Unit	Remarks		
	Fre	quency	1/te	60.0	65.0	68.0	MHz	15.385ns (typ.)		
CLK	1	Duty	-				•			
	Rise tim	ne, Fall time	-		-		ns	-		
	CLK-DATA	Setup time	-				ns			
DATA	CLK-DAIA	Hold time		-			ns	-		
	Rise tim	ne, Fall time	-				ns			
		Cycle	th	19.67	20.676	22.4	μs			
	Horizontal	Cycle	u	-	1,344	-	CLK	48.363kHz (typ.)		
		Display period	thd		1,024		CLK			
		Cuala	tu	13.3	16.666	18.5	ms			
DE	(One frame)	Cycle	LV .	780	806	-	Н	60.0Hz (typ.)		
	(one name)	Display period	tvd		768		Н			
	CLK-DE	Setup time	-				ns			
	CLK-DE	Hold time	-		-		ns	-		
	Rise tim	ne, Fall time	-				ns			

- Horizontal Blanking = 1344 1024 = 320
- Vertical Blanking = 806 768 = 38



- Fill out corresponding section in tool:
- Horizontal blanking (320) is divided among HPW, HBP, and HFP



a	Panel Info								
	Panel Vendor								
	Panel Model								
	Resolution	1024 p	ixels x 76	8 lines					
	LVDS Mode	Single	~						
	Test Pattern								
	Pixels						Lines		
	L	VDS Char	nnel A	LVDS Ch	annel B			LVDS Channel A	
	LVDS_HPW	107					LVDS_VPW	13	
	LVDS_HBP	107					LVDS_VBP	13	
	LVDS_HFP	106				-	LVDS_VFP	12	
	LVDS_HActive	1024					LVDS_VActive	768	
	Htotal	344		0			Vtotal	806	0
	Additional Pane	l Info							
			Channel /	Δ.					
	FORMAT		Format 1	ι ~					
	Data Enable Pola	arity	Positive	$\sim$					
	Horizontal Sync	Polarity	Negative	• ~					
	Vertical Sync Po	larity	Negative	• ~					
	Rite Dee Divel		24bpp	~					





- From display datasheet, identify HSYNC, VSYNC, and DE polarity
- This particular display operates in DE mode, so HSYNC/VSYNC
  Polarity don't matter.
- DE is positive during active display, so DE polarity is positive

Horizontal signal

Note1





• Fill out corresponding section in tool:

Panel Info Panel Vendor Panel Model Resolution LVDS Mode Test Pattern	Channel A	els x 768 lines			
Pixels LVDS_HPW LVDS_HBP LVDS_HFP LVDS_HActive Htotal Additional Par FORMAT Data Enable Pe Horizontal Sync P Bits Per Pixel	LVDS Chann 107 107 106 1024 1344 rel Info c Polarity [ c Polarity [ clarity [	lel A LVDS Channe	B LVDS_VPW LVDS_VBP LVDS_VFP LVDS_VActive Vtotal	LVDS Channel A	



• Switch to "DSI\_Inputs" window by either clicking the tab or clicking the arrow:

DSI83/84/85/86 Tuner - SN65DSI83	—
Panel Inputs DSI_Inputs Outputs	
Panel Inputs DSI_Inputs Outputs  Panel Info Channel A Panel Vendor Panel Model Resolution 1024 pixels x 768 lines LVDS Mode Single Test Pattern Pixels LVDS Channel A LVDS Channel B LVDS_HPW 107 LVDS_HBP 107	Lines LVDS_VPW 13 LVDS_VBP 13
LVDS_HFP         106           LVDS_HActive         1024	LVDS_VFP         12           LVDS_VActive         768
Htotal     1344     0       Additional Panel Info     Channel A       FORMAT     Format 1 ~       Data Enable Polarity     Positive ~       Horizontal Sync Polarity     Negative ~       Vertical Sync Polarity     Negative ~	Vtotal 806 0
Bits Per Pixel 24bpp ~	
	DSI83/84/85/86 Tuner - SN65DSI83   Panel Inputs   DSI_Inputs   Outputs     Panel Inputs   DSI_Inputs   Outputs     Panel Vendor   Panel Model   Resolution   1024 pixels x 768   LVDS Mode   Single    Test Pattern     Pixels   LVDS_HBW   107   LVDS_HBP   107   LVDS_HFP   106   LVDS_HFP   106   LVDS_HAT   Format 1   Data Enable Polarity   Negative   Vertical Sync Polarity   Negative   Vertical Sync Polarity   Negative   Bits Per Pixel



- The inputs to this window mainly depend on the DSI source
- The parameters entered **must** match the actual DSI parameters transmitted by the DSI source DSI83/84/85/86 Tuner - SN65DSI83

DSI Channel A el Resolution 1024x768 Ch Mode Single ~ tright or even odd CROP Enable OE ~	DSI Chann LP All Burst Mode Burst Sync Mode Event	All DSI Char All Burst	annel B
Cels     DSI Channel A Inputs     DSI C       SI_HPW	hannel B Inputs	es D: SI_VPW SI_VBP SI_VBP SI_VFP SI_VActive 7 SI_VActive 7 SI_Vtotal 76	SI Channel A Inputs DSI Channel B Inputs
ditional Channel info DSI Channel A input SI DDR LK rate(MHz) SI # of lanes 1 ~ SI Video Mode RGB888 EFT_CROP RIGHT_CR	DSI Channel B Inpu	t <table-cell></table-cell>	CLK LVDS CLK(MHz) - nominal LVDS CLK source DSI CLK ~ Ref CLK(MHz) Multiplier(1-4) 1 DSI Ch A CLK Divisor(1-25) 1 ~ LVDS CLK(MHz) – Actual



• Since the display is 24bpp, select "RGB888" as the DSI Video Mode

DSI Info Panel Resolution DSI Ch Mode Left right or even odd LR CROP Enable	DSI Channel A 1024x768 Single OE No Single Sync Mode	DSI Channel A DSI All ~ All Burst ~ Bu Event ~ Ev	rst v	
Pixels     DSI Channel       DSI_HPW	nel A Inputs DSI Channel B Inputs	Lines DSI_VPW DSI_VBP DSI_VFP DSI_VActive DSI_Vtotal	DSI Channel A Inputs	DSI Channel B Inputs
Additional Channel info DSI DDR CLK rate(MHz) DSI # of lanes 1 DSI Video Mode RG LEFT_CROP	Channel A input DSI Cha DSI Cha DSI Cha DSI Cha DSI Cha Channel A input DSI Cha Channel A input DSI Cha DSI Ch	5 packed	CLK LVDS CLK(MHz) - LVDS CLK source Ref CLK(MHz) Multiplier (1-4) DSI Ch A CLK Divisor (1-25) LVDS CLK(MHz) -	nominal DSI CLK ~





- The "DSI # of lanes" depends on the required throughput to meet the display resolution
- Each lane can support up to 1 Gbps

DSI Info     DSI Channel A     DSI Channel A     DSI Channel A       Panel Resolution     1024x768     LP     All       DSI Ch Mode     Single     Burst Mode     Burst       Left right or even odd LR CROP Enable     OE     Sync Mode     Event
Pixels       DSI Channel A Inputs       DSI Channel B Inputs       Lines         DSI_HPW
Additional Channel info       DSI Channel A input       DSI Channel B Input       IVDS CLK(MHz) - nominal         DSI DDR       IVDS CLK source       DSI CLK ~         CLK rate(MHz)       I       Multiplier(1-4)       I         DSI Video Mode       RGB888       RGB666 packed       DSI Channel A CLK       DSI CLK ~         LEFT_CROP       RIGHT_CROP       RIGHT_CROP       I       I



• Enter the pixel/line information. Typically this will match the display inputs:

ן [ [	DSI83/84/85/86 Tuner - SN65DSI83      Panel Inputs DSI_Inputs Outputs	
	DSI InfoInformationalPanel ResolutionDSI Channel APanel Resolution1024x768DSI Ch ModeSingleLeft right or even odd LR CROP EnableOENoSync ModeEvent	
	Pixels       DSI Channel A Inputs       DSI Channel B Inputs         DSI_HPW       107	



- Enter the "LVDS CLK(MHz) nominal value from the frequency specified in the display datasheet
- The LVDS CLK range for the SN65DSI83/84/85 is 25 to 154MHz, so make sure you're within this range DSI83/84/85/86 Tuner - SN65DSI83 🖹 🕸 📶 🕜

Panel Inputs DSI\_Inputs Outputs

DSI Channel A

1024x768

Informational

DSI Channel A DSI Channel B

DSI Info

Panel Resolution

									DSI Ch Mode Left right or e LR CROP Ena	single even odd OE ble No	Burst Mod     Sync Mod	e Burst $\checkmark$ E	lur: ive
	Parameter		Symbol	min.	typ.	max.	Unit	Remarks	Divels			Lines	
	Free	quency	1/tc	60.0	65.0	68.0	MHz	15.385ns (typ.)		DSI Channel A Inputs	DSI Channel B Inp	uts	
CLK	I	Duty	-				-		DSI_HPW	107		DSI_VPW	
DE (C	Rise tim	e, Fall time	-		-		ns	-	DSI_HBP	107		DSI_VBP	
	CLK-DATA	Setup time	-				ns		DSI_HFP	106		DSI_VFP	
DATA CLK-DATA Rise time,	CLK-DAIA	Hold time			-		ns	-	DSI_HACO	1024		DSI_VActive	2
	e, Fall time	-				ns		DSI_Htotal	1344		DSI_Vtotal		
	Cycle	th	19.67	20.676	22.4	μs		- Additional Ch	annel info				
	Horizontal	Cycle	u	-	1,344	-	CLK	48.363kHz (typ.)		DSI Channel A in	put DSI	Channel B Input	Т
Horizontal		Display period	thd		1,024		CLK		DSI DDR				
	Marcine 1	Cuele	t.	13.3	16.666	18.5	ms		CLK rate(MHz				
DE	(One frame)	Cycle	LV .	780	806	-	Н	60.0Hz (typ.)	DSI # of lane	s 4 ~	1	$\sim$	
	(one mane)	Display period	tvd		768		Н		DSI Video Mo	de RGB888	∼ RG	B666 packed 🔍 🗸	
	CLK-DE	Setup time	-				ns						
	CLK-DE	Hold time	-		-		ns	-	LEFT_CROP	R			
	Rise tim	e, Fall time	-				ns						

ts DSI Ch	annel B Inputs
•	
nominal	65
irce	DSI CLK 🗸
,	
)	1 ~
	1 ~
iz) – Actual	



• The LVDS CLK source can be derived from either the DSI Ch A CLK (DSI DDR CLK) or an external reference clock

Panel Resolution DSI Ch Mode Left right or even od LR CROP Enable	DSI Channel A 1024x768 Single ~ Id OE ~ No ~	LP Sync Mode	DSI Channel A DS All ~ A Burst ~ B Event ~ E	SI Channel B			
Pixels DSI_HPW 107 DSI_HBP 107 DSI_HBP 106 DSI_HActive 1024 DSI_Htotal 1344	Dannel A Inputs DSI	Channel B Inputs	Lines DSI_VPW DSI_VBP DSI_VFP DSI_VActive DSI_Vtotal	DSI Channel A 13 13 12 768 806	A Inputs DSI	Channel B Inputs	
Vdditional Channel	info SI Channel A input 4 ~ RGB888 RIGHT_C	DSI Chann 1 ~ RGB666 ; ROP	packed	CLK LVDS C LVDS C Ref CLI Multiplin DSI Ch Divisori	LK(MHz) - nomi LK source K(MHz) er (1-4) A CLK (1-25)	nal 65	



- To calculate the minimum required DSI CLK frequency, use the below equation:
- *Minimum DSICLK frequency* =  $\frac{Throughput}{2 \times \# of DSI Lanes} = \frac{LVDS CLK \times bpp}{2 \times \# of DSI Lanes}$
- For this example:
- Minimum DSICLK frequency =  $\frac{65 \text{ MHz} \times 24 \text{ bpp}}{2 \times 4} = \frac{1560 \text{ Mbps}}{2 \times 4} = 195 \text{ MHz}$



• Fill out the corresponding section in the tool and select the correct divisor:

SI Info Panel Resolu DSI Ch Mode Left right or LR CROP Ena	tion even odd able	DSI Channel A 1024x768 Single OE No	>	Informational LP Burst Mode Sync Mode	DSI Ch All Burst Event	annel A	All Burs Ever	t v			
ixels	DSI Char	nnel A Inputs	DSI Ch	annel B Inputs		Lines		DSI Channel A Input:	5 DS	I Channel B Inputs	
DSI_HPW	107					DSI_VPW		13	1 [		
DSI_HBP	107					DSI_VBP		13			
DSI_HFP	106	06			DSI_VFP			12			
DSI_HActive	1024					DSI_VAct	ve	768	1 [		
DSI_Htotal	1344					DSI_Vtota	al	806			
dditional Ch DSI DDR CLK rate(MH	nannel int DSI z)	fo I Channel A inp 5	ut	DSI Cha	nnel B Ir	nput		CLK LVDS CLK(MHz) - n LVDS CLK source	ominal	65 DSI CLK v	~
DSI <b># of la</b> ne	es 4	$\sim$		1 🗸				Ref CLK(MHz) Multiplier(1-4)		1 ~	
DSI Video Mo	de R0	GB888	`	RGB666	o packed			DSI Ch A CLK		195	<
LEFT_CROP		RIC	GHT_CRO	)P				Divisor (1-25) LVDS CLK (MHz) – A	Actual	3 ~ 65.0 <b>()</b>	*



• The "Informational" section depends on the DSI source:

DSI Info	tion	DSI Channel / 1024x768	A LF	formational	DSI Ch	annel A	DSI C	Channel B			
Left right or e	even odd ble	OE No	→ Bi	urst Mode ync Mode	Burst Event	~	Burs	t v nt v			
Pixels						Lines					
DSI HPW	DSI Chan	nnel A Inputs	DSI Chann	el B Inputs		DSI VPW		DSI Channel A	Inputs [	SI Channel I	B Inputs
DSI_HBP	107					DSI_VBP		13			
DSI_HFP	106					DSI_VFP		12			
DSI_HActive	1024					DSI_VAct	ve	768			
DSI_Htotal	1344					DSI_Vtota	al	806			
Additional Ch	annel inf DSI	fo [ Channel A inp	put	DSI Cha	nnel B I	nput		CLK LVDS CLK(M	IHz) - nomina	al 65	
CLK rate(MH	:) 19	5						LVDS CLK so	ource	DSI CLK	~
DSI # of lane	s 4	~		1 🗸				Multiplier(1-	(Z) (4)	1	~
DSI Video Mo	de RG	B888	$\sim$	RGB666	6 packed	4 ~		DSI Ch A CL	к	195	
LEFT_CROP		RI	GHT_CROP					Divisor(1-25	5) IHz) – Actua	3 65.0 🚹	~



- Click the calculator icon in the lower right to get to the "Outputs" window
- Make note of the LINE TIME requirement. The line time (horizontal sync to the next horizontal) on the input is preserved when outputting onto the LVDS interface. DSI83/84/85/86 Tuner - SN65DSI83  $\sim$





22

- Click the icon in the upper left to export/save the .dsi file
- You can import it later without having to re-enter all the settings

DSI8 💽	—	- ×						
<b>E</b> 🕸	ISI ?							
Ex	port File	Ctrl+E	e					
Im	port File	Ctrl+I	3					
Re	set	Ctrl+R						
Exi	it	Ctrl+Q		Channel A	Channel B			
LII RE	NE TIME(SYNO	C to SYNC) (us)		20.677	N/A			
MI to	N DSI Ch* CL meet the line	LK REQUIREMEN time requiremer	T(MHz) nt	194.99927	N/A			
Da DS	ata burst time SI Ch*CLK and	based on actual d data throughpu	l ut(us)	20.676924	N/A			



• Click the 🚈 icon in the upper left and Generate CSR list

	DSI83/84/85/86 Tuner - SN65DSI83			—
	🕸 🔟 🕐			
	CSR Debug Mode			
*	Senerate CSR List			
	Outputs			
		Channel A	Channel B	
	LINE TIME(SYNC to SYNC) REQUIREMENT(us)	20.677	N/A	
	MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement	194.99927	N/A	
	Data burst time based on actual DSI Ch*CLK and data throughput(us)	20.676924	N/A	
	-			



• When the "Control and Status Registers" window pops up, click the **w** icon to export the settings to a .txt file

Control and St	atus Regi	sters			-	[		×
ontrol and	Statu	s Registers					<u>≩</u>	
O Registers							Expo	rt To Text File
ADDRE \$ \$	BIT(S)	CSR Names	Access	Bit Field Value	CSR ADDR VALUE			
0x00	7:0	Reserved	RO	00110101	0x33			
0x01	7:0	Reserved	RO	00111000	0x38			
0x02	7:0	Reserved	RO	01001001	0x49			
0x03	7:0	Reserved	RO	01010011	0x53			
0x04	7:0	Reserved	RO	01000100	0x44			
0x05	7:0	Reserved	RO	00000010	0x20			
0x06	7:0	Reserved	RO	00000010	0x20			
0x07	7:0	Reserved	RO	00000010	0x20			
0x08	7:0	Reserved	RO	0000001	0x01			
east and Clark	Decistor							
ADDRESS	BIT(S)	CSR Names	Access	Bit Field Value	CSR ADDR VALUE			
0x09	0	*SOFT_RESET	WO	0	0x00			
	7	PLL_LOCK	RO	0				
0x0A	3:1	LVDS_CLK_RANGE	RW	010	0x05			
	0	HS_CLK_SRC	RW	1				





25

• Open up the .txt file that was just generated. The column on the left contains the I2C register addresses, and the column on the right contains the values that need to be written CSR.txt - Notepad

File Edit Format Vi	ew Help
//	
// Filename : (	CSR.txt
11	
// (C) Copyrigh	nt 2013 by Texas Instruments Incorporated.
// All rights r	reserved.
//	
//	
0×09	0×00
0x00	0x05
0×0R	0x03
0x0D	
0×10	0x26
0-11	0x20
0,11	0x00
0x12	0x27
0x13	0x70
0x10	0x/0
0x19	0000
0.18	0.00
0x10	0.00
0x20	0x00
0x21	0x04
0x22	0.00
0x25	0.00
0x24	0x00
0x25	0.00
0x26	0x00
0x27	0x00
0x28	0x21
0x29	0x00
0x2A	0x00
0x2B	0x00
0x2C	UX6D
0x2D	0x00
0x2E	0x00
0x2F	0x00
0x30	0x00
0x31	0x00
0x32	0x00
0x33	0x00
0x34	0x6b
0x35	0x00
0x36	0×00
0x3/	0x00
0x38	0x00
0x39	0×00
0x3A	0×00
0x3B	0x00
0x3C	0x00
0x3D	0x00
0x3E	0x00

not set as they need to be set per the recommended sequence



26

# Thanks for your time!



