Hercules™ ARM® Cortex®-R4 System Architecture

Memory Protection Unit (MPU)

Memory Protection Unit (MPU): Regions

- 8, 12, or 16 regions
  - ARM Cortex-R5 has 16 regions
  - ARM RM42 (Corona) has 8 regions
  - All other Hercules ARM processors have 12 regions
- The region with highest region number has the highest priority.
- Overlay of regions is possible.
- Regions are defined based on the following:
  - Base address
  - Region size
  - Sub-regions
  - Region attributes
  - Region access permissions

NOTE: Before enabling the MPU, at least one region has to be defined. Otherwise the CPU can get into a state which can only be recovered by reset!

Memory Protection Unit: Memory map by region

Region 12

Region1

TMS570 Default Memory Map

		Instruction Memory Type		Data Memory Type		
Address Range		**Cache enabled**	**Cache disabled**	**Cache enabled**	**Cache disabled**	**Execute Never**
0xFFFFFFFF 0xFFF80000	System Registers	Normal	Normal	Strongly Ordered	Strongly Ordered	Execute Never
0xFFF7FFFF 0xFFF78000	Peripheral Registers	Normal	Normal	Strongly Ordered	Strongly Ordered	Execute Never
0xFFA0FFFF 0xFFA00000	Coresight Debug	Normal	Normal	Strongly Ordered	Strongly Ordered	Execute Never
0xFF7FFFFF 0xFF000000	Peripheral Memory	Normal	Normal	Strongly Ordered	Strongly Ordered	Execute Never
0xFEFFFFFF 0xFE000000	CRC	Normal	Normal	Strongly Ordered	Strongly Ordered	Execute Never
0xFDFFFFFF 0xFD000000	HPI	Normal	Normal	Strongly Ordered	Strongly Ordered	Execute Never
0x64FFFFFF 0x60000000	External Memory	Normal, Cacheable, Non-Shared	Normal, Non-Cacheable, Non-Shared	Normal, WBWA-Cacheable, Non-Shared	Normal, Non-Cacheable, Shared	Execution Permitted
0x1FFFFFFF 0x18000000	Flash Swap	Normal, Cacheable, Non-Shared	Normal, Non-Cacheable, Non-Shared	Normal, WBWA-Cacheable, Non-Shared	Normal, Non-Cacheable, Shared	Execution Permitted
0x17FFFFFF 0x08000000	eSRAM	Normal, Cacheable, Non-Shared	Normal, Non-Cacheable, Non-Shared	Normal, WBWA-Cacheable, Non-Shared	Normal, Non-Cacheable, Shared	Execution Permitted
0x00FFFFFF 0x00000000	Program Memory	Normal, Cacheable, Non-Shared	Normal, Non-Cacheable, Non-Shared	Normal, WBWA-Cacheable, Non-Shared	Normal, Non-Cacheable, Shared	Execution Permitted

Memory Protection Unit: Memory Attributes

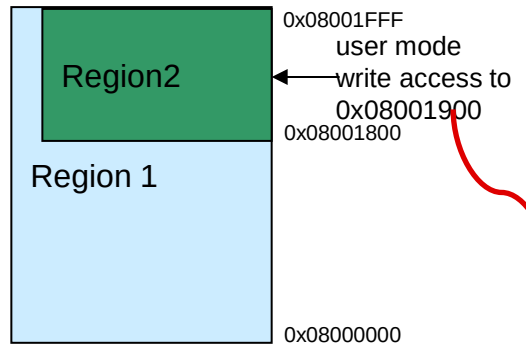
- Strongly-ordered (so) and Device (dev):
  - Explicit load/stores to strongly-ordered and device regions always produce the exact size and number of transactions.
  - Accesses to strongly-ordered and device regions always appear in the order they are listed in the program.
- Strongly-ordered versus Device:
  - Strongly-ordered access are ordered with respect to *all* other explicit load/stores.
  - Device accesses are only ordered with respect to other device accesses.
- Normal (norm):
  - Load/stores to normal memory regions may result in any size and number of transactions.
    For example: Two neighboring half-word stores might be merged into a single-word write.
  - With respect to ordering, accesses to normal memory may be reordered.
- Examples:
  - load-norm-A, load-dev-B, load-dev-C, load-norm-D could be performed as ADBC, or even DBCA;
  - load-norm-A, load-so-B, load-so-C, load-norm-D must be performed as ABCD.

Memory Protection Unit: Memory Regions

- Base Address
  - Defines start of memory address range
  - Has to be multiple of region size (e.g. 256 byte region aligned on 256 byte boundary)
  - Non-size aligned regions might result in unpredictable behavior
- Region size: From 32B up to 4GB
- Region attributes:
  - Define access permissions for a region
  - Memory type (strongly ordered, normal, device)
  - Shared, non-shared
  - Non-cachable
  - Write-through cachable
  - Write-back cachable

Memory Protection Unit: Overlapping Memory Regions & Sub-regions

- Overlapping regions:
  - Higher-numbered region defines access permission.
  - Provides more flexibility to protect memory which is not region-size aligned.

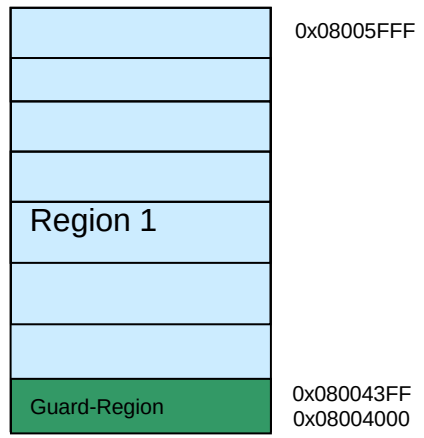


Region 1:
- User mode Read/Write

Region 2:
- Privileged Write

→ **Data Abort**

- Sub-regions:
  - Each region can be split into 8 equal size, non-overlapping sub-regions.
  - Sub-regions can be enabled/disabled in the CP15 (MPU Region Size and Enable Register).
  - Region sizes below 256 bytes do not support sub-regions.



Region 1:
- Has 8 sub-regions
- Sub-region 1 is disabled

→ **Data Abort**

For more information

- **SafeTI Web Page: www.ti.com/safeti**
- **Hercules Web Page: www.ti.com/hercules**
  - Data sheets
  - Technical Reference Manual
  - Application notes
  - Software & tools downloads and updates
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- **Hercules Safety Microcontrollers Training Series training.ti.com/hercules**
  - Cortex-R Processor Architecture
  - Peripherals
  - Software
  - Functional Safety
- **For questions about this training, refer to the Engineer-2-Engineer Support Forum www.ti.com/hercules-support**
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