Digitally Controlled High Efficiency and High Power Density PFC Circuits

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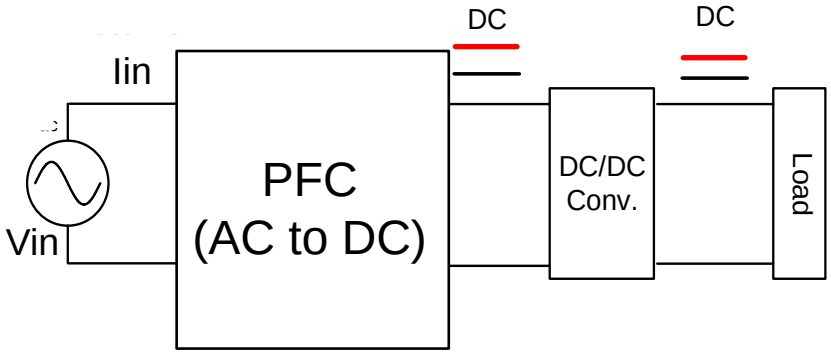
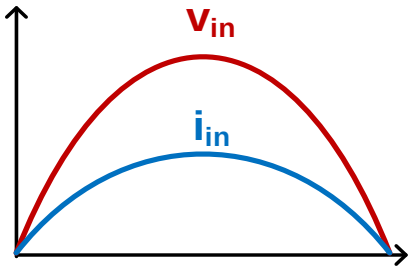
C2000 Digital Power System Solutions

Detailed Agenda

- PFC Stage, PF, THD, Modes of Operation, Evolution of PFC Circuits
- 3Ph Interleaved CCM Totem Pole PFC Ref Design (TIDM-1007)
  - Overview
  - Software Structure
  - Digital Control Design
  - Experimental waveforms and test data
  - Improvements in efficiency, Transient Response & Power Factor
- 2Ph Interleaved TRM Totem Pole PFC Ref Design (TIDA-0961)
  - Overview
  - Challenges and Solutions
  - Software Structure
  - Experimental waveforms and test data

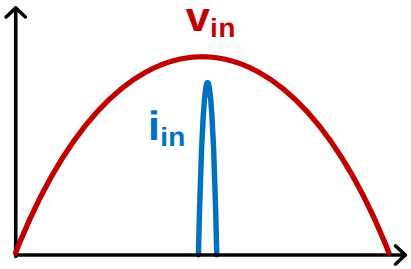
PFC Stage, Power Factor & THD





Sinusoidal Current. PF ≅ 1

Good

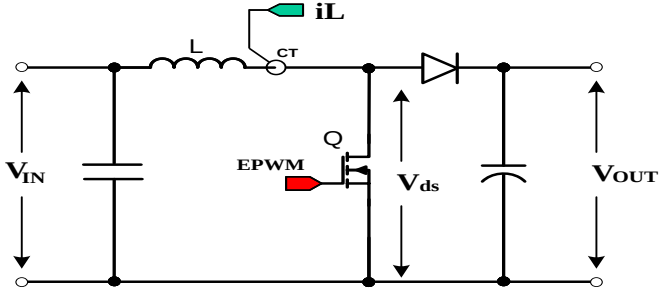


Non Sinusoidal Current. PF ≪ 1

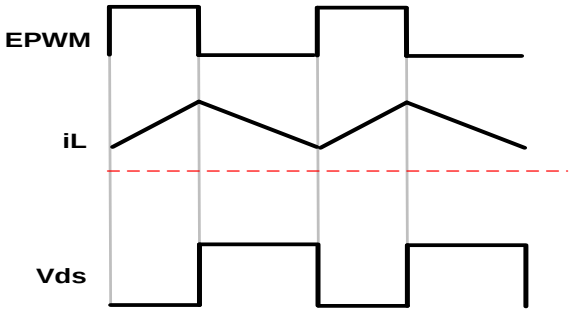
BAD

- Power Factor is affected by Distortion factor(K_d) and Displacement factor (K_θ)
  - $PF = \frac{I_{rms,1}}{I_{rms}} \cos\theta = KdK_{\theta,}$ where θ is the phase angle between fundamentals of V_{in} and i_{in}
- THD is affected by Distortion factor
  - THD = $\sqrt{\{(I_{rms}/I_{1,rms})^2 - 1\}}$. $I_{rms,1} = I_{rms}$ implies $K_d = 1$. Then THD = 0.
- PFC circuit is controlled to achieve PF ≅ 1 and THD ≈ 0 in AC to DC conversion

PFC Modes of Operation – CCM, DCM & TRM

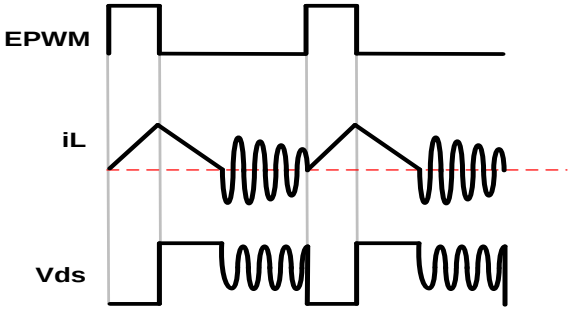


CCM Mode of operation



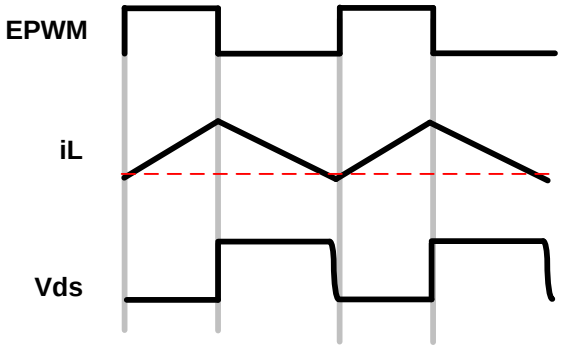
CCM Mode TIDM-1007
Fixed Frequency

DCM Mode of operation



TIDM-2PHILPFC (under light load)
Fixed Frequency

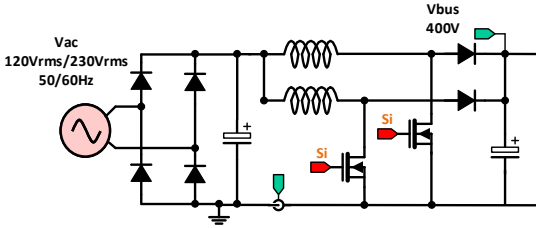
TRM/CRM/BCM Mode of operation



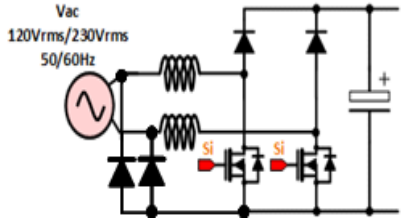
CRM Mode TIDA-00961,
Variable Frequency

Evolution of PFC Circuits

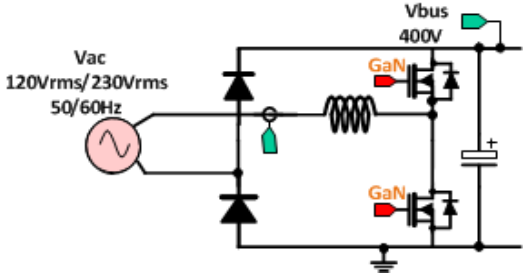
Interleaved Boost PFC TIDM-2PHILPFC



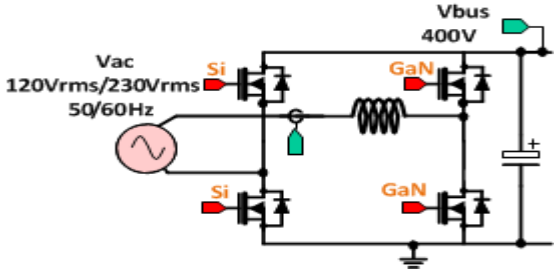
Bridgeless PFC BLPFCKIT



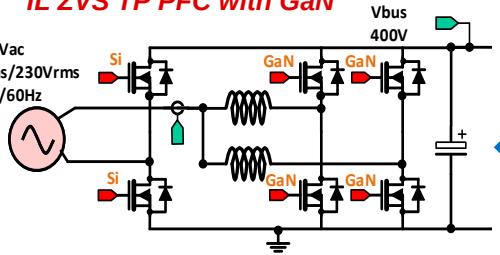
Traditional Totem Pole PFC



ZVS Totem Pole PFC



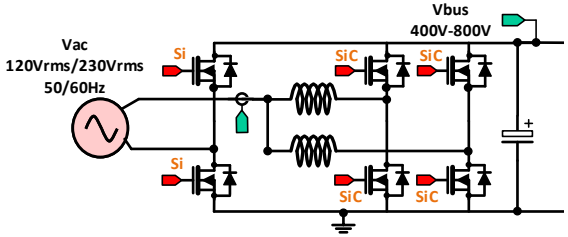
IL ZVS TP PFC with GaN



CCM Mode TIDM-1007
CRM Mode TIDA-00961

IL ZVS TP PFC with SiC

CCM Mode TIDA-01604



➢ *Challenges in Totem Pole Bridgeless PFC*

- Control Design: Voltage and Current Loops
- Zero crossing current spike/ distortion
- Meeting Spec : Power Factor, THD, Efficiency

TIDM-1007

Interleaved CCM Totem Pole PFC Reference Design

C2000 System Solutions: Digital Power

TIDM-1007 Interleaved CCM TP PFC

Features

- GaN based Totem Pole 1PH PFC with three interleaved phases using LMG3410 & controlled using C2000 MCU
- Power Spec
  - Input: 80-260 Vac , 50/60Hz
  - Output: 400V DC
  - Power: 3.3KW at 220Vrms &1.6KW at 110Vrms
  - Efficiency : > 98.67% peak efficiency
- Low total harmonic distortion (THDi) < 2% (at low line)
- 100 kHz PWM switching
- Soft starting for totem pole bridge
- Phase shedding to enable higher efficiency
- Non Linear control loop to reduce voltage spikes

Applications

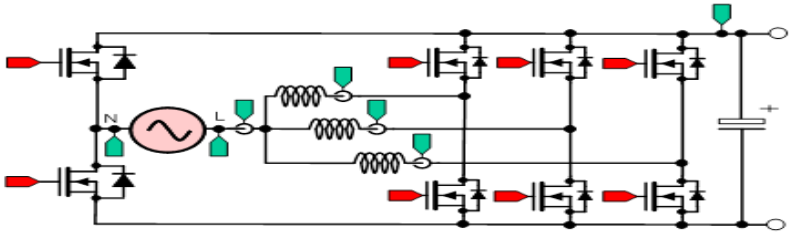
- On –board chargers for EV
- Telecom Rectifiers
- Other industrial applications

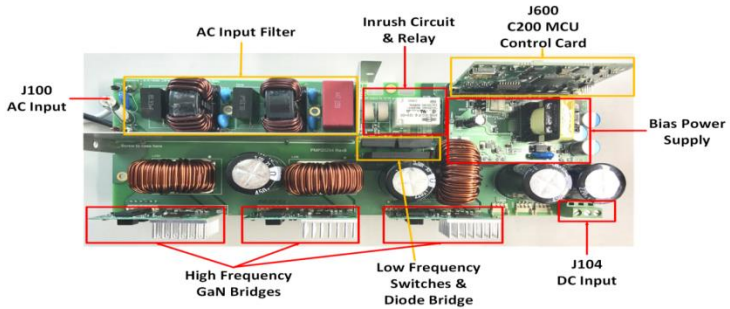
Tools & Resources

- **Key TI Devices:** TMS320F28075, LMG3410, UCC27714D, UCC28740, UCC24636

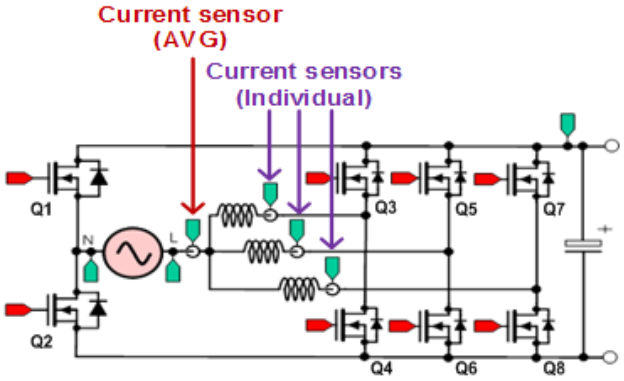
Benefits

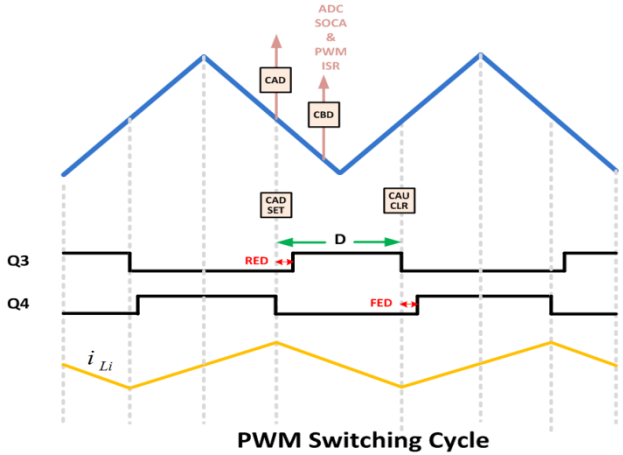
- High power density design, with form factor matching OEM specifications
- TI-GaN with integrated gate drivers - greater integration.
- High performance C2000 controller enables superior and advanced control scheme to be implemented
- poweSUITE support enables easy adaptation of software





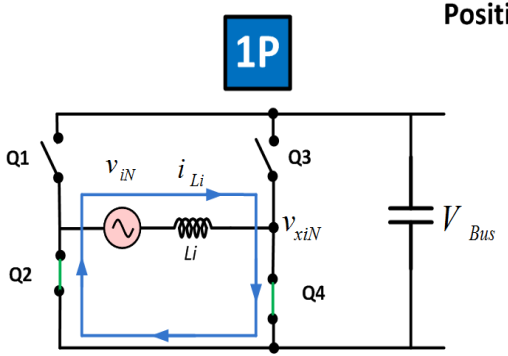
CCM TP PFC Operation

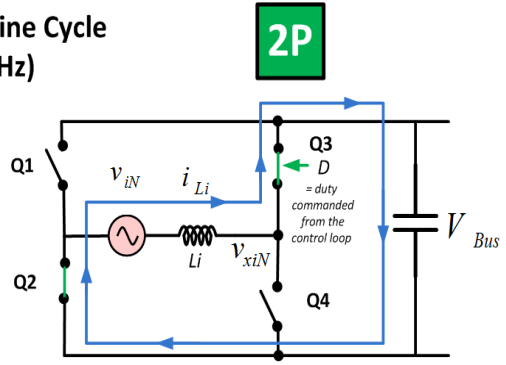




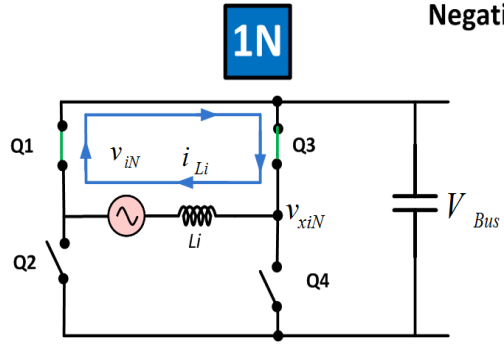
PWM Switching Cycle

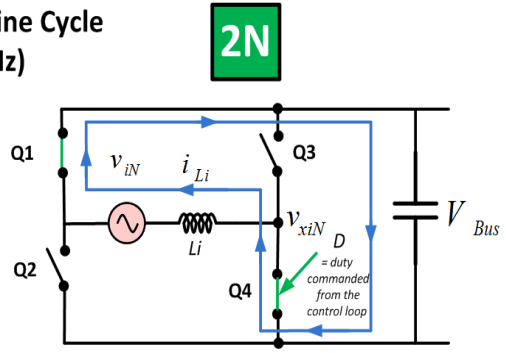
Positive Vin Line Cycle (50/60 Hz)





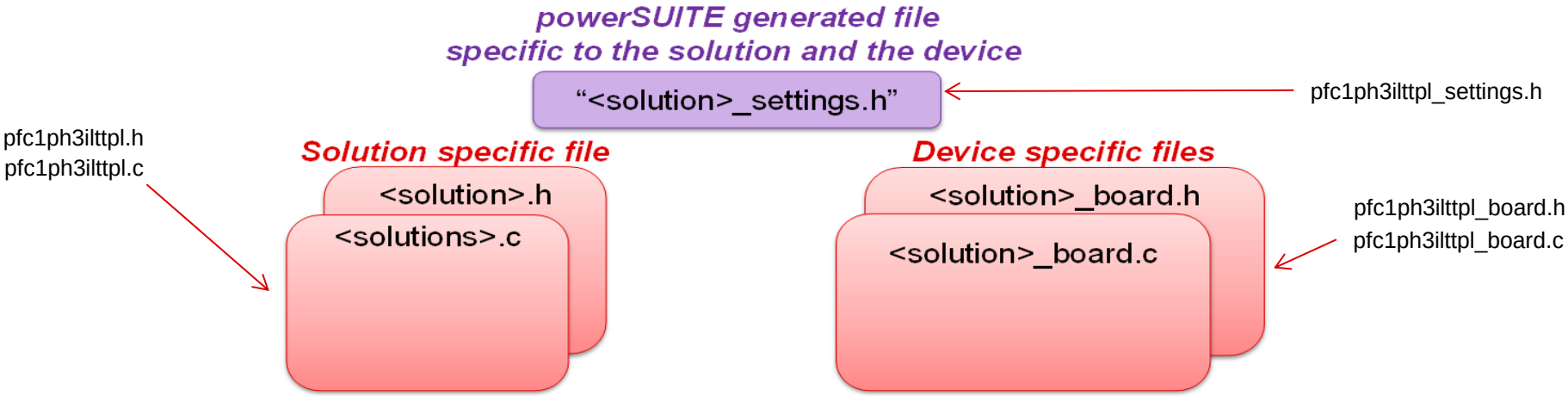
Negative Vin Line Cycle (50/60 Hz)





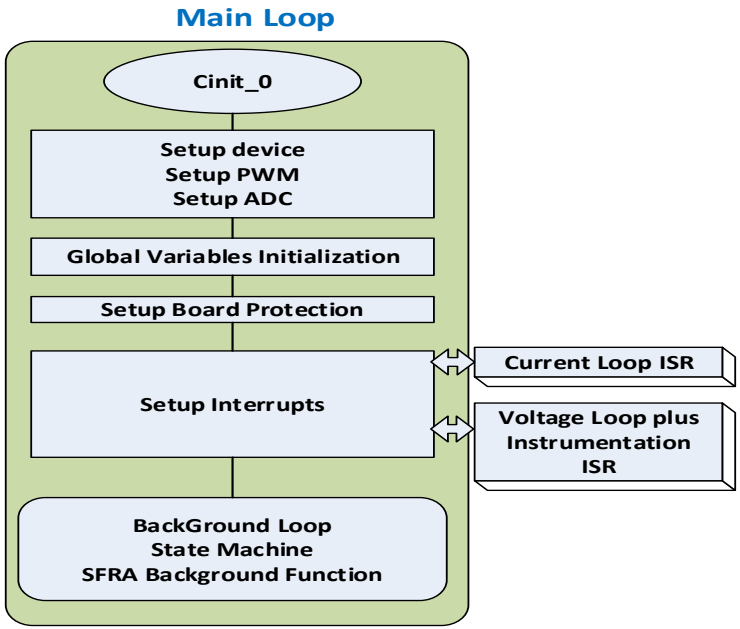
CCS Software Structure

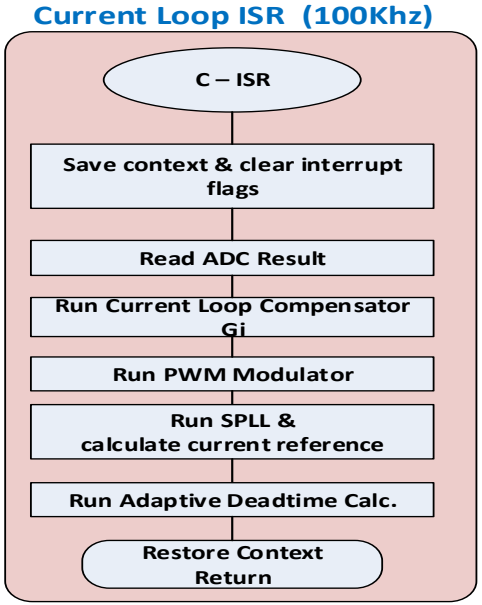
CCS Project Structure

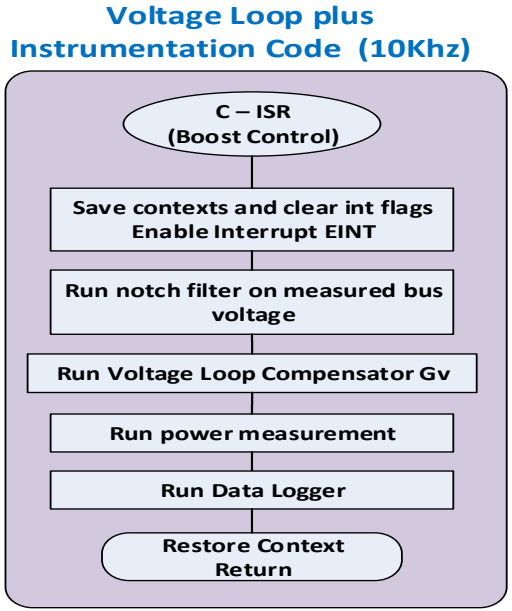


Incremental Build Levels to Simplify the Design of the System

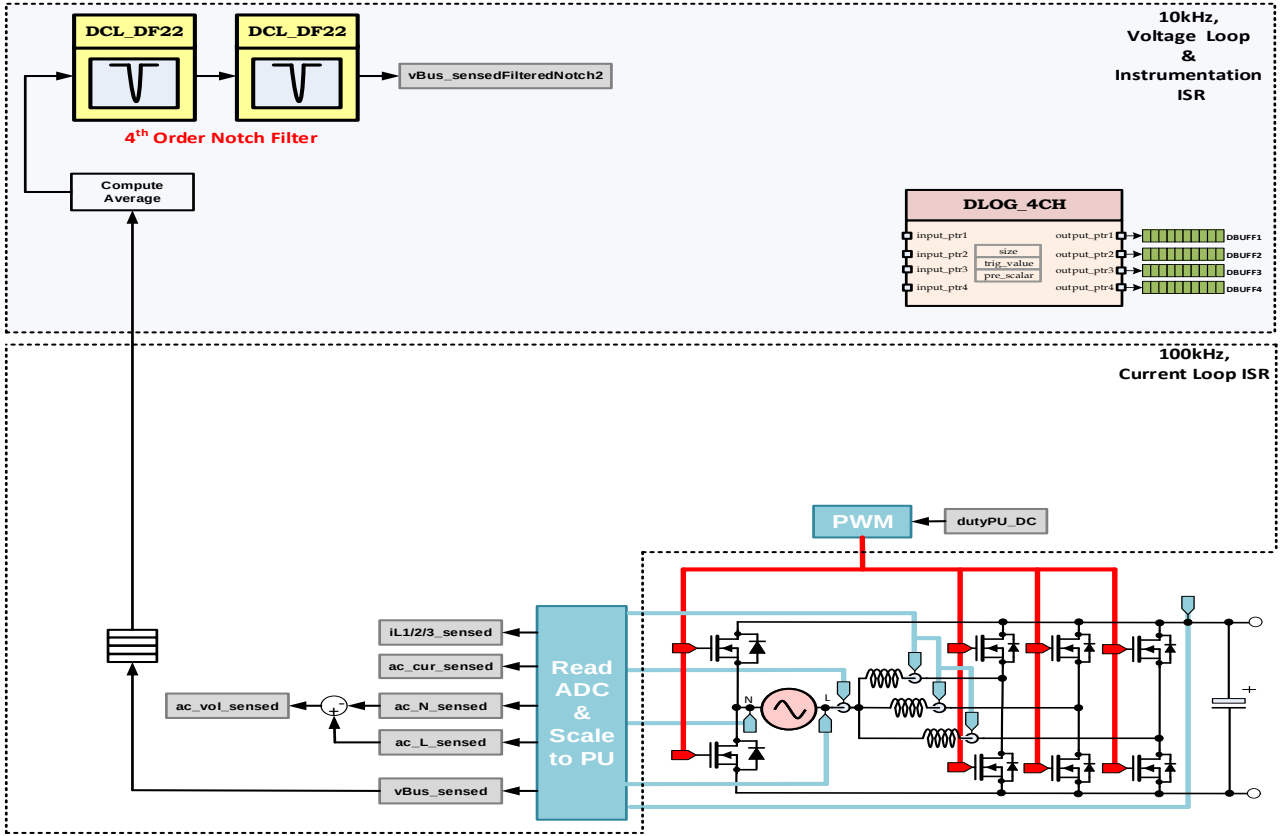
INCR_BUILD 1 : Open Loop Check under DC input
INCR_BUILD 2 - DC : Closed Current Loop Check under DC input
INCR_BUILD 2- AC : Closed Current Loop under AC input
INCR_BUILD 3 : Closed Voltage and Current Loop under AC input



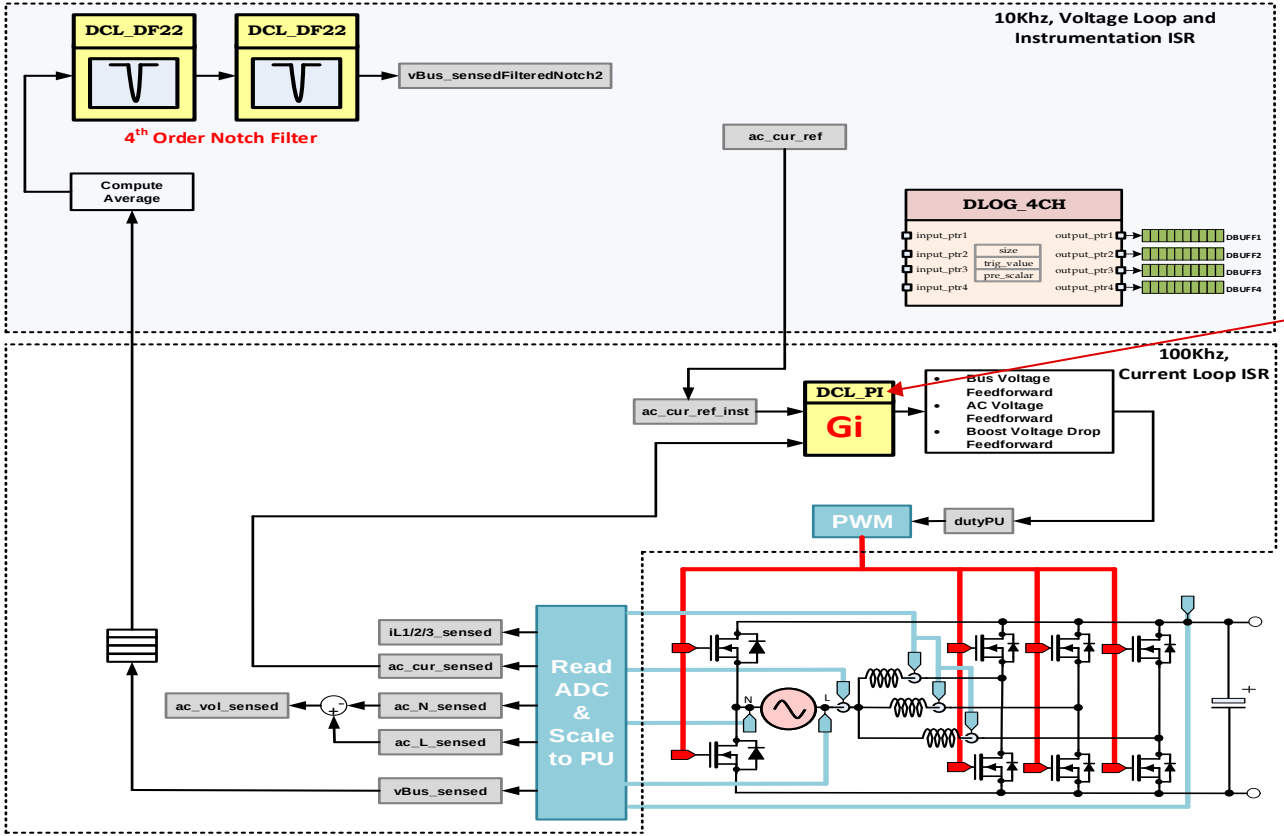




Build Level 1- DC: Open Loop Check

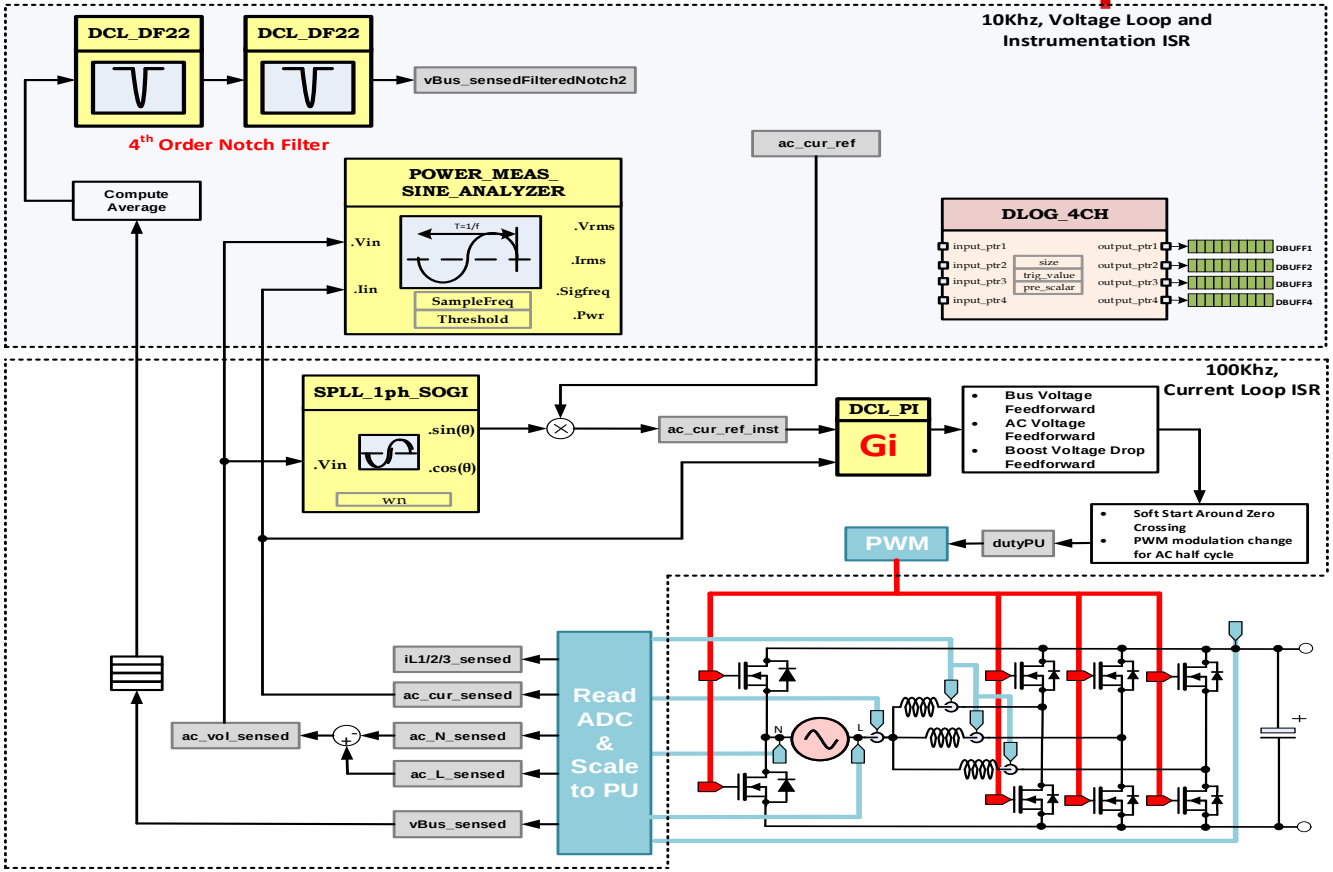


Build Level 2 - DC: Closed Current Loop

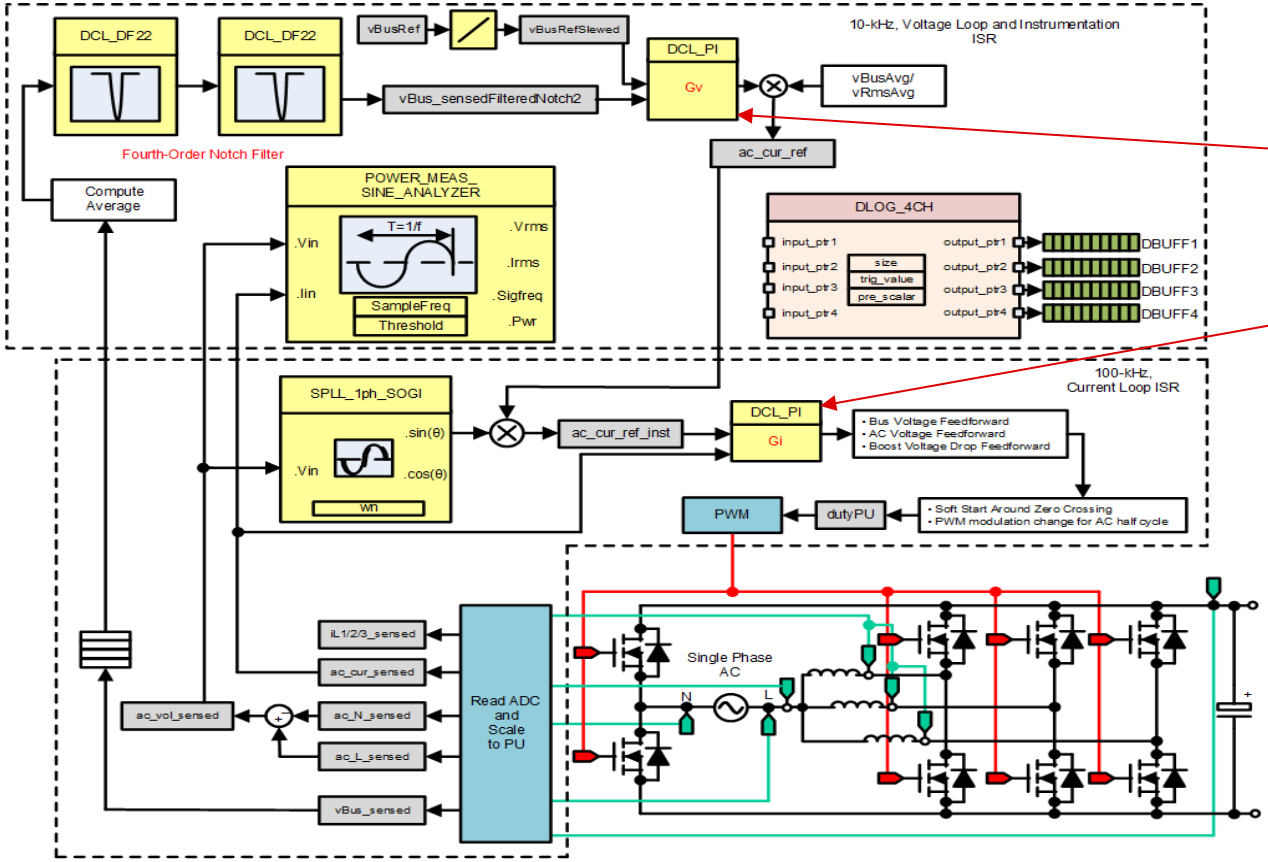


PFC Current Controller Gi

Build Level 2 - AC: Closed Current Loop



Build Level 3: Closed Voltage and Current Loop

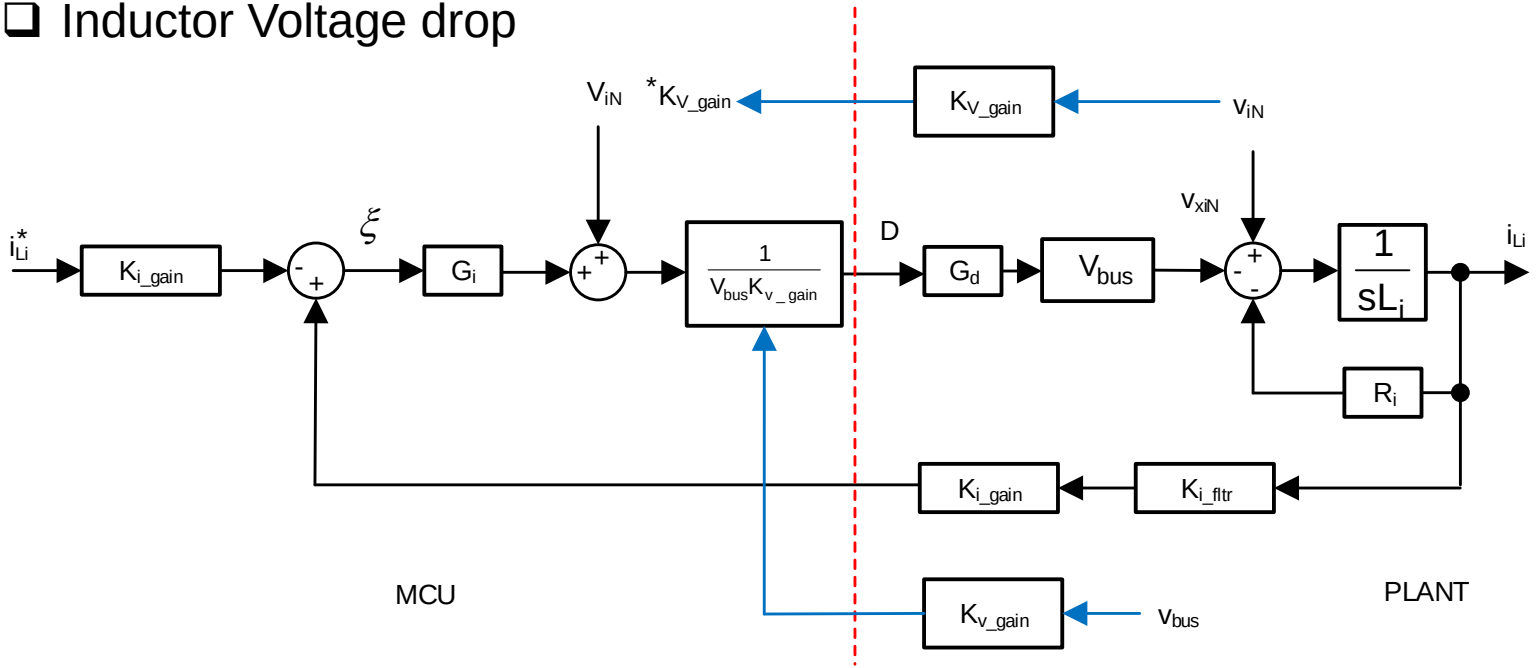


CCM TP PFC
Control Loop Design

CCM TP PFC Current Loop Model

Current Loop Model includes sync FET control and feedforward for

- ❑ Input AC voltage
- ❑ Output bus voltage
- ❑ Inductor Voltage drop



CCM TP PFC Voltage Loop Model

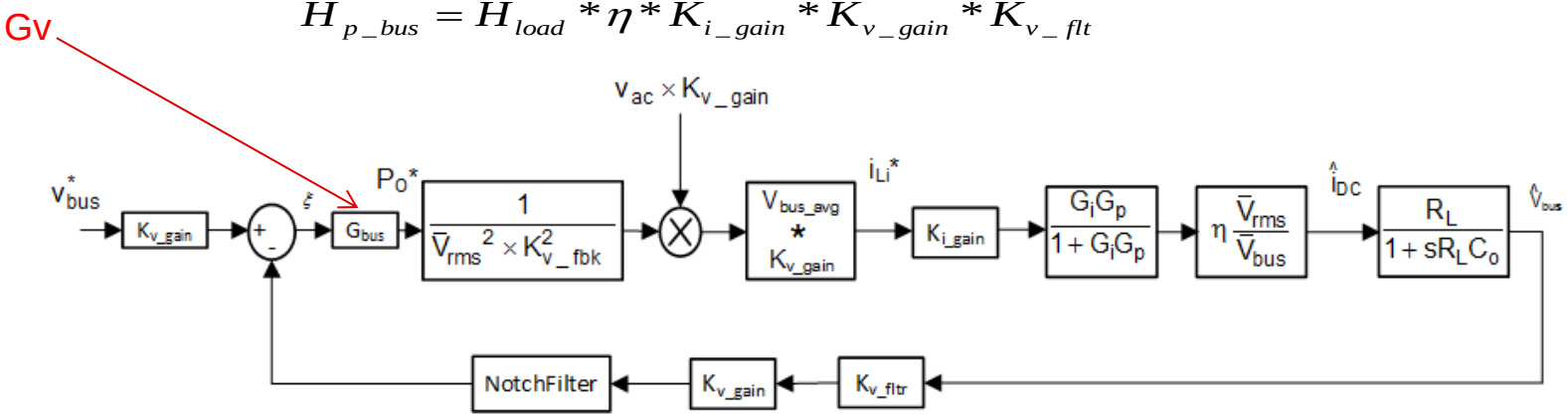
- Small signal model of the DC Bus regulation loop is developed by linearizing the following power equation

$$i_{DC} v_{bus} = \eta v_{Nrms} i_{Nrms} \Rightarrow \hat{i}_{DC} = \eta \frac{\overline{V}_{Nrms}}{\overline{V}_{bus}} i_{Li}$$

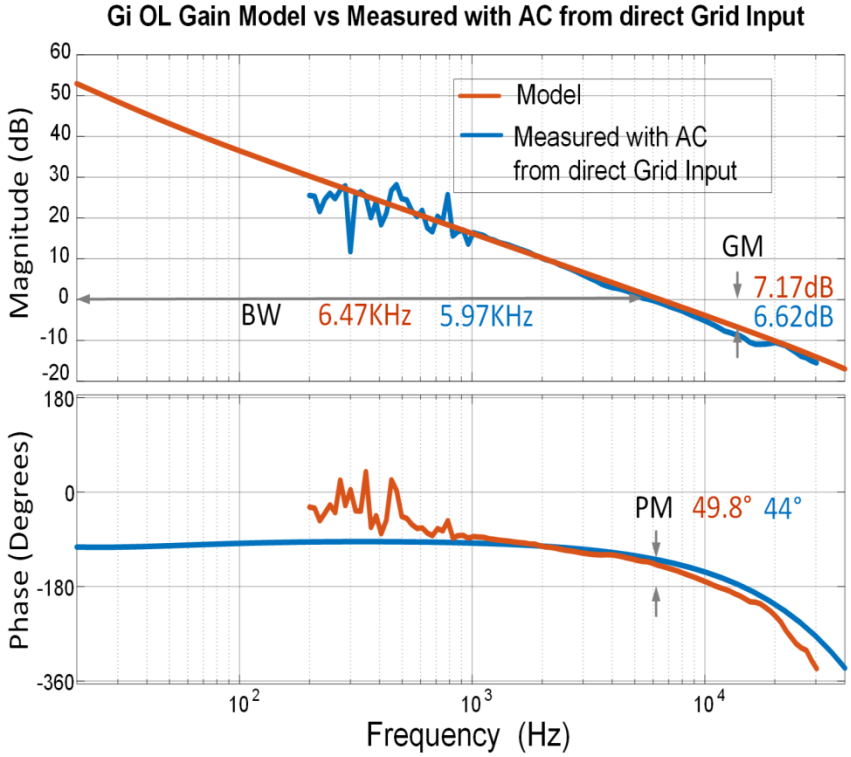
- For resistive load the bus voltage and current are relating as $\hat{v}_{bus} = \frac{R_L}{1 + sR_L C_o} \hat{i}_{DC}$

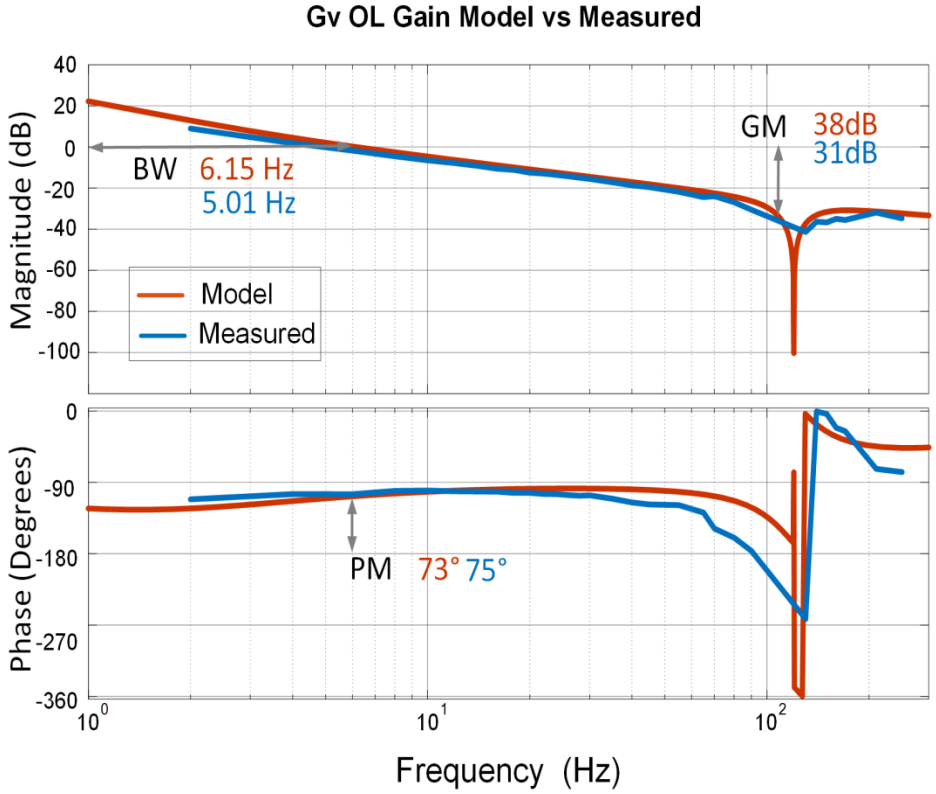
- The plant model for the bus control can be written as below:

$$H_{p\_bus} = H_{load} * \eta * K_{i\_gain} * K_{v\_gain} * K_{v\_flt}$$

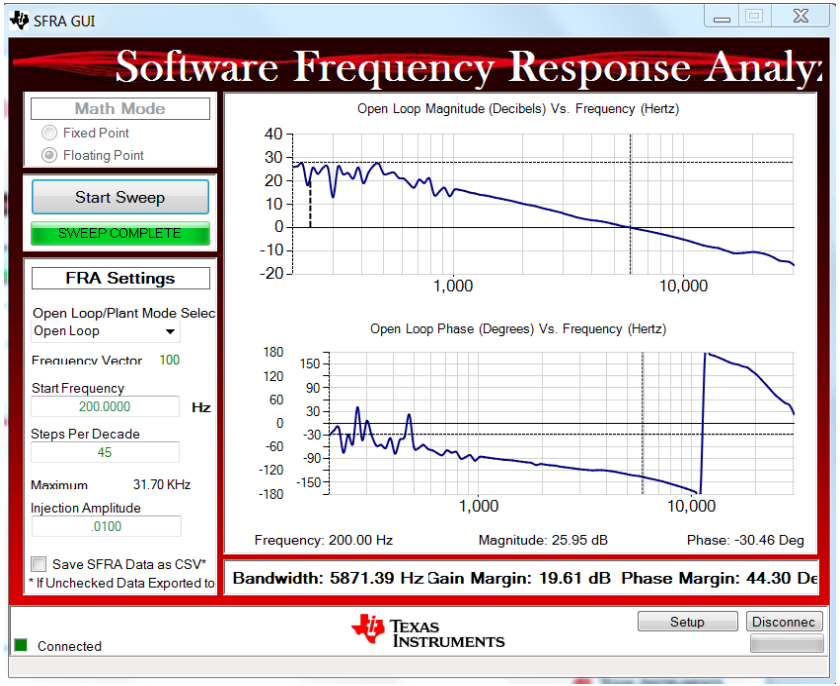


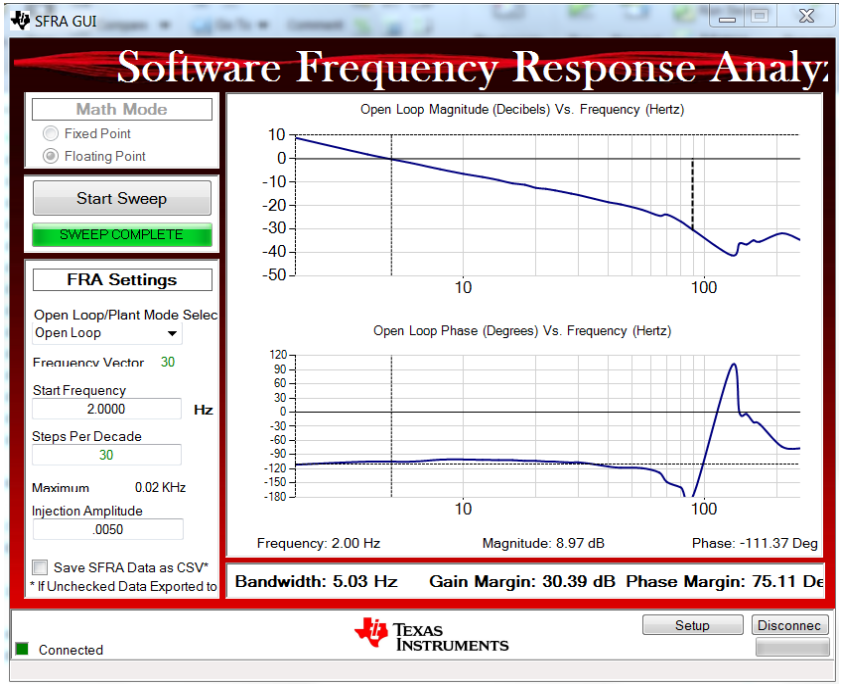
Current & Voltage Loop Verification Using SFRA





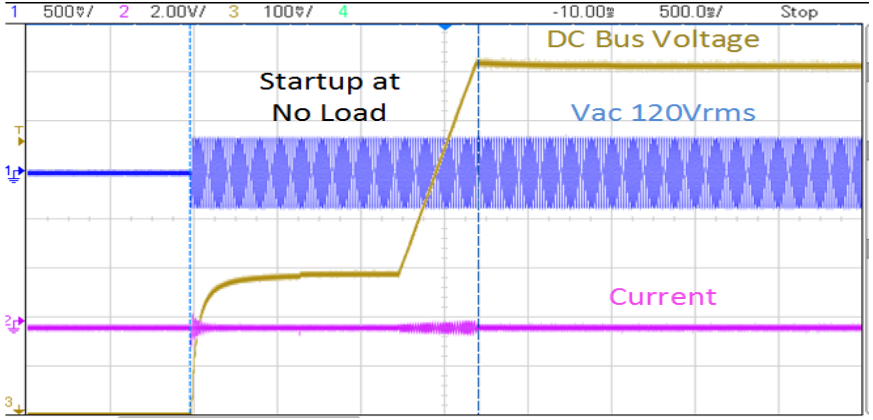
CCM TP PFC Current & Voltage Loops SFRA Plots

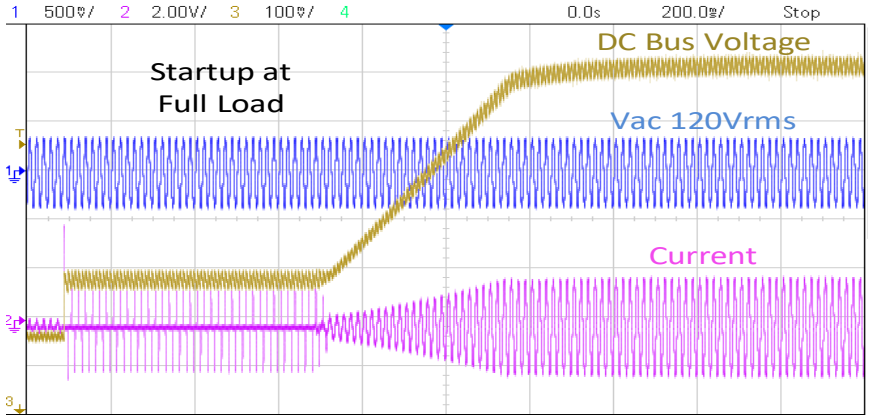




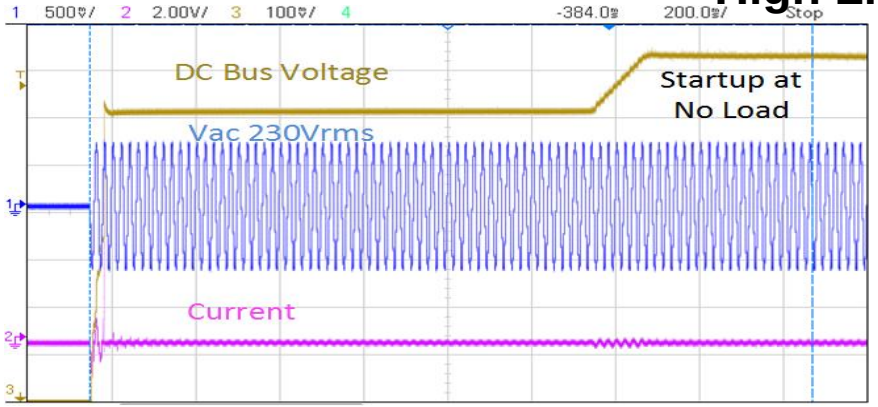
Startup Waveforms

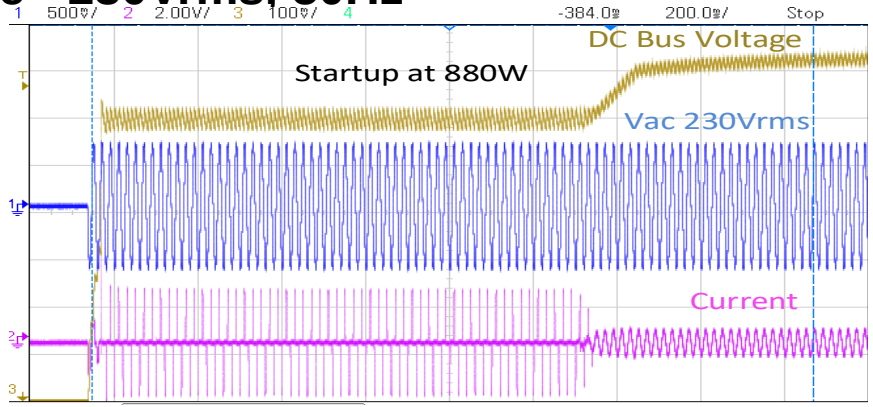
Low Line - 120Vrms, 60Hz





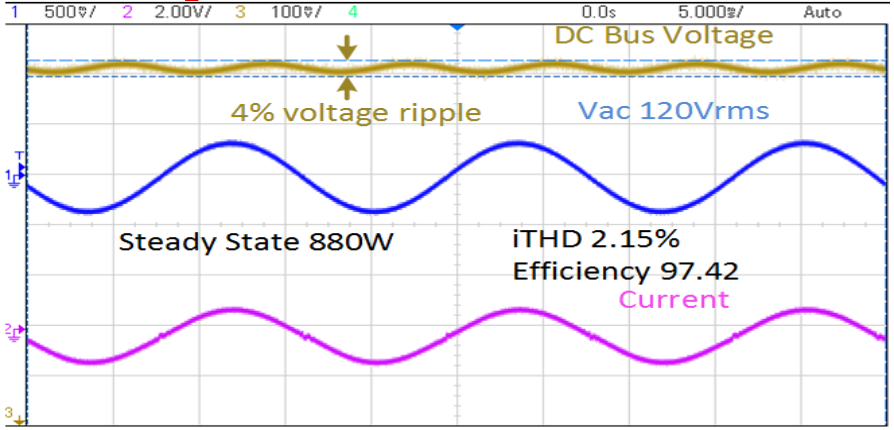
High Line - 230Vrms, 50Hz

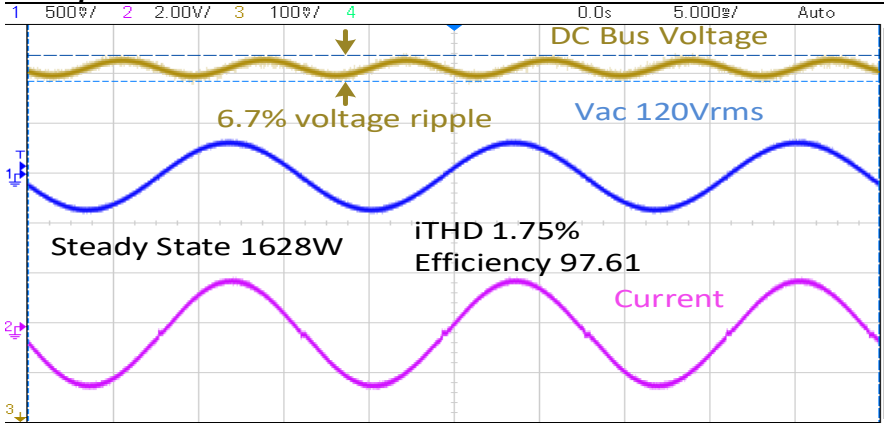




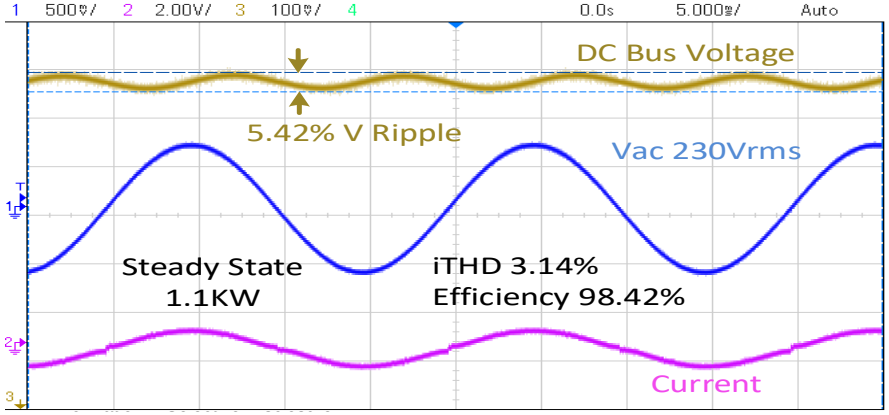
Steady State Waveforms

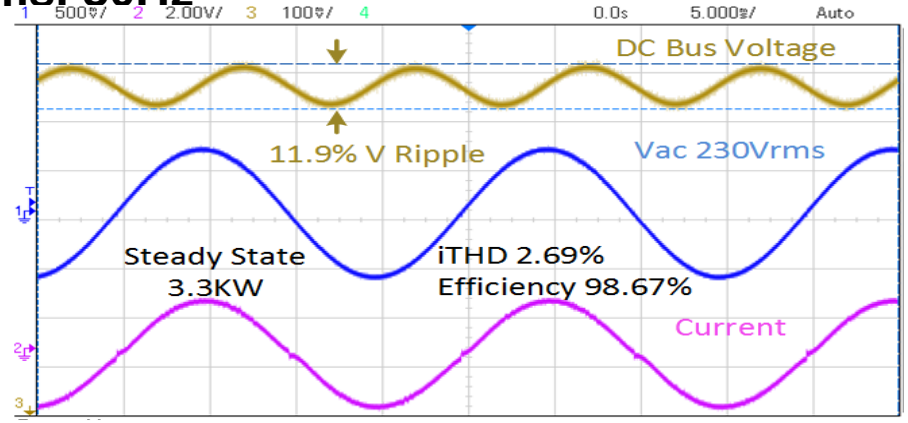
120Vrms, 60Hz





230Vrms, 50Hz





PF, THD & Efficiency

Vin	Vout	Pin	Iout	Pout	Efficiency %	iTHD%	PF	%Rated Load
120.31	381.98	27.97	0.876	18.01	68.15%	52.20%	0.8336	1.1%
120.40	381.95	47.38	0.095	36.22	80.72%	32.21%	0.8898	2.3%
120.30	381.97	84.57	0.191	72.92	88.68%	19.50%	0.9786	4.6%
121.40	381.95	121.40	0.286	109.21	91.57%	13.50%	0.9891	6.8%
120.05	382.02	154.27	0.375	143.47	92.98%	10.54%	0.9927	9.0%
119.86	382.01	301.30	0.750	286.36	95.14%	5.50%	0.9974	17.9%
119.49	382.01	444.40	1.120	427.76	96.30%	4.16%	0.9987	26.7%
119.42	382.03	579.10	1.469	561.40	96.94%	2.89%	0.9950	35.1%
119.16	382.02	721.30	1.837	701.80	97.30%	2.42%	0.9995	43.9%
119.02	382.05	863.00	2.202	841.50	97.52%	2.15%	0.9995	52.6%
118.78	381.96	1007.20	2.573	983.30	97.64%	1.92%	0.9995	61.5%
118.63	382.08	1152.00	2.944	1125.30	97.69%	1.82%	0.9995	70.3%
118.40	382.08	1298.40	3.319	1268.20	97.70%	1.72%	0.9994	79.3%
118.25	382.08	1442.00	3.685	1408.30	97.69%	1.87%	0.9991	88.0%
118.03	382.08	1593.80	4.071	1555.50	97.65%	1.80%	0.9991	97.2%
117.98	382.05	1716.40	4.449	1674.80	97.61%	1.75%	0.9991	104.7%

Low Line

Vin	Vout	Pin	Iout	Pout	Efficiency %	iTHD%	PF	%Rated Load
230.22	382.00	25.84	0.047	18.02	69.61%	62.00%	0.5758	0.6%
230.88	381.98	44.13	0.779	36.22	82.12%	53.00%	0.7784	1.1%
230.73	381.99	81.29	0.191	72.94	89.73%	33.08%	0.9247	2.3%
230.70	381.97	117.95	0.286	109.23	92.61%	23.10%	0.9599	3.4%
230.68	381.98	151.28	0.372	142.16	94.03%	18.20%	0.9775	4.4%
230.43	382.00	292.24	0.736	281.41	96.29%	9.15%	0.9936	8.8%
230.25	382.03	435.90	1.109	423.62	97.18%	6.12%	0.9938	13.2%
230.06	382.06	576.40	1.473	562.86	97.66%	4.85%	0.9972	17.6%
229.80	382.05	856.80	2.201	841.00	98.15%	4.16%	0.9974	26.3%
229.70	382.11	1140.10	2.935	1121.90	98.42%	3.14%	0.9989	35.1%
229.52	382.08	1418.80	3.659	1398.40	98.57%	2.42%	0.9993	43.7%
229.28	382.08	1699.20	4.386	1676.40	98.66%	2.74%	0.9995	52.4%
229.06	382.09	1977.70	5.106	1951.90	98.71%	2.46%	0.9996	61.0%
229.09	382.11	2261.50	5.840	2232.40	98.73%	2.62%	0.9995	69.8%
228.91	382.11	2548.30	6.580	2515.60	98.73%	2.50%	0.9994	78.6%
228.86	382.11	2840.60	7.332	2803.20	98.71%	2.89%	0.9990	87.6%
228.51	382.14	3132.80	8.083	3091.10	98.69%	2.80%	0.9989	96.6%
228.22	382.03	3439.10	8.873	3392.30	98.67%	2.69%	0.9988	106.0%

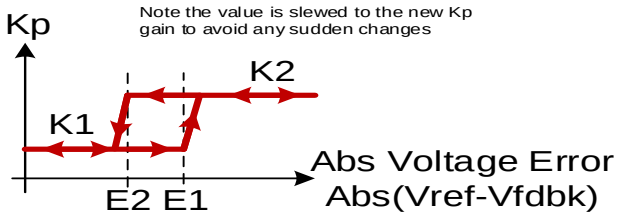
High Line

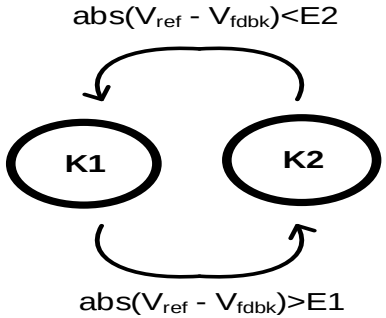
Improved Transient Response

- Non Linear Voltage Loop

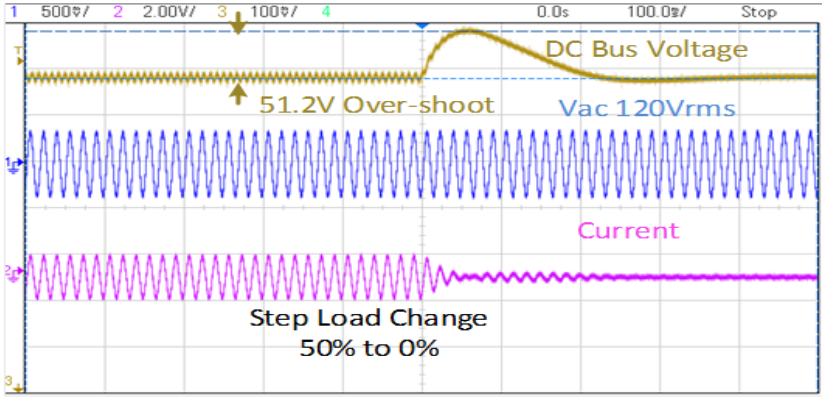
Fast Transient Response - Non Linear Voltage Loop

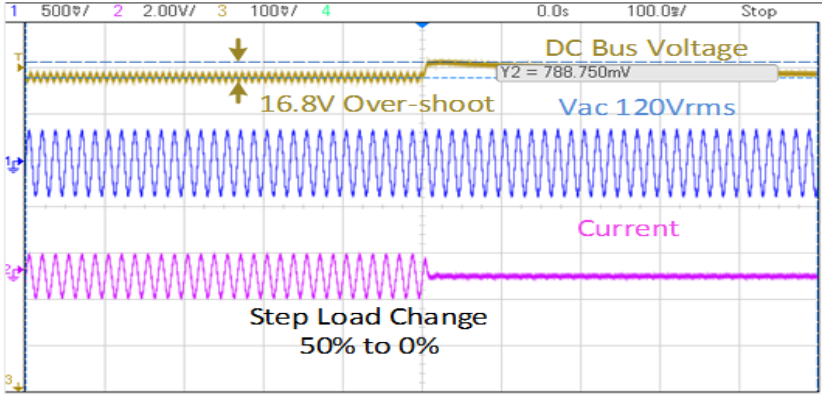
- Use parallel form of DCL Controller, enables to prevent integral term causing issues when changing voltage loop gain



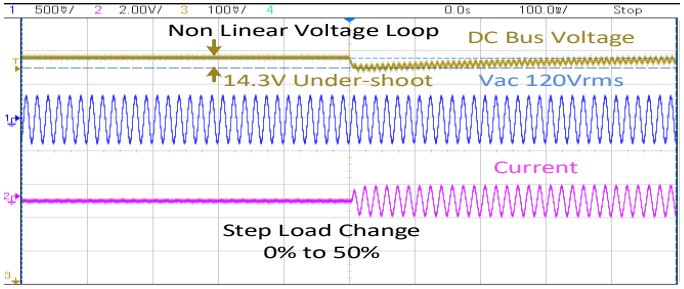


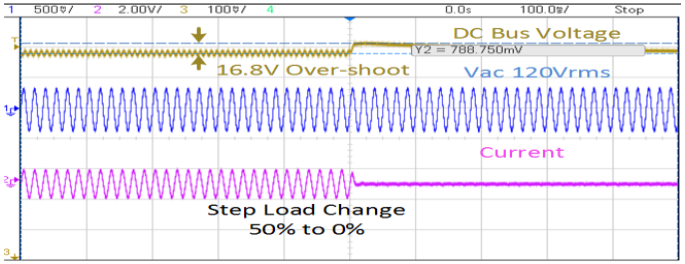
Voltage Transient Waveform : Linear Voltage Loop (Left), Non Linear Voltage Loop (Right)
Overshoot Reduced from 51.2V to 16.8V

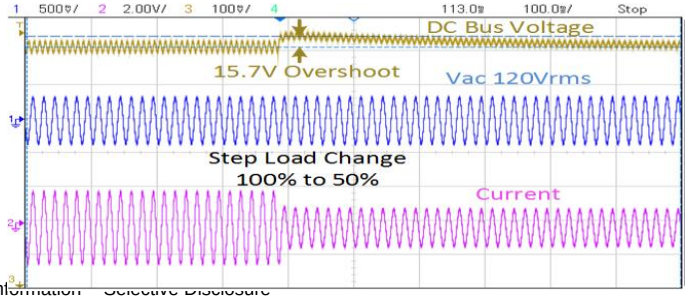


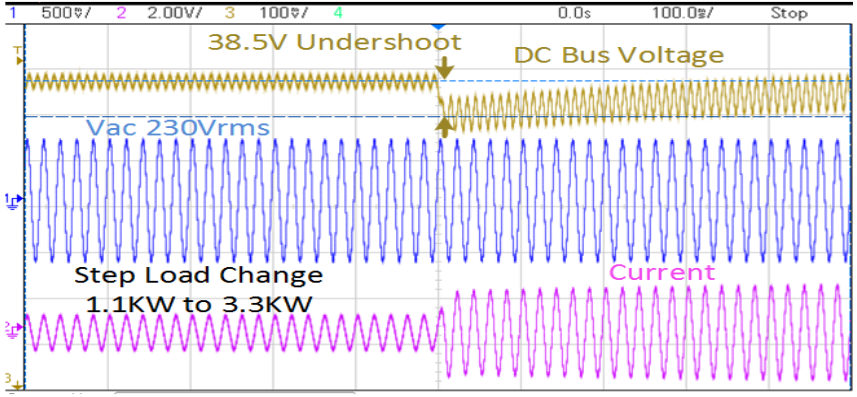


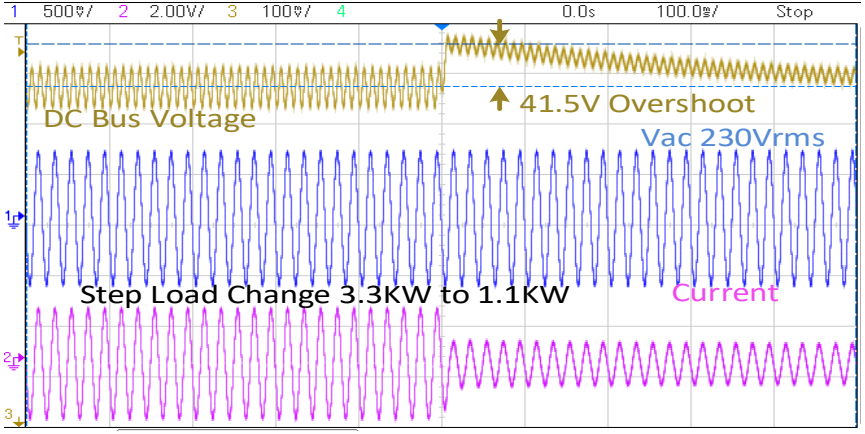
Transient Response at 120/230Vrms









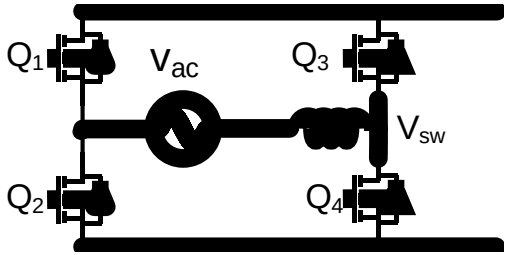


Improved Efficiency

- **Adaptive Deadtime**

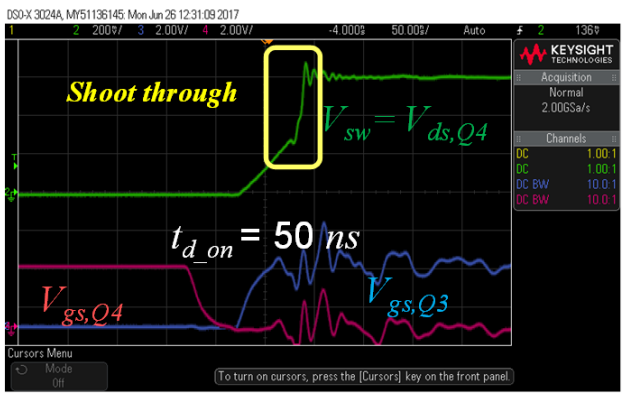
ZVS Operation - Adaptive Dead Time Control

- The optimal dead time calculation
  - Waveforms are provided in different $t_{d,on}$
  - The optimal dead time : $t_{d,on} = \frac{2C_{oss}V_{out}}{i_{L,peak}}$



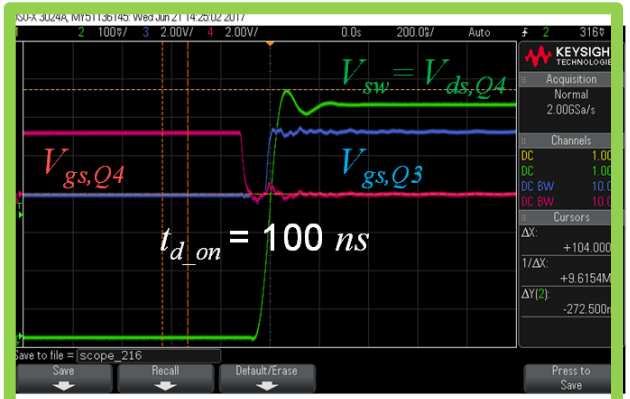
Q4 turns OFF => DT t_{d_on} => Q3 turns ON

BAD



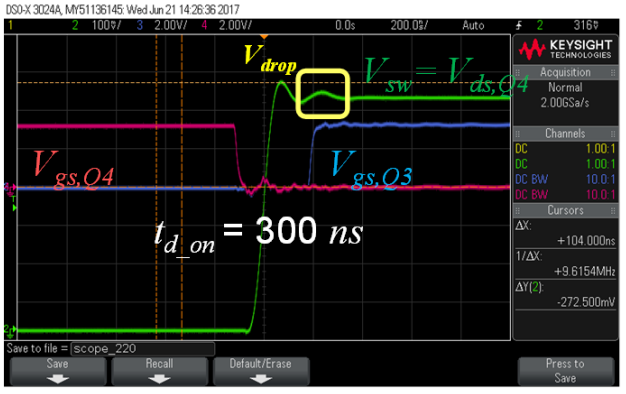
Too short $t_{d,on}$

GOOD



Optimal $t_{d,on}$

BAD

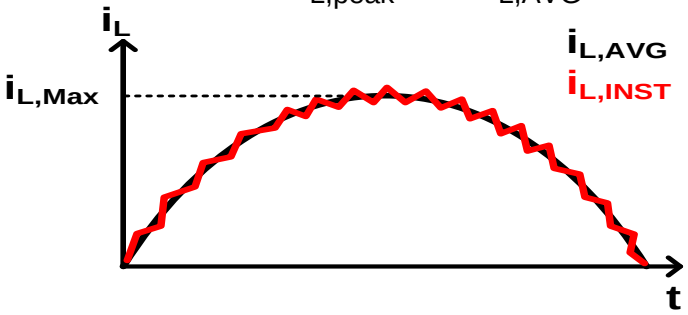


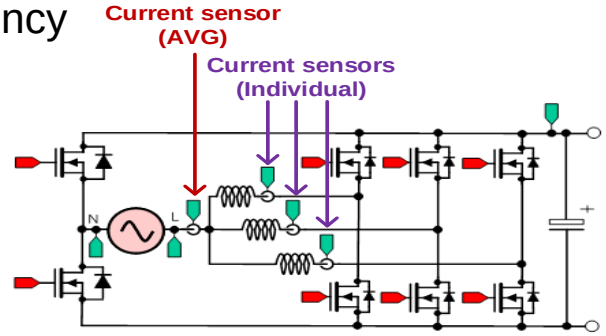
Too long $t_{d,on}$

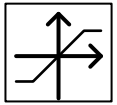
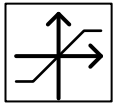
Adaptive Dead Time Control Implementation

In PFC, the operating point changes in every line cycle (60 Hz or 50 Hz), the optimal $t_{d,on}$ should be calculated in real time with respect to $i_{L,peak}$

A.D.T from individual $i_{L,peak}$ and $i_{L,AVG}$ show almost same efficiency

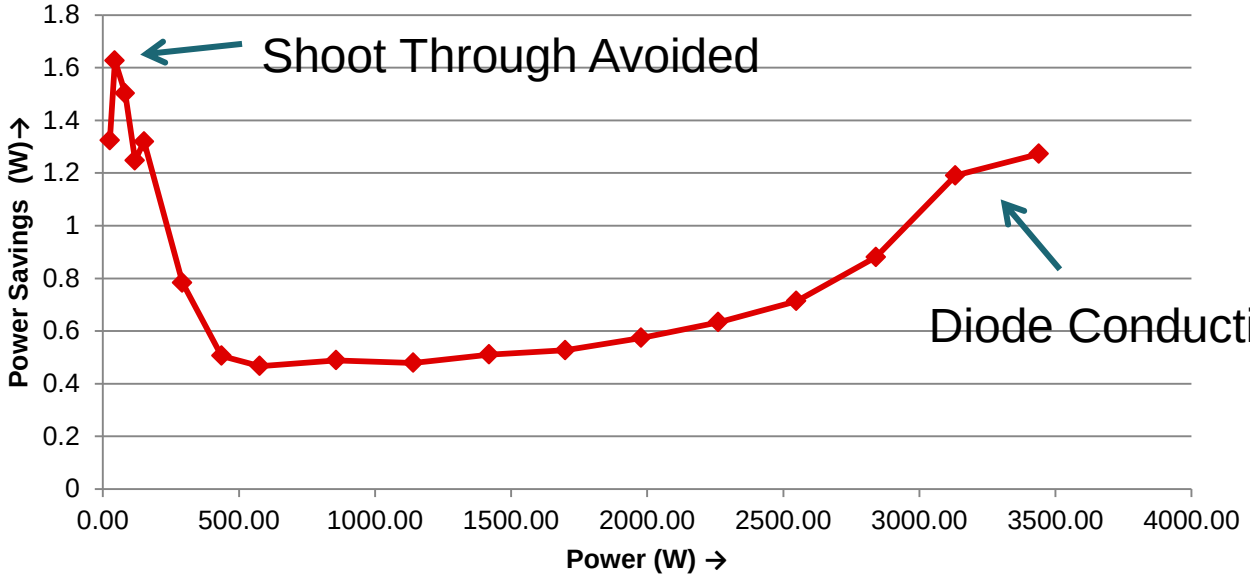




Senseing $i_{L,AVG}$	→	Absolute value function	→	Limitter	→	A.D.T Calculation	→	Limitter	→	Update ePWM DBRED
$i_{L,AVG}$		$\lvert i_{L,AVG} \rvert$				$A.D.T = \frac{2C_{oss}V_{out}}{\lvert i_{L,AVG} \rvert}$				DBRED=A.D.T

Adaptive Dead time Power Savings

Power savings data for using Adaptive Dead Time (20ns-200ns).
Power savings compared to fixed Dead Time of 100ns.



Vin 230V , 50Hz,

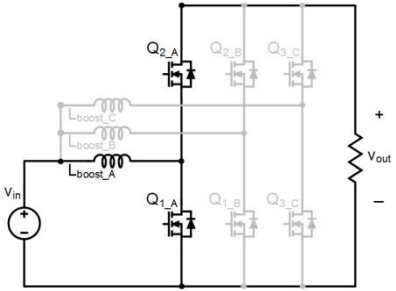
Diode Conduction Optimized

Improved Light Load Efficiency

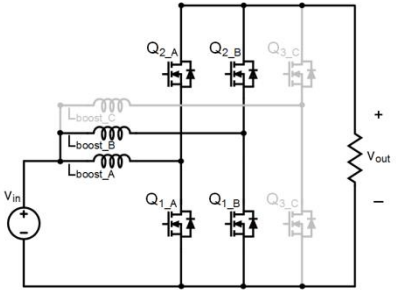
- Phase Shedding Control

Light Load Efficiency Improvement - Phase Shedding

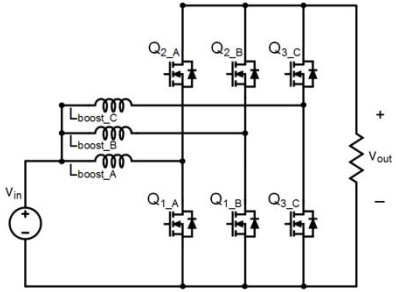
- The concept of phase shedding
  - Phase shedding technique is control the # of operating phases
  - It improves the light load efficiency



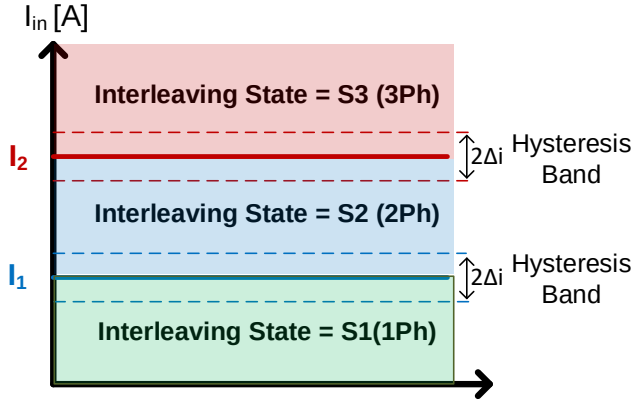
1Phase Operation
(For light load)



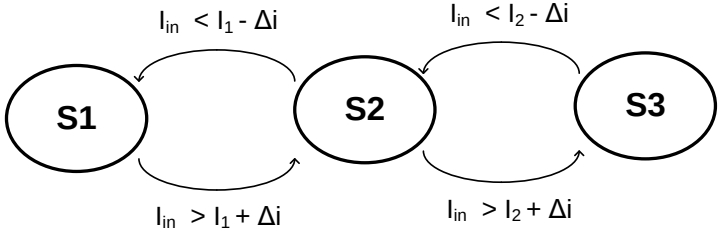
2 Phase Interleaving Operation
(For mid load)



3 Phase Interleaving Operation
(for heavy load)

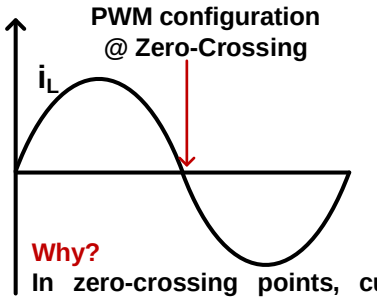


- State-machine for phase shedding control
  - The # of operating phase is determined by state machine
  - $I_{in} < I_1$, 1-Ph has the highest efficiency
    $I_1 < I_{in} < I_2$, 2-Ph has the highest efficiency
    $I_{in} > I_2$, 3-Ph has the highest efficiency
  - Hysteresis Band is used for reliable transition



Phase Shedding Control Implementation

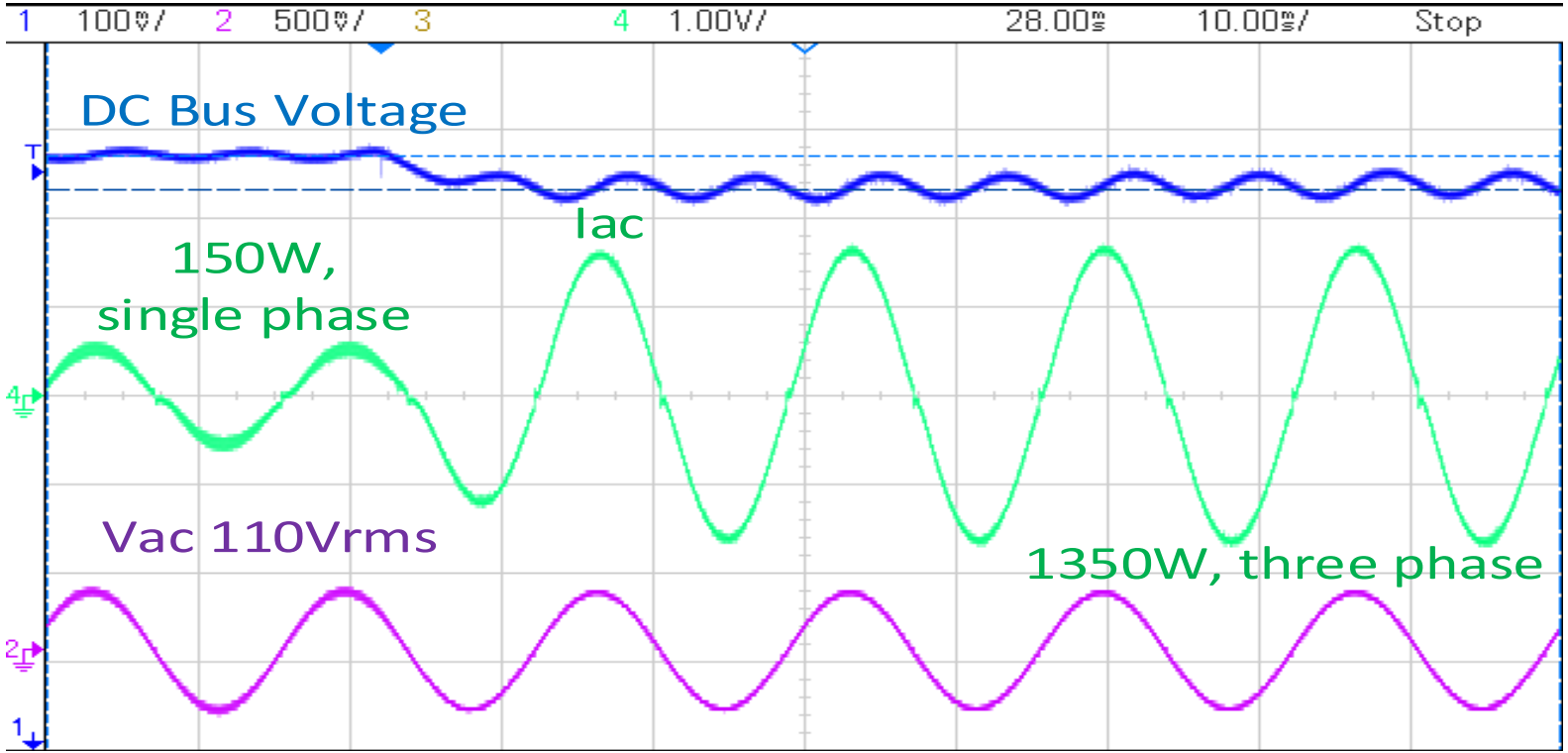
- MCU (F28004x) Implementation
  - The # of phases is determined by state-machine
  - In state transition, PWM settings are changed near zero crossing point (PWM on/off, Phase shift)



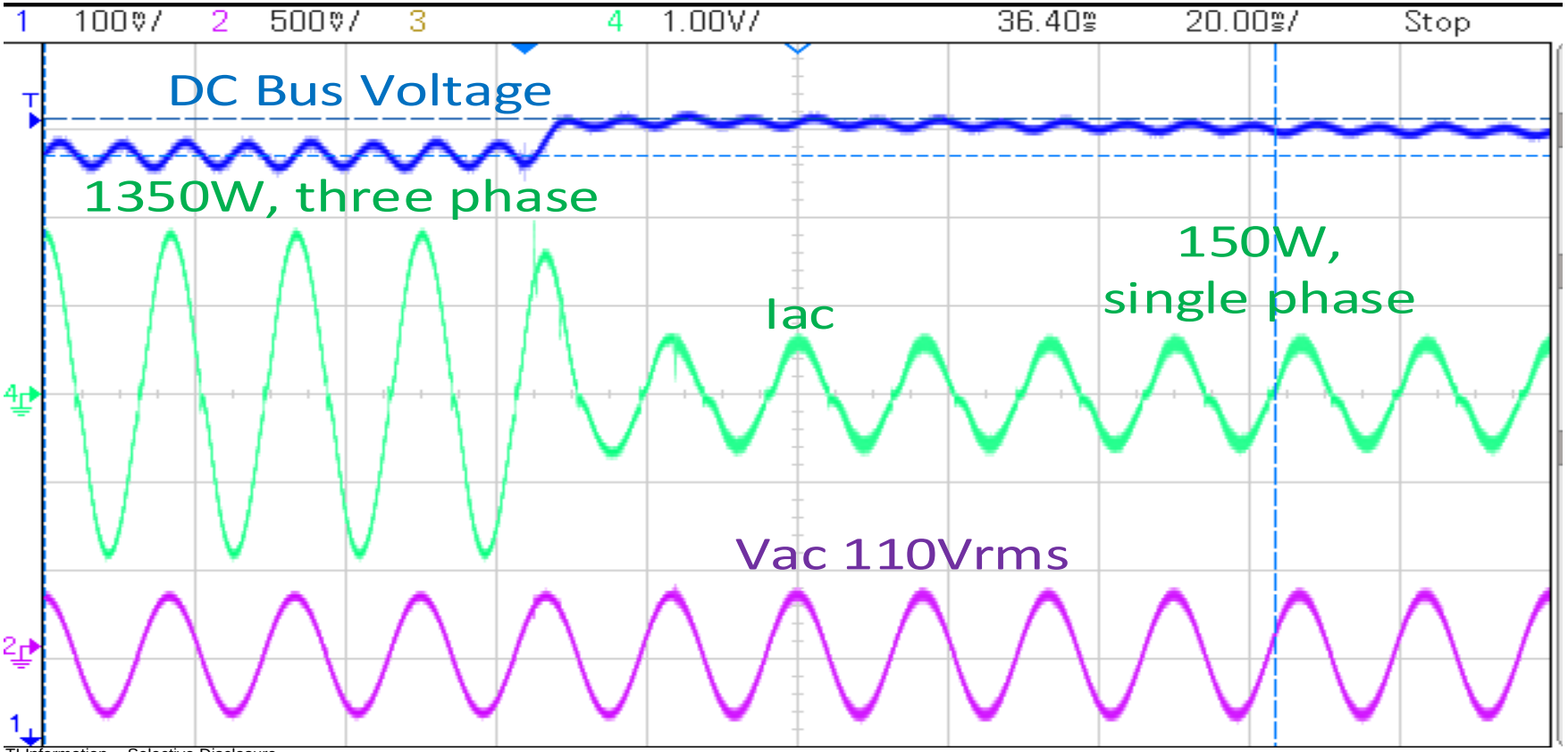
Why?
In zero-crossing points, current goes down to zero and do not introduce disturbance from PWM configuration

Senseing $i_{L,AVG}$	State Machine	Phase ON/OFF	TBPHS Setting
$i_{L,AVG}$	S1 : $I_1 < i_{L,AVG}$	Set GPIO4 = ePWM4 (ON) Set GPIO5 = GPIO (OFF) Set GPIO6 = GPIO (OFF)	ePWM4 TBPHS = 0
	S2 : $I_1 < i_{L,AVG} < I_2$	Set GPIO4 = ePWM4 (ON) Set GPIO5 = ePWM5 (ON) Set GPIO6 = GPIO (OFF)	ePWM4 TBPHS = 0 ePWM5 TBPHS = 180
	S3 : $i_{L,AVG} > I_2$	Set GPIO4 = ePWM4 (ON) Set GPIO5 = ePWM5 (ON) Set GPIO6 = ePWM6 (ON)	ePWM4 TBPHS = 0 ePWM5 TBPHS = 120 ePWM5 TBPHS = 240

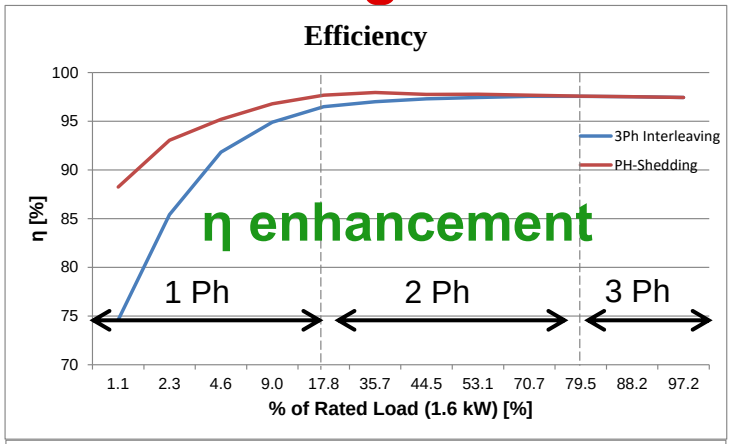
Phase Adding

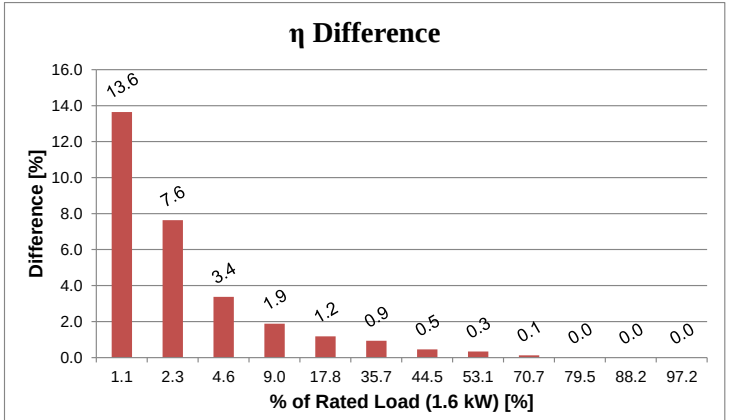


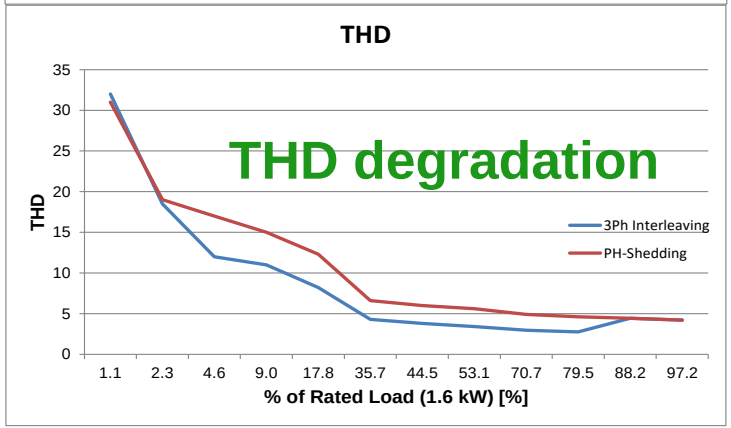
Phase Shedding

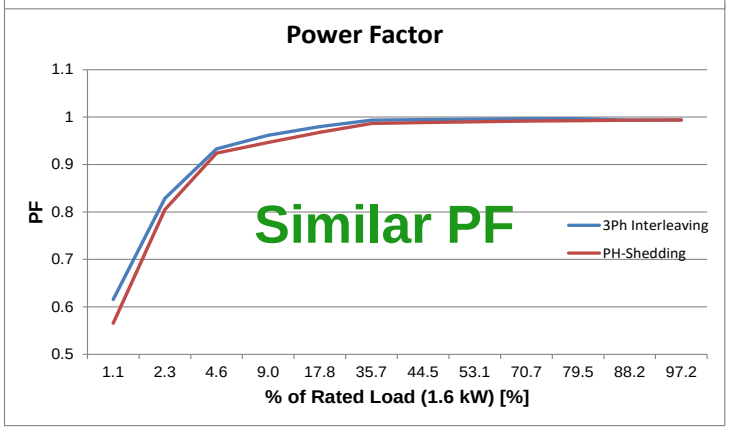


Phase shedding Test Result (120V, 60Hz)

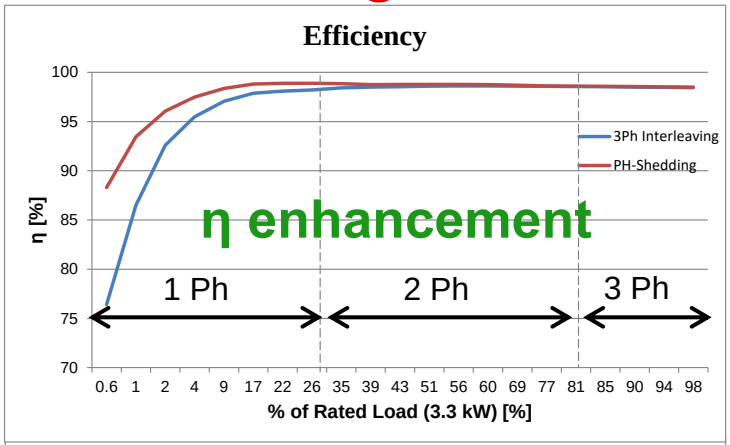


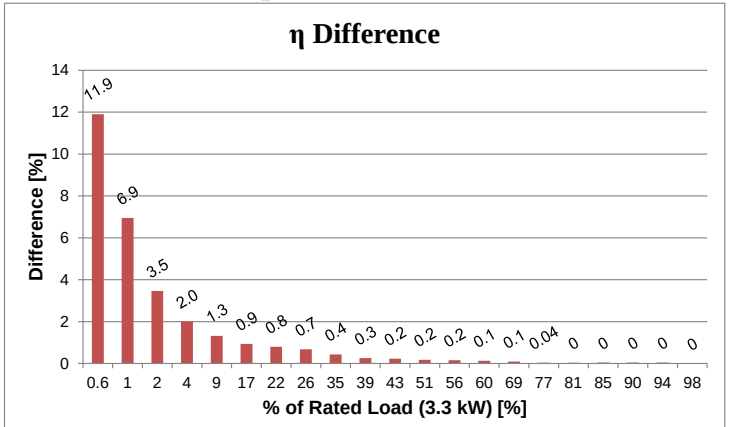


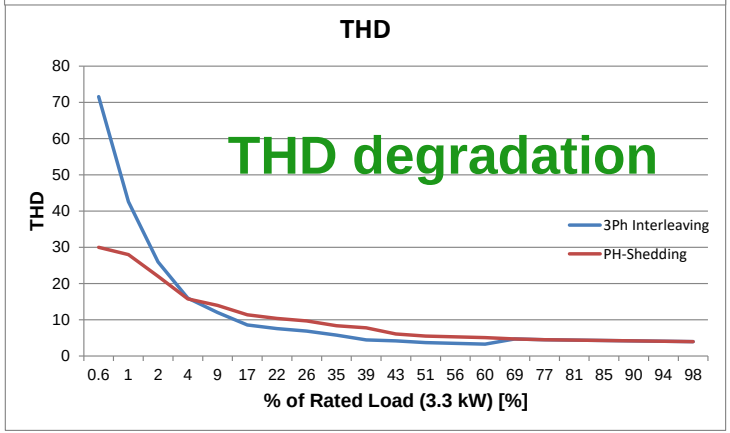


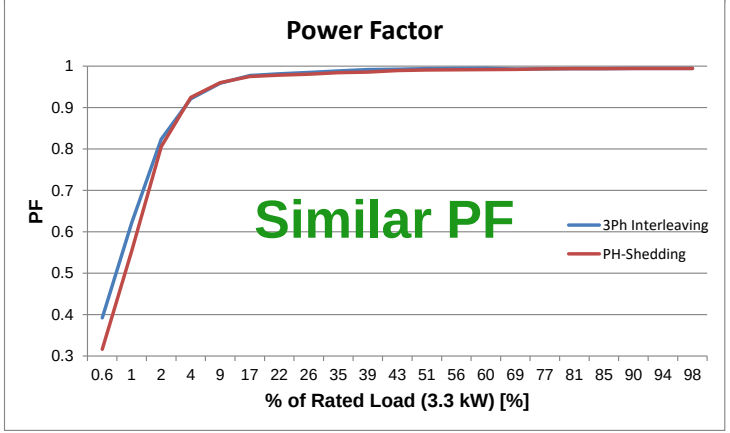


Phase shedding Test Result (230V, 50Hz)







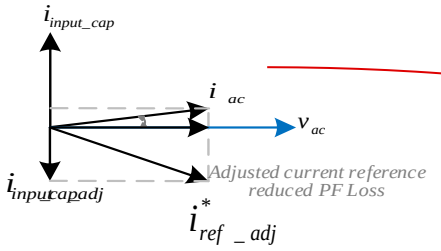


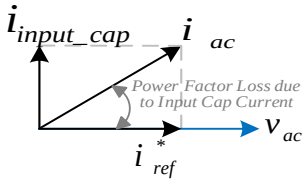
Improved Light Load Power Factor (PF)

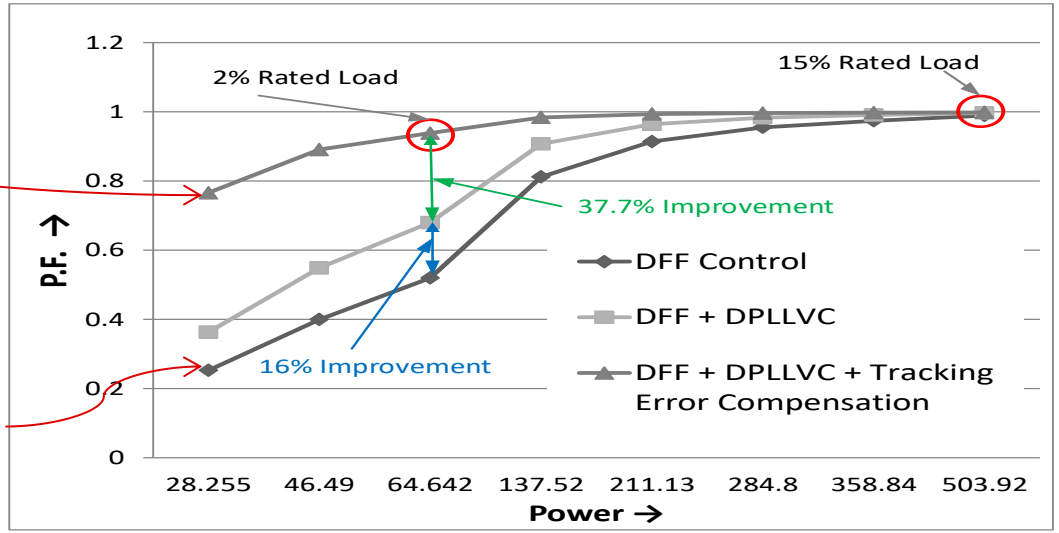
- Input Cap Compensation

Light Load PF Improvement - Input Cap Compensation

- Input capacitor current draw causes significant PF loss at high line and light load
- Execution of SPLL enables Vector Cancellation based techniques to adjust the current reference to compensate for PF loss
- At 10% load the improvement is ~ 18% and at 2% load more than 40% improvement







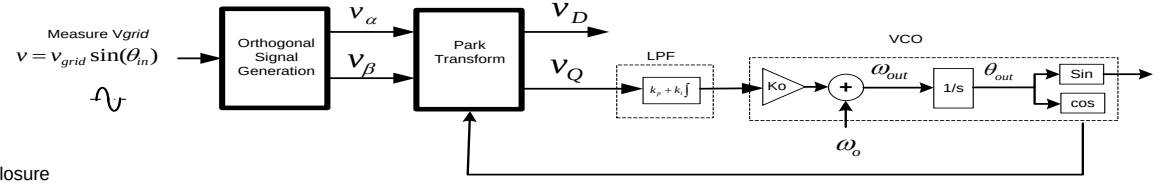
Other Improvements

TP PFC Accurate Zero Cross Detection - SPLL with TMU

- Cost sensitive PFC application uses resistor divider network to sense the AC input voltage.
- Totem Pole PFC PWM driver requires accurate zero crossing detection. This can be specially challenging with the low cost voltage sensing method.
- Phase Locked Loop (PLL) Based AC angle is used to accurately detect the grid angle and change modulation based on that.
- TMU on C28x CPU reduces cycle counts to run the PLL algorithm and enables integration on the current loop which can run at 100-200KHz.

	C28x FPU	C28x FPU + TMU
SPLL_1PH_SOGI	175	115

35% Improvement

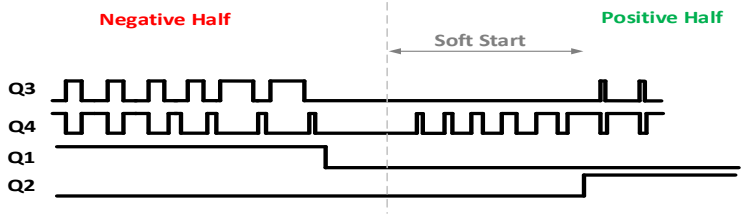


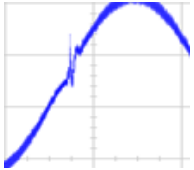
SPLL SOGI Structure

Accurate PWM Generation for IL TP PFC - Type 4 PWM

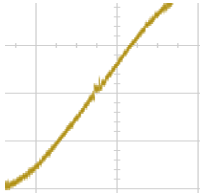
- Interleaved topologies require PWM updates to happen in a give interval of time, otherwise an in-accurate pulse can be applied to the power converter. The time interval reduced with number of phases.

- Totem Pole PFC Topology requires PWM to be started and stopped in a particular sequence to reduce zero current spike. In addition to this the active switch is swapped from positive half to negative half of the AC sine wave.





Zero crossing spike if in-correct SW pulses applied on interleaved TTPL PFC



Zero crossing with Type 4 PWM on interleaved TTPL PFC

- Type 4 PWM features such as **shadowed dead band and shadowed action qualifier** enable accurate generation of PWM pulses in a straight forward manner.

TIDA-0961

Interleaved TRM/TCM/CRM/BCM Totem Pole PFC Reference Design

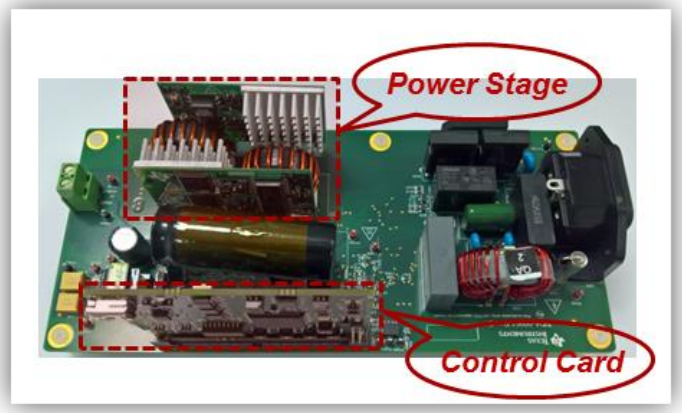
C2000 System Solutions: Digital Power

TIDA-0961 Interleaved TRM Totem Pole PFC

TIDesigns

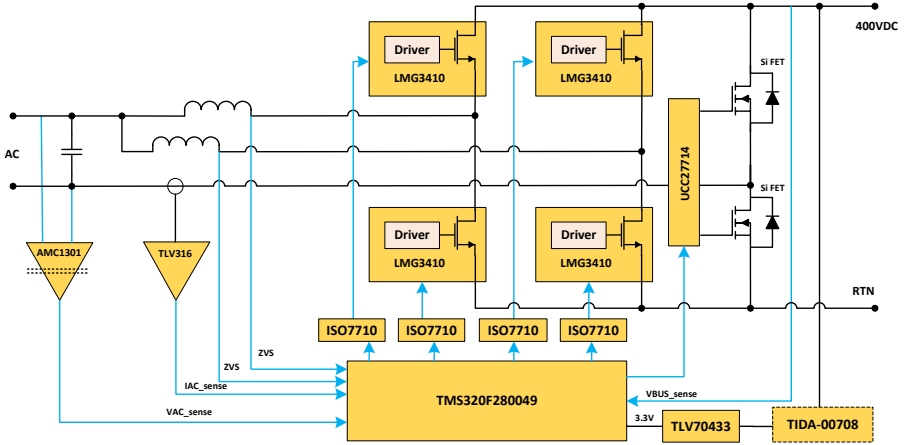
Features

- TMS320F280xx Controller based full digital control PFC
- Wide input voltage range: 85 – 265 VAC
- Output Power: 1.6 KW, 4.1A @ 390V
- Efficiency: 99% ; Power Factor : >0.99
- 200 kHz ~1.2MHz PWM switching
- Compact Form Factor (65 x 30 x 40 mm)
- Power density about **80W/in^3**

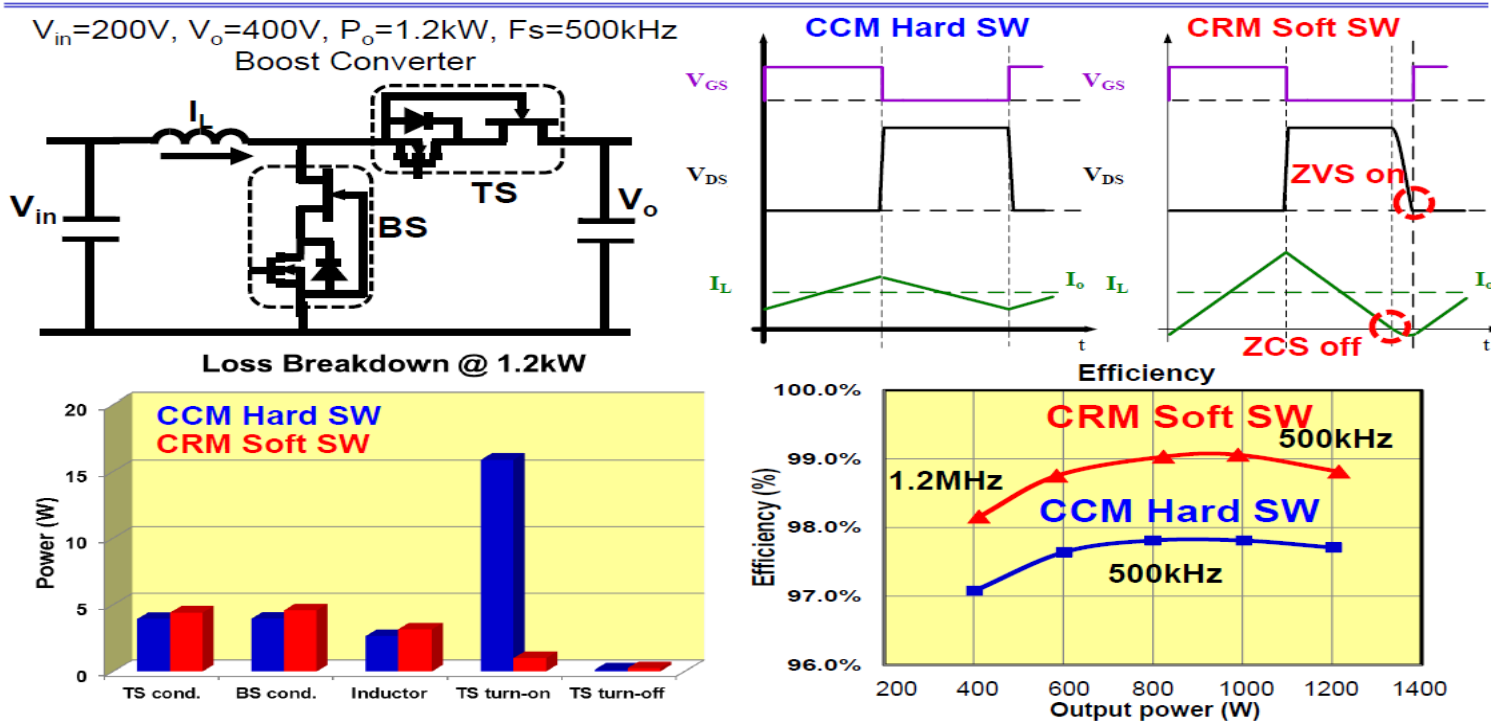


Benefits

- **Super High Efficiency** makes thermal design simpler
- **Extremely compact** solution with low component count
- Makes compliance with **80 Plus Titanium specs** easier
- Integrated GaN FET and driver eases layout constraints
- High PF > 0.99 and less than 5% THD for 20% to full load
- High performance C2000 controller enables superior control scheme and high PWM frequency operation
- poweSUITE support enables easy adaptation of software



GaN at High Frequency – Soft Switching vs Hard Switching

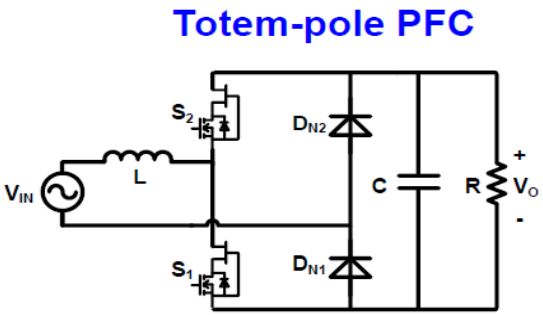


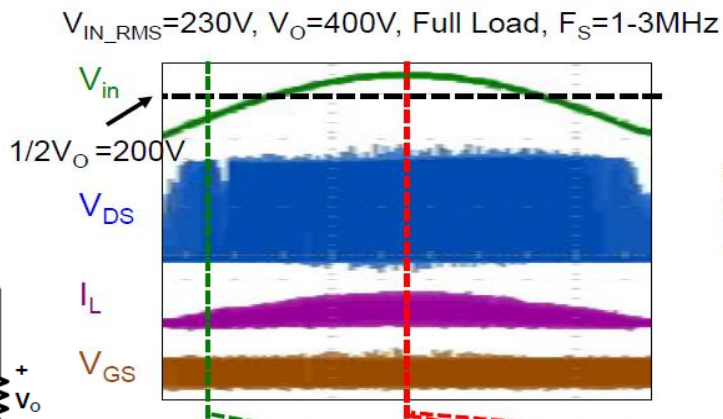
Soft switching significantly benefits GaN

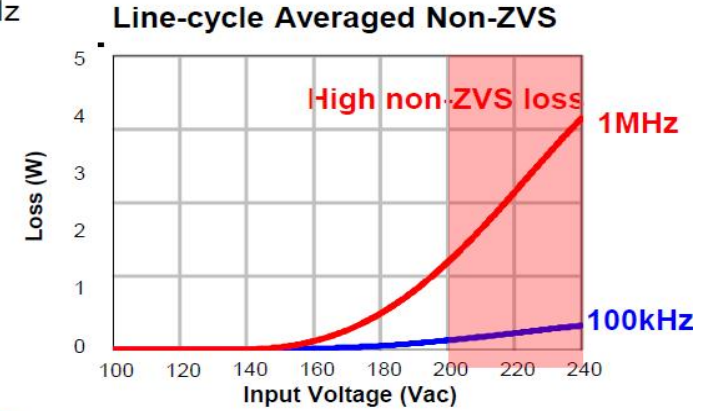
* Source: CPES, Virginia Tech

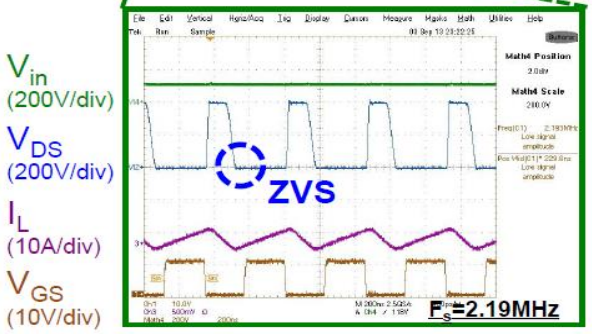
High Frequency TP PFC Challenges

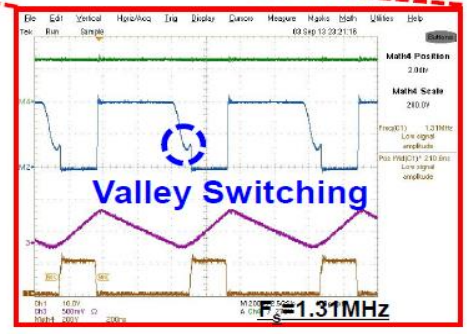
#1 Achieving ZVS across line-load and over full AC cycle



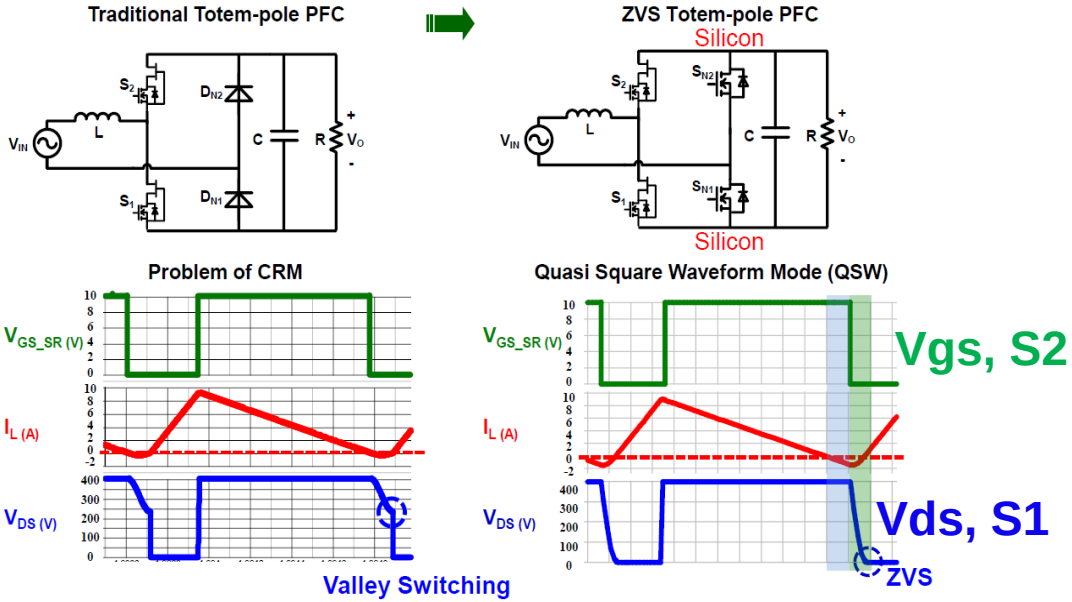








ZVS Extension



* Bin Su, Junming Zhang, and Zhengyu Lu, "Totem-Pole Boost Bridgeless PFC Rectifier With Simple Zero-Current Detection and Full-Range ZVS Operating at the Boundary of DCM/CCM", IEEE Transactions on Power Electronics, Vol. 26, No. 2, pp. 427 – 435, Feb 2011

* Christoph Marxgut, Florian Krismer, Dominik Bortis, and Johann W. Kolar, "Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier", in IEEE Transactions on Power Electronics, Vol. 29, No. 2, pp. 873 – 882, Feb 2014

* Source: CPES, Virginia Tech

Conventional Solution

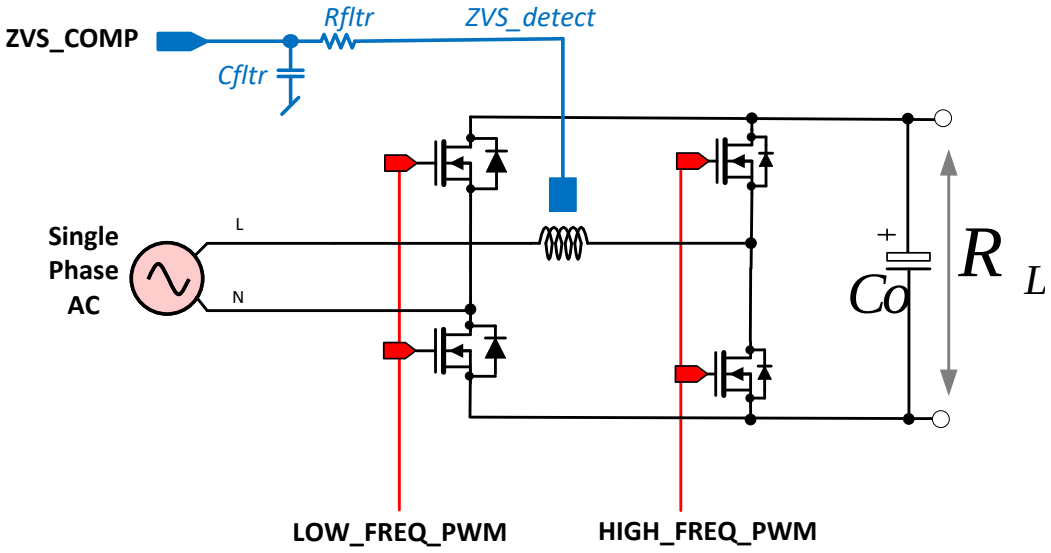
- Inductor current zero crossing sensing

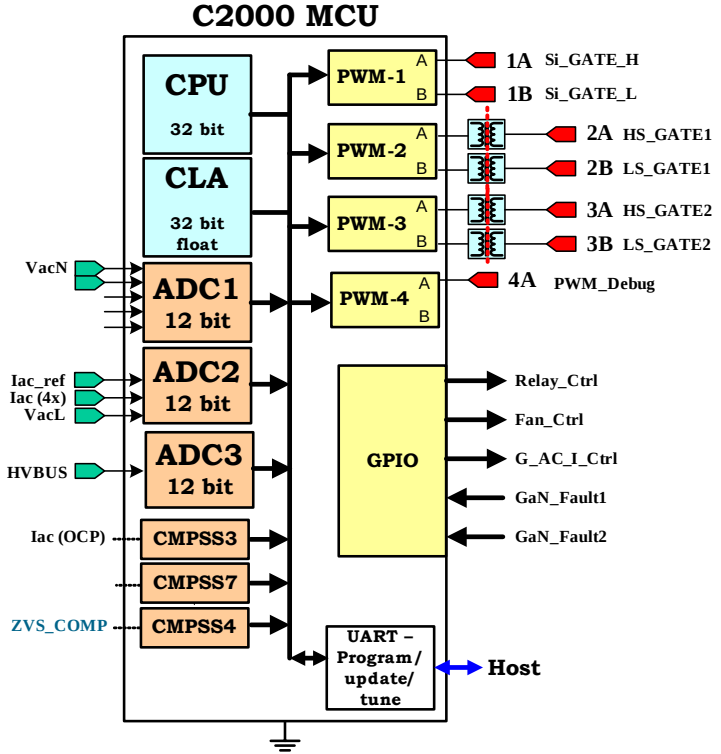
- Low SNR
- Worse under high-line low-load

C2x Solution

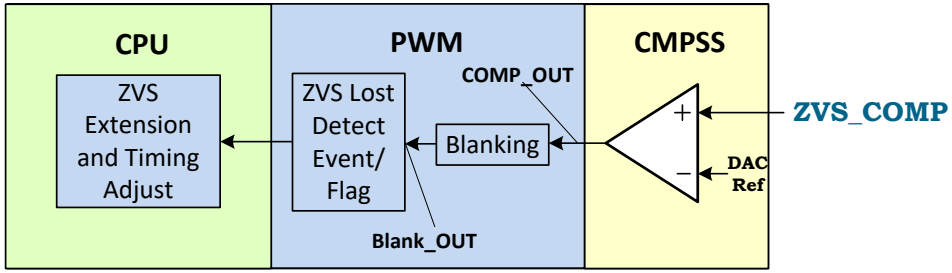
- Sensing voltage across the inductor
- On-chip CMPSS and type-4 PWM features on C2000 are used to solve this

ZVS Detection

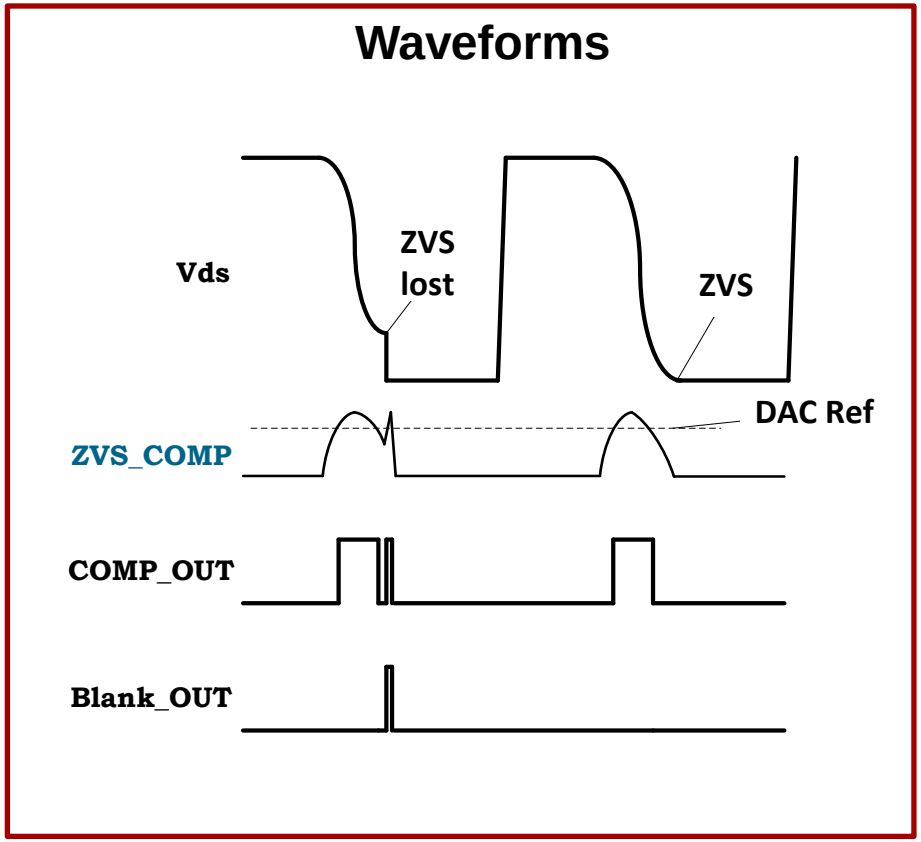




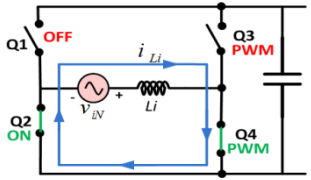
ZVS Detection

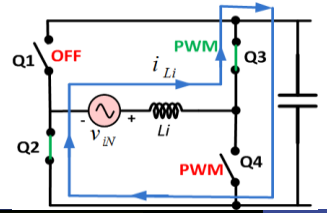


- 3 control loops (Voltage, Current and ZVS)
- Blanking may also be implemented as part of CMPSS (comparator).

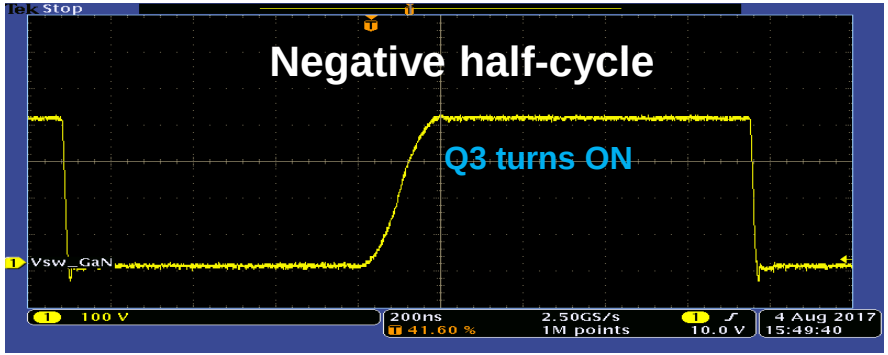


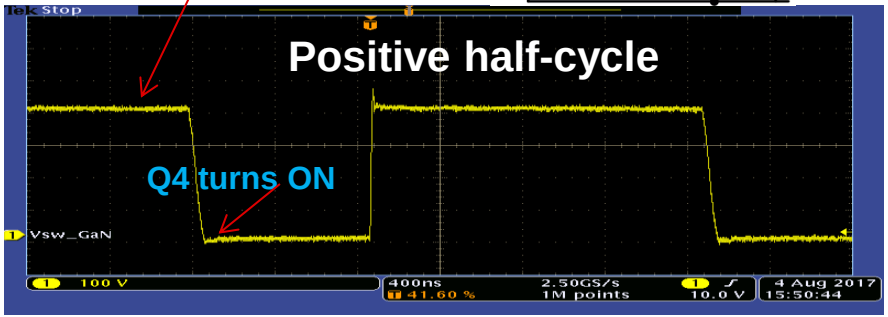
ZVS with AC Input

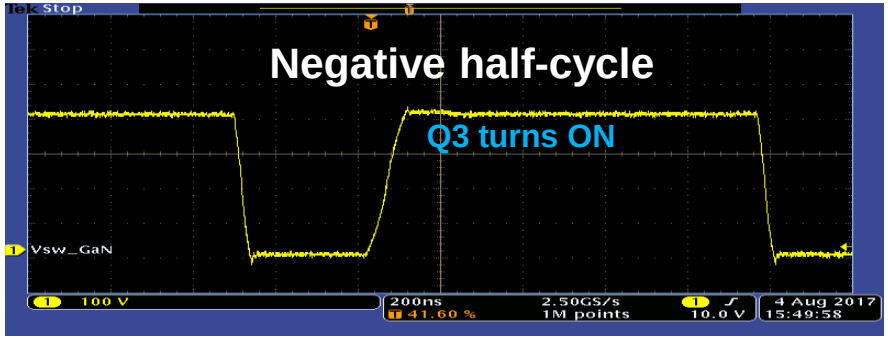


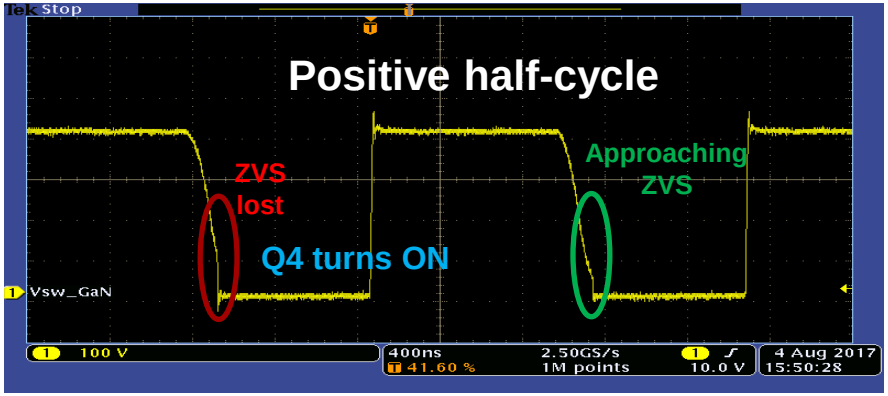


Vsw









#2 Cycle Intensive Calculations

- Calculating correct turn-on and turn-off durations at every switching/control instant

Solution

- C2000's TMU helps reduce the MIPS requirements considerably

  Example: From possible > 10us calculation time to <0.5us calculation time

Ton Calculations

$$f_1(T_{on}) = \frac{V_{in}V_o}{(V_o - V_{in})L} \cdot \frac{T_{on}^2}{2I_{ref}\sqrt{2LC_{oss}}} - \frac{T_{on}}{\sqrt{2LC_{oss}}} - \sqrt{\frac{V_{in}^2}{(V_o - V_{in})^2}\left(1 + \frac{T_{on}^2}{2LC_{oss}}\right) - 1}$$

$$f_2(T_{on}) = \frac{(V_o - V_{in})T_{on} + \sqrt{V_{in}^2T_{on}^2 + 2LC_{oss}(2V_{in}V_o - V_o^2)}}{(V_o - V_{in})\sqrt{2LC_{oss}} - (V_o - V_{in})T_{on}\sqrt{V_{in}^2T_{on}^2 + 2LC_{oss}(2V_{in}V_o - V_o^2)}}$$

$$C = \frac{V_o^2(2V_{in} - V_o)}{V_{in}(V_o - V_{in})} \cdot \frac{1}{2I_{ref}}\sqrt{\frac{2C_{oss}}{L}} - 2\pi - \frac{\sqrt{V_o^2 - 2V_{in}V_o}}{V_{in}} + \tan^{-1}\frac{\sqrt{V_o^2 - 2V_{in}V_o}}{V_{in}}$$

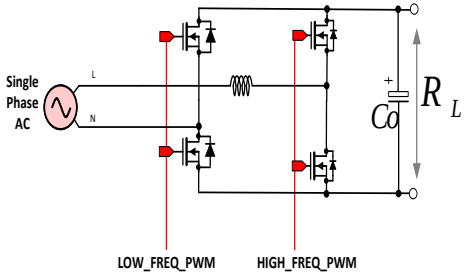
Dead-time Calculations

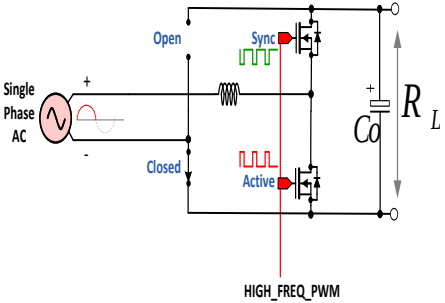
$$t := \sqrt{Lo \cdot 2 \cdot Coss} \cdot \left[3.14159 - \operatorname{atan}\left[\frac{\sqrt{(2Vin - Vo) \cdot Vo}}{Vo - Vin}\right]\right]$$

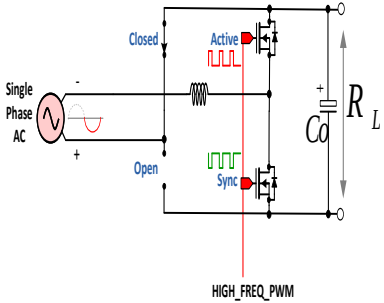
- Possibility of negative current/current spikes
- Body diode losses

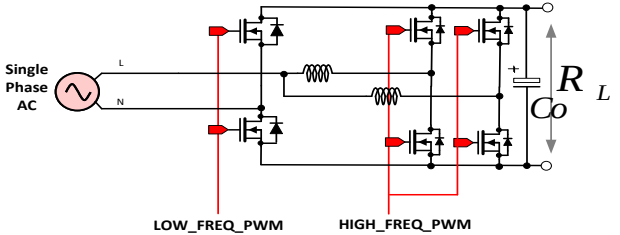
#3 Clean cross-over transitions

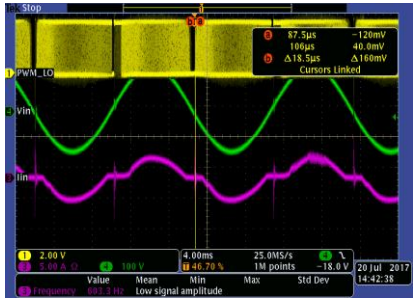
- High Freq TRM PFC uses small boost inductor and therefore small voltage across the inductor can cause fast current rise time.
- During AC voltage transitions, the stored charge across the output capacitance of the Si FET (in off state) discharges at a very high rate as soon as the GaN active FET is turned ON causing current spikes at zero crossing point

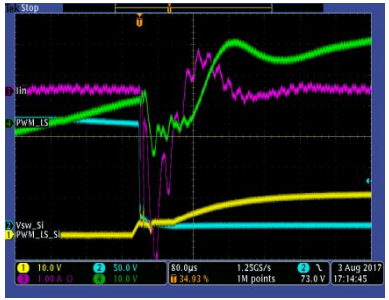






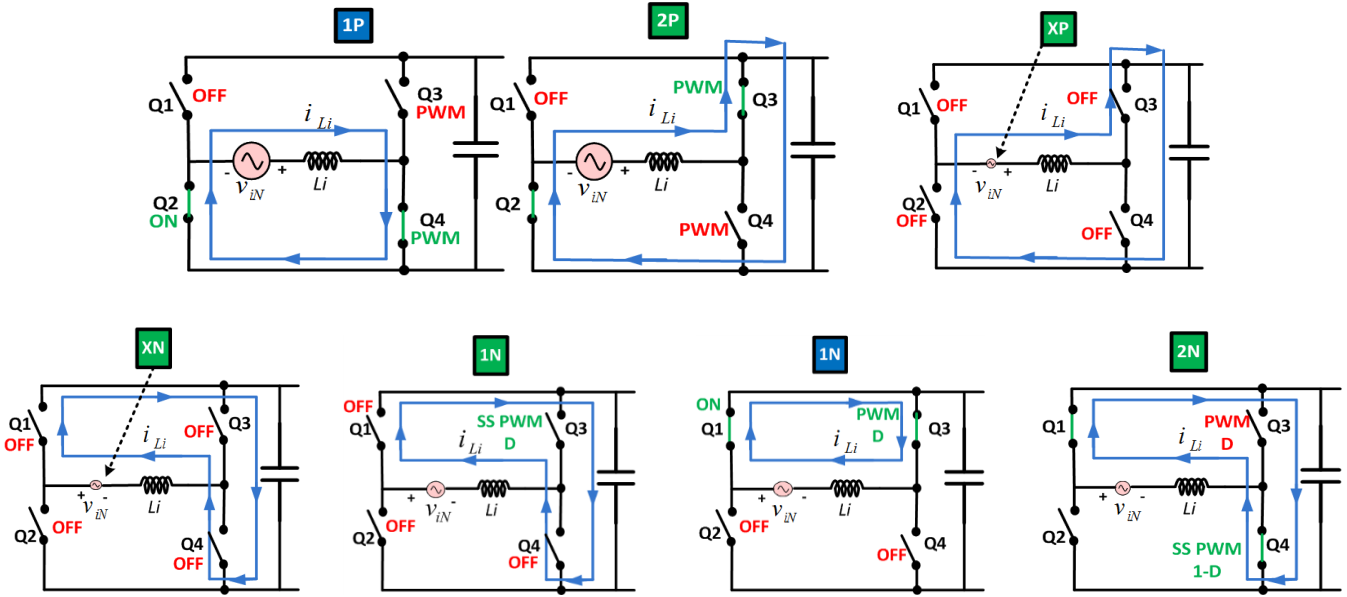




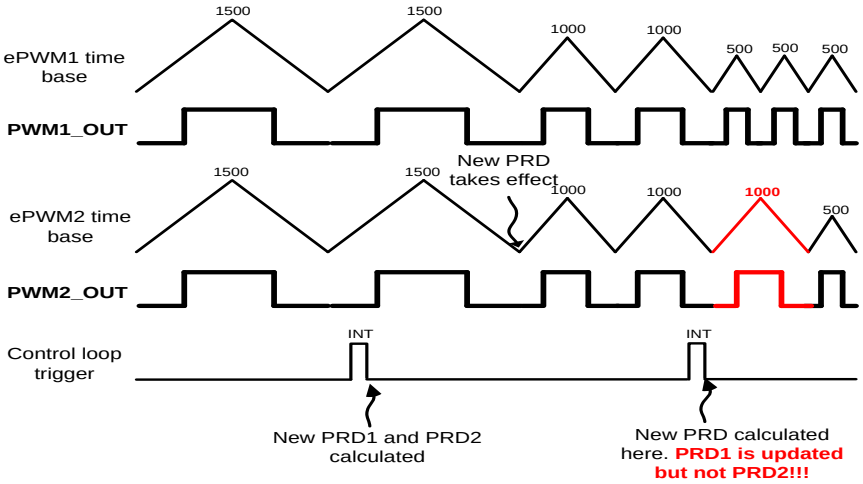


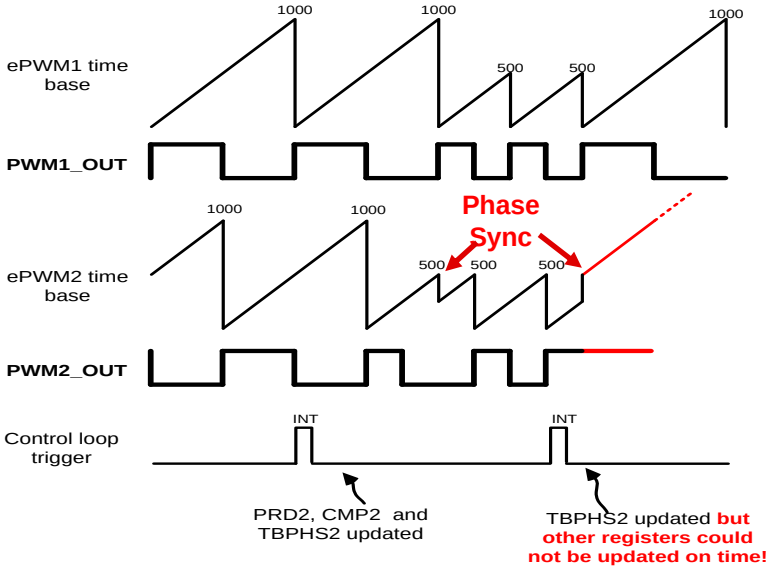
#3 Clean cross-over transitions - Solutions

- Soft-start for active FETs during zero voltage crossover providing a soft transition
- Proper sequence to turn-on silicon FET and the GaN sync FET must be followed
- These are implemented using a software state-machine



#4 Correct PWM waveform generation with HRDB

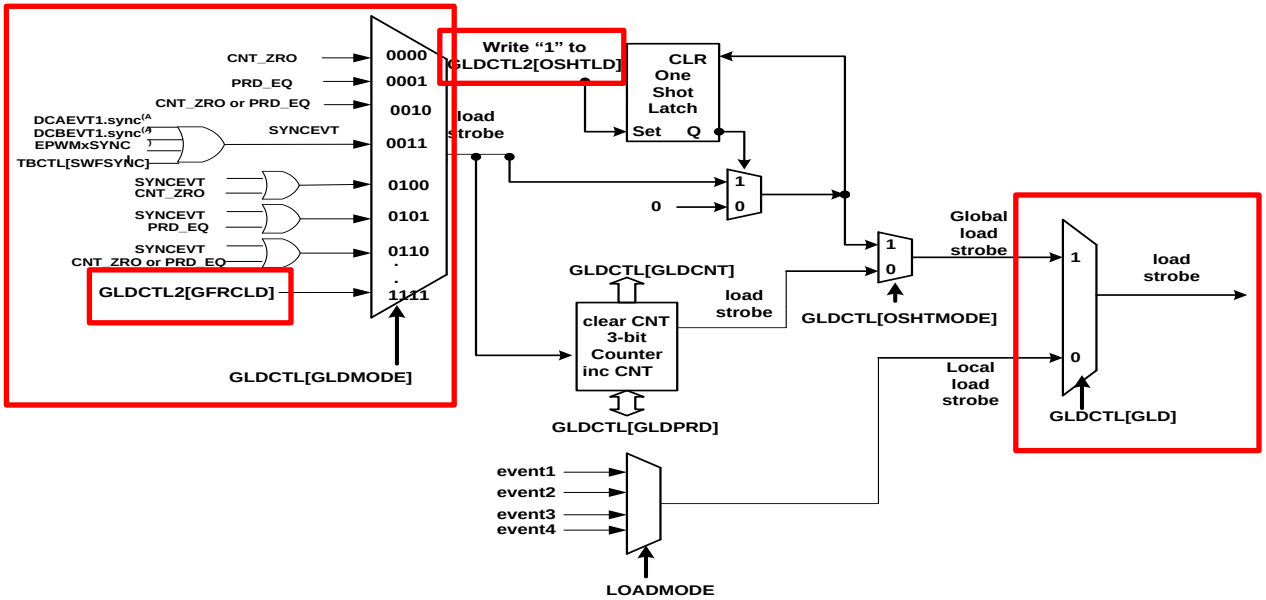




What is missing?

- A clean and easy way to update multiple registers in a PWM module
- A clean and easy way to update registers in multiple PWM modules

Solution: One Shot & Global Reload (Type-4 PWMs)



One shot reload usage

Initialization

- Enable global reload
- Link GLDCTL2 registers

Run Time

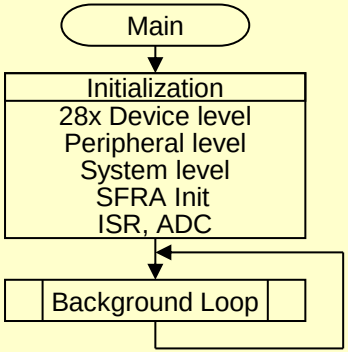
- Update all registers
- Write '1' to GLDCTL2[OSHTLD]
- Write '1' to GLDCTL2[GFRCLD], if desired

TRM PFC operating at high switching frequencies also requires **hi-res dead-band (HRDB)** between the turn-off of the active FET and the turn-on of the sync FET

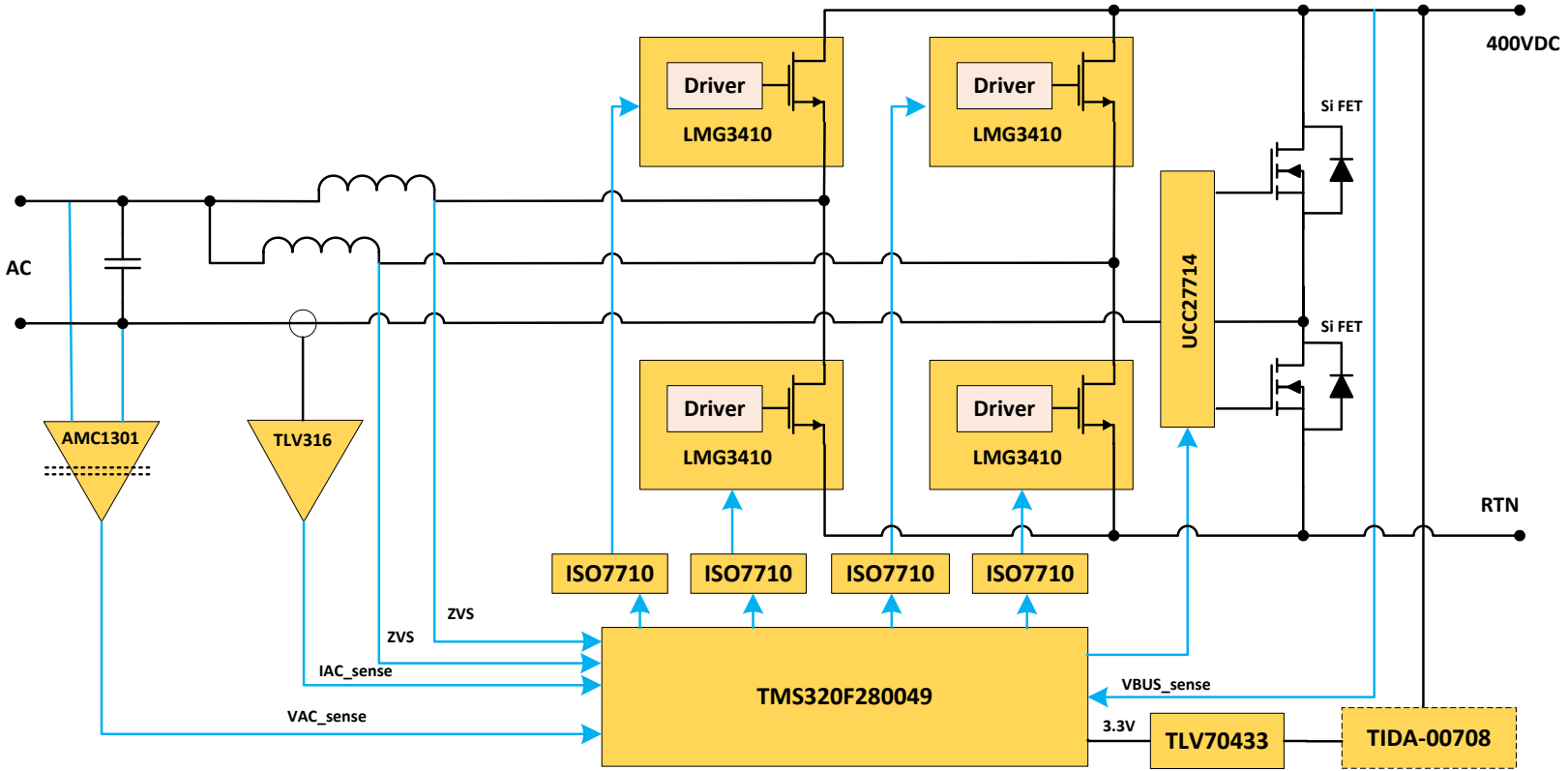
Software Flowchart

C Environment

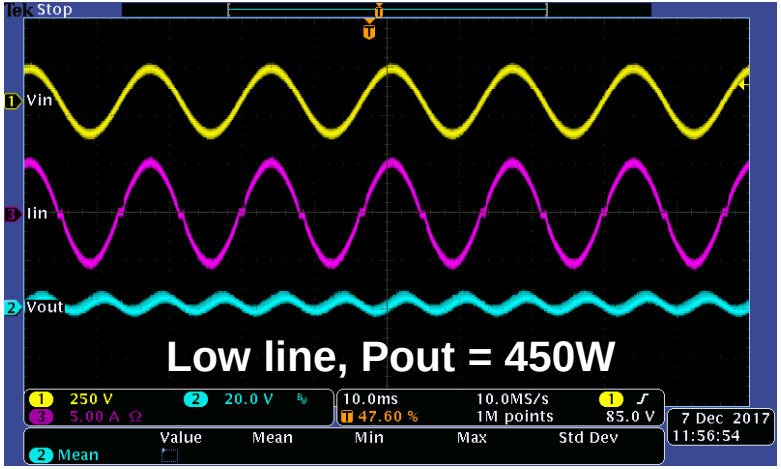
System Level Management

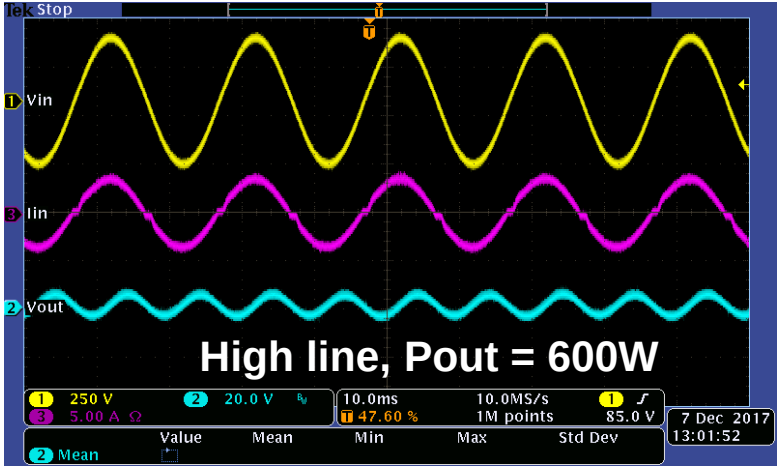


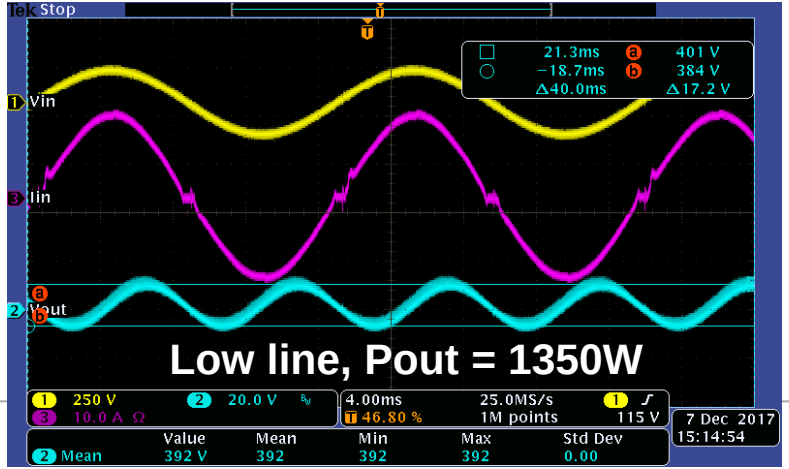
System Block Diagram

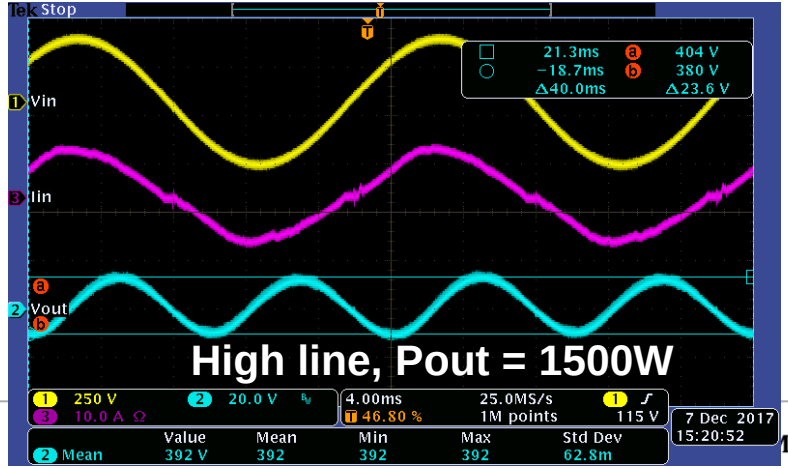


Input Voltage, Current and Output Ripple

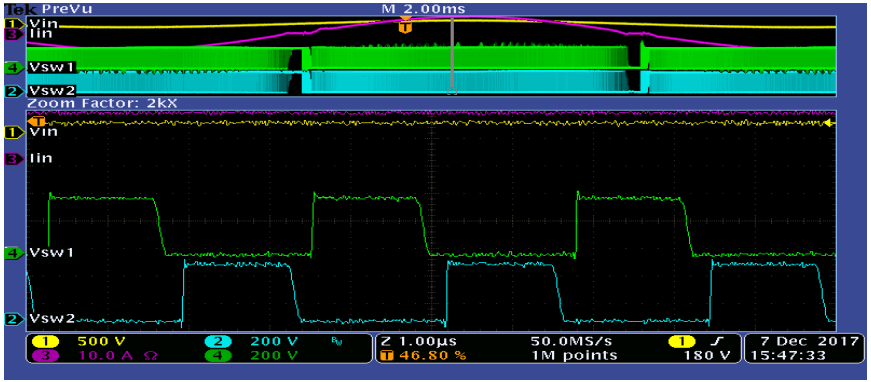




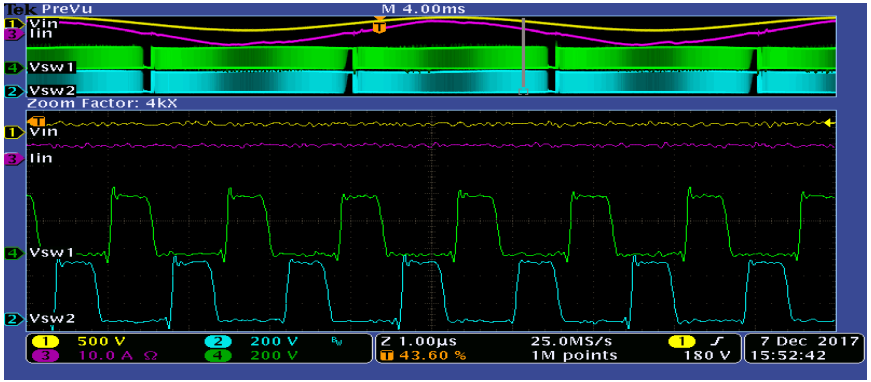




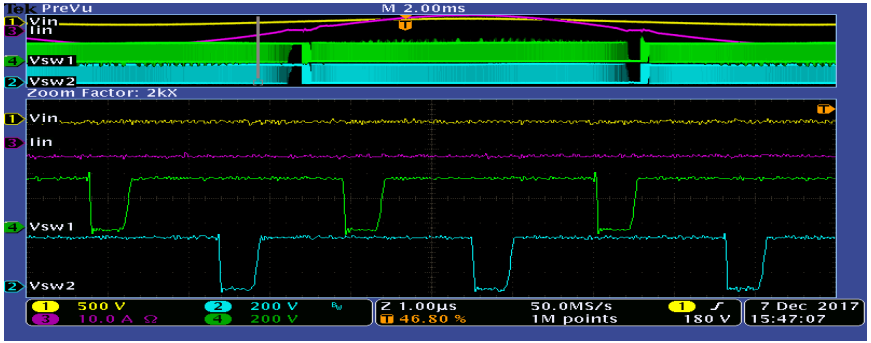
ZVS Across AC Cycle



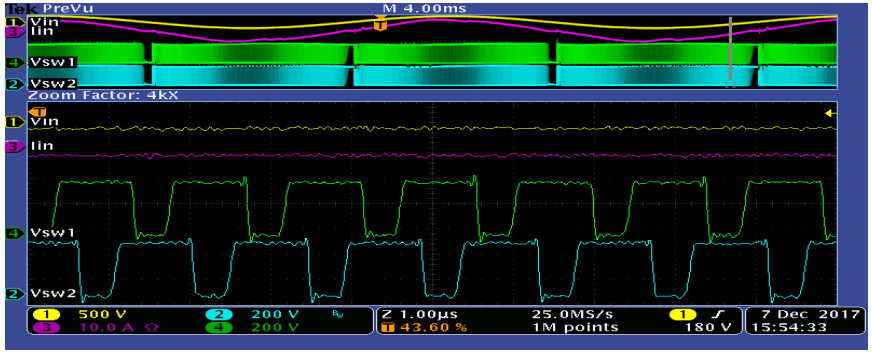
Low Line, Full Load, +ve Cycle



High Line, Full Load, +ve Cycle

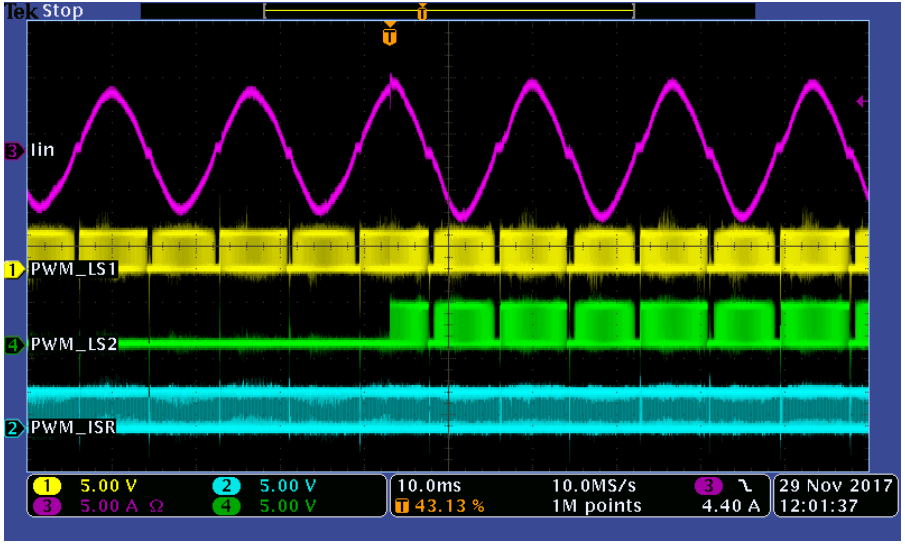


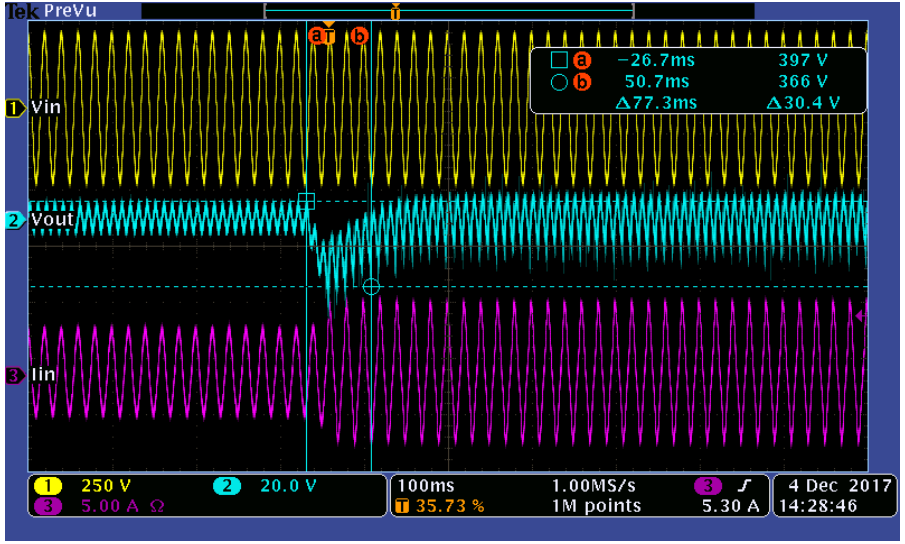
Low Line, Full Load, -ve Cycle



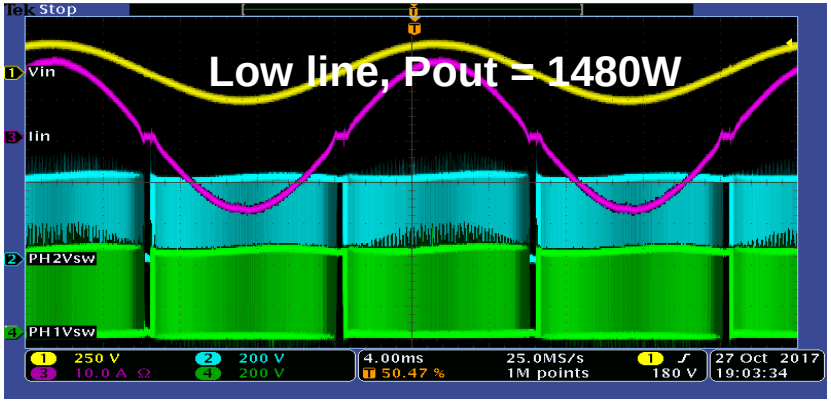
High Line, Full Load, -ve Cycle

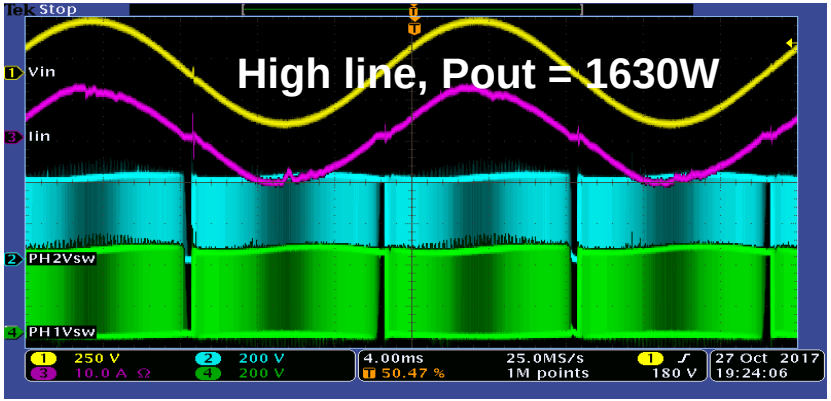
Phase Adding/Shedding

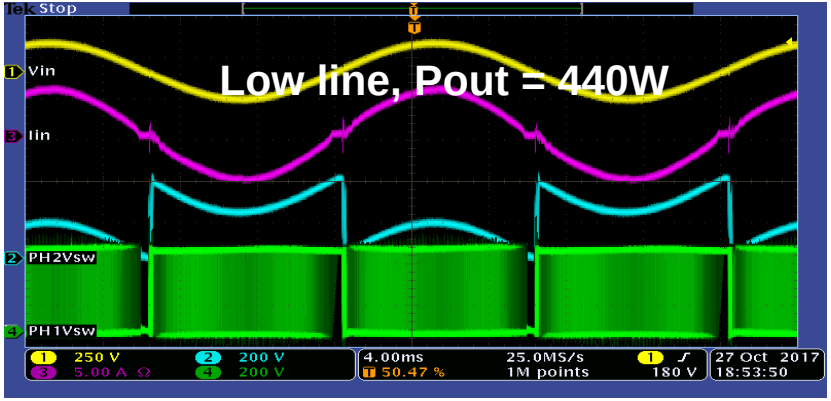




Phase Shedding – Low Line & High Line



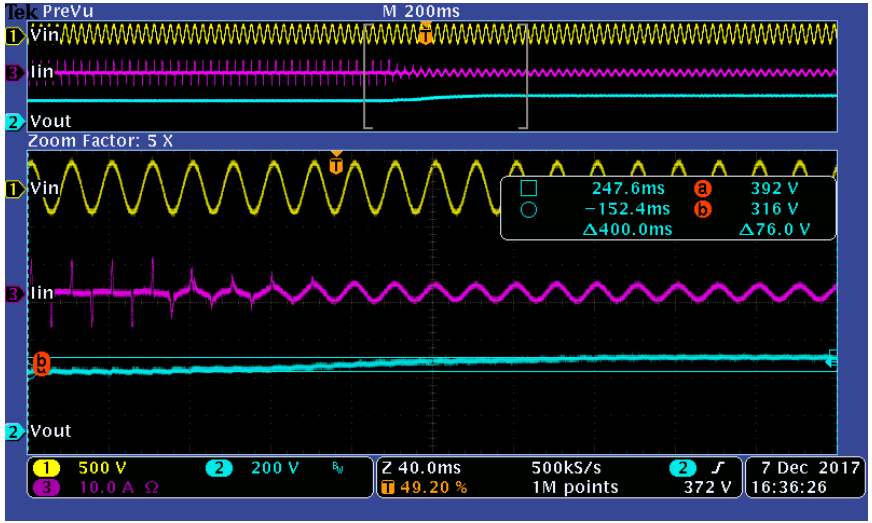




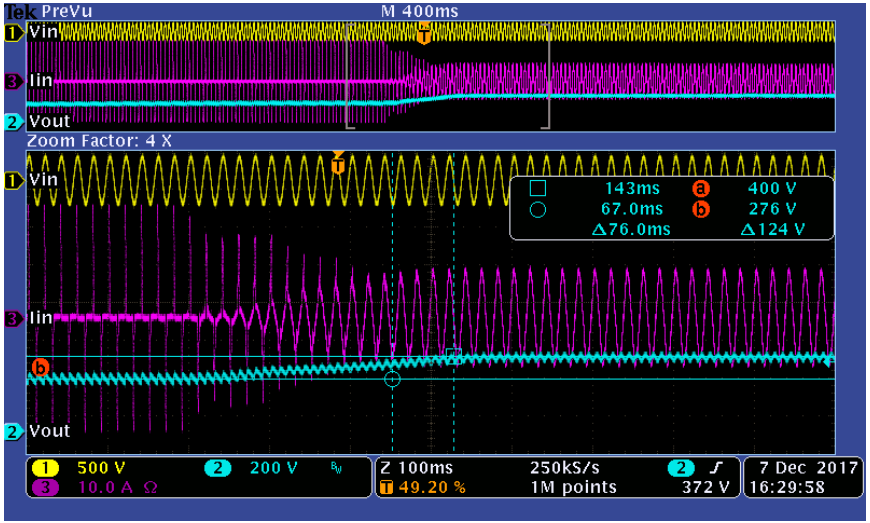
Low Line

High Line

Turn-on Characteristics

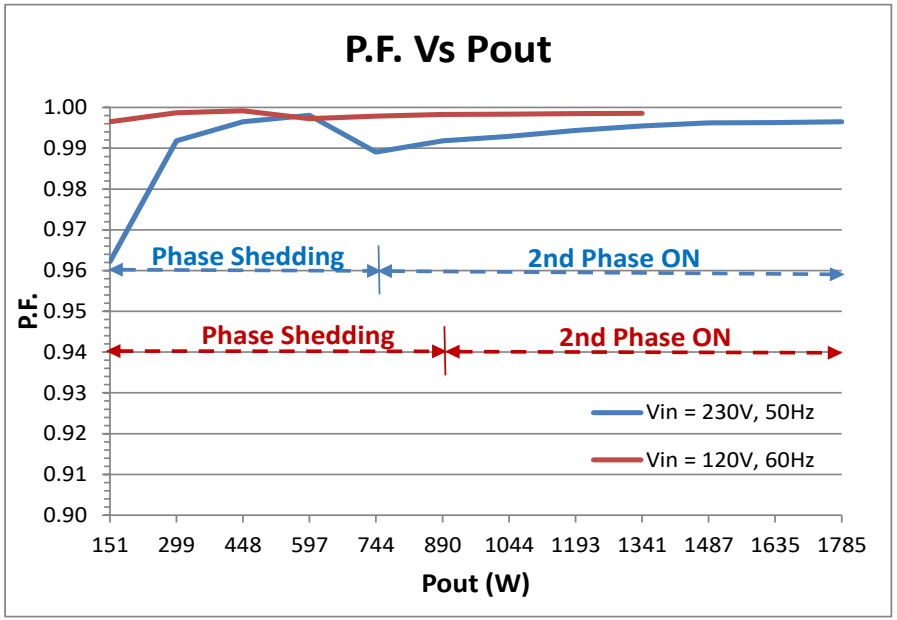


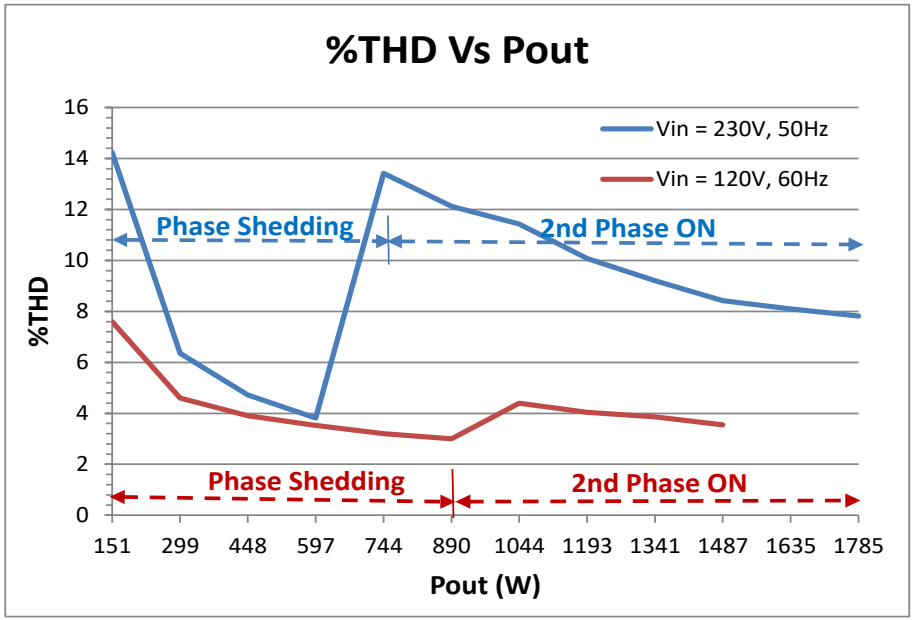
High Line Low Load (300W)



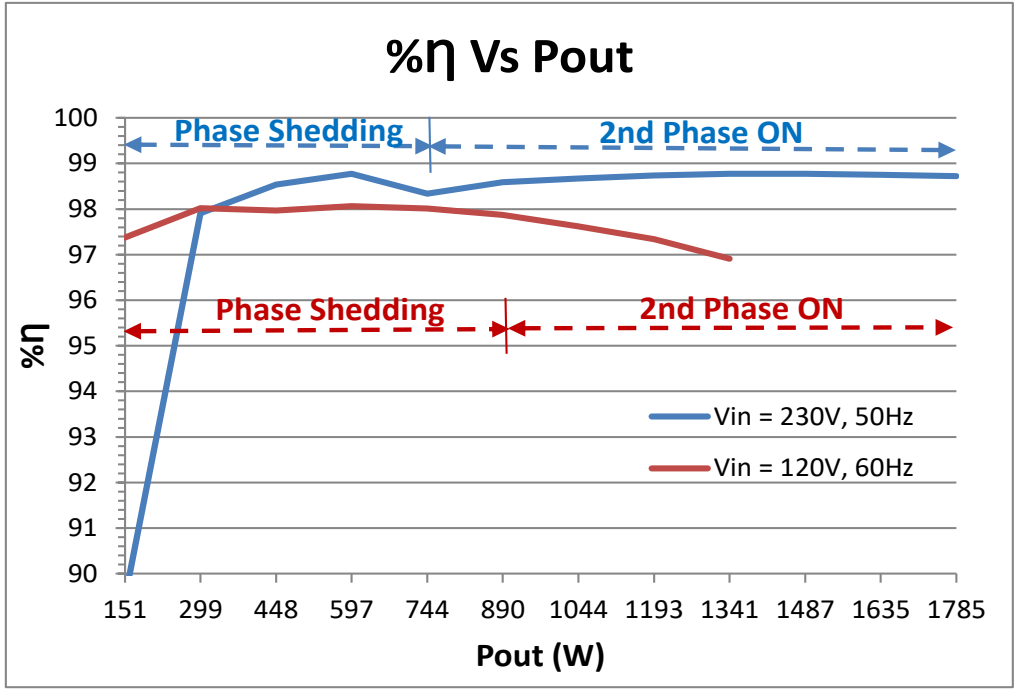
High Line Full Load (1800W)

Two Phase Interleaved PFC





Two Phase Interleaved PFC



Thank You