Modern Op Amps in Old School Designs

More Than Just a Spec Table

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Hi, My name is Zak Kaye. I'm an applications engineer with the precision amplifiers team and today I'd like to talk to you about designing with modern op amps in customer applications.

TI training – summary

TI Op-Amps in ADI Sockets summary:

The Precision Op Amps sales and marketing teams are focused on replacing every competitor op amp with a TI op amp. Customers are seeing how TI's op amp specs are better than or equal to nearly all of the competitor's specs. So naturally, they request our lower cost, improved performance op amp samples. Only to find out… it doesn't work! Now what and why? Whether your focus is on personal electronics, industrial or medical, every FAE interested in learning how to combat the problem of why our higher performance, lower cost op amps don't work in competitor sockets should attend this training. Learn from a training structured "definition by example", based on real world cases to de-mystify these "TI doesn't work in my competitor socket" occurrences.

What you'll learn: Some of the complexities of modern op-amps that transcend spec tables and influence performance

- When to use and NOT to use different op-amp topologies
- How to "Trust But Verify" anybody's op-amp macromodel
- Op-Amp rules of thumb and design tricks

Course details:

- Type: PPT overview/On-demand/ Training Series/ Webinar
- Format: SWF/ PDF/ etc.
- Duration: 90 Minutes
- Language: English
- Cost: Free
- Audience: Field Engineers

The goal of this presentation is to discuss some of the characteristics of modern op amps that you wont see in a spec comparison table that can heavily influence the success of a design. By the end of this you will be equipped with the tools necessary to understand where to look when customers encounter issues using a new op amp in their design, and even how to fix some of these issues. We will discuss different op amp topologies and technologies in addition to op amp macromodels and finally real world applications and rules of thumb.

Overview

- Replacing a competitor device is not always as simple as having better specs or lower cost.
- Improvements in op-amp technologies have allowed us to develop high quality precision devices, but achieving this performance entails added complexity, and added complexity means there are more ways to get in trouble.
- Understanding the application and the role of the op-amp makes it easier to recommend the right part without customer issues.
- Making the right part recommendation the first time means less time spent troubleshooting, and more time finding new sockets.
- Recognizing potential design issues before they become a problem increases mindshare with customers.

If you've ever tried to sell an op amp to a customer than you know that it isn't always as simple as having a device with better specs or lower cost. Many improvements have been made to op amps over the years and new technologies have resulted in a drastic increase in performance. Reaching these performance involves additional design complexity though, and that complexity can sometimes make it easier to get into trouble with the amplifier. Understanding the application and the role of the op amp can make it easier to recommend the right part without encountering issues. If we can make the right part recommendation early on, it means we can spend less time troubleshooting problems and more time finding new sockets. Most importantly, recognizing design issues before they occur or being able to quickly solve customer problems increases our reputation with our customers and makes them more eager to come to us first.

Detailed agenda

- **Introduce customer problem**
- **Op-amp stability review**
  - Poles & zeros
  - Capacitive loading
  - Loop gain, Aol, 1/β and rate of closure
- **Op-amp output impedance**
  - Zo vs Zout
  - “Trust but verify” series
  - Interaction with reactive loads and impact on Aol
- **Real world applications and commonly encountered issues**
  - TLV07 vs. OP07
  - Driving an ADC
  - Using different op-amp topologies

In this presentation we will start by presenting a common application issue. We will then do a brief stability and output impedance review to equip ourselves with the tools necessary to understand and fix the issue. From there, we will look at some real world applications and other commonly encountered issues, including an overview of when to use and when not to use certain types of devices.

Customer application

Let’s start by taking a look at a common application issue.

TLV07: TLV07ID

Internal Device Positioning

Parameter	Unit	OP07C (TI)	TLV07 (TI)
			Upgrade from legacy commodity op amp
Supply Voltage Range	V	6 to 36	2.7 to 36
GBW MHz	MHz (Typ)	0.6	1
Slew Rate	V/µs (typ)	0.3	0.4
Rail-to-Rail		-	Out
Vos	µV (Max)	-	100
Vos	µV (Typ)	60	50
Offset Drift	µV/°C (Typ)	0.5	0.9
Input Bias Current	nA (Typ)	1.8	0.04
Vn @ 1kHz	nV/√Hz (Typ)	9.8	19
Quiescent Current	mA (Typ, Max)	2.4, 5	0.95, 1.8
CMRR dB (typ)	dB (Typ)	120	120
Architecture		Bipolar	CMOS
Operating Temperature Range	°C	0 to 70	-40 to 125
Package Group		SOIC, PDIP, SO-8	SOIC
Price (1ku)	USD ($)	0.23	0.35

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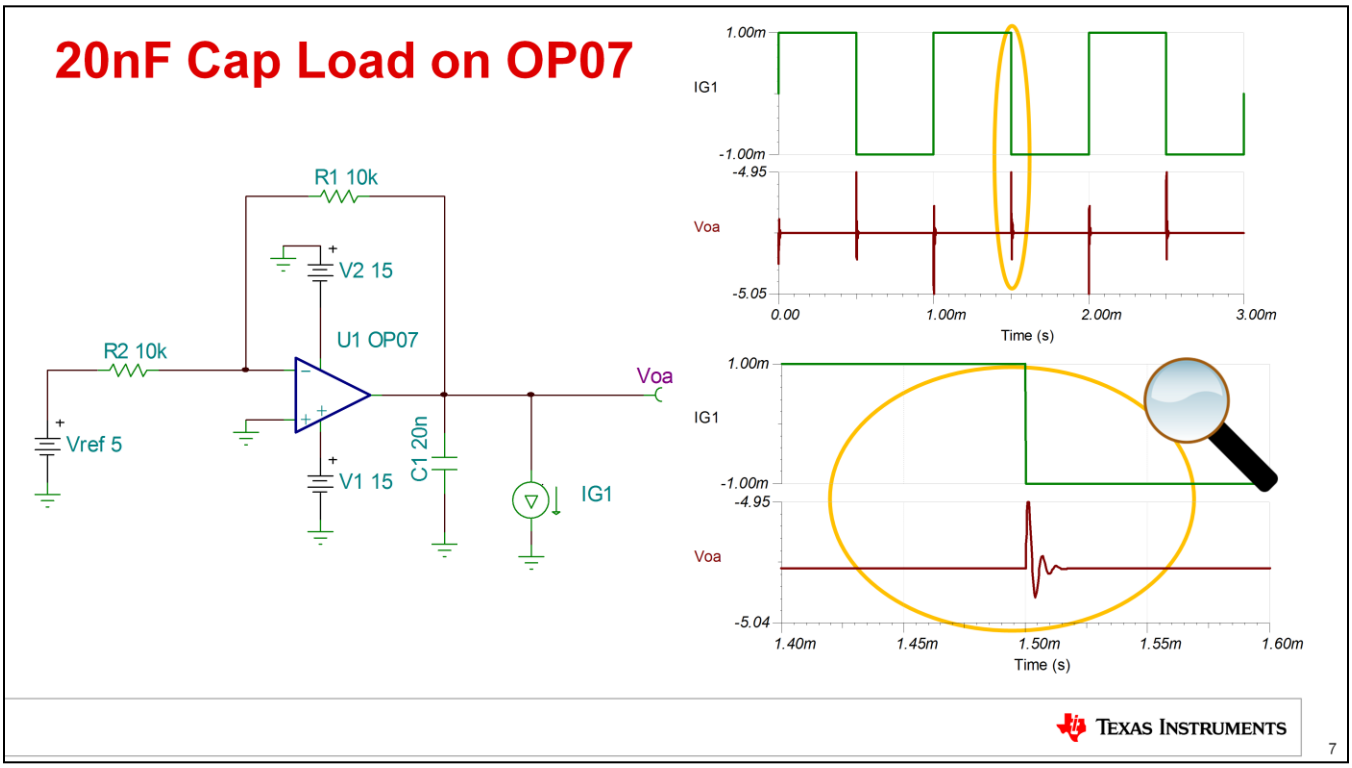
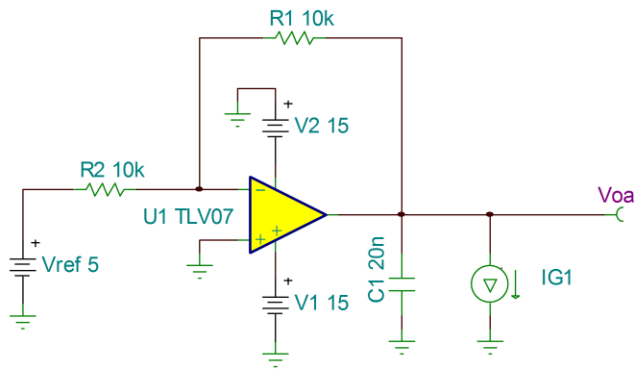
As new technologies become available and newer processes evolve our portfolio does too. In many cases, we use these newer technologies to refresh legacy parts and allow customers to upgrade their systems. The TLV07 and OP07 are one example of this strategy. Many customers treat these upgrades as drop in replacements, but as we will see this is not always a safe assumption…



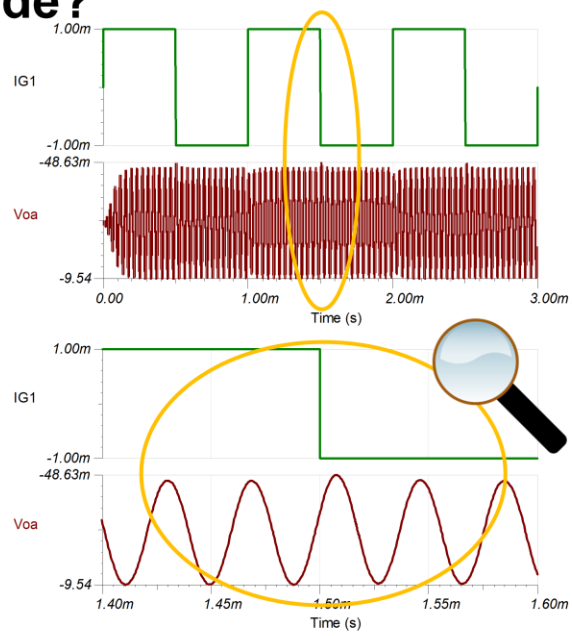
This OP07 circuit is used to generate a negative 5V reference from a positive 5V reference. A capacitor is placed on the output to filter out some of the noise and hold the output steady. If we inject a small current disturbance on the output, such as that which might occur when a light load is switched on, we see a slight amount of ringing and some overshoot before the circuit settles back to negative 5V.

While it is generally not good practice to drive a capacitive load with no compensation, everybody has seen and probably even built a circuit like this. In this instance, though there is some overshoot and ringing in response to a current disturbance on the output, the OP07 is able to respond and settles reasonably quickly. Let's see what happens when we apply the same disturbance to this circuit with our upgraded TLV07.

TLV07: Upgrade or downgrade?



Oscillation at 25.97kHz!



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Here we have the exact same circuit, with the OP07 replaced with a TLV07. From the spec comparison we would expect to see greater accuracy and a faster response. But unless the intention was to create an oscillator, this is definitely not the response we are looking for. But if the TLV07 is an upgrade to the OP07 and even has more bandwidth, why does it oscillate in the same configuration? To understand this we'll have to revisit some of our stability fundamentals.

Op amp stability review

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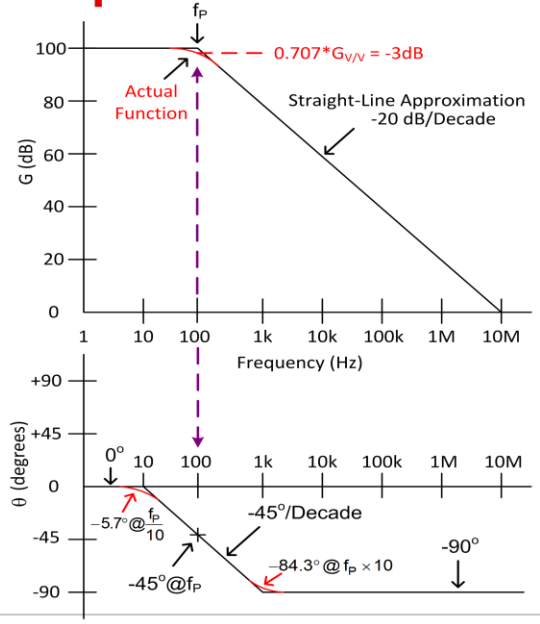
This section is a revised and condensed version of the TI precision labs on op amp stability.

Bode plots: Pole



$$G_{v/v} = \frac{V_{out}}{V_{in}} = \frac{G_{dc}}{i\left(\frac{f}{f_P}\right) + 1}$$ As a complex number

$$G_{v/v} = \frac{V_{out}}{V_{in}} = \frac{G_{dc}}{\sqrt{\left(\frac{f}{f_P}\right)^2 + 1}}$$ Magnitude

$$\Theta = -\tan^{-1}\left(\frac{f}{f_P}\right)$$ Phase

$$G_{dB} = 20\mathrm{Log}(G_{v/v})$$ Magnitude in dB

- Pole Location = f_P (Cutoff Freq)
- Magnitude ($f < f_P$) = G_{dc} (e.g. 100dB)
- Magnitude ($f = f_P$) = -3dB
- Magnitude ($f > f_P$) = -20dB/Decade
- Phase ($f = f_P$) = -45°
- Phase ($0.1f_P < f < 10f_P$) = -45°/Decade
- Phase ($f > 10f_P$) = -90°
- Phase ($f < 0.1f_P$) = 0°

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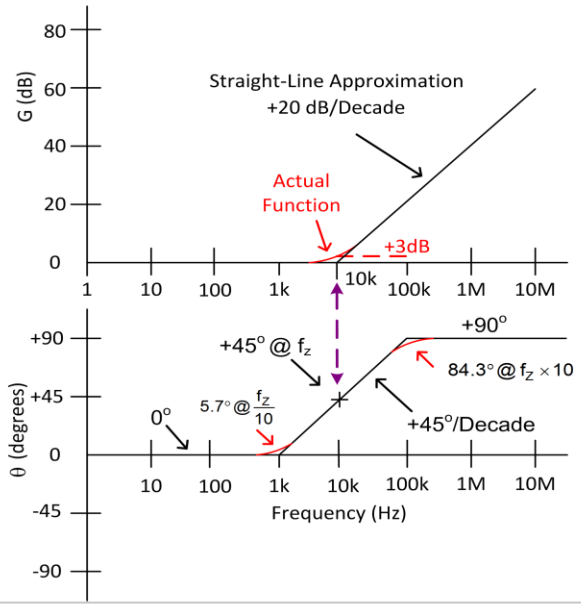
First, a quick review of Bode plots. A bode plot is an asymptotic approximation of how something behaves over frequency. A pole in a bode plot causes a negative 20 dB/decade decrease in the slope of the magnitude response after the pole frequency, fp. The pole also causes a negative 90 degree phase shift in the phase response beginning roughly a decade before fp and ending roughly a decade afterwards.

At fp the magnitude response will have decreased by negative 3 dB, and the phase will have shifted by negative 45 degrees. The equations above give the exact transfer function for a pole.

Bode plots: Zero



$$G_{v/v} = \frac{V_{out}}{V_{in}} = G_{dc}\left[i\left(\frac{f}{f_Z}\right) + 1\right] \quad \text{As a complex number}$$

$$G_{v/v} = \frac{V_{out}}{V_{in}} = G_{dc}\sqrt{\left(\frac{f}{f_Z}\right)^2 + 1} \quad \text{Magnitude}$$

$$\Theta = \tan^{-1}\left(\frac{f}{f_Z}\right) \quad \text{Phase}$$

$$G_{dB} = 20\text{Log}(G_{v/v}) \quad \text{Magnitude in dB}$$

- Zero Location = f_Z
- Magnitude ($f < f_Z$) = 0dB
- Magnitude ($f = f_Z$) = +3dB
- Magnitude ($f > f_Z$) = +20dB/Decade
- Phase ($f = f_Z$) = +45°
- Phase ($0.1f_Z < f < 10f_Z$) = +45°/Decade
- Phase ($f > 10f_Z$) = +90°
- Phase ($f < 0.1f_Z$) = 0°

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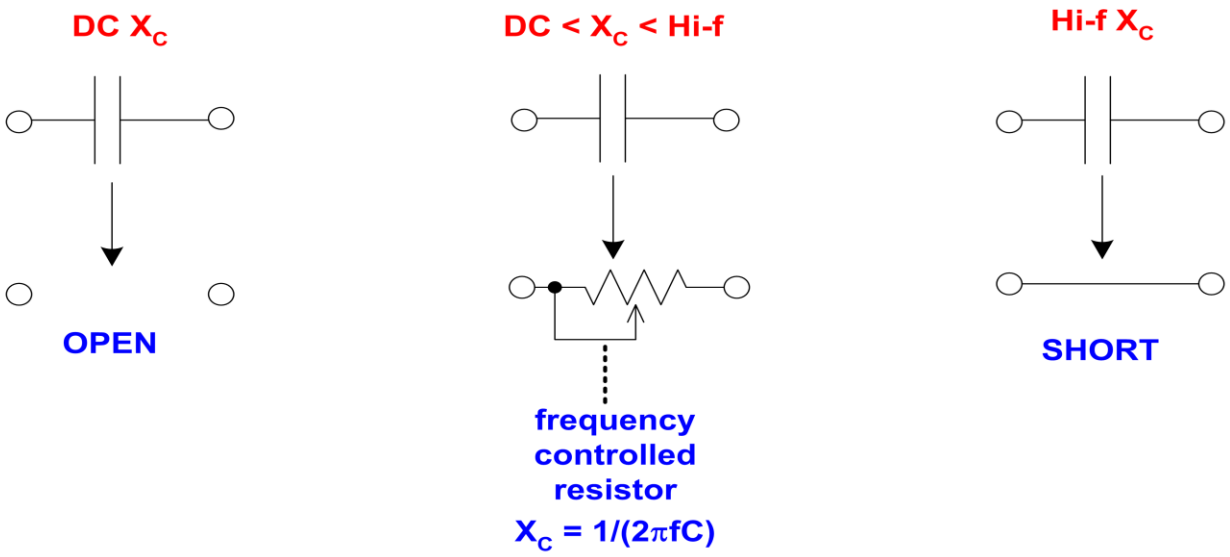
In contrast to a pole, a zero causes a positive 20dB/decade increase in the slope of the magnitude response after the zero frequency, fz. The zero also causes a positive 90 degree phase shift in the phase response beginning roughly a decade before fz and ending roughly a decade afterwards.

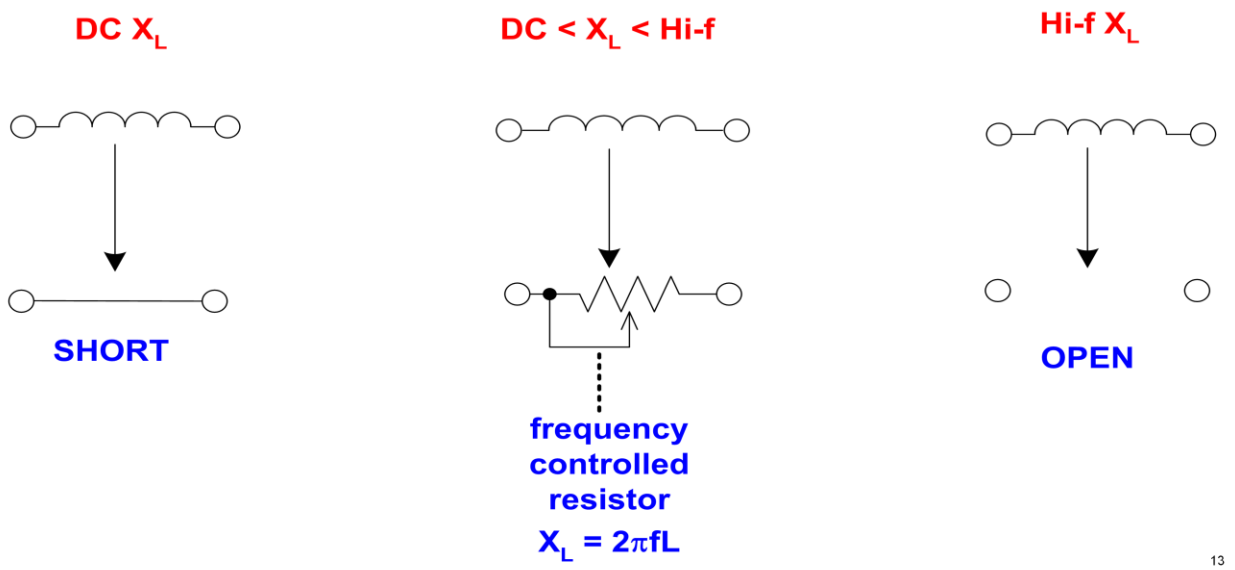
At fz the magnitude response has increased by plus 3 dB and the phase has shifted by positive 45 degrees. Again the equations above give the transfer function for a zero

Capacitor: Intuitive model



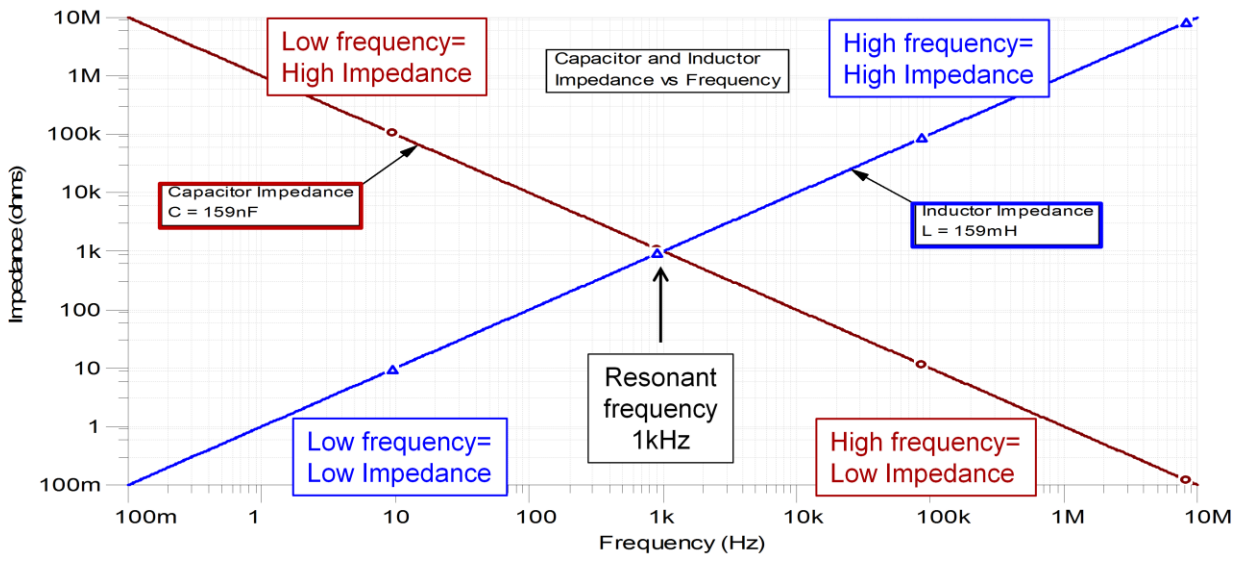
This slide defines an intuitive model for a capacitor, that consists of 3 different operating regions. At "DC" the capacitor will be viewed as an open circuit. At "High Frequency" the capacitor will be viewed as a short circuit. In between the capacitor will be viewed as a frequency controlled resistor with a 1/2πfC decrease in impedance as frequency increases.

Inductor: Intuitive model



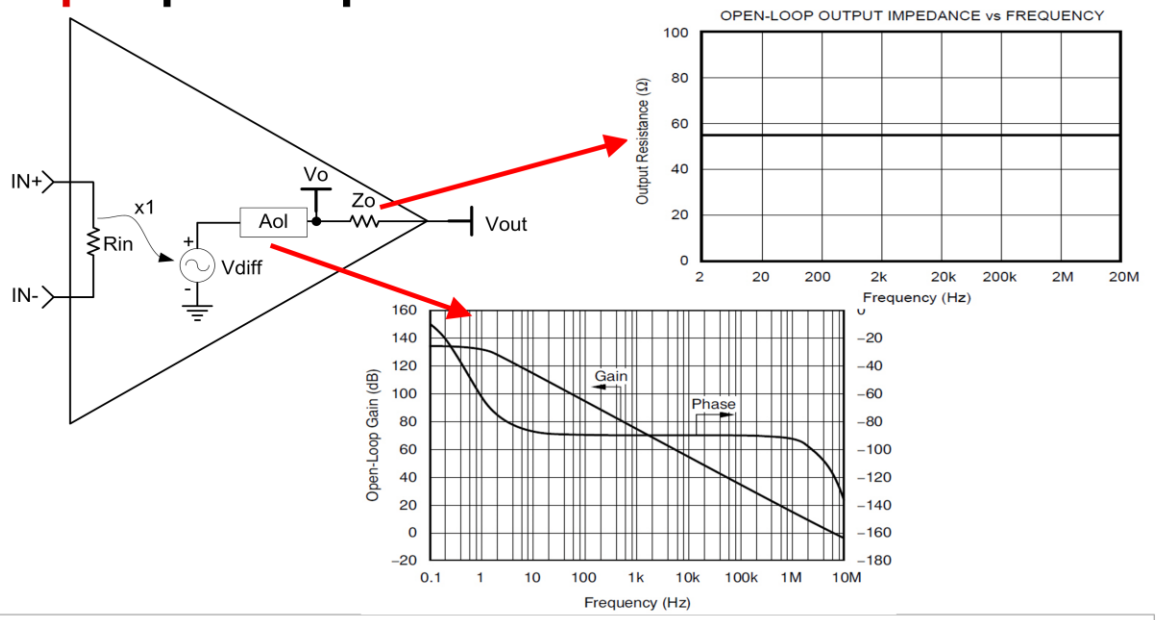
This slide defines an intuitive model for an inductor, which again consists of three distinct operating areas, exactly reciprocal to the capacitor. At “DC” the inductor is viewed as a short circuit. At “High Frequency” the inductor is viewed as an open circuit. In between the inductor will be viewed as a frequency controlled resistor with a 2πfL increase in impedance as frequency increases.

Capacitor and inductor: Impedance vs frequency



SPICE simulation confirms that the inductor and capacitor do behave as expected over frequency. Real components will have non ideal characteristics that cause the behavior to deviate from that shown in these plots, but for most practical purposes we can treat the components as ideal. If we had this 159nF capacitor and 159mH inductor in a circuit together, then the circuit would have a resonant frequency at the point where the two impedance curves intersect, or in this case 1kHz.

Op amp: Open loop model

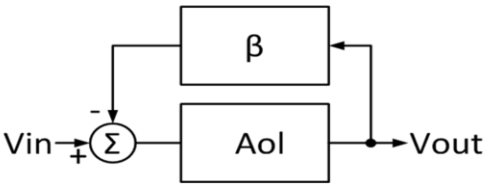


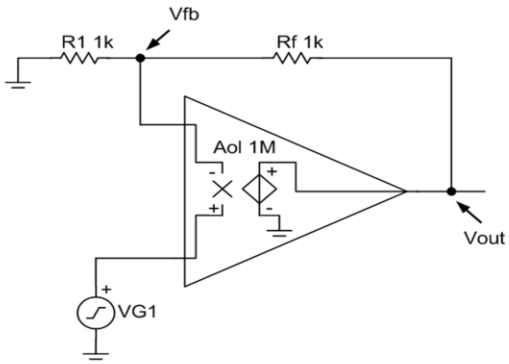
It is helpful to use an intuitive model for the op amp when performing ac stability analysis because of the complexity of modern op amps. In this simplified “stability” model, the differential input voltage applied to the inputs is passed to the amplifier output stage where it passes through the amplifier open-loop gain, followed by the open-loop output impedance before it reaches the output terminal.

The open-loop gain, or Aol, of an op amp represents the maximum gain that can be applied over frequency to the differential voltage applied between the inputs of the device. Aol for an ideal amplifier is infinite and is not limited by frequency. Modern op amps can have open loop gains in excess of 1 million volts per volt, or 120dB at low frequencies and unity-gain bandwidths from 10’s of kHz up to several GHz.

The open-loop output impedance, Zo, is a measure of the impedance of the output stage of the op amp. We will discuss this parameter in more detail in the next section.

Op amp: Closed loop model





A_{ol} = Open loop Gain

β = Feedback Factor = $\frac{V_{fb}}{V_{out}} = \frac{R_1}{R_1 + R_f}$

A_{cl} = Closed Loop Gain = $\frac{A_{ol}}{1 + A_{ol}\beta}$

$A_{ol}\beta$ = Loop Gain

$A_{cl} = \lim_{A_{ol} \to \infty} \left(\frac{A_{ol}}{1 + A_{ol}\beta}\right) = \frac{1}{\beta} = 1 + \frac{R_f}{R_1}$

To control the large open-loop gain of modern amplifiers, negative feedback is required between the output of the amplifier and the inverting input. In this circuit, the loop is closed with Rf and R1 which create a voltage divider, and therefore an attenuation, between the output and the inverting input. The ratio of the resistors determines the amount of the output that is fed back to the input which is defined as the feedback factor, or Beta, of the circuit.

Closing the loop results in a closed-loop gain, Acl, that is equal to Aol divided by 1 plus Aol multiplied by Beta. Aol multiplied by Beta is such a special term that we give it its own name, Loop-gain. When the loop-gain is large, the closed-loop gain formula can be simplified to equal 1/Beta. In this example 1/Beta equals 1+Rf/R1, which can be recognized as the gain of a non-inverting amplifier circuit.

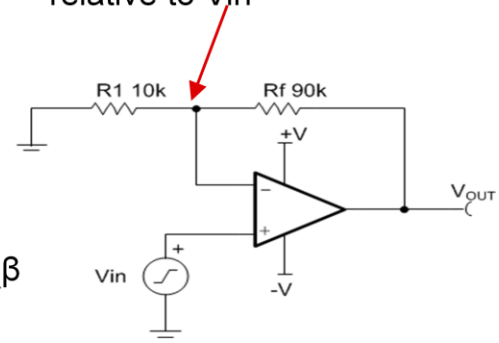
If Beta is the portion of the output that gets fed back to the input, then you could consider 1/B to represent how the output of the amplifier must change in order to close the feedback loop.

When is an amplifier unstable?

$$\mathbf{A_{CL}} = \frac{\mathbf{A_{OL}}}{\mathbf{1 + A_{OL}\beta}}$$

- A circuit is unstable when $A_{OL}\beta = -1$
- $A_{OL}\beta = -1$ sets the denominator of $A_{CL} = 0$
- $A_{OL}\beta = -1$ when $A_{OL}\beta$(dB) = 0dB and phase shift($A_{OL}\beta$) = 180°
  - Phase shift is relative to the DC phase

$A_{OL}\beta = -1$ when the phase at V_{FB} has shifted 180^0 relative to Vin



Phase Margin (PM)

How close the system is to a 180° phase shift in $A_{OL}\beta$

- PM = Phase($A_{OL}\beta$) when Gain($A_{OL}\beta$) = 0dB
- Ex: 10° phase margin = 170° phase shift in $A_{OL}\beta$

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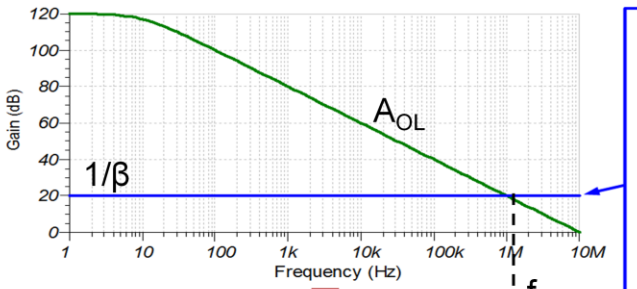
So when does an amplifier actually become unstable? Well, looking back at the op amp closed-loop gain equation, we remember that Acl = Aol / 1+ AolB. Taking a closer look, we can see that if AolB, or the loop gain, equals -1, we get zero in the denominator and therefore Acl becomes undefined. This is the mathematical definition of instability. How can this happen in a real circuit?

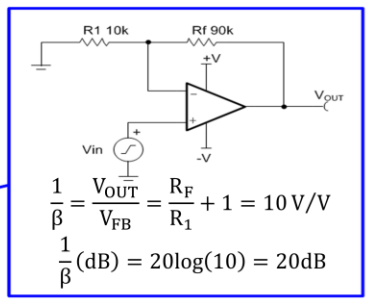
Well, at some point in frequency AolB will equal 0dB, which is equal to 1V/V. If enough delay is introduced into the feedback path, the phase in the feedback network will shift 180 degrees relative to Vin. A 180 degree phase shift is equivalent to an inversion of the input, or -1. Therefore, when the magnitude of AolB = 0dB and the phase has shifted by 180 degrees, the result is AolB = -1.

The term “Phase Margin” is used to define how close a circuit is to this condition. Phase margin is simply the phase of AolB at the frequency where loop gain = 0dB. For example, 10 degrees of phase margin means that AolB has shifted by 170 degrees at the point where AolB = 0dB.

As you can see, loop gain is a key component of stability analysis. How can we observe this?

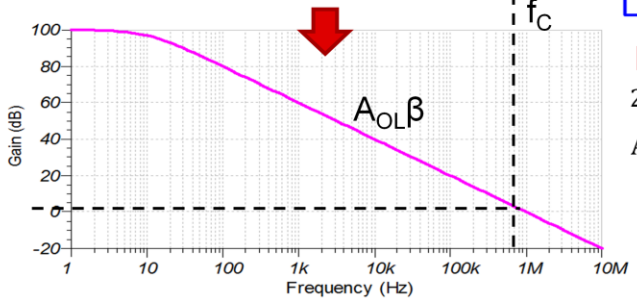
Loop gain magnitude: $A_{OL}\beta$





$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$



Loop gain in dB:

$$20\log(A_{OL}\beta) = 20\log(A_{OL}) - 20\log\left(\frac{1}{\beta}\right)$$

$$A_{OL}\beta(dB) = A_{OL}(dB) - \frac{1}{\beta}(dB)$$

Note: $A_{OL}\beta(dB) = 0dB$ when A_{OL} and $\frac{1}{\beta}$ intersect

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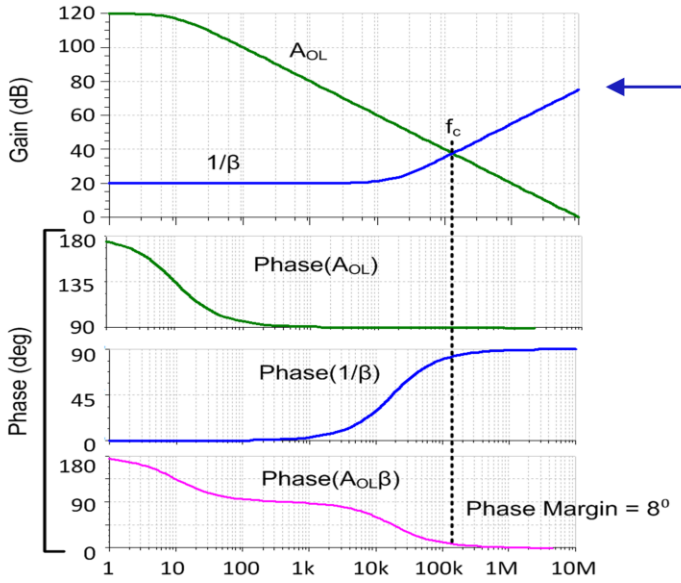
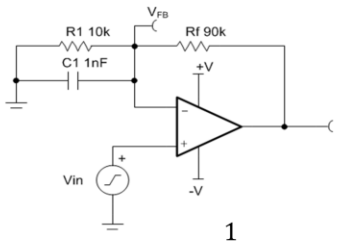
Well, first we can consider the loop gain magnitude using a Bode plot. Using the same circuit as before, we have a gain of 10V/V, or 20dB, so 1/B is a constant 20dB over frequency. The amplifier's Aol is also shown. To find the magnitude of AolB, we can simply subtract 1/B from Aol. This might not seem intuitive at fist glance, but thanks to the properties of logarithms it can be justified mathematically as shown above.

Remember in the last slide we stated that the phase margin is the loop gain phase at the frequency where AolB = 0. This frequency is called fc. This is also the frequency where Aol and 1/B intersect, which makes sense because the difference of two equal values is always zero.

Loop gain phase: phase($A_{OL}\beta$)





C1 introduces a zero in $\frac{1}{\beta}$

$$\frac{1}{\beta} = \frac{Z_f}{Z_1} + 1$$

At DC the capacitor is open, so gain = 10V/V. At high frequency the capacitor causes Z_1 to decrease, so gain increases by +20dB/decade

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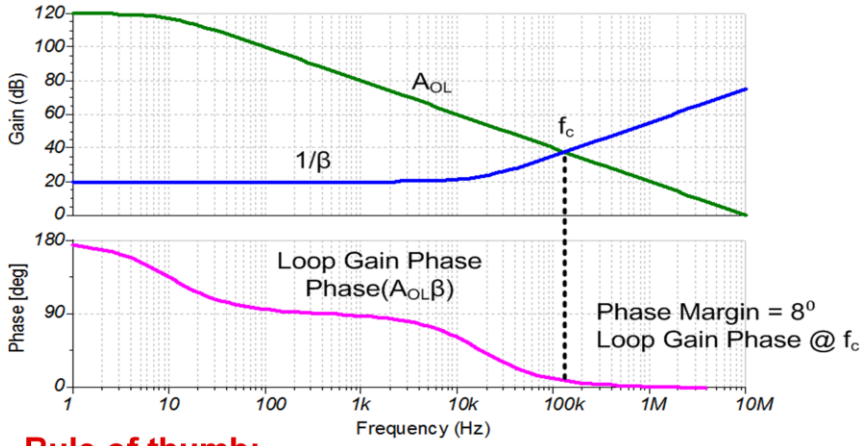
To measure the phase margin, we need to know the loop gain phase, or phase of AolB, over frequency. Using the same log properties as before, we can simply subtract the phase of 1/B from the phase of Aol to get the phase of AolB.

In this example, a capacitor was added to the feedback network of the op amp circuit. At DC the capacitor is open, so the gain is the same as before at 10V/V. At some higher frequency, the capacitor causes the impedance of the combination of R1 and C1 to decrease, so the gain of the circuit increases by +20dB/decade. This can be seen from the zero in the 1/B plot. Looking at the phase, the 90° increase in the phase of 1/B creates a 90° decrease in the phase of AolB, so phase margin becomes very low at only 8°.

Phase margin



Rule of thumb:

Phase margin > 45° is required for optimal stability!

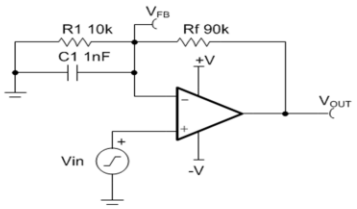
Phase margin < 45° is considered "marginally stable."

This does not ensure a robust design over process variation

Now that we know how to observe phase margin, let's review what it's actually telling us. Remember that what we want is to avoid the condition where the loop gain, AolB, equals -1. That means we have a phase shift of 180 degrees at fc, or 0 degrees of phase margin. For optimal stability, we use a rule of thumb which states that a phase margin of 45 degrees or higher is required. While a circuit may work with phase margin less than 45 degrees, it is considered to be only marginally stable and will still show overshoot and ringing. Also keep in mind that different devices will have different characteristics due to process variation, temperature, component value tolerances, and other fluctuations, so for a robust design you should really meet the 45 degrees of phase margin minimum requirement.

That being said, phase margin isn't the only way to analyze stability. Another method exists which is simpler, and can actually give more information about what causes the stability problem in a circuit.

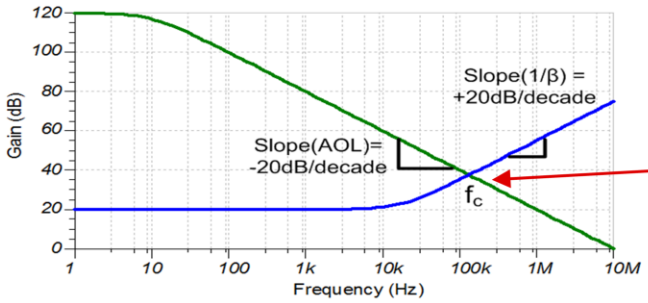
Rate of closure: Unstable example



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = 10\left(\frac{f}{f_C} + 1\right)$$

1/β(dB) = 20dB at DC, then increases by +20dB/decade after the zero frequency

Rule of thumb: Rate of closure = 20dB is required for optimal stability!



$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20\text{dB} - (+20\text{dB})| = 40\text{dB}$$

Unstable because rate of closure > 20dB!

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One quick way to evaluate stability is by looking at the rate of closure. The rate of closure is defined as the difference between the slope of the AoI magnitude curve and the slope of the 1/B curve at the frequency where the two curves intersect. These plots have well-defined slopes due to the poles and zeros in their transfer functions. By analyzing the rate of closure of AoI and 1/B at fC, the point where they intersect, we can quickly determine the stability of a circuit. The rule of thumb for this method is that the rate of closure at fc must equal 20dB for optimal stability.

Let's use our same circuit example from earlier with a capacitor on the op amp negative input. That capacitor causes a zero in 1/B, which makes 1/B increase with a slope of 20dB/decade. The AoI curve of the op amp is decreasing at 20dB/decade due to the op amp's dominant pole. When they intersect at fc, the rate of closure is the absolute value of the slope of AoI minus the slope of 1/B, which works out to be 40dB. Since the rate of closure is greater than 20dB, we can conclude that the circuit is unstable.

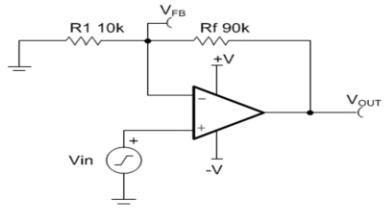
Besides being quick and easy to check, the rate of closure method has another benefit of showing us what in the circuit is contributing to instability. In this example, the slope of AoI is normal, and we see only the effect of the op amp dominant pole. However, the rise in 1/B indicates a zero in the feedback network, so we can then take steps to compensate for it. Phase margin alone does not give us this information.

The rate of closure method works because the slopes of AoI and 1/B are linked to the poles and zeroes in the circuit. A 20dB rate of closure means a circuit is only under the net influence of 1 pole, which means the phase margin is at least 45 degrees, enough for optimal stability.

Another way to think of this problem is to consider what is happening at the output of the op amp in

this circuit. Remember 1/B represents how the output of the amplifier must change to maintain feedback. In this circuit, our 1/B curve tells us that to maintain the desired feedback level the output of the amplifier needs to increase over frequency. The Aol of the amplifier limits how much gain we can actually get out of the circuit, and it decreases over frequency. So when these curves intersect with a poor rate of closure, its like we're telling the op amp it needs to increase its output voltage over frequency while it is simultaneously running out of gain to do so!

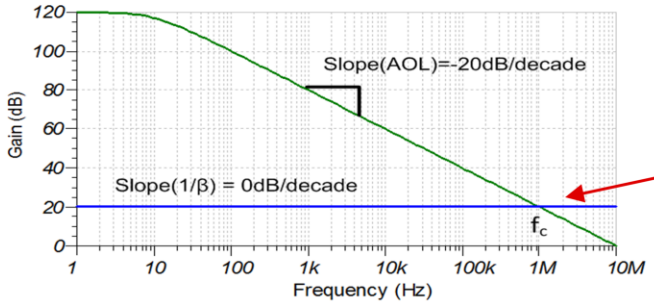
Rate of closure: Stable example



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

Rule of thumb: Rate of closure = 20dB is required for optimal stability!



$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20dB - 0dB| = 20dB$$

Stable because rate of closure = 20dB!

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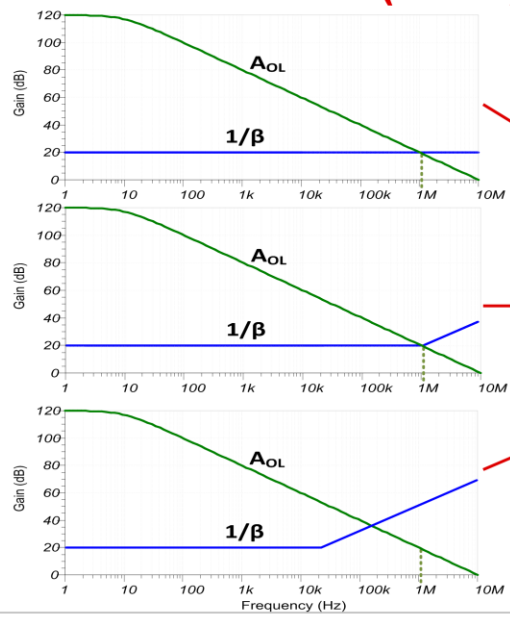
TEXAS INSTRUMENTS

We can also analyze this circuit from earlier in the presentation using the rate of closure method. In this case, there is no capacitor in the feedback network, so there is no zero and therefore no increase in 1/B. Aol is still decreasing with a slope of -20dB/decade as before. The rate of closure is now the absolute value of -20dB – 0dB, or 20dB. We can thus conclude that this circuit is stable. In more complicated circuits there are ways to cause instability that won't necessarily be reflected in the rate of closure, but the rate of closure analysis gives a quick and easy first order look at stability and in many cases is all you need to look at.

Rate of closure (ROC) and phase margin



ROC (dB/decade)	Phase Margin (°)
20	45 < PM < 90
20 < ROC < 40	45
40	0 < PM < 45

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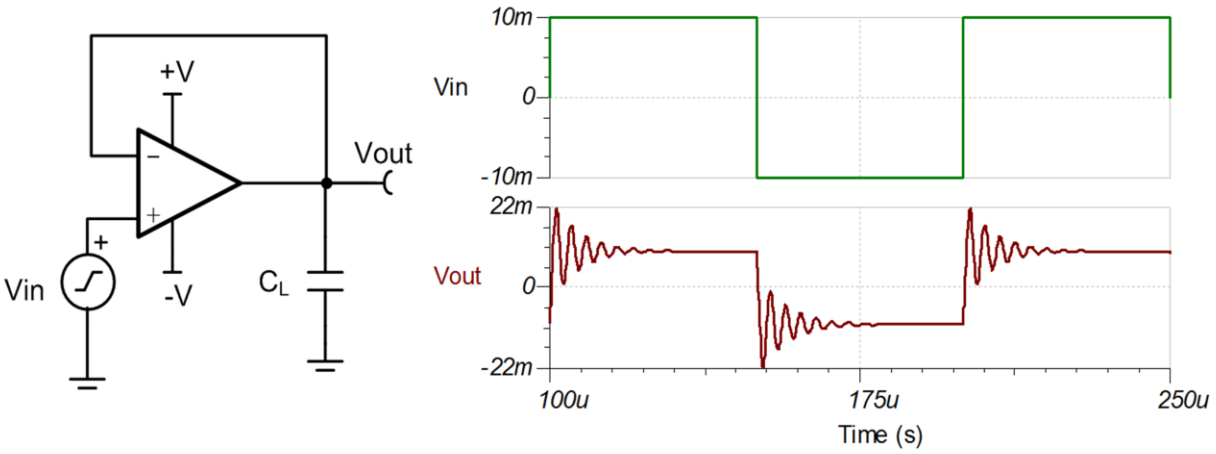
As shown in the previous slides, rate of closure and phase margin are closely connected. We can predict one value based on the other, and this slide gives three different examples of rate of closure and their corresponding phase margins.

In the first case, we have a rate of closure of 20dB/decade, so the circuit is stable and we have between 45 and 90 degrees of phase margin. Ideally, this is where we'd like to be.

In the second case, we have a zero in 1/B right at fc, so the rate of closure is beginning to change. At fc the rate of closure is somewhere between 20 and 40dB per decade, which corresponds to about 45 degrees of phase margin. Remember that a zero causes a total phase shift of 90 degrees, but 45 degrees of phase shift right at the zero frequency, so we get a total of 90 degrees of phase shift from the Aol dominant pole and 45 degrees of phase shift from the zero at fc. This leaves 45 degrees of phase margin.

In the final case, we have a zero in 1/B well before fc, so the rate of closure is exactly 40dB/decade. This results in between zero and 45 degrees of phase margin, which is generally not acceptable performance.

Why do capacitive loads cause instability?



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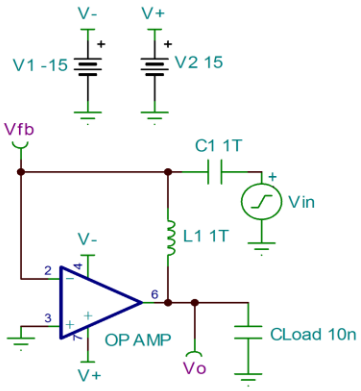
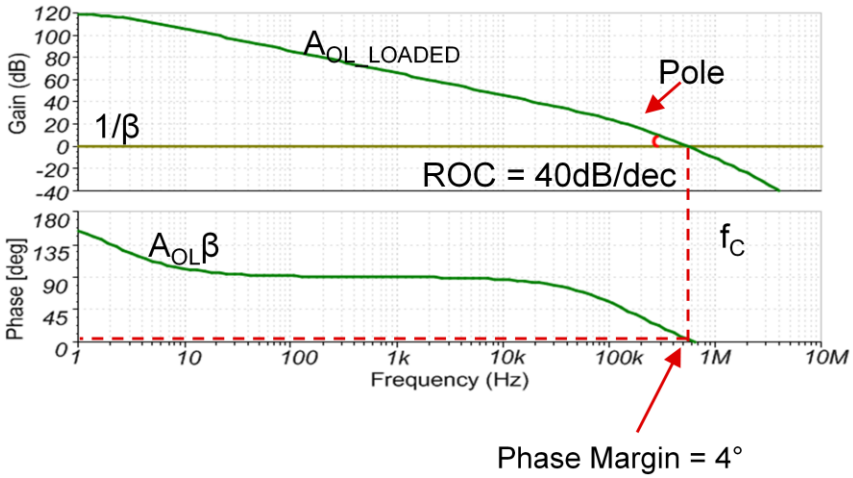
We saw earlier in the presentation, and you may have seen in your own experience, that capacitive loads can cause instability such as the overshoot and ringing shown on the right. Why does this happen? Let's see if we can use our plots to understand this behavior.

Simulating the effects of output capacitance

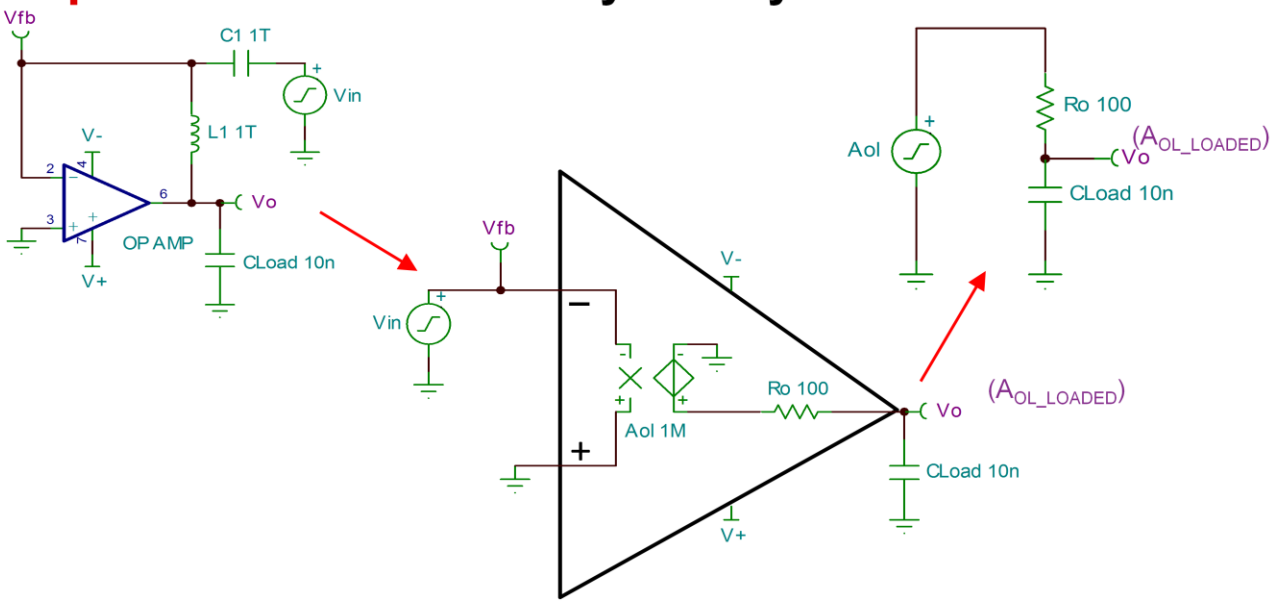
Run open-loop analysis on buffer circuit with capacitive load





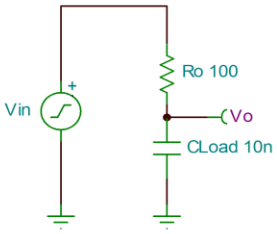
We've spent a lot of time looking at open loop curves, but how do we actually generate these in simulation? Well if we want to see Aol we have to run the op amp in an open loop configuration, but this will almost certainly cause the op amp to saturate and give us invalid results. The solution to this is to provide a way for the op amp to find a linear dc operating point, but run in open loop for ac signals. This is exactly what the oversized inductor and capacitor do in the circuit on the left. At dc, the inductor looks like a short circuit and the capacitor looks like an open circuit, so the simulation is able to find a stable dc operating point that keeps the amplifier in the linear region. Since the components are so large, once we start to apply any amount of ac, the indcutor looks like an open circuit and the capacitor looks like a short circuit. This allows us to inject a signal into one of the inputs and observe the open loop response of the amplifier. In this example we ran an open-loop simulation on the circuit shown here with a 10nF capacitor on the op amp output. As the results show, the 10nF capacitive load results in a pole in the Aol curve which degrades the Aol*ß phase to only 4 degrees at fc. Let's examine why this happens.

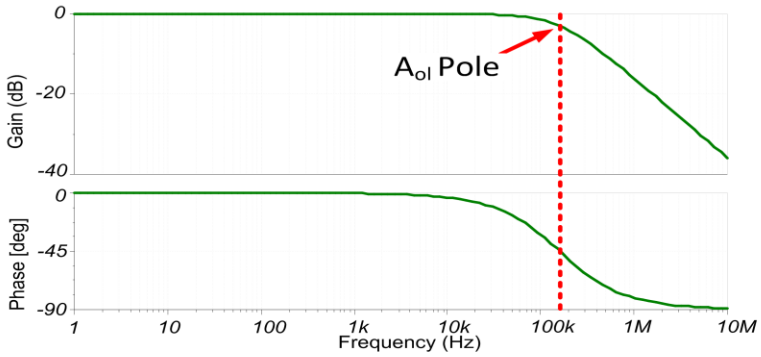
Capacitive loads: Stability theory



If we take a look at a simplified representation of the open-loop circuit, we see that the input signal passes through the Aol gain block and then the series open-loop output impedance, Ro, before reaching the op amp output, Vo. With a capacitor, Cload, on Vo, the op amp loaded Aol curve is divided down by an RC voltage divider. This creates a pole in the output of our amplifier.

Capacitive loads: Pole in Aol



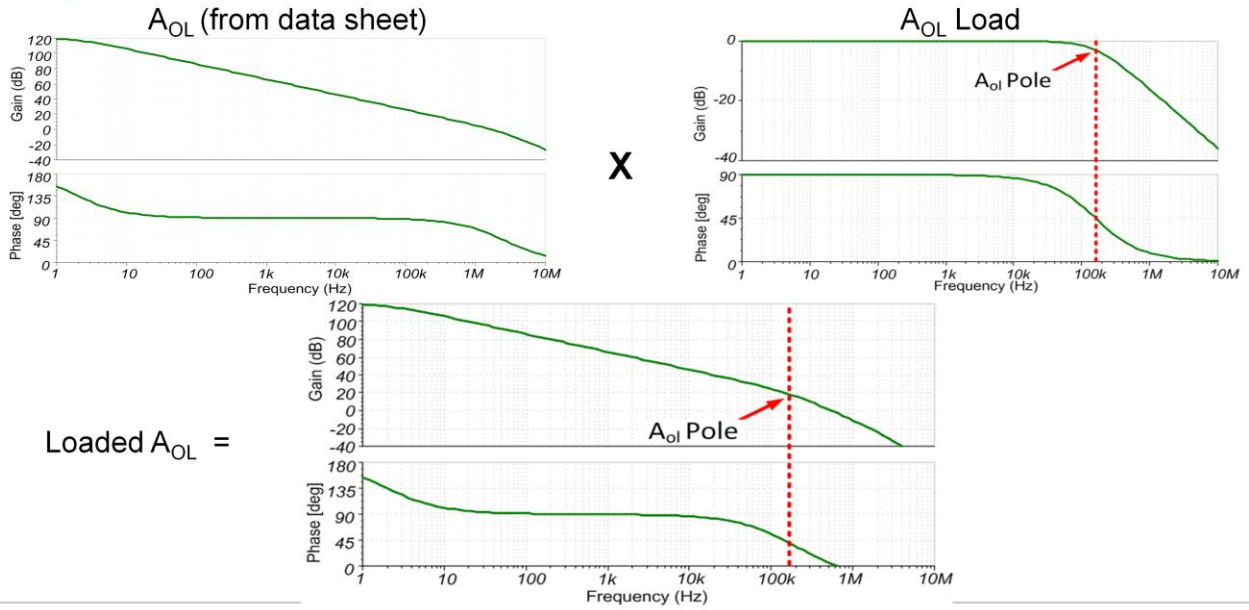


Transfer Function: $\frac{V_o}{V_{in}}(s) = \frac{1}{1 + s * Ro * C_{LOAD}}$

Pole Equation: $f_{POLE} = \frac{1}{2 * \pi * Ro * C_{LOAD}}$

The AC transfer function of the equivalent load RC circuit has been plotted here. The pole location can be calculated from the transfer function and is shown at the bottom of the slide.

Capacitive loads: Loaded Aol



If the original op amp Aol curve and the Aol load curve are combined, the result is the loaded Aol curve shown on the bottom. As shown, the pole from the interaction of Ro and Cload causes a change to a -40dB/decade Aol magnitude slope and a degraded unity-gain phase margin. It is this loss of phase margin in Aol that results in a degraded phase margin for our loop gain, which ultimately causes the amplifier to become unstable. In a unity gain configuration, we can see in this circuit our rate of closure would be 40dB.

There are only 2 things you need in an op amp macromodel to analyze stability problems:

Aol

(AC open loop gain)

Zo

(AC open loop output impedance)

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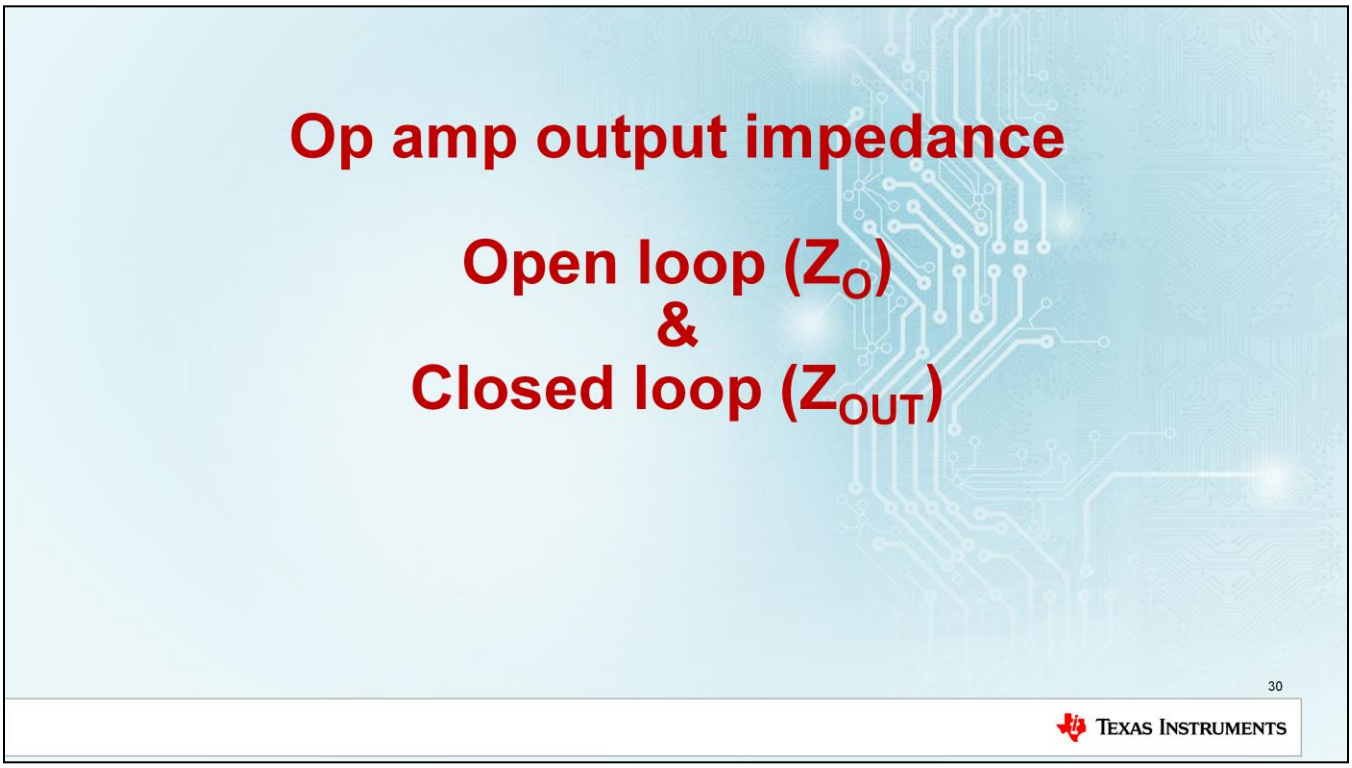
When analyzing stability problems there are only two parameters the absolutely must be modeled to see reliable curves: 1) The Aol and 2) The open loop output impedance. We just discussed why Aol is so important and how it can be used to understand stability, now let's talk about output impedance.



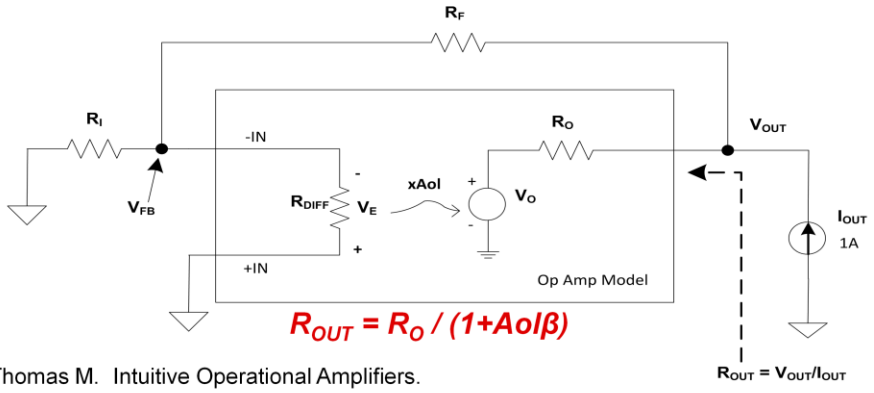
In the previous section, we took a look at the open loop gain of an amplifier and how it relates to stability. Now let's take a look at the other key parameter that is necessary to understand stability problems, the amplifier's output impedance.

Op amp impedance: Output resistance

Definition of Terms:

R_O = Op Amp ***Open Loop*** Output Resistance

R_{OUT} = Op Amp ***Closed Loop*** Output Resistance



$R_{OUT} = R_O / (1+Aol\beta)$

From: Frederiksen, Thomas M. Intuitive Operational Amplifiers. McGraw-Hill Book Company. New York. Revised Edition. 1988.

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There are two types of output resistance we can discuss when looking at an op amp. The first is R_O, the open loop output resistance of an op amp. The second is R_{OUT} defined as the closed loop output resistance of an op amp.

R_O and R_{OUT} are intimately related as we can see in the relationship defined in this slide. R_{OUT} is R_O reduced by one plus the loop gain. If we consider the effects of feedback, then intuitively this makes sense. Imagine that we sat on the output and injected a current into the amplifier. This current would produce a corresponding change in voltage through the output resistance of the amplifier. As this happens, the output voltage would tend to increase. But the output voltage is set by the input voltage and the feedback network, and the amplifier wants to keep the two inputs at the same potential to maintain linear operation. To account for this, the op amp tries to adjust its internal Vo to maintain the same Vout, and this effectively causes the closed loop output resistance to appear much lower than the open loop resistance! Remember that we can think of loop gain as the op amp's ability to adjust its output to correct for errors, and this is exactly what our equation for Rout is telling us. The more loop gain we have, the lower the output impedance and consequently the lower the impact of a disturbance on the output.

Op amp Impedance: Derivation of R_{OUT}

1. $\beta = V_{FB} / V_{OUT} = [V_{OUT} (R_I / \{R_F + R_I\})]/V_{OUT} = R_I / (R_F + R_I)$
2. $R_{OUT} = V_{OUT} / I_{OUT}$
3. $V_O = -V_E \, Aol$
4. $V_E = V_{OUT} [R_I / (R_F + R_I)]$
5. $V_{OUT} = V_O + I_{OUT} R_O$
6. $V_{OUT} = -V_E Aol + I_{OUT} R_O$ *Substitute 3) into 5) for V_O*
7. $V_{OUT} = -V_{OUT} [R_I/(R_F + R_I)] \, Aol + I_{OUT} R_O$ *Substitute 4) into 6) for V_E*
8. $V_{OUT} + V_{OUT} [R_I/(R_F + R_I)] \, Aol = I_{OUT} R_O$ *Rearrange 7) to get V_{OUT} terms on left*
9. $V_{OUT} = I_{OUT} R_O / \{1+[R_I Aol/(R_F+R_I)]\}$ *Divide in 8) to get V_{OUT} on left*
10. $R_{OUT} = V_{OUT}/I_{OUT} = [\, I_{OUT} R_O / \{1+[R_I Aol / (R_F+R_I)]\} \,] / I_{OUT}$
    - *Divide both sides of 9) by I_{OUT} to get R_{OUT} [from 2)] on left*
11. $R_{OUT} = R_O / (1+Aol\beta)$ *Substitute 1) into 10)*

$R_{OUT} = R_O / (1+Aol\beta)$

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Using the op amp model in the previous slide we can solve for R_{OUT} as a function of R_O and Aolβ. We see that Aolβ, loop gain, reduces R_O so that the output resistance of the op amp with feedback, R_{OUT}, will be much lower than R_O, for large values of Aolβ.

Op amp impedance: R_{OUT} vs R_O

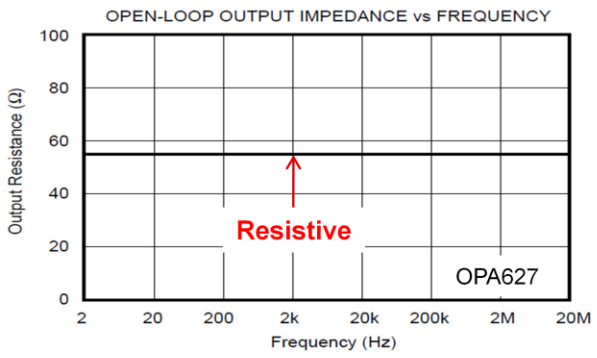
- **R_O does *NOT* change when closed loop feedback is used**
  - ❑ It does change with output current
- **R_{OUT} is the effect of R_O, Aol, and β controlling V_O**
  - ❑ Closed Loop feedback (β) forces V_O to increase or decrease as needed to accommodate V_O loading
  - ❑ Closed Loop (β) increase or decrease in V_O appears at V_{OUT} as a reduction in R_O
  - ❑ R_{OUT} increases as Loop Gain (Aolβ) decreases

The key things to remember, Ro is a characteristic of the output stage of the amplifier. It does not change when feedback is used, however it will change with the output current level as the on resistance of the output resistance changes.

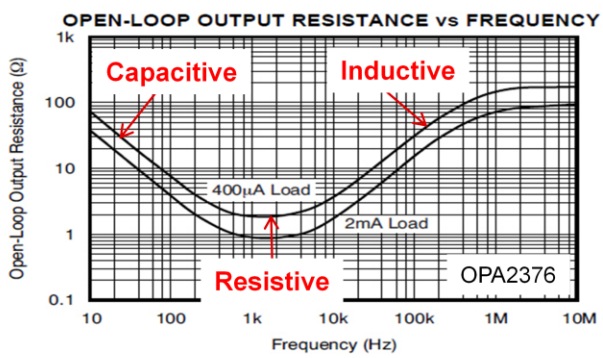
Rout is the result of Ro, Aol, and B controlling the internal “voltage source” of the op amp, which will increase or decrease as needed to hold the output voltage constant.

Op amp impedance: When R_O is really Z_O!

OPA627 has R_O



OPA2376 has Z_O



Note: **Some op amps have Z_O characteristics other than pure resistance – consult data sheet / manufacturer**

Most of the early op amp designs had purely resistive, low output impedances. While many devices today still retain this characteristic, it is becoming increasingly common for devices to have complex, reactive output impedances. In this example, the open loop output impedance of the OPA376 starts off capacitive, becomes resistive for a decade or so, and then becomes inductive over the remaining bandwidth of the device before it flattens out again. This can present additional design challenges that aren't encountered with resistive outputs. So what is responsible for this shift in output impedance and why would we want to design with devices that exhibit this behavior?

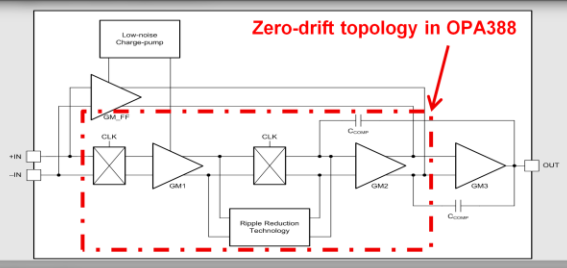
Amplifiers with reactive Zo: Zero drift

OPA388 | OPA333/0 | OPA188/0/9 | OPA334/5 | OPA2187 | OPA378 | LMP2021 | LMP2011

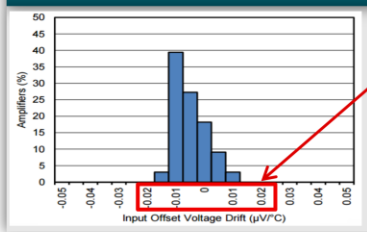
Overview

- Zero-drift (chopper stabilized or auto-zero) operational amplifiers continuously correct for error to achieve the lowest possible input offset voltage and drift, as well as minimized low-frequency noise.
- This circuitry also ensures excellent DC specifications (AOL, CMRR, and PSRR), allowing better performance in harsh environments.

Implementation

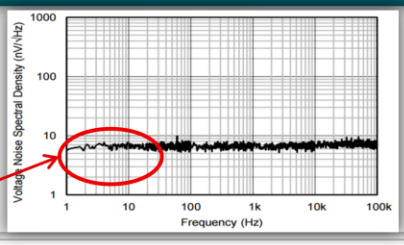


Problems solved



Ultra-low temperature drift (-40°C to +125°C)

Minimized low-frequency noise



Device Example:

Specifications	Zero-Drift OPA388	Non-Zero-Drift Amp
V_{os} (µV) (Typ, Max)	0.25, 5	200, 1000
V_{os} drift (µV/°C) (Typ, Max)	0.005, 0.05	0.3, 1.5
0.1Hz - 10Hz voltage noise (μV_{pp})	0.14	2.5

TI TechNotes *Zero-Drift Amplifiers: Features and Benefits"* LIT #: sboa182 Texas Instruments

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There are a lot of benefits to zero-drift amplifiers. These devices achieve incredibly low offset voltage and drift by continuously correcting for the offset error. This has the added benefit of eliminating 1/f noise. For dc precision zero-drift devices are hard to beat, but that precision comes at a cost. Every zero-drift amplifier exhibits a reactive output impedance that tends to be inductive over most of the amplifier's usable bandwidth. Consequently, this adds another layer of design considerations if you actually hope to see the performance improvements zero-drift amplifiers can offer.

Amplifiers with reactive Zo: Multi-stage feedback

OPA376 | OPA209 | OPA211 | OPA140 | TLV07 | OPA277 | LPV811

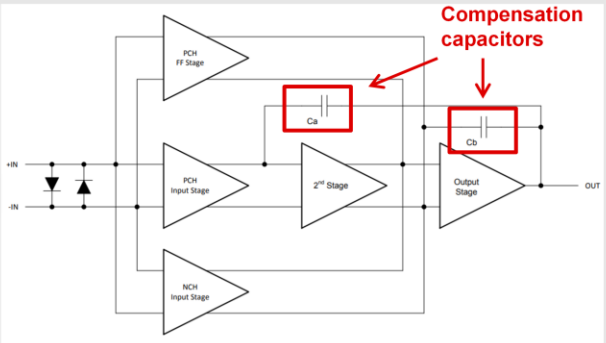
Overview

- Some Op amps use multiple gain stages to achieve the desired open loop gain.
- This is especially useful in low voltage rail-to-rail applications that want to avoid cascoded input stages.
- This requires compensation between stages for overall loop stability.

Advantages

- Many bipolar devices use this architecture to improve the output swing to the rail, because wider swing requires additional base current.
- Using a three-stage architecture allows for optimized distortion performance.

Implementation



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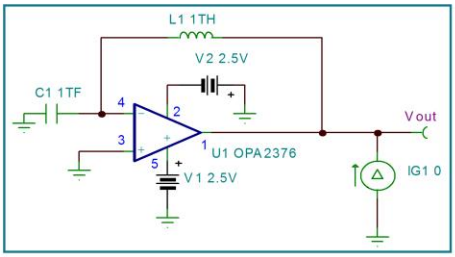
Zero-drift devices aren't the only kinds of amplifiers that produce these output characteristics though. Some amplifiers are designed with multiple stages. There are a variety of reasons to do this, for bipolar output devices it is necessary to have an intermediate stage to boost the base current to allow the device to swing closer to the rail. Having multiple stages is a simple way to increase the overall gain without having to design a single high gain stage. When multiple stages are used in order to achieve stability in the amplifier as a whole you have to have compensation between the stages. As different compensation capacitors come into play across frequency, the output characteristics of the amplifier change. Texas Instruments is not the only company that uses these techniques. In fact you can find op amps across industry that exhibit these same output characteristics!

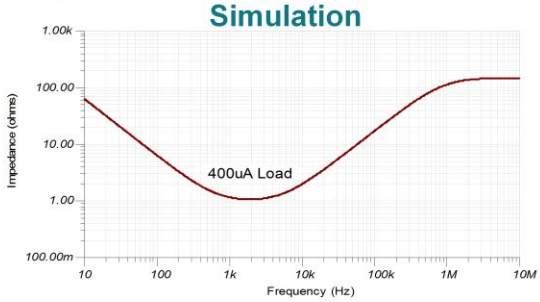
Complex Zo: Accurate models are key!



Z_O SPICE Test of Op Amp Macromodel:

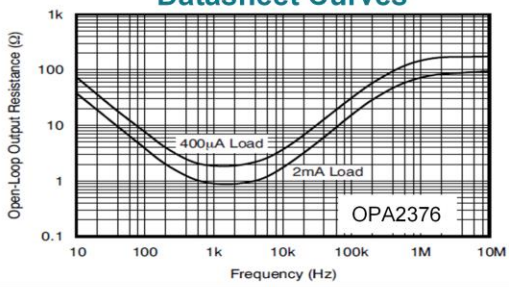
1. Run SPICE AC Analysis
   1. IG1 is an AC Current Generator
   2. IG1 DC Value=0A for unloaded Z_O
2. $Z_O = V_{OUT}$
3. Convert V_{OUT} (dB) to V_{OUT} (Logarithmic)
4. Z_{OUT} (ohms)=V_{OUT} (Logarithmic)

Simulation



VS

Datasheet Curves



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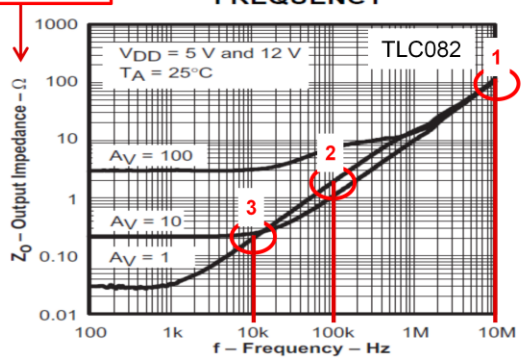
As previously stated, to analyze the stability of an op amp circuit in simulation there are two parameters that must be accurately modeled: 1) the open loop gain and 2) the output impedance. This slide shows how we can make a slight modification to our Aol test circuit to test the open loop output impedance instead. The inductor serves the same role of establishing a dc operating point, and the capacitor keeps the inverting terminal shorted to the same ground potential as the non-inverting input for ac signals. By perturbing the output with a current source and observing the resulting voltage response, we can characterize the open loop output impedance of the model. It is always a good idea to verify that the model matches the datasheet to a reasonable degree of accuracy.

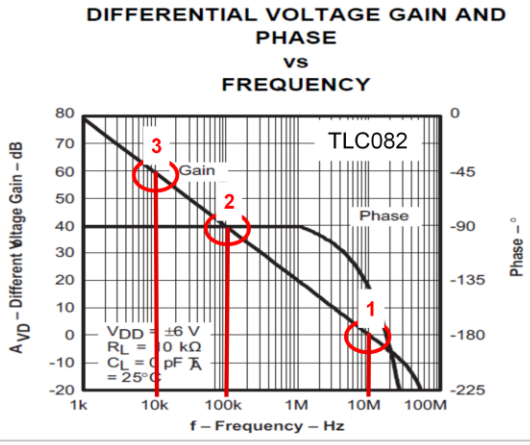
Some data sheets specify Z_{OUT} *NOT* Z_O

Recognize R_{OUT} instead of R_O:

- R_{OUT} inversely proportional to Aol
  - $R_{OUT} = \frac{R_O}{1+Aol\beta}$, where $R_{OUT} \propto \frac{1}{Aol}$
- R_{OUT} typically <100Ω at high frequency

This is really Z_{OUT} or R_{OUT}!





Not all manufacturers will specify parameters in the same way or provide the same curves, so it is important to understand which curve you are looking at. Within TI, we try to use the term Zo to refer to the open loop output impedance and Zout to refer to the closed loop output impedance, but not all datasheets conform to this standard. The easiest way to identify which curve you are looking at is to check for a gain specification associated with the curve. In the above example we can see curves for a gain of 1, 10, and 100. This immediately tells us the amplifier must have been in a closed loop configuration for the measurement and thus we know we are looking at the closed loop output impedance. Additionally, the closed loop output impedance is going to be inversely proportional to Aol, whereas the open loop output impedance is completely independent of Aol. The last hint is that the closed loop output impedance will tend to be much smaller and is typically less than 100 Ohms even out at high frequency.

Some data sheets specify Z_{OUT} *NOT* Z_O

Calculating R_O From R_{OUT}

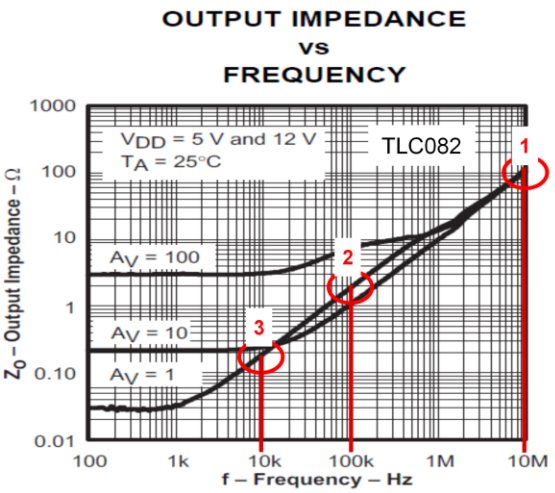
Computing R_O from R_{OUT} where $\beta = 1(0dB)$:

R_{OUT}=100Ω for A_V=1, f=10MHz, Aolβ=1(0dB)

$$R_{OUT} = \frac{R_O}{1 + Aol\beta}$$

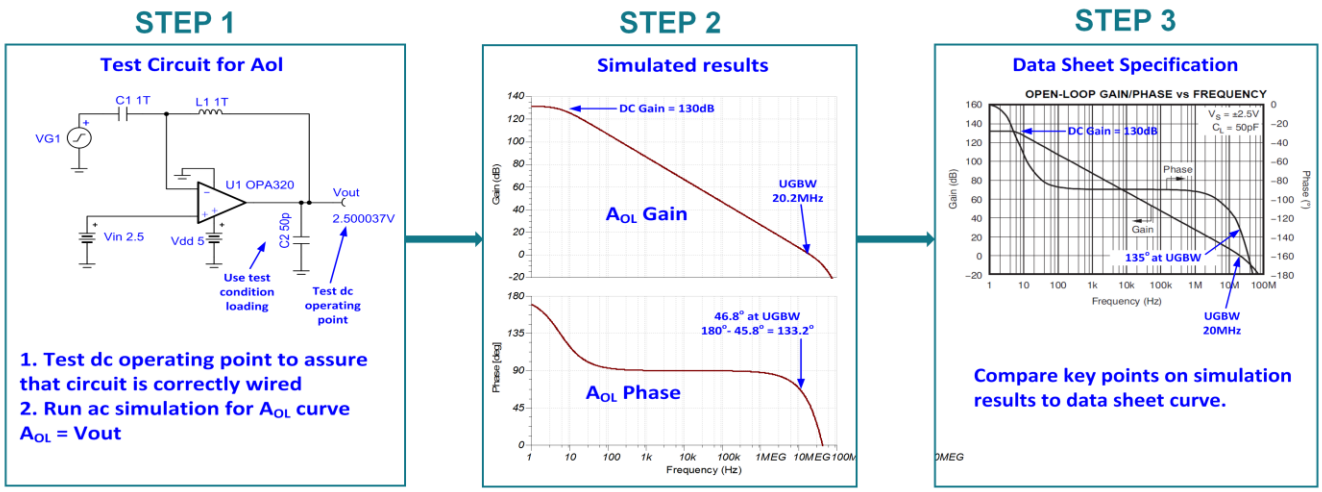
$$100\Omega = \frac{R_O}{1+1} \rightarrow R_O = 200\Omega$$

Point	frequency	Aol	R_{OUT} (A_V=1) Datasheet	R_{OUT} (A_V=1) Computed
----------	(Hz)	(dB)	(ohms)	(ohms)
1	10M	0	100	100
2	100k	40	2	2
3	10k	60	0.2	0.2



If we are given the closed loop output impedance but want to understand what the open loop output impedance looks like, then it's easy to calculate one from the other. We just have to remember that the two are related through the Aol. In this example if we take a look at the closed loop output impedance curve with the amplifier in a gain of 1 (where Beta = 1, or 0dB), then we can look at the point where Aol goes to 1, or again 0db. This is the unity gain bandwidth specified in the datasheet. For the TLC082 used in this example, this occurs at 10MHz. So if we look at the unity gain closed loop output impedance at 10MHz, we see that it is roughly equal to 100 Ohms. Since at this frequency our loop gain is equal to 1, our equation for closed loop output impedance simplifies to Rout = Ro/2, which is equal to 100 Ohms. Now we can see that our open loop output impedance must be 200 Ohms. If we use this value to calculate the closed loop output impedance for different frequencies where loop gain is greater than 1, then we see very good correlation between our calculation and what is shown in the curve.

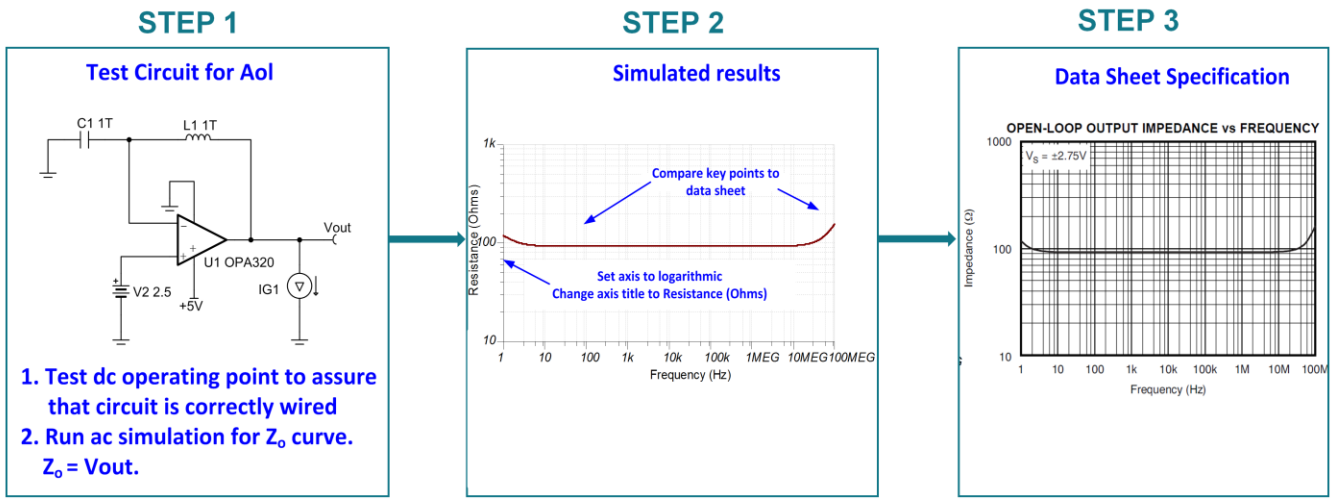
Op amp model: Open loop gain



AoI = -1*V_{OUT} for same phase in datasheet

Simulation can be an incredibly powerful tool, but if you are going to rely on models to design your system then it is always a good idea to double check that the model behaves according to the datasheet specifications. Most modern models are sophisticated and cover many of the parameters that concern designers. However, it's easy to check the models and it's better to be confidant in its operation. This slide shows how you would test the model for open loop gain. First we see the AoI test circuit we discussed previously. In the center you can see the TINA spice simulation results, and at the right the data sheet specification for open loop gain of this particular device. To compare two plots look at a few points on the magnitude and phase plot. Some key points to consider are the dc gain, and the unity gain bandwidth on the magnitude plot. In the phase plot check the phase at the unity gain bandwidth frequency. Note that sometimes the phase plot will be off by a 180° as the phase depends on how the circuit is measured, to have the simulation phase match the datasheet you can use the post-processor tool to generate the negative of the AoI curve. In this example you can see good agreement between the simulated results and the data sheet curve.

Op amp model: Open loop output impedance

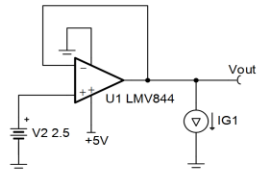


As discussed, another important curve is the open loop output impedance. The circuit used for this test is similar to the open loop gain test, as the feedback loop is broken for AC but is shorted for DC operation. The output here is connected to an AC current generator, and a voltage measurement probe is included. Also notice that the input is biased so that the output will be in a linear voltage range. This is necessary if you choose to simulate the device with a single supply. Again, for any simulation it is important to verify the DC operation before the AC simulation. This helps avoid problems caused by incorrect wiring. Once the circuit is connected and it's DC operation is confirmed you can run the "AC Analysis>AC Transfer Characteristic". For this simulation the output voltage is equal to the open loop output impedance, that is Zo (dB) = Vout (dB). Make sure that you change the vertical axis to logarithmic and scale to match the data sheet curve. In this case, you can see that the simulation result closely matches the data sheet specification so this model has properly modeled open loop output impedance.

Op amp model: Closed loop output impedance

STEP 1

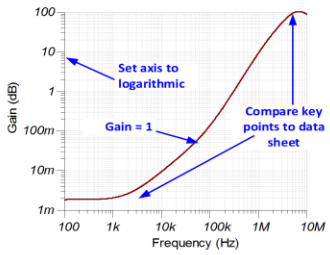
Test Circuit for Zout



1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for Z_{out} curve. Z_{out}= Vout.
3. Change the vertical axis to logarithmic scale

STEP 2

Simulated results



STEP 3

Data Sheet Specification

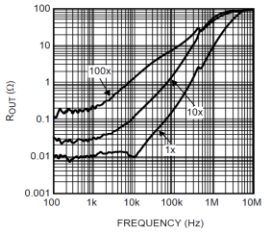


Figure 33. Closed-Loop Output Impedance vs Frequency

If the manufacturer only provides a closed loop output impedance curve, the open loop output impedance is directly related so it is sufficient to verify either curve. So in cases where the data sheet provides a closed loop output impedance curve, you can simulate this test circuit. Since this is closed loop impedance the feedback network is set according to the required gain. This example shows a gain of 1, but other gains may be needed depending on the data sheet graph. The output is connected to a current generator and a voltage measurement probe. Closed loop output impedance is equal to the output voltage in this simulation, that is Zout (dB) = Vout(dB). By changing the Y-axis to Logarithmic we get Zout in ohms (Zout(ohms) = Vout(Logarithmic)). Notice that the simulation results closely match the data sheet curve for unity gain. As long as the Aol and Zout curves of the model match the datasheet, then you can be confident that the open loop output impedance is also modeled accurately.

Summary: Overview

Op Amp Output Impedance

1) Before any stability analysis is done check the SPICE op amp macromodel for proper Aol.

2) Before any stability analysis is done check the SPICE op amp macromodel for proper Z_O (open loop output impedance).

2) Newer TI op amp datasheets give a Z_O curve. Test in SPICE for Z_O and compare.

3) Older TI and competitor op amps usually have a Z_{OUT} (closed loop impedance) curve. Test for Z_{OUT}. If Z_{OUT} and Aol are correct then so is Z_O.

4) If the macromodel is wrong, then there are ways to fix it. Contact the precision amps team at https://e2e.ti.com/support/amplifiers/precision_amplifiers/

To summarize what we've just discussed, before conducting any stability analysis, it's always a good idea to check the macromodel you are using to make sure it properly models Aol and output impedance. Most newer TI datasheets will provide an open loop output impedance curve that can be used to verify the model. Older TI datasheets, and datasheets from competitors often provide a closed loop output impedance curve, which can also be used to verify the model. If you find that the macromodel is wrong, then there are ways to fix it. Contact the precision amplifiers team at precisionamps@list.ti.com. We looked at just a few test circuits since we are primarily concerned with stability, but there are many other op amp parameters that may be important to verify depending on what you want from the simulation. Ian Williams has developed a "Trust but Verify" macromodel series that shows the various test circuits you can use to verify these other parameters. A link to this series can be found at the end of this presentation.

TLV07: TLV07ID

Internal Device Positioning

Parameter	Unit	OP07C (TI)	TLV07 (TI)
			Upgrade from legacy commodity op amp
Supply Voltage Range	V	6 to 36	2.7 to 36
GBW MHz	MHz (Typ)	0.6	1
Slew Rate	V/µs (typ)	0.3	0.4
Rail-to-Rail		-	Out
Vos	µV (Max)	-	100
Vos	µV (Typ)	60	50
Offset Drift	µV/°C (Typ)	0.5	0.9
Input Bias Current	nA (Typ)	1.8	0.04
Vn @ 1kHz	nV/√Hz (Typ)	9.8	19
Quiescent Current	mA (Typ, Max)	2.4, 5	0.95, 1.8
CMRR dB (typ)	dB (Typ)	120	120
Architecture		Bipolar	CMOS
Operating Temperature Range	°C	0 to 70	-40 to 125
Package Group		SOIC, PDIP, SO-8	SOIC
Price (1ku)	USD ($)	0.23	0.35

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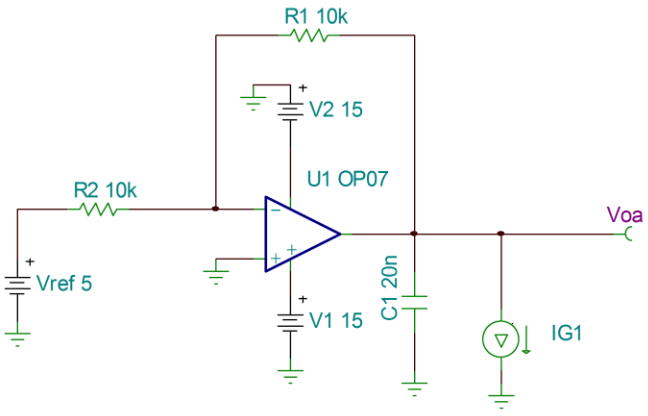
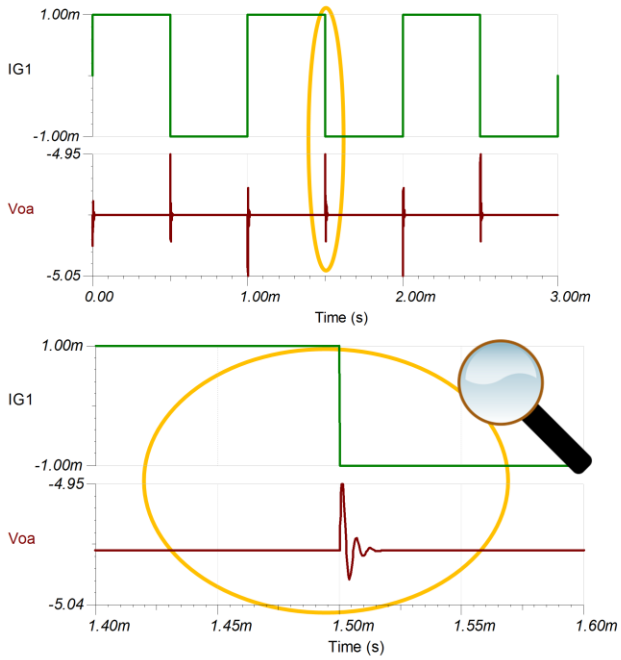
So now that we understand stability and output impedance, let's take another look at this problem!

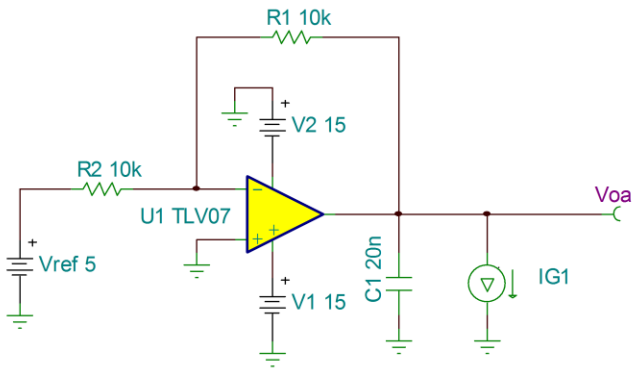
OP07: 20nF cap load



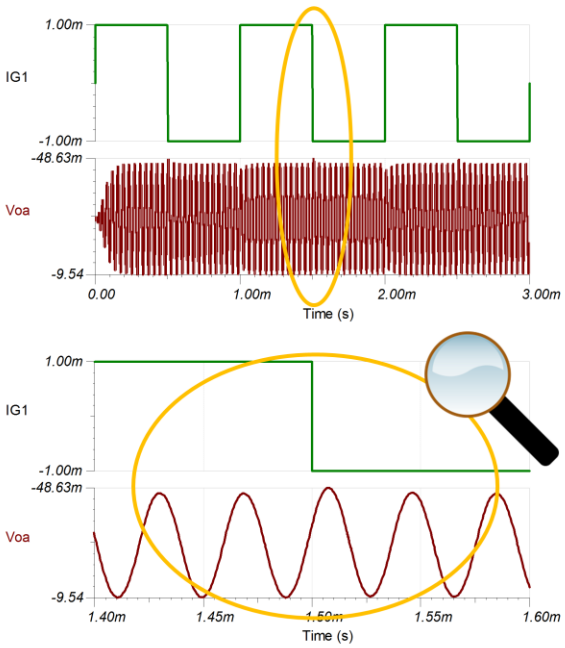


Here we have our OP07 circuit that achieves satisfactory performance.

TLV07: 20nF cap load

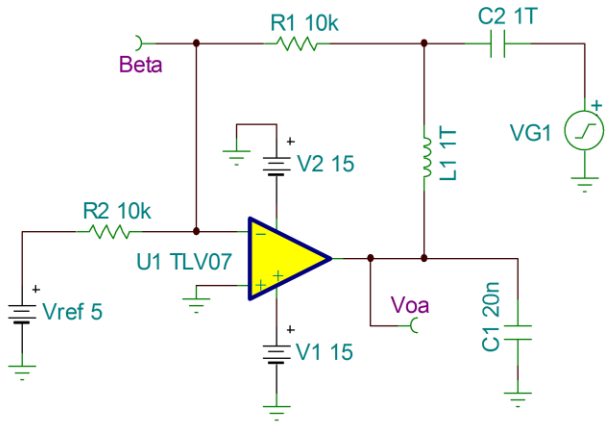


Oscillation at 25.97kHz!

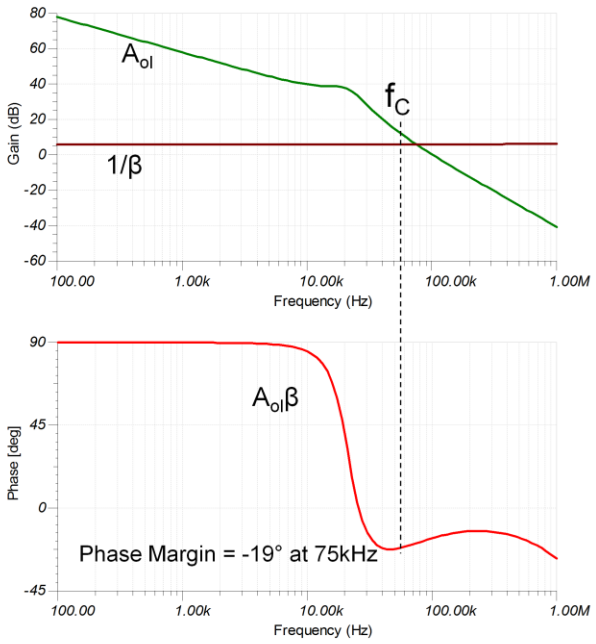


And our TLV07 oscillator…We can clearly see that this circuit is unstable, let's use some of our newfound tools to try to understand why.

TLV07: Loop stability



Voa = Aolβ
Voa/β = Aol



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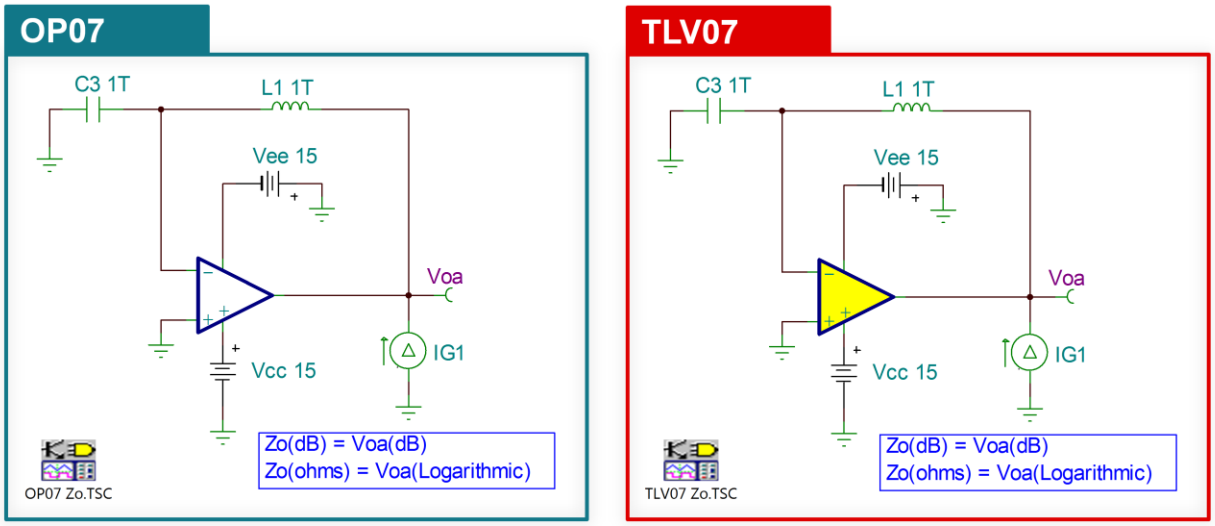
Using our open loop test circuit we can see from the Aol and 1/β curves that Aol is decreasing at ~40dB/decade when it intersects 1/β. This violates our rate of closure criteria and we can see from the loop gain phase that we actually have negative phase margin! But what is causing this? Based on our previous discussion on stability, the output impedance might be a good place to start looking.

TLV07 vs OP07: Output impedance (Zo)



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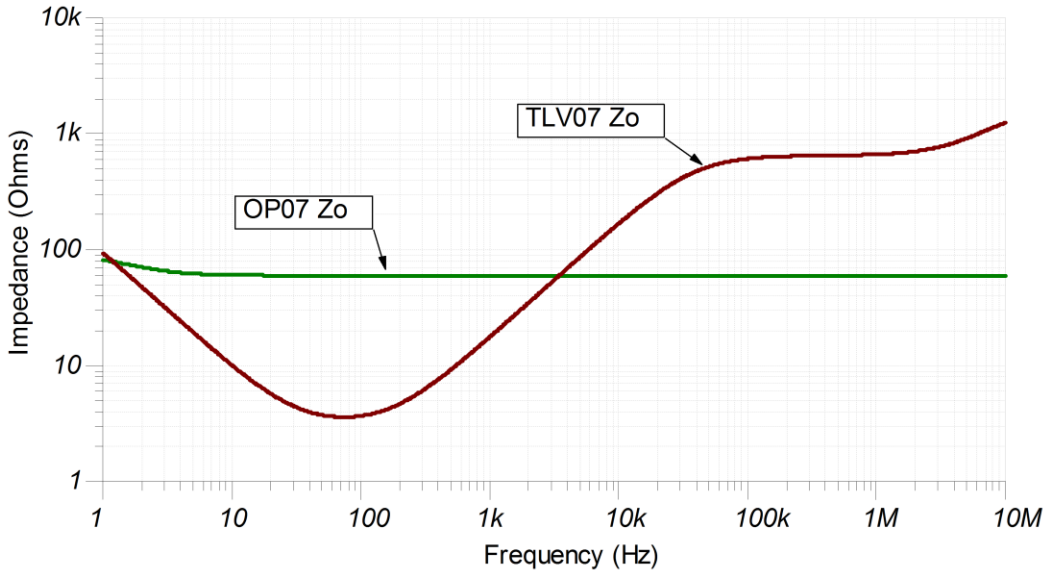
Let's test the macromodels of the OP07 and TLV07 using the open loop test circuits we discussed to see what their respective output impedances look like (and of course verify that they match the datasheet!).

TLV07 vs OP07 Zo



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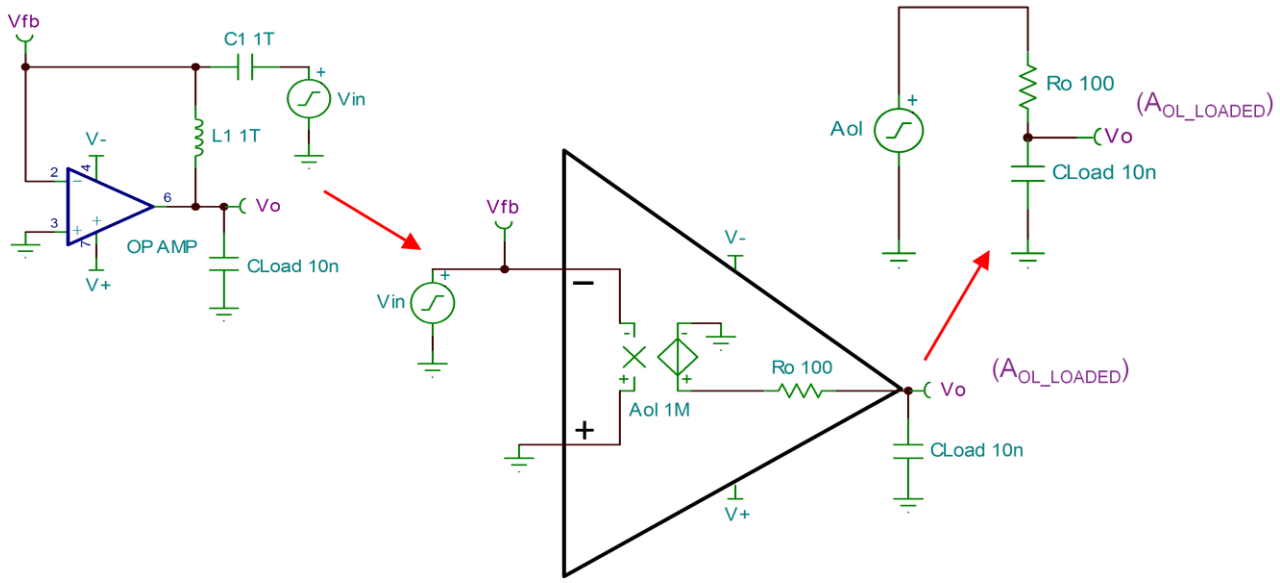
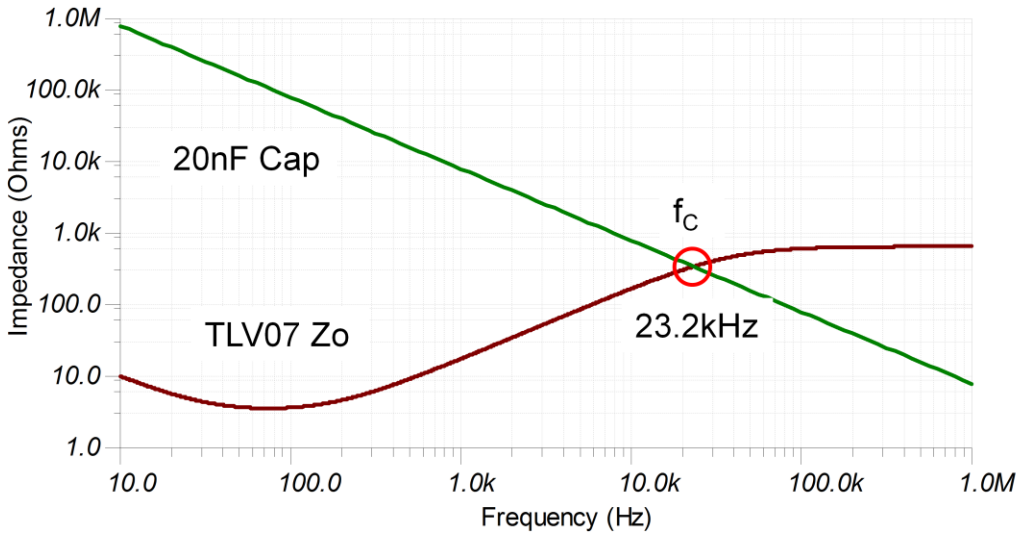
Sure enough, the OP07 has a well behaved resistive open loop output impedance while the TLV07's impedance looks inductive over the majority of its usable bandwidth. Now we might start to suspect that this is the root cause of our oscillation, but how can we verify this?

Capacitive loads – Stability theory



From our stability discussion on capacitive loads, we know how to find the pole created by a resistive output impedance and a capacitor, but what do we do if the output impedance has reactive elements to it?

Is it really output impedance?



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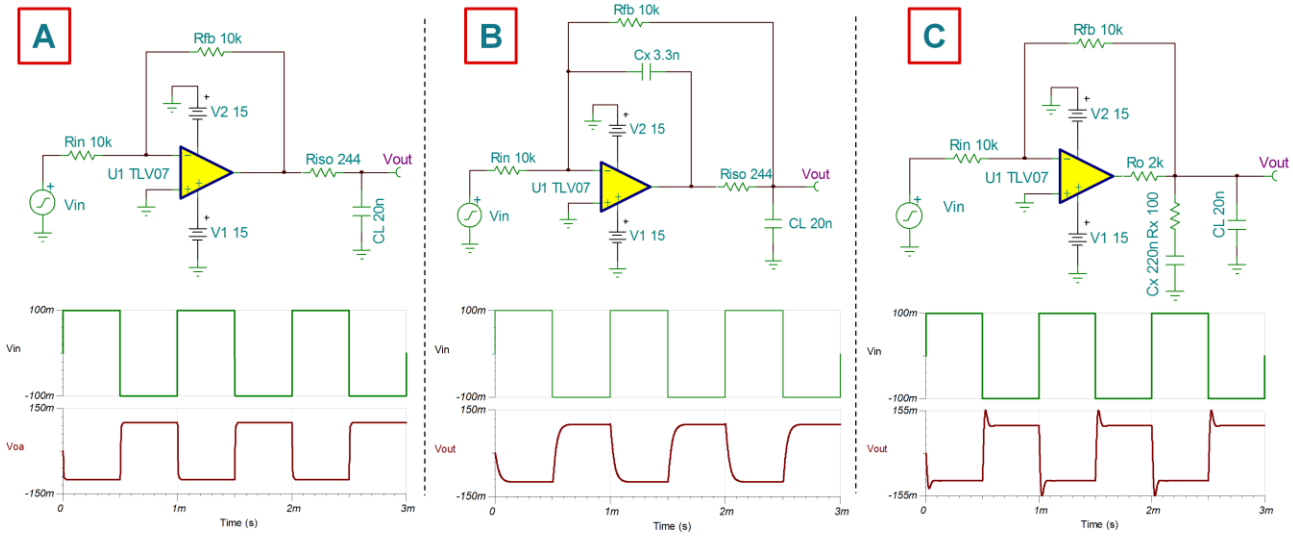
Well one thing we could do is look at the output impedance of the op amp over frequency against the impedance of our capacitive load, just like we would to understand the interaction between an inductor and a capacitor. From this perspective it is easy to see that we have an LC resonance between the output capacitor and the TLV07 Zo. Even better, the intersection of the curves roughly predicts the observed oscillation frequency! This gives us some confidence that what we are seeing really is the root cause of our issue.

Looking at Aol vs. looking at output impedance

- Output impedance isn't resistive so it's not straightforward to understand how to comp the op amp!
- Most stability problems can be solved by manipulating the feedback **IF** the output impedance is resistive.
- With a complex output impedance there is potential for complex conjugate poles in Aol, and manipulating the feedback will never fix this resonance!

So we've discussed looking at the open loop gain curves alongside the feedback network and looking at the output impedance interaction with a load, but how do we know which one to look at to understand our problem? As is generally the case in engineering, the answer is it depends. Both approaches are really two sides of the same coin and showing you the same problem from a different perspective. It's useful to look at the Aol and 1/β curves to understand phase margin and see what your rate of closure looks like, but these curves don't always offer much insight into the interactions that shape the curves. Looking at the output impedance curves against the load gives us insight into those interactions and allows us to see exactly why the Aol curve looks the way it does. This can be a useful perspective because if you have a resonance between your open loop output impedance and your load, no amount of compensation in your 1/β network is going to fix the problem, even if you satisfy the rate of closure criteria! You must first eliminate this resonance, and then the circuit can be compensated with traditional techniques.

How do we fix it?



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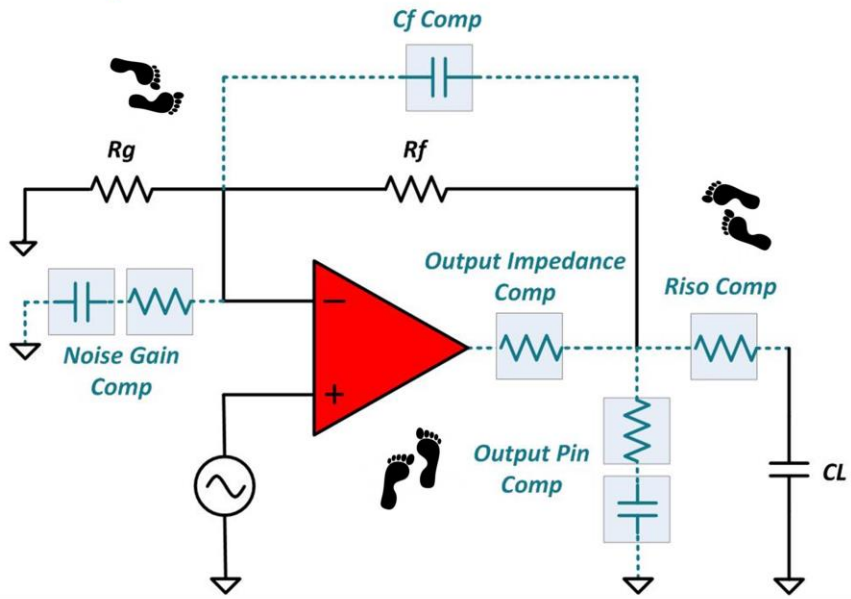
So once we understand the problem, what can we do to fix it? Well, there are many ways to fix this problem without changing the value of the capacitive load and which one is ideal depends on what the customer cares about most. Circuit A gives the fastest step response, but the isolation resistor results in a voltage drop if the op amp needs to source/sink current and this degrades the accuracy. Circuit B adds a second feedback path to account for this voltage drop, but its response is a little slower. Circuit C accounts for the voltage drop and settles faster than case B, but also produces an underdamped response with overshoot, and still can't source much current because of the relatively large output resistor required. All of these solutions involve isolating the reactive output impedance of the op amp from the capacitor in some way or another, and thus eliminating the resonance between the two.

Compensation schemes: check for footprints



- An op-amp driving a cap load almost always requires compensation!
- Encourage customers to leave space for these components!

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There are many ways to compensate an op amp for stability. Some of the more common approaches are shown above. Each method has its merits and can be more or less suitable depending on what the customer cares about and what kind of load they are driving. The point of this slide is to show the different ways you can fix a problem if it occurs. One of the most frustrating situations to be in is when a customer has a major issue with their design that they want you to fix, but they aren't willing to add anything to the schematic to fix it. This often occurs when they are too far along in the design process to make layout revisions without incurring significant cost. An extra footprint added in the initial design phase, doesn't cost anything but a little extra board space and a zero ohm resistor if the component is not needed. Encouraging customers to include footprints around their device ensures that if they do encounter problems, we have the necessary tools to fix it!

Summary

1) OP07 Zo (open loop output impedance) is predominantly resistive within the unity gain bandwidth of the op amp.

2) TLV07 Zo (open loop output impedance) is predominantly inductive over four decades of its the unity gain bandwidth.

3) Any design replacing OP07 with TLV07 should be verified for stability!

4) ***Problem:*** Most customers using DC voltage circuits don't bother to test for stability, but a disturbance on any pin could potentially cause erratic behavior and lead to invalid readings or system shutdown.

To summarize what we've discussed, the issue with our circuit ultimately boiled down to the fact that the OP07 has a predominantly resistive output impedance over the bandwidth of the op amp, while the impedance of the TLV07 is primarily inductive over its bandwidth. This causes problems with the capacitive load on the output and requires compensation. Most customers don't necessarily think to verify dc circuits for stability, but a disturbance on any pin of the device can potentially lead to oscillation. Therefore, it is highly recommended that any design that attempts to replace a device with a flat output impedance with one that has a reactive output impedance should be verified for stability.

Output impedance and driving converters

Let’s take a look at another very common customer application, driving analog to digital converters. Most modern systems rely on data taken from transducers to be reliably and accurately quantized into digital bits that controllers can process to establish how the system is performing and what it should do next. Accurately translating the information from the sensor into the digital realm can be a challenging task in itself, and to make sure you achieve the performance you are after special attention must be paid to the amplifier design.

ADS8363

1 MSPS | 16-bit | 4x2/2x2 Simultaneous Sampling ADC

Features

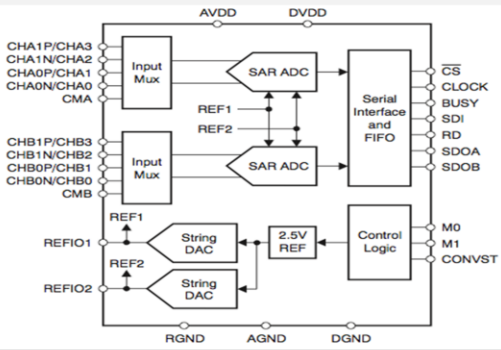
- Dual, 4-Ch pseudo-differential or 2-Ch differential configurable inputs coupled with a dual 2.5V programmable reference
- Dual ADCs with true 16-bit Performance
  - NMC @ 93dB SNR (typ)
- Integrated Industrial Solution
  - 4 deep per-channel FIFO
  - Auto-scan Mode

Benefits

- Input muxes and **dual programmable internal reference** enable input range scaling and monitoring up to 8 different signals
- Allows **resolution flexibility** without board or control software redesign

Applications

- Motor control
- Power quality measurement
- Protection relays
- Industrial automation



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Let's say you have a customer that is working on a resolver in a motor control circuit. This application requires accurately measuring the voltage across two windings that are physically positioned 90 degrees from one another with respect to a rotary transformer. By comparing these two signals the position of the motor can be accurately determined. Doing this accurately requires that the two signals from the winding are measured at roughly the same time, so many customers like to use devices like the ADS8363, which offers simultaneous sampling of two channels at a time, 16-bit resolution, and a maximum sampling rate of 1MSPS.

ADC input drive design

			MIN	MAX	UNIT
t_{DATA}	Data throughput, f_{CLK} = max		1		µs
t_{CONV}	Conversion time	Half-clock mode	17.5		t_{CLK}
		Full-clock mode	35		
t_{ACQ}	Acquisition time		100		ns
f_{CLK}	CLOCK frequency	Half-clock mode	0.5	20	MHz
		Full-clock mode	1	40	

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input range	(CHxxP – CHxxN) or CHxx to CMx	$-V_{REF}$		$+V_{REF}$	V
V_{IN}	Absolute input voltage	CHxxx to AGND	–0.1		AVDD + 0.1	V
C_{IN}	Input capacitance	CHxxx to AGND		45		pF

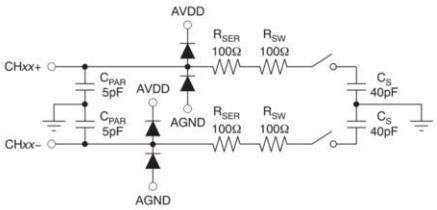
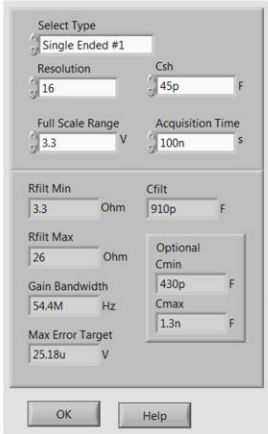
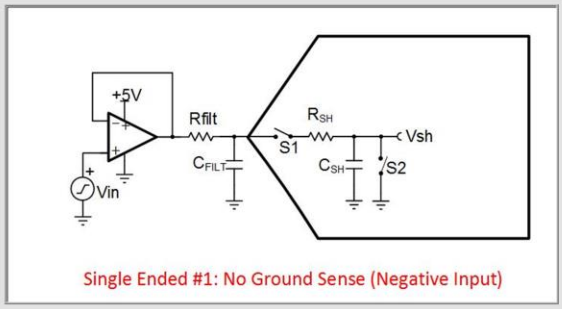


Figure 28. Equivalent Analog Input Circuit





Single Ended #1: No Ground Sense (Negative Input)

http://www.ti.com/tool/ANALOG-ENGINEER-CALC

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So the customer has decided to use the ADS8363, and now they are looking to design the input amplifier circuit to properly drive the converter. So they turn to TI's handy design calculator tool to help them figure out what they need. By plugging in a few values from the datasheet (resolution, sample and hold capacitance, full scale input range, and the acquisition time), the calculator tells you what kind of bandwidth you need for your op amp and a range of values to choose from for the RC output filter. For the parameters shown above, we see that we need roughly 55MHz of bandwidth to achieve the desired settling performance. From the calculator, something like 1nF and 10 Ohms would be a good starting point for our RC filter.

OPA835 Ultra-Low Power, 56MHz, RRO, Negative Rail In, VFB

Features

- Single/Dual Channel Options
- **Ultra-Low Power:**
  - 250µA/ch, Power-Down: <1µA
- **Ultra Low Distortion:** 0.00003%
- **Bandwidth:** = 56MHz G = 1V/V
- Input Voltage Noise: 9.3nV/√Hz
- RRO – Rail-to-Rail Output
- +2.5 to +5V Single Supply
- -40°C to 125°C Operating Temp

Channels	Packages	Body Size
1-Ch	6-pin SOT-23	2.9 mm x 1.6 mm
	10-pin QFN	2.0 mm x 2.0 mm

Benefits

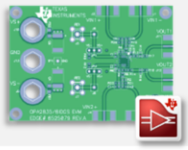
- Flexible supply for power sensitive applications
- Exceptional performance at very low power
- Increased dynamic range / sensitivity
- Low signal distortion
- Larger outputs in low voltage applications
- Integrated gain setting resistors enables smallest PCB footprint

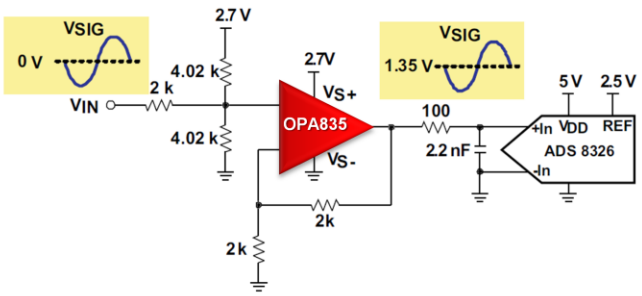
Applications

- Low Power Signal Conditioning
- Low Power SAR and ΔΣ ADC Driver
- Portable Audio Systems
- Ultrasonic Flow Meter

Tools & Resources

- Device Product Overview: LINK
- Device Evaluation Board (EVM): LINK
- Support: LINK
- Reference Design: LINK TIDesigns





TEXAS INSTRUMENTS

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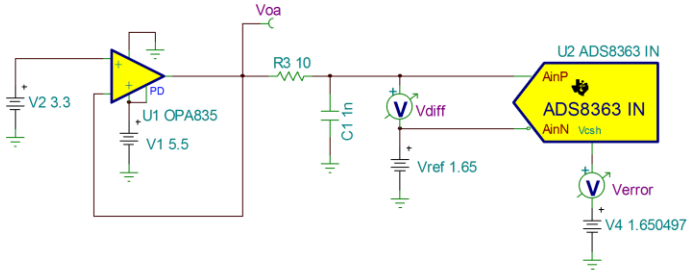
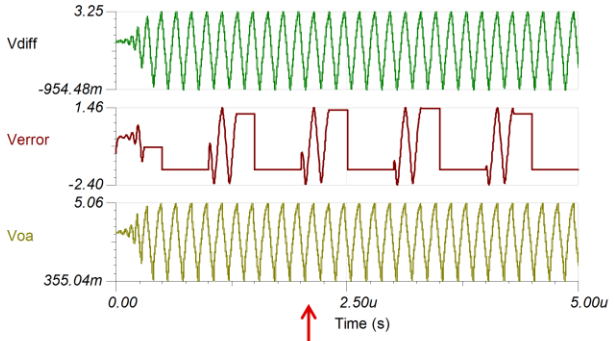
From the calculator tool we see that we need an amplifier that has a bandwidth of 55MHz. Let's suppose that the customer is also concerned about the package size and the power consumption, so you direct them towards the OPA835, an ultra low power 56MHz amplifier that is offered in a QFN package.

OPA835: ADC drive





Customer

You

Customers usually read ADC codes and don't observe this directly!

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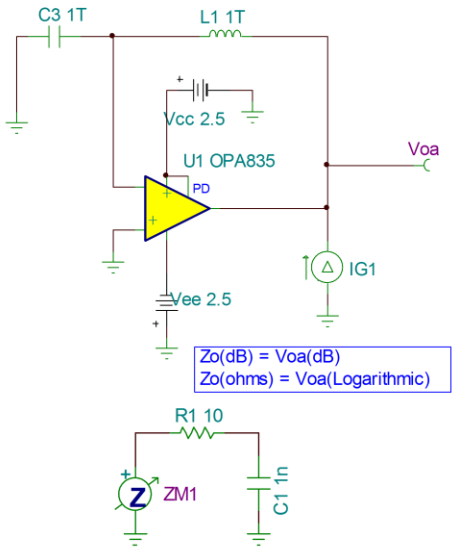
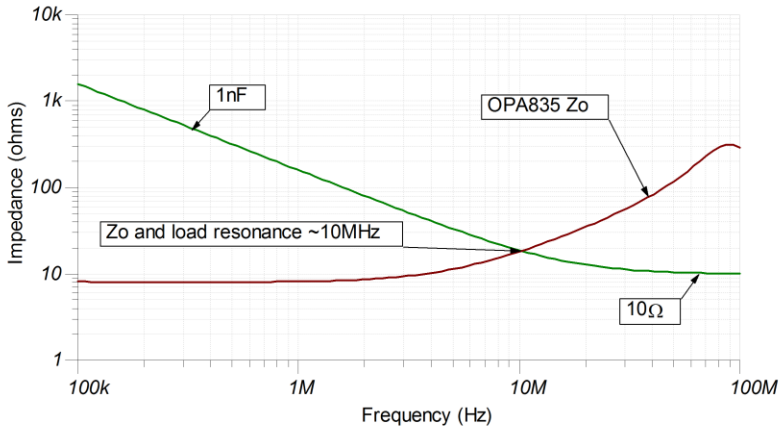
So we take this amplifier and we start with the nominal RC values given by the calculator. The customer connects it to the ADC only to find it doesn't work! Now the customer is angry and telling you things like "The op-amp is very noisy", or "the offset drift is too high", and they threaten to use a competitor part if you can't fix the issue. If we were to look at the output of the OPA835 directly, we'd be able to see that the circuit is actually oscillating, but given that customers will typically use the readings from the ADC to determine what is happening, the behavior is not always clear. Let's take a step back and use our analysis tools to try and figure out what the problem is. Based on our previous discussions it's probably a good idea to double check the output impedance to see if this could help us understand the issue.

OPA835: Zo and load impedance





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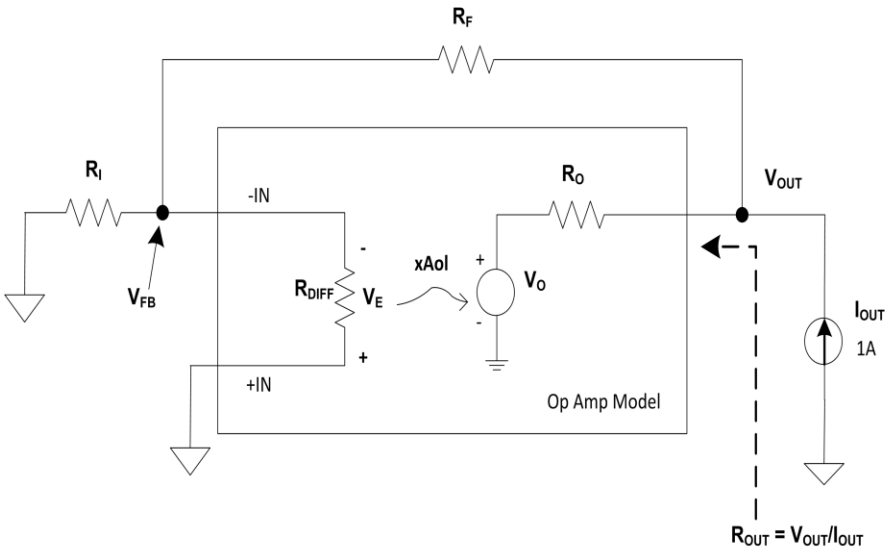
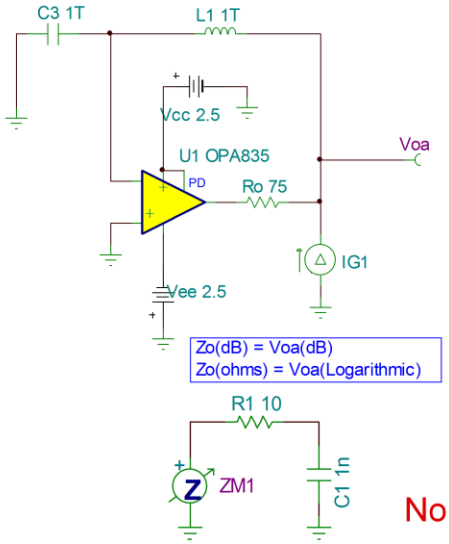
This slide shows the open loop output impedance of the OPA835 against the impedance of a load consisting of a 10 Ohm resistor and a 1nF capacitor. Sure enough, we can see that the open loop output impedance of the OPA835 is inductive over the region where it interacts with our RC load and this effectively produces an LC resonance that is causing our circuit to oscillate. We chose the RC values we did in order to satisfy the settling error requirements for the converter, so we'd like to avoid changing them too significantly if we can. What else can we do to address this problem?

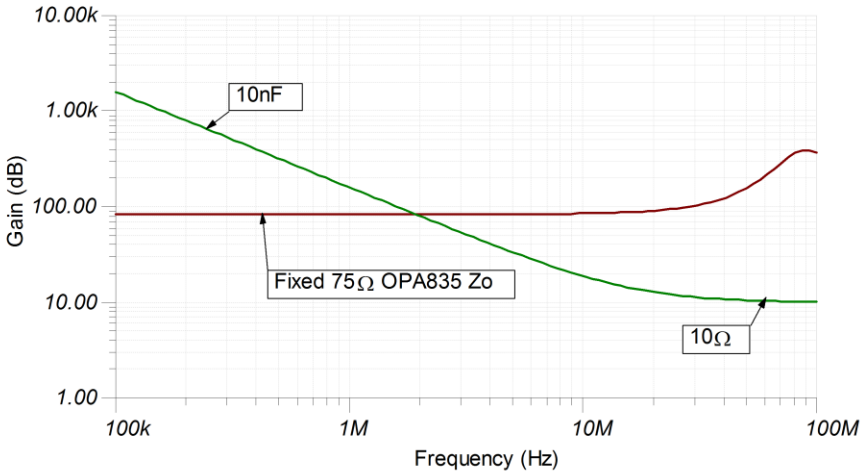
Open loop output impedance: Can I change it?



Well let's take another look at our simplified op amp model. We know that the open loop output impedance of the op amp is a parameter of the device, and we can't directly change the characteristics of the output stage. But what if we could change the effective impedance that is seen looking back into the output? Based on our model, the Zo looks like a resistor between the output and the internal "voltage source." One thing we might try is placing a resistor in series with the output BEFORE we close the feedback loop. Let's see what this does…

OPA835 Zo and load impedance: Compensated

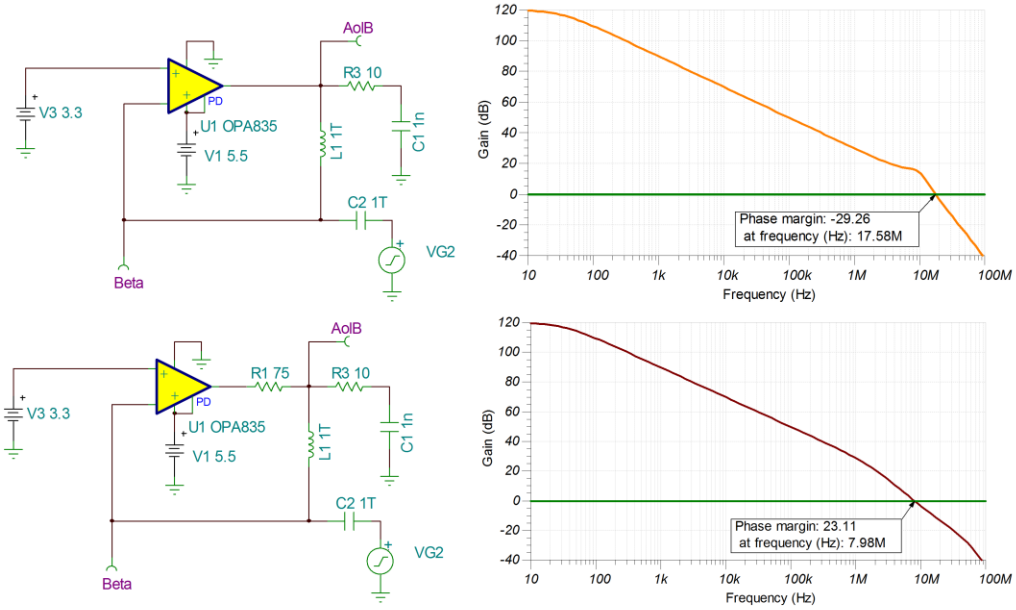




No resonance! Does this mean the circuit is stable???
Not necessarily…

In this slide we can see how the open loop output impedance of the amplifier effectively “changes” if we add a resistor in series with the op amp output inside the feedback loop. Remember that when two resistors (or impedances) are in series, the larger of the two will dominate. We can see from the curve above, that by adding a 75 Ohm resistor to the circuit we are able to make the output impedance look mostly resistive in the low frequency range and the inductive region doesn’t become dominant until we are out in the higher frequencies. Now the interaction with the 10nF capacitor does not cause resonance. Now that we have fixed the resonance, does this mean our circuit is going to be stable? Well not necessarily, but it certainly gets us a lot closer as we will see.

Loaded Aol: With and without Ro



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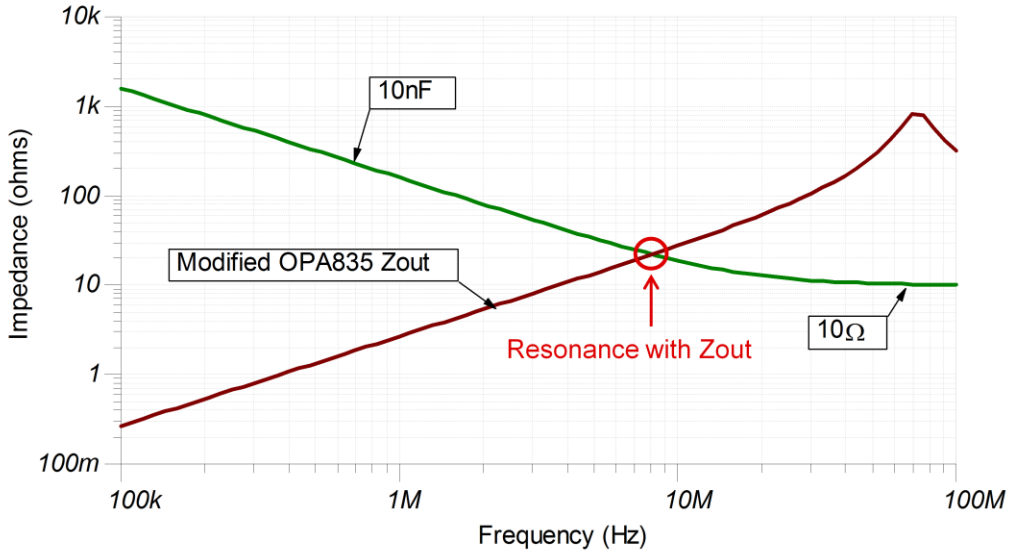
Without the resistor inside the feedback loop we can see the complex conjugate pole pair manifesting in Aol and a resulting phase margin of -30 degrees. This explains why the circuit was oscillating! Once we add the resistor, we've eliminated the complex conjugate poles, but we can see that we still have a 40dB rate of closure and thus are only marginally stable. If we were to use this circuit as is, we wouldn't see sustained oscillation anymore, but there would still be excessive overshoot and ringing before the output settles to its steady state value and this may not happen quickly enough to drive our converter to the resolution we want.

Another perspective: Zout and load impedance



TEXAS INSTRUMENTS

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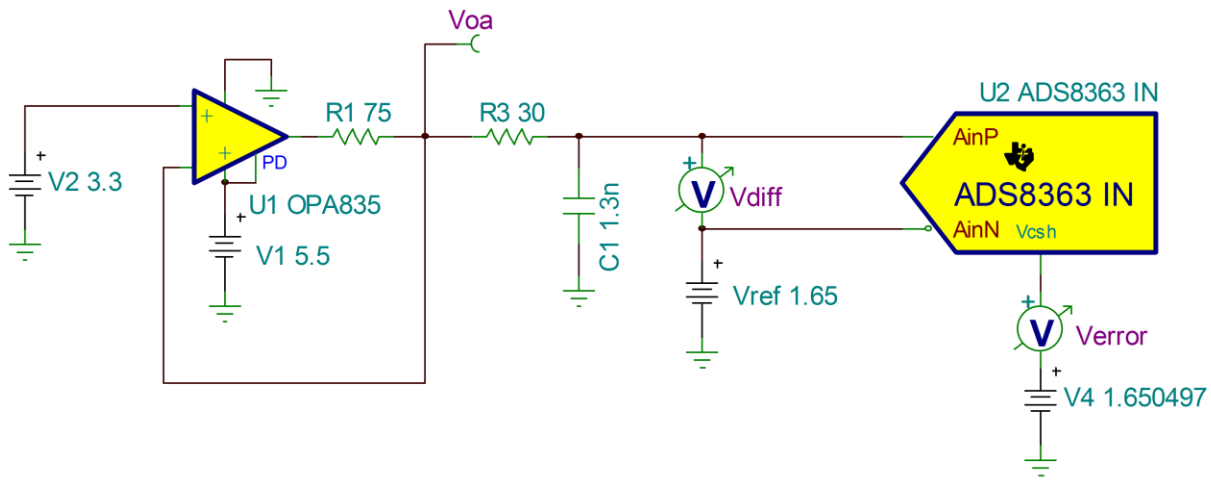
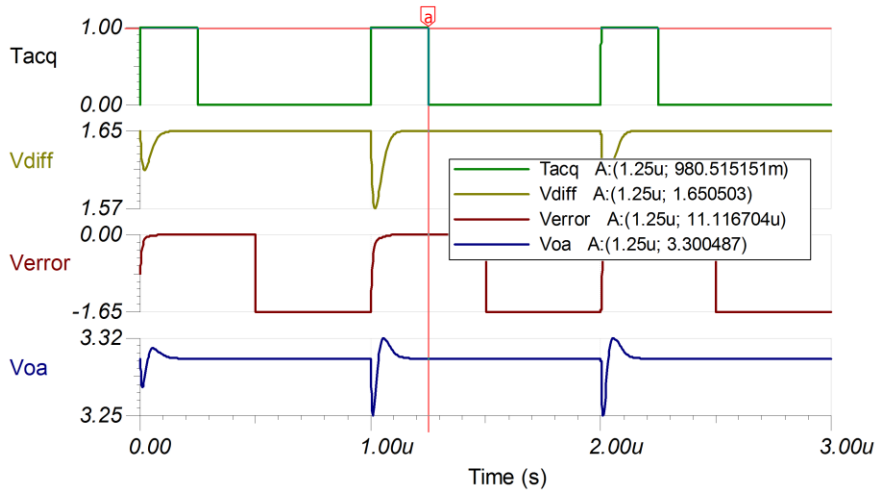
Up until now we have been looking at the interaction between the open loop output impedance, Zo, and the load to get some additional insight into our stability issues. But the interaction between the closed loop output impedance, Zout, and the load can also tell us useful information. Remember that Zo and Zout are related to each other through Aol and β. For a buffer, β = 1, so Zout is inversely proportional to Aol. If we see a resonance between Zout and the load then it implies that Aol is being modified in a way that is going to result in a bad rate of closure. So this is really just another way of looking at the same thing that our Aol and 1/β curves are telling us. In fact, the resonance predicted here at approximately 8MHz is exactly the frequency where 1/β and Aol intersect with a 40dB rate of closure in the previous slide. Having these different perspectives can make it easier to find a way to compensate the device because we have more curves that we can try to manipulate!

Final solution



For the final solution it turns out that we can't use the exact values we'd like to from the calculator, so we have to increase them a little to balance the stability of the amplifier with the settling performance into the converter. In the final solution we increase the RC values to 30 Ohms and 1.3nF.

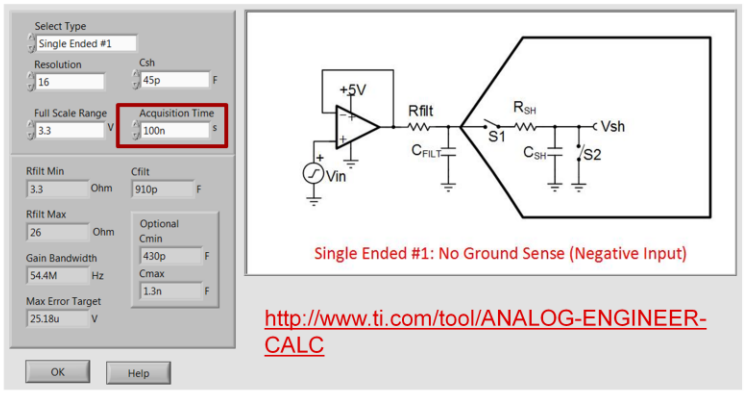
Final solution

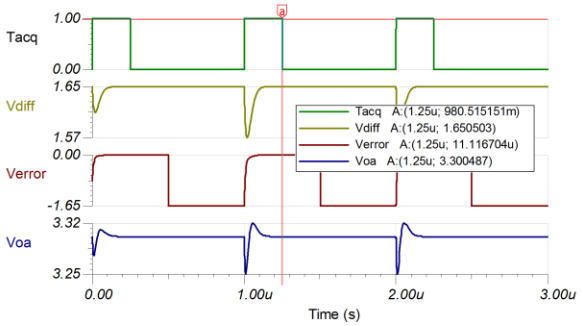


Target error: 25.81uV
Actual error: 11.11uV

Once we do this, we can see that our op amp no longer oscillates and is able to settle to within a ½ least significant bit (LSB) by the end of our acquisition cycle. Now you might be asking yourself what's the tradeoff, because as every good engineer knows you seldom get something for nothing.

What is the tradeoff?





Acquisition time = 250ns

- Load transient response time depends on Zout, which depends on Zo, Aol, and 1/β
- Compensation usually sacrifices loop gain, which effectively increases Zout!

$$Z_{OUT} = Z_O / (1+AolB)$$

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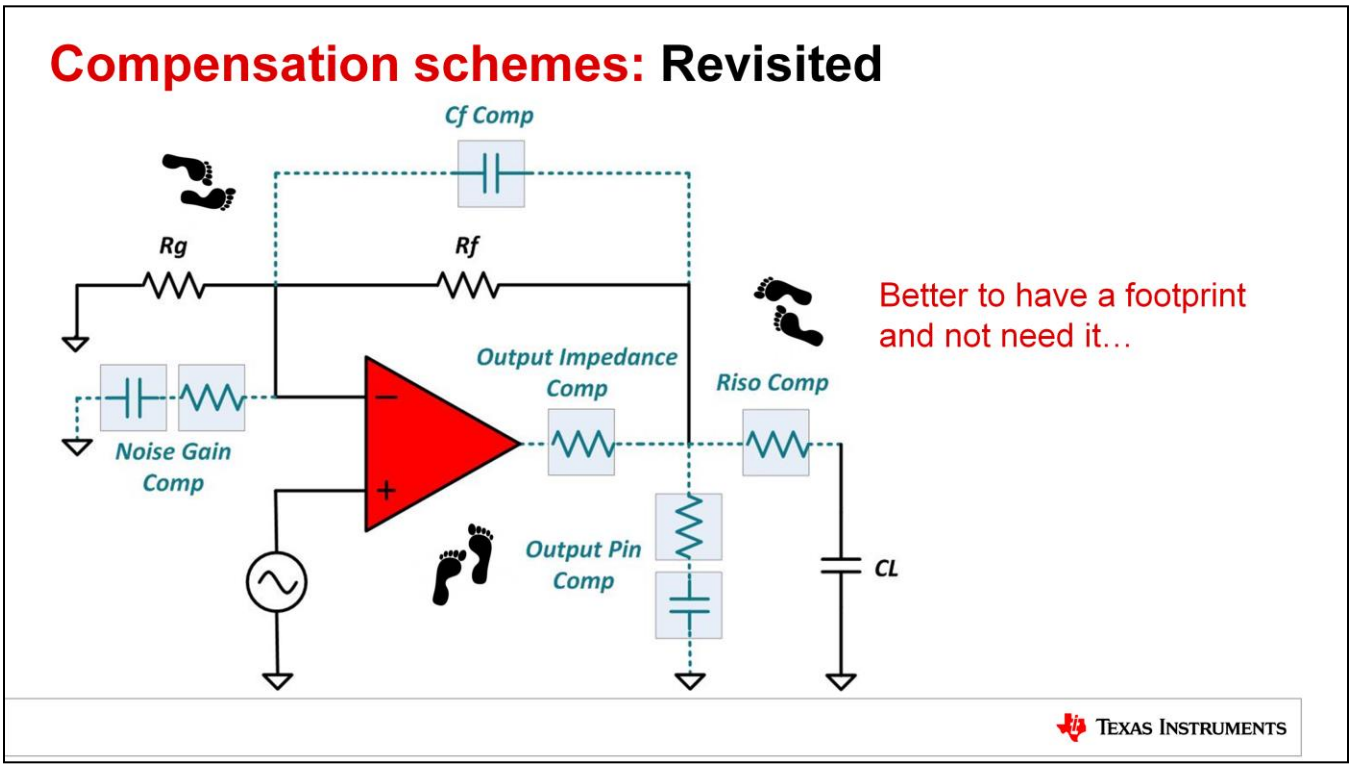
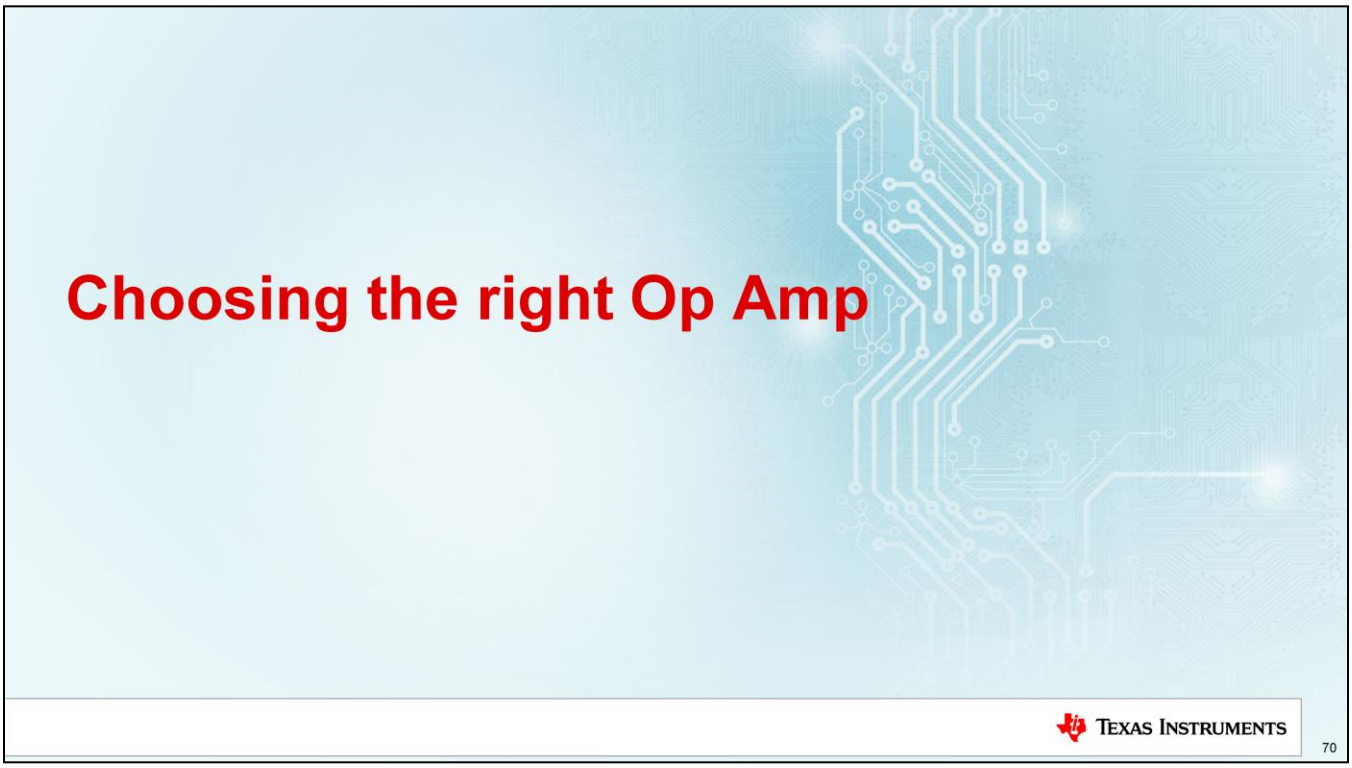
It turns out if we want to achieve the error performance we are after, we have to sacrifice the 100ns acquisition time and extend it to 250ns to give the amplifier enough time to respond. Alternatively, we could have used an amplifier that had the necessary bandwidth without a reactive output impedance.

The need to increase the acquisition time can also be understood through the output impedance. You can think of the output of the amplifier forming an RC time constant with the RC filter and the sample and hold capacitance of the converter. You need to dump a certain amount of charge on the sample and hold capacitor before the end of the acquisition cycle, but how quickly you can do that is limited by the effective RC time constant. If the output impedance of the amplifier increases, then it takes longer for it to recharge the RC filter and push charge into the converter, and you can't settle as quickly. Most compensation schemes end up sacrificing loop gain (AolB), and this directly translates to an increase in output impedance.



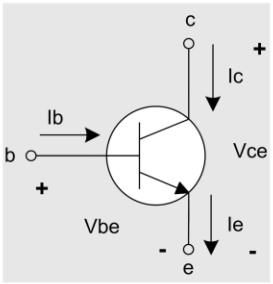
In this design we were able to fix the issue by adding a component to our schematic and adjusting a few things. This can be much more difficult to address however if the customer already has their layout locked in and doesn't want to add anything. In that case, our only choice would have been to use a different amplifier, and sometimes that is undesirable. The takeway here is having footprints around these devices will make things easier even if they don't end up being necessary. Having these in the prototype phase can allow you to determine if it is necessary to add anything and then you can go back and adjust things without major layout revisions.

Next we will talk about some of the things to consider to choose the right op amp for the application.



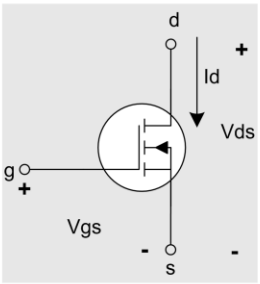
There are many op amps in TI's portfolio, and the list grows larger every year. This breadth allows us to offer something for most of the sockets in the market, but it can also make it really difficult to identify the best part for the socket. Understanding some of the general technology tradeoffs and the conventions behind the part names can make it a lot easier to narrow down the search.

Bipolar, CMOS, JFET: Op Amp input device structures



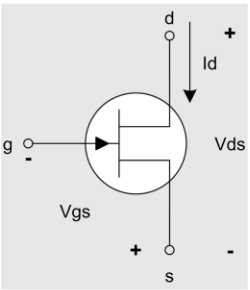
NPN **Bipolar**

1) Current Controlled Device
2) "Current Controlled Current Source"
3) Ic = Ib *hfe
4) Ib = 0A turns bipolar off
5) Base is op amp +/- input
6) Highest Op Amp input current



N-Channel **CMOS**

1) Voltage Controlled Device
2) "Voltage Controlled Resistor"
3) Vgs > 2V controls Rds_on
4) Vgs=0V turns MOSFET off
5) Gate is op amp +/- input
6) Very Low Op Amp input current



N-Channel **JFET**

1) Voltage Controlled Device
2) "Voltage Controlled Resistor"
3) 0V< Vgs < -2V controls Rds_on
4) Vgs < -2V turns JFET off
5) Gate is op amp +/- input
6) Very Low Op Amp input current

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When the term bipolar, CMOS, or JFET op amp is used it is referring to the type of transistors used in the input differential pair (+/-input) of the op amp. An NPN bipolar transistor is shown as a current controlled device. Both the CMOS and JFET devices are N-Channel and are voltage controlled devices.

The NPN Bipolar Transistor is a current controlled device. The collector current is equal to the base current times a current high gain factor called hfe. The emitter current is the summation of the collector current and the base drive current. Since hfe is usually high, Ib is small when compared to Ic. Therefore, Ie is about equal to Ic. A bipolar op amp will have transistor bases connected to its inputs and therefore require some drive current into these inputs.

The N-Channel CMOS device is a voltage controlled device. It can be viewed as a voltage controlled resistor in its linear region of operation such that the drain to source resistance or Rds_on is controlled by the gate to source voltage or Vgs. For a typical N-Channel device Vgs=0V turns it off and Vgs > 2V will begin to turn it on. A CMOS op amp will have transistor gates connected to its inputs and therefore require next to no input drive current since it is a voltage controlled device.

The N-Channel JFET device is a voltage controlled device. Similar to a MOSFET, it can be viewed as a voltage controlled resistor in its linear region of operation. For a typical N-Channel device Vgs=0V turns it on and Vgs < -2V will begin to turn it off.

Summary CMOS vs. Bipolar vs. JFET

Parameter	CMOS	Bipolar	JFET
Vos	☒ Generally Larger than bipolar. Complex trim. Inherent ≈ 5mV, Trimmed ≈ 500uV ☑ Can use zero drift, and package trim.	☑ Generally smaller than JFET and CMOS. Laser Trim Only. Inherent ≈ 200uV, Trimmed ≈ 20uV	☒ Generally Larger than bipolar. Complex trim. Laser Trim Only. Inherent ≈ 1mV, Trimmed ≈ 100uV
Vos Drift	☒ Generally Larger than bipolar. Complex trim. ☑ Very good if using chopper.	☑ Inherently linear and easer to trim. Laser Trim Only.	☒ Generally Larger than bipolar. Complex trim. Laser Trim Only.
Ib	☑ Low compared with bipolar Ib ≈ 1pA @ 25C	☒ Much larger than CMOS and JFET. Can use bias current calculation. Inherent ≈ 100nA, Canceled ≈ 1nA	☑ Low compared with bipolar Ib ≈ 1pA @ 25C
Ib Drift	☒ Doubles every 10C, diode leakage I_{B_room} ≈ 1pA , T = 25C I_{B_hot} ≈ 1000pA , T = 125C	☑ Small compared to room temp I_{B_room} ≈ 1nA , T = 25C I_{B_hot} ≈ 3nA , T = 125C	☒ Doubles every 10C, diode leakage I_{B_room} ≈ 1pA , T = 25C I_{B_hot} ≈ 1000pA , T = 125C
Ibos	☒ Large offset current that is comparable to Ib. Don't use resistor to cancel effects. Ib ≈ ±1pA, Ibos = ±1pA	☑ When bias current cancellation is not used Ibos is low relative to Ib. Resistor can help cancel effects. Ib = 100nA, Ibos = ±1nA ☑ When bias current cancellation is used Ibos is comparable to Ib. Don't use resistor to cancel effects. Ib = ±1nA, Ibos = ±1nA	☒ Large offset current that is comparable to Ib. Don't use resistor to cancel effects. Ib ≈ ±1pA, Ibos = ±1pA

The following two slides summarize the key trade-offs in specifications when considering CMOS, Bipolar, and JFET op amp topologies. These slides can serve as a useful reference when trying to determine what kind of device you need. Generally speaking, a bipolar device is going to have inherently better offset and drift performance and can be trimmed to a very high degree of accuracy. However, Zero-drift CMOS devices boast the greatest offset performance. For bias currents, bipolar devices tend to be the worst performing and are not typically suited for things like transimpedance amplifiers.

Vos:	CMOS, largest Vos, complex trim, unless Chopper or Auto-zero.
	Bipolar, smallest Vos, laser trim only, simple trim
	JFET, larger than Bipolar, laser trim only, complex trim
Vos Drift:	CMOS, largest drift, complex trim, unless Chopper or Auto-zero.
	Bipolar, linear drift, laser trim only, simple trim
	JFET, larger drift than Bipolar, laser trim only, complex trim
Ib:	CMOS, lowest Ib (pA)
	Bipolar, high Ib, can be minimized with Ib cancellation (nA)
	JFET, Lowest Ib (pA)
Ib Drift:	CMOS, doubles every 10C, ESD diode leakage dominant (pA to nA)
	Bipolar, small change over temperature (nA)
	JFET, doubles every 10C, ESD diode leakage dominant (pA to nA)
Ios:	CMOS, Ios comparable to Ib (but pA)
	Bipolar, high Ib, can be minimized with Ib cancellation (nA)
	JFET, lowest Ib, Ios comparable to Ib (but pA)

Summary CMOS vs. Bipolar vs. JFET

Parameter	CMOS (3xx)	Bipolar	JFET
Broadband Noise	☒ Generally Larger than bipolar. Noise decreases to the square root of Id.	☑ Generally smaller than JFET and CMOS. Noise decreases directly with Id.	☒ Slightly higher than Bipolar
1/f Noise	☒ Generally worse than bipolar. Noise Corner > 1kHz	☑ Generally better than CMOS. Noise Corner < 10Hz	☑ Generally better than CMOS, but not as good as bipolar. Noise Corner < 100Hz
Back-to-Back Diodes	☑ May or may not be required. Check Data Sheet!	☒ Generally required	☑ Not required. Check Data Sheet
Integrated Digital?	☑ Yes. i.e. Chopper, package trim	☒ No	☒ No
Rail to Rail Input	☑ Yes	☒ No.	☒ Not common. Difficult
Rail to Rail Output	Very close to the rail. 10mV	Close to the rail. 200mV	Same as bipolar
Output vs. Load	☒ Falls off quickly with load. Ron of output transistor.	☑ Relatively flat until you reach current limit. Vsat not related to Ron as with CMOS.	Same as bipolar

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When it comes to noise, Bipolar tends to be the best followed by JFETs. However, if 1/f noise is a major concern, then CMOS chopper amplifiers are the best. When it comes to swing to the rails, CMOS devices can get the closest because the saturation voltage scales with the size of the transistor. If you understand what is important in the application, then these slides can help you figure out what kind of device you should use.

Next we compare the broadband noise, 1/f or low-frequency noise, presence of back-to-back input diodes, integrated digital logic, rail-to-rail input and output, and output voltage vs. load capabilities of the different topologies.

Broadband Noise: CMOS, largest noise
Bipolar, smallest noise
JFET, slightly larger than Bipolar, smaller than CMOS

1/f Noise: CMOS, largest noise, >1kHz 1/f frequency, Chopper can eliminate 1/f noise
Bipolar, lowest noise, 1/f frequency <10Hz
JFET, lower than CMOS, higher than Bipolar noise, 1/f frequency <100Hz

Back-to-back Diodes: CMOS, may or may not be needed – check datasheet
Bipolar, generally required
JFET, generally not required – check datasheet

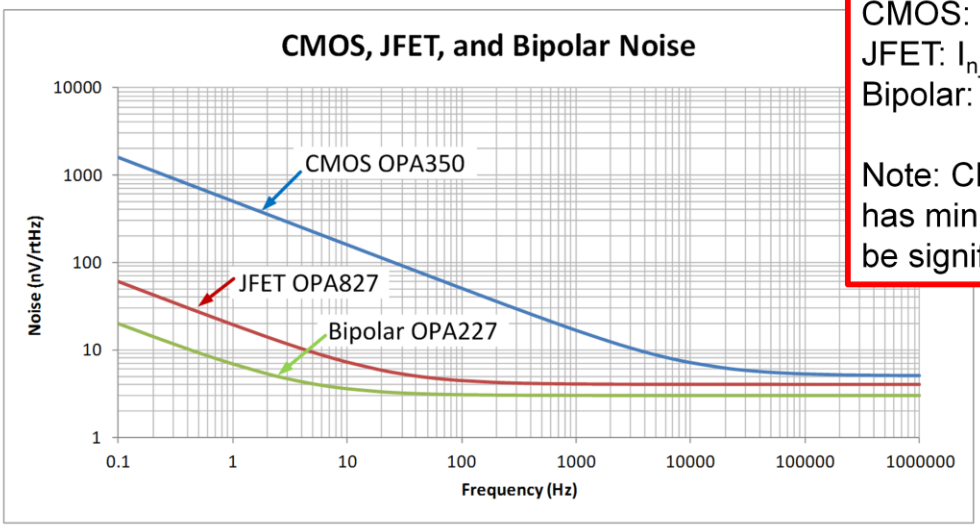
Integrated Digital: CMOS, yes for Auto-zero or Chopper or e-Trim
Bipolar, no
JFET, no

Rail to Rail Input: CMOS, yes
Bipolar, no
JFET, not common

Rail to Rail Output: CMOS, close to rail (i.e. 10mV)
Bipolar, within 200mV of rail
JFET, within 200mV of rail

Output vs. Load: CMOS, falls off quickly with load due to Rds_on
Bipolar, relatively flat until current limit
JFET, relatively flat until current limit

JFET, Bipolar, and CMOS: Noise



CMOS: I_{n_350} = 4fA/rtHz
JFET: I_{n_827} = 2.2fA/rtHz
Bipolar: I_{n_277} = 200fA/rtHz

Note: CMOS current noise has minimal 1/f, but it may be significant in bipolar

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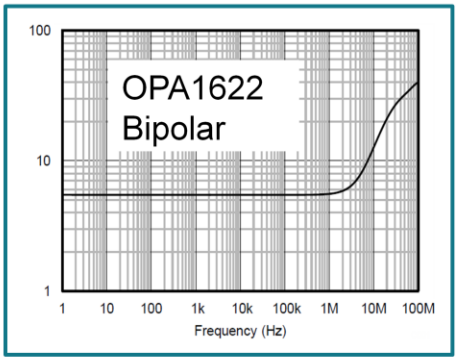
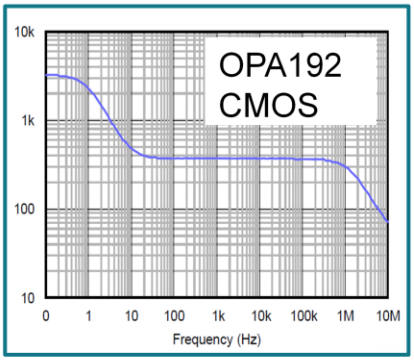
The 1/f Noise corner is often considered to be a figure of merit. The noise corner is the place at which the 1/f and broad band noise curves interest or the bend in the curve. The 1/f noise corner is typically much higher for CMOS devices. JFET and bipolar have comparable 1/f noise although bipolar is generally somewhat better. In fact, the JFET input is often selected to provide very low Ib with good 1/f noise performance. In other words with JFET, you get good Ib performance like a CMOS device, with good noise performance like a bipolar device. CMOS chopper devices while not shown in the slide, will have broadband noise comparable to standard CMOS devices, but without any 1/f noise! This is because the internal switching mechanism that allows choppers to achieve such low offset voltages also corrects for 1/f noise.

The current noise is shown in the red box. Note that current noise doesn't always have a curve as current noise for FET devices is generally considered to be flat over frequency. Also note that the current noise is substantially smaller with CMOS and JFET devices than with bipolar devices. Finally, note that the bipolar current noise may have a 1/f component that makes it much higher at low frequencies.

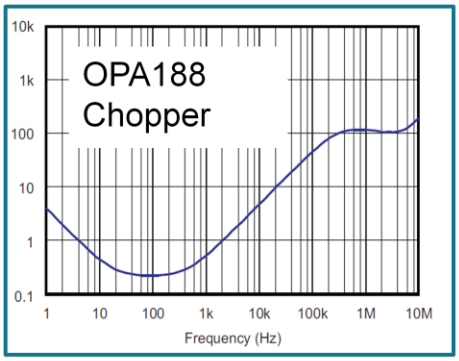
Bipolar vs. CMOS: Open loop output impedance



Bipolar is generally the flattest and lowest Zo



CMOS Zo is often higher and not as flat as Bipolar.



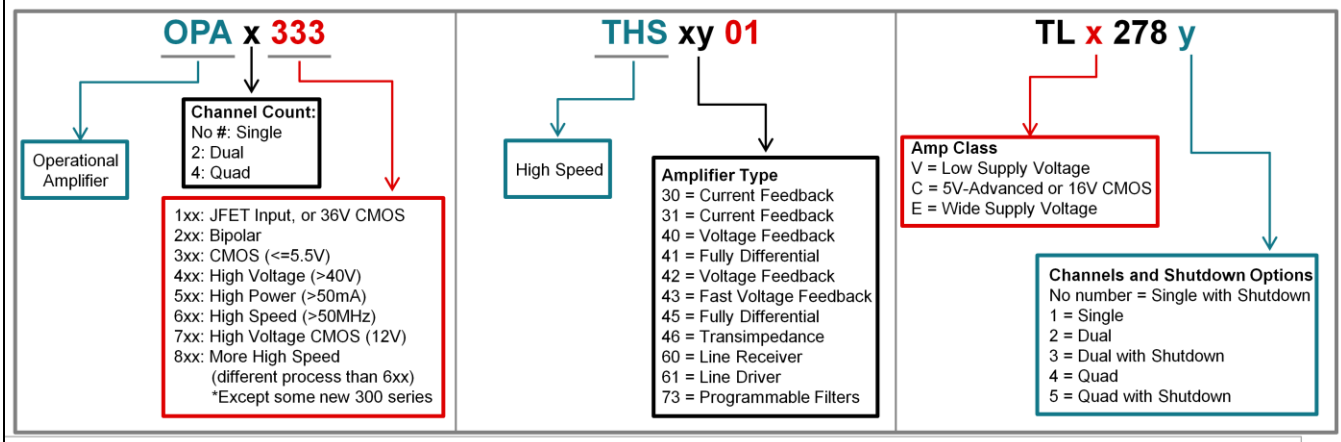
Zero Drift and µPower amplifiers often have complex Zo.

This slide compares the open loop output impedance, Zo, for a bipolar, CMOS, and chopper amplifier. Notice how we don't show a curve for JFETs, that is because it generally isn't practical to have a JFET output stage because of the current sourcing limitations inherent to JFET structures. As we have seen, having low and flat open loop output impedance makes stabilizing amplifiers considerably easier. The best amplifier type from a Zo perspective is the bipolar amplifier. Of course, different internal topologies and design tradeoffs will affect the Zo curves as well. CMOS amplifiers tend to have higher output impedance that is generally not as flat as bipolar. Zero drift amplifiers and microPower amplifiers can have very complex output impedance curves, and consequently these devices tend to be more challenging to stabilize.

Amplifier naming conventions: TI trends

PREFIX:

- OPA: Linear Operational or Audio Amplifier
- INA: Instrumentation or Difference Amplifier
- LOG: Logarithmic Amplifier
- XTR: Current Loop Driver
- PGA: Programmable Gain Amplifier (digital)
- VCA: Voltage-Controlled Variable Gain Amplifier
- IVC: Current-to-Voltage Converter
- TLV: Low-Voltage CMOS-Input
- TLC: CMOS-Input
- TL: Bipolar- or BiFET-Input
- THS: Bipolar-Input, High Speed
- TPA: Audio Power Amps
- LM, LMV: Commodity Second Sources
- NE, MC: Commodity Second Sources



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With so many parts in our portfolio, you might be relieved to know that there is actually a convention behind the naming of our amplifiers. This convention helps to easily differentiate between the different op amp types and technologies. While there are certainly exceptions to the rules, such as hybrid devices, these guidelines are applicable to the majority of amplifiers in the portfolio and should serve as a useful guide to quickly narrow down your search.

With everything we have talked about we have only just scratched the surface of problems that you can run into in op amp circuits. The topic of output impedance was made the focus because this is one of the most critical and most often overlooked parameters that contribute to the overall stability and performance of a design. The goal here is not to convince you to stay away from these amplifiers. Many of these amplifiers offer amazing performance in many areas, but it is important to be aware of their characteristics to understand the additional design considerations that come along with using them.

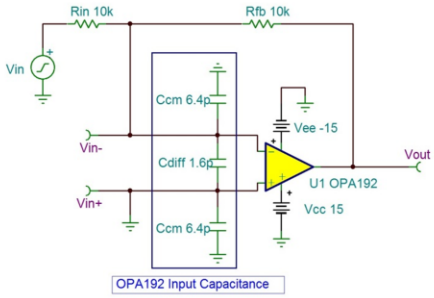
In the next section, we'll take a quick look at a few other common issues that customers may encounter.

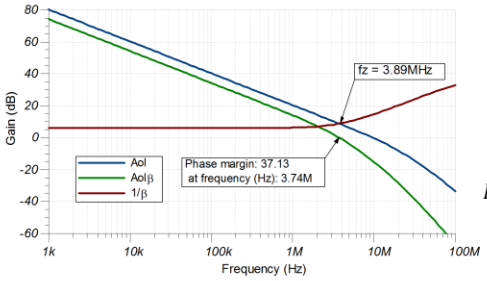
Common application issues

Since there are many other common pitfalls that one can encounter when designing with op amps, let's take a quick look at a few more!

Input capacitance and the rule of 10: OPA192

INPUT IMPEDANCE				
Z_{ID}	Differential		100 || 1.6	MΩ || pF
Z_{IC}	Common-mode		1 || 6.4	10^{13}Ω || pF





$$Cin(eq) = Ccm + Cdiff = 8pF$$

$$Req = \frac{Rfb \times Rin}{Rfb + Rin} = 5k\Omega$$

$$Fz = \frac{1}{2\pi \times Cin(eq) \times Req} = 3.98MHz$$

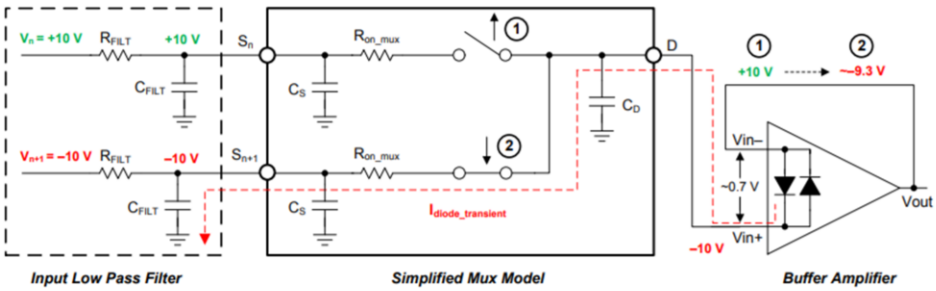
Problem: 10MHz amplifier + 10kΩ resistors results in instability from input capacitance

Solution: Place a capacitor in parallel with Rfb.

Choose Cfb ≥ Cin(eq)

As a general rule of thumb, you should be weary if you see a 10MHz amplifier with 10kOhm resistors around it and no compensation capacitors. This is because the resistors will interact with the input capacitance and the gain will start to increase over frequency. If this happens before the Aol crossing, then you will have a rate of closure greater than 20dB and the circuit will be marginally stable at best. This can happen for other combinations as well, it ultimately depends on how much bandwidth and input capacitance the amplifier has, and how large your resistors are. The easiest solution is to place a capacitor in parallel with the feedback resistor that is at least as large as your equivalent input capacitance.

Anti-parallel input diodes: Bipolar, Chopper, HV CMOS

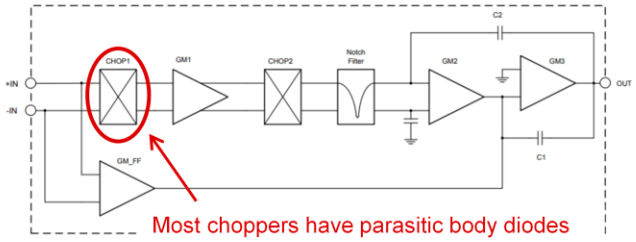


Avoid input diodes in these applications:

- Comparators
- Multiplexed inputs
- Square wave input circuits that require fast settling

Use MUX friendly input devices!

http://www.ti.com/lit/an/sbot040/sbot040.pdf



Most choppers have parasitic body diodes from MOSFET switches (OPA189 and OPA388 are exceptions)

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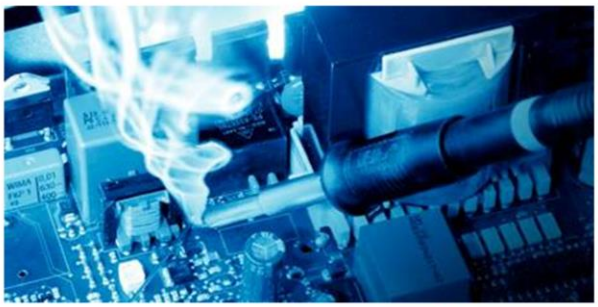
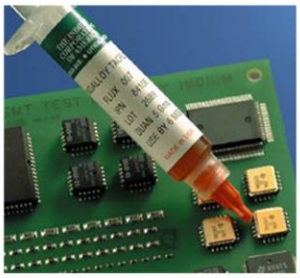
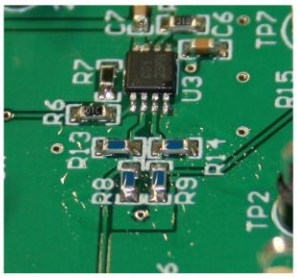
Another common issue is trying to use an amplifier with back to back diodes on the input in applications that attempt to pull the inputs apart. This can occur if you are using a MUX to switch different signals in, or if you are attempting to use the amplifier as a comparator. The back to back diodes limit the differential voltage which limits the slew rate and slows down the response time. Depending on the circuit, it may also result in excess current flowing between the inputs that could potentially damage the device. All bipolar amplifiers have these input diodes to protect the bases of the input transistors, as they can not tolerate an excessive base-emitter drop. Most zero-drift chopper amplifiers also have these diodes as a result of the parasitic body diodes that are present on the internal MOSFET switches, the OPA189 and OPA388 however are expections. Many high voltage CMOS devices will also utilize these diodes to ensure the breakdown voltage of the input MOSFETs is not exceeded during large transients. If your application requires you to pull the inputs apart, then you should be sure to use a MUX friendly input device such as the OPA189 or OPA191.

Flux contamination

- Improper cleaning of solder flux can cause **huge** DC voltage errors!
  - These errors are random in nature and are nearly impossible to predict
- Use an Ultrasonic bath (or similar) for final cleaning of all hand-assembled or reworked PCBs
  - PCBs assembled by a contracted assembly house should already use suitable post-assembly cleaning methods
- Bake assembled and cleaned PCBs at slightly elevated temperature to remove any residual moisture
  - e.g. 70°C, 10 minutes
- Place guard rings around critical signal traces to reduce PCB surface leakage currents
  - See "Op Amp Precision Design: PCB Layout Techniques" for more information







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One surprisingly common issue that arises in customer applications actually has nothing to do with the design, but the assembly and layout! Flux residue can cause all sorts of issues if boards are not properly cleaned, and often times even flux labeled "no clean" can result in parasitic paths on the PCB that cause current to flow in places it shouldn't! These errors will typically manifest as large dc offsets. 4-20mA XTR devices are especially susceptible to this because they operate with such low input current levels and a reference voltage is typically provided on an adjacent pin. Given that these errors occur randomly and depend on the chemical makeup as well as amount of flux present, they can be nearly impossible to predict. It is highly recommended that all PCBs undergo a suitable cleaning method after soldering. If a contract manufacturer is used for PCB assembly then they will typically have a cleaning process in place.

More to come!

FAE op amp troubleshooting guidelines

Chopper bias current/output voltage spikes and how they manifest

Instrumentation amplifiers: applications and challenges

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The precision amplifiers group is constantly working to improve and develop new collateral to make it easier for customers to complete their designs. Here is a glimpse of things to come

The remaining slides highlight additional resources not previously discussed that may be useful for customers and field engineers.

DIYAMP-EVM: ti.com/diyamp-evm

The industry's most versatile amplifier EVM!

Features

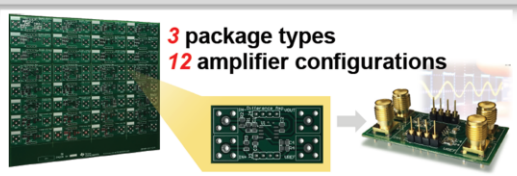
- **3 packages** to choose from (for single):
  - *SC70-5, SOT23-5, SOIC-8*
- **12 functions** to choose from, including:
  - *Noninverting, Inverting, Active Filters, Difference Amp, Comparator and more!*
- Optimized for robustness:
  - *Standardized layout is configured for optimum performance*
- Multiple interface options:
  - *SMA, Header, Bluewire, Breadboard*

Benefits

- Multiple package and function options increases speed and versatility of prototyping
- Flexible prototyping and debugging
- Efficient evaluation of multiple amplifiers or comparators under identical test conditions
- Allows for precise side by side comparisons

Applications

- Existing designs: performance enhancement
- New designs: prototyping, trouble shooting and debugging



Compatible with ADC and DAC EVMs
Includes: 32 coupon boards, Terminal strips

Click For More Information

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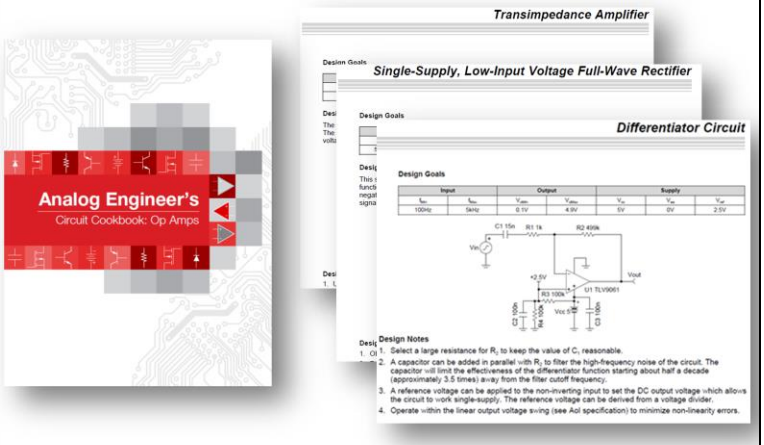
The DIY AMP EVM is a really easy way to quickly build up a high fidelity signal chain with minimal impact from parasitics. It is offered in 3 different package types and provides multiple ways to interface with the circuits to evaluate performance.

Analog Engineer's Op-Amp Cookbook

Analog Engineer's Op-Amp Cookbook:

- Includes examples of common op amp topologies
- Walks through design techniques
- Provides unique amplifier circuits, including SPICE models, for quick adaptation to any end equipment or product
- Includes >25 common op-amp circuits, from inverting amplifier to PWM generation and more
- ***Free download on ti.com***

Coming 1Q18 to TI.com!



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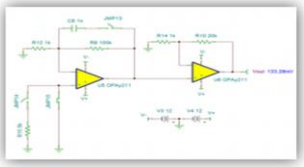
TEXAS INSTRUMENTS

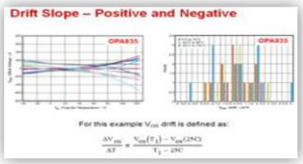
TI has recently released the op amp cookbook, which provides easy to use circuit functions with a design by example approach to design that allows you to quickly and easily realize a circuit function in your design. Stay tuned because this cookbook will be update quarterly with new circuits!

TI Precision Labs- online analog learning

www.ti.com/precisionlabs

- < 15 minute each video
- Lectures & Labs with quizzes and experiments
- For both new and experienced engineers





Op Amps

Input Offset Voltage (V_{OS}) & Input Bias Current (I_B)
TIPL 1100
TI Precision Labs – Op Amps
Presented by Ian Williams
Prepared by Art Kay and Ian Williams

Comparators

Comparator Applications 3
TIPL 2103
TI Precision Labs – Op Amps
Presented by Ian Williams
Prepared by Thomas Kuehl and Ian Williams

MUXes

Basics of Analog Multiplexers 2
TIPL 2602
TI Precision Labs – Op Amps
Created by Abhijeet Godbole, Art Kay
Presented by Peggy Liska

ADCs

DC Specifications:
input capacitance, leakage current, input impedance, reference voltage range, INL, and DNL
TIPL 4001
TI Precision Labs – ADCs
Created by Art Kay
Presented by Peggy Liska

More than 70 videos!

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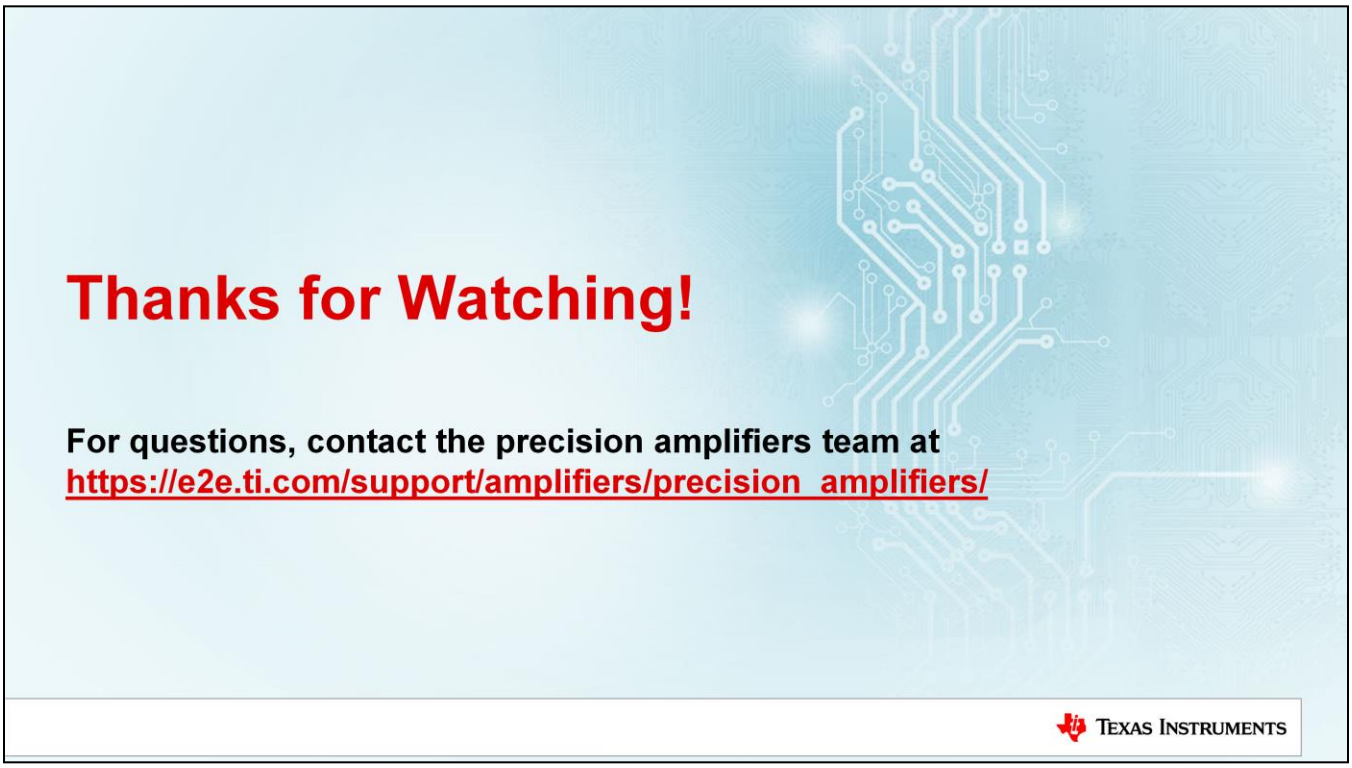
TI precision labs is an excellent resource for cultivating a deeper understanding of some of the most common devices found in an analog signal chain. There are currently more than 70 instructional videos and the list continues to grow.

Additional resources

- Tim Green and Collin Wells' stability series
  - https://e2e.ti.com/support/amplifiers/precision_amplifiers/w/design_notes/2645.solving-op-amp-stability-issues
- How to verify a macromodel against the datasheet
  - Ian Williams' "Trust but Verify" series - https://e2e.ti.com/blogs_/b/analogwire/archive/2017/07/27/trust-but-verify-spice-model-accuracy-part-1-common-mode-rejection-ratio-cmrr

Finally, if you are interested in learning more about stability and different techniques for stabilizing op amps not discussed here, check out Tim Green and Collin Wells' op amp stability series.

As mentioned previously, Ian Williams has developed a series that teaches you how to test many of the common op amp parameters to make sure your model matches the datasheet.



Thank you for watching this video, I hope you found it useful. If you have questions or ideas for what you'd like to see next, feel free to contact us at the precision amplifiers mailing list.

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