TECH DAYS
Texas Instruments

You Think LDOs are Simple?

Kyle Van Renterghem
Apps & Validation Manager
LDO Product Line

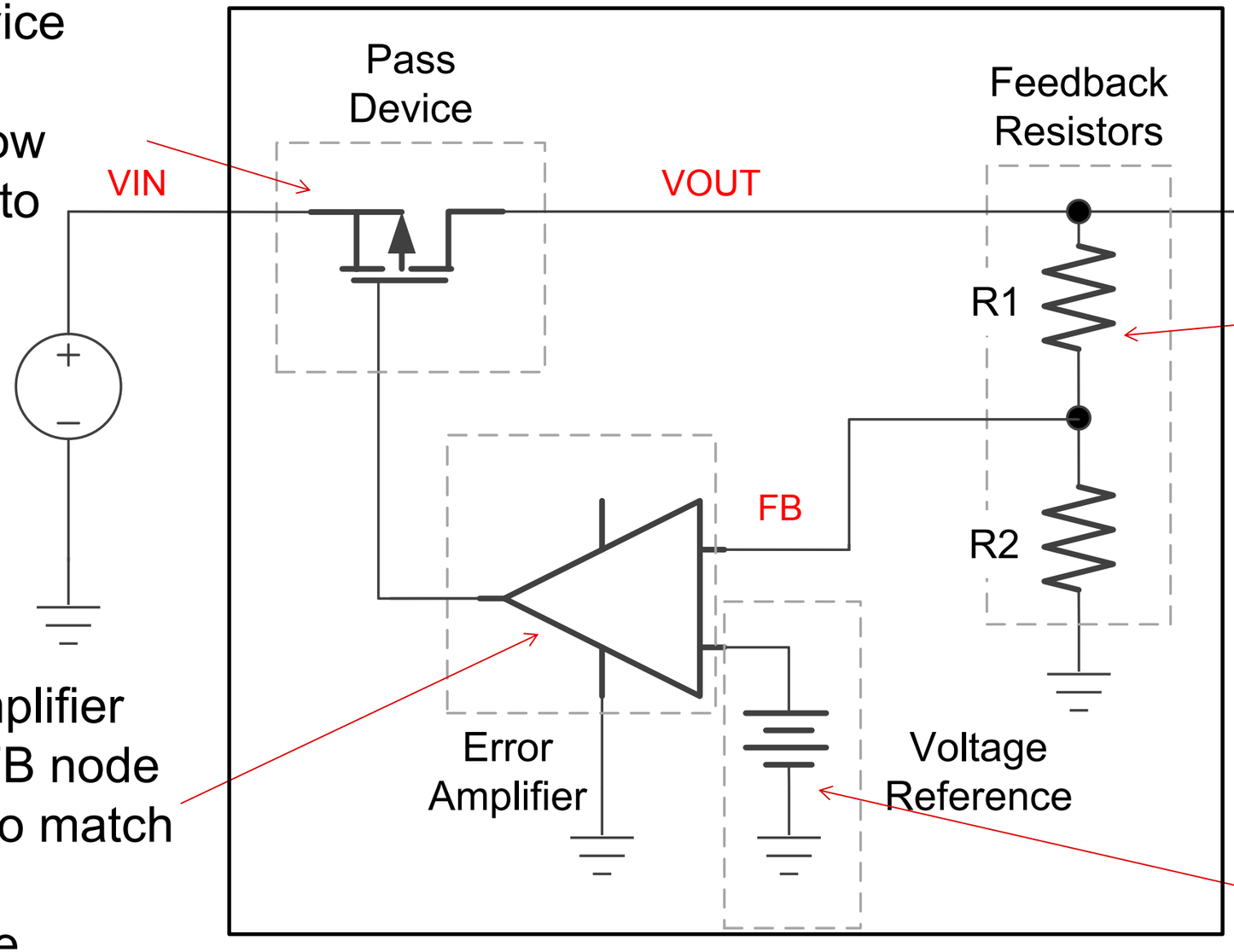
Topics

- Noise
- PSRR
- Thermal Performance
- Capacitor vs Capacitance
- Getting Answers to Your LDO Questions ASAP

Quick LDO Architecture Refresher

TECH DAYS
Texas Instruments

Pass Device controls current flow from VIN to VOUT



Feedback Resistors set Vout

Error Amplifier forces FB node voltage to match voltage reference.

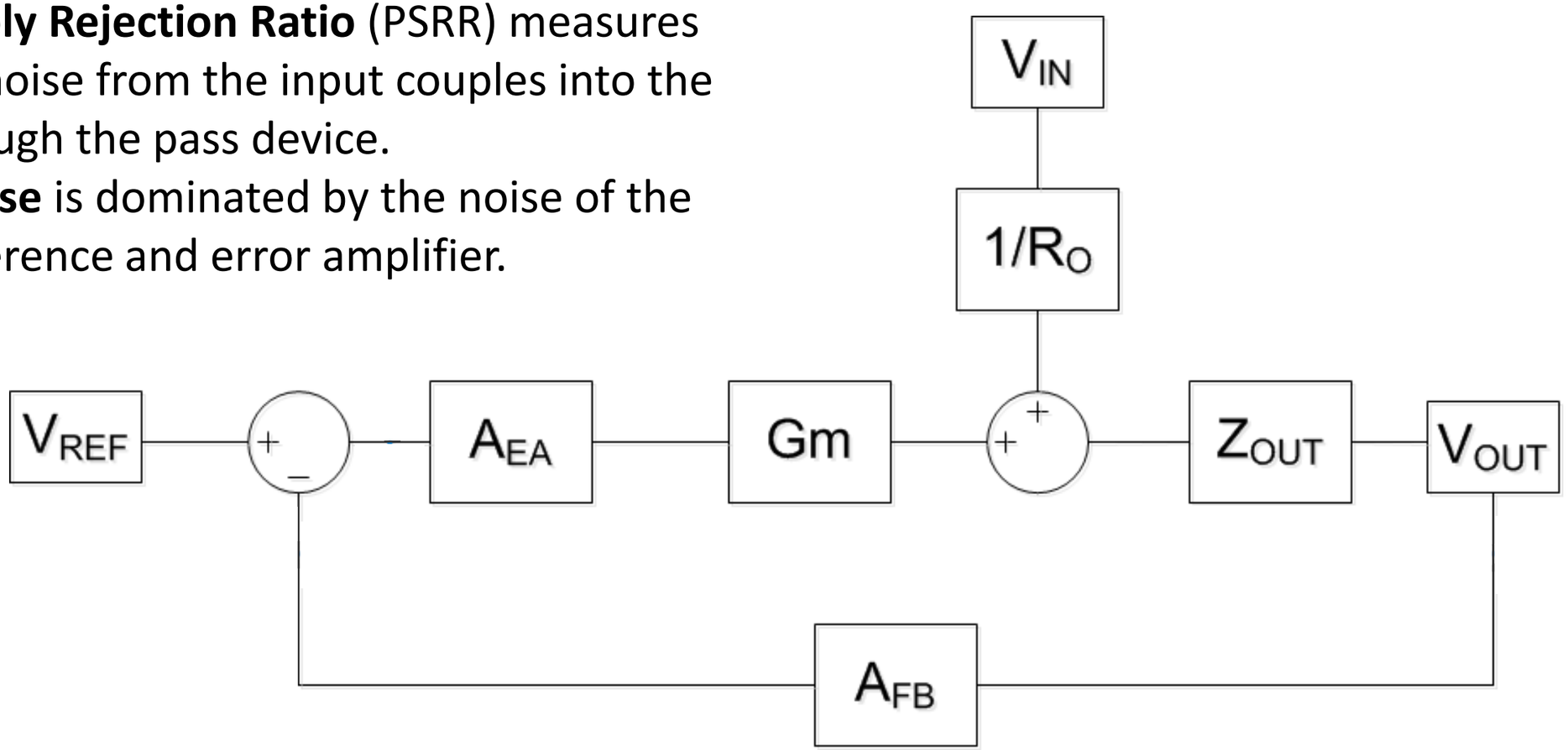
Voltage Reference provides accurate DC voltage.

Topics

- Noise
- PSRR
- Thermal Performance
- Capacitor vs Capacitance
- Getting Answers to Your LDO Questions ASAP

Where Does Noise Come From?

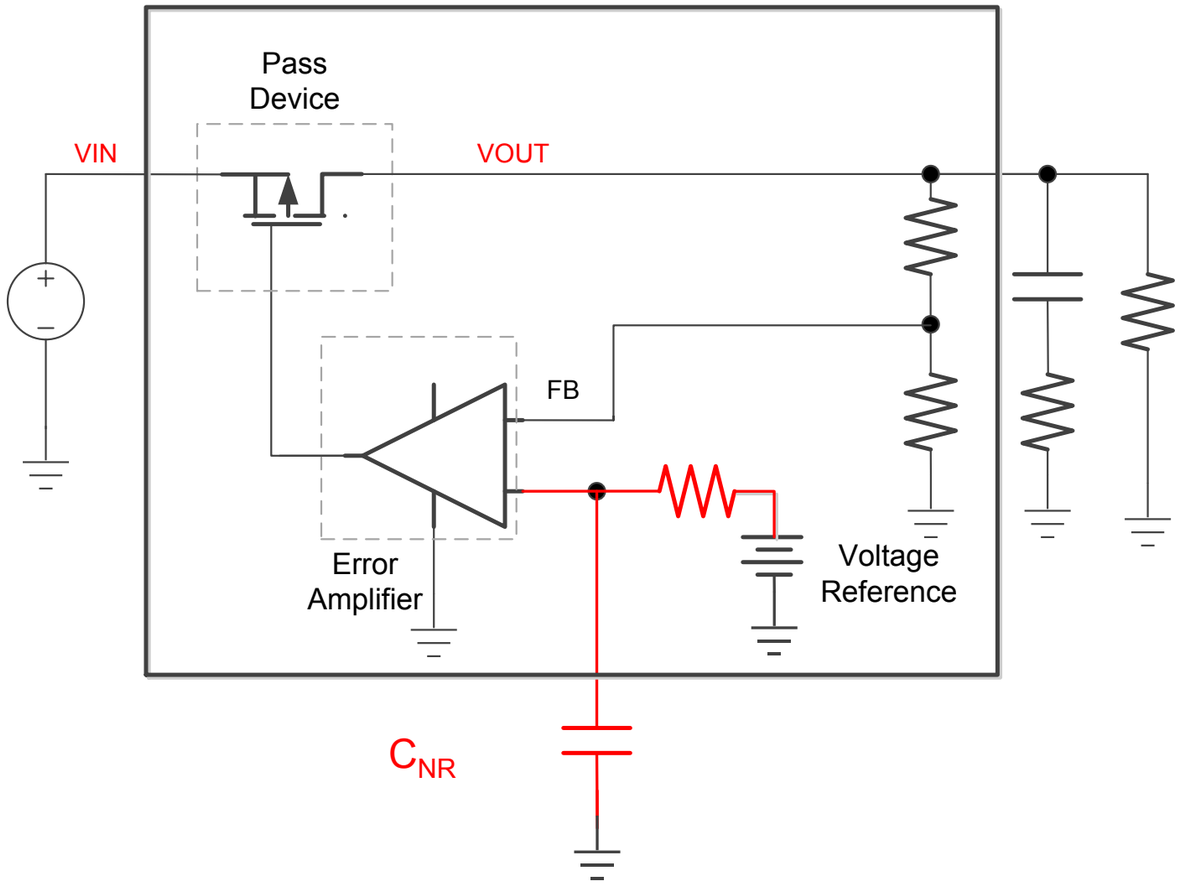
- Total LDO output voltage noise is composed of **Input noise** that is coupled to the output, as well as **intrinsic noise** generated by the LDO.
  - **Power Supply Rejection Ratio** (PSRR) measures how much noise from the input couples into the output through the pass device.
  - **Intrinsic noise** is dominated by the noise of the internal reference and error amplifier.



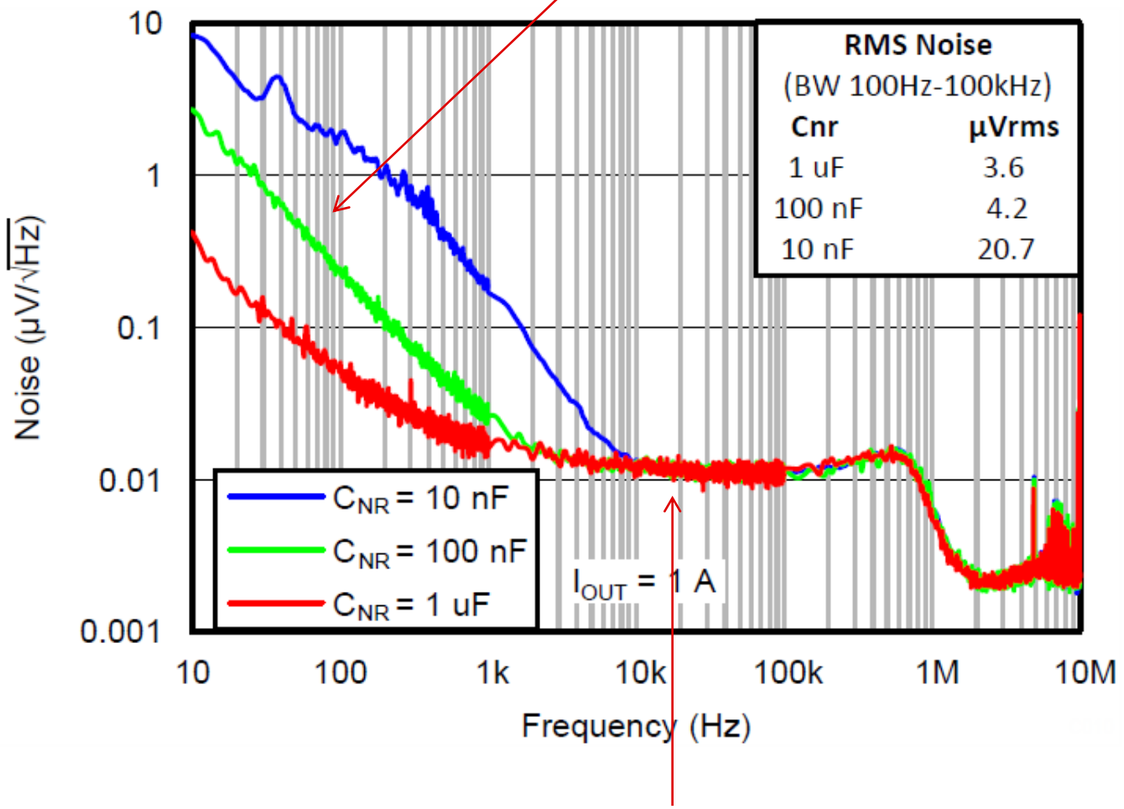
Bandgap Filter Using Noise Reduction (NR) Pin
Ex: TPS7A83A, TPS7A47

TECH DAYS
Texas Instruments

The Reference Voltage noise can be filtered with an RC filter. This can be external or internal. On external devices, add a capacitor to the NR pin.

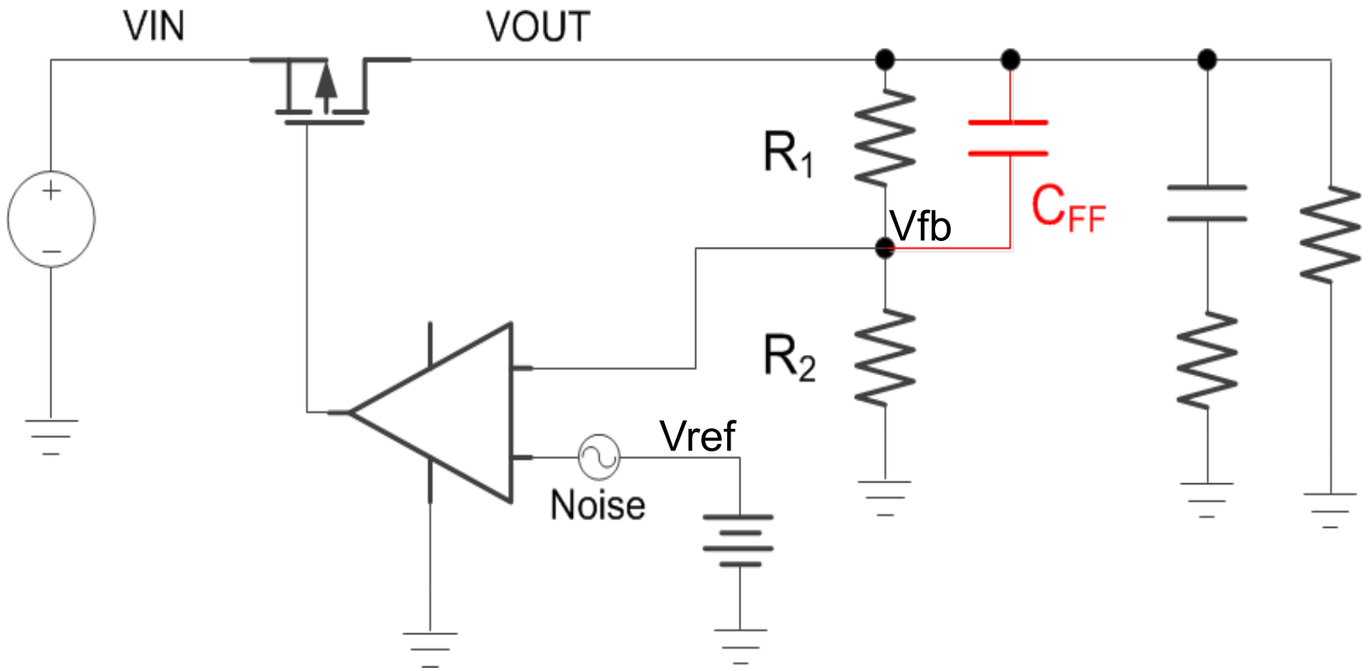


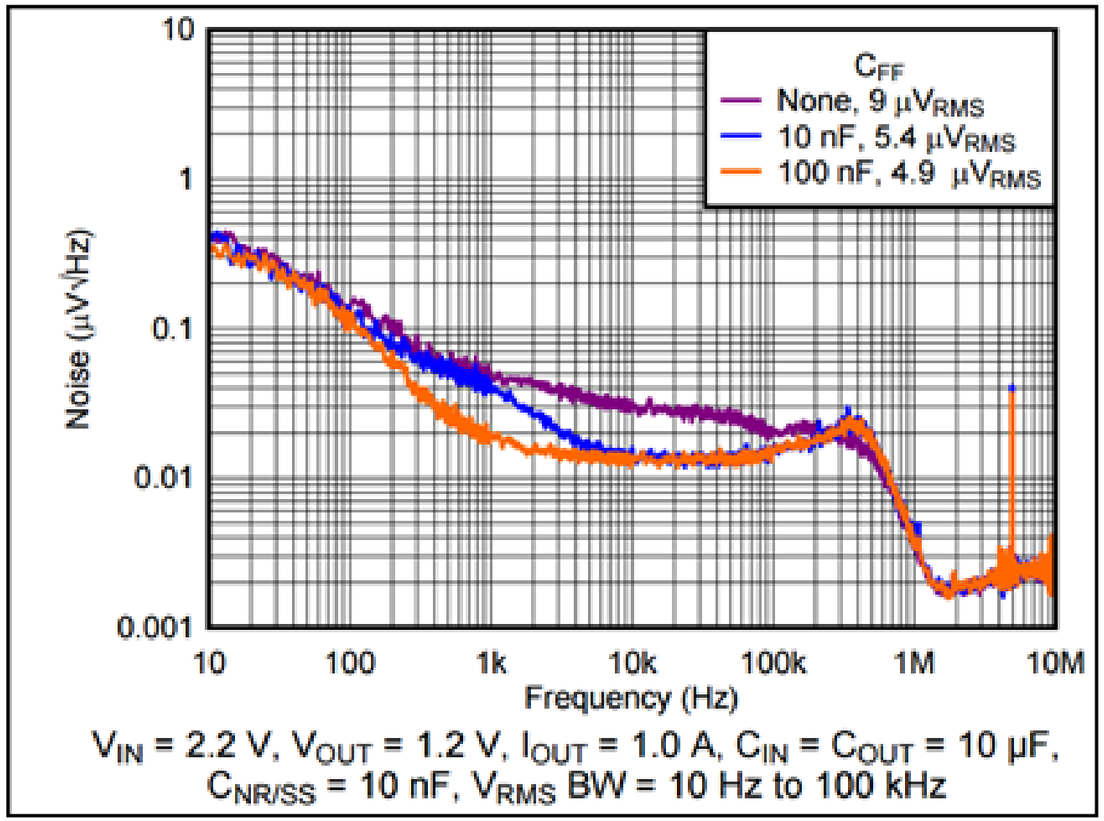
Increasing C_{NR} pushes noise lower.



However, noise in this region is limited by thermal noise from the error amplifier.

Feed Forward Cap Reduces AC-Gain





- Error amp regulates so that Vfb=Vref, so any noise on Vref will also be present on Vfb.
  - $V_{out} = V_{ref} * \frac{R_1+R_2}{R_2}$
  - Any noise on Vref is gained up!
- C_{FF} acts as a short at higher frequencies which reduces the closed-loop gain reducing the amplification at higher frequencies
- With a C_{FF}, noise should be similar to values in unity gain configuration.
- App note on the pros and cons of using a Cff http://www.ti.com/lit/an/sbva042/sbva042.pdf

What Conditions Effect Noise

TECH DAYS
Texas Instruments

Number one thing that effects noise performance is the output voltage

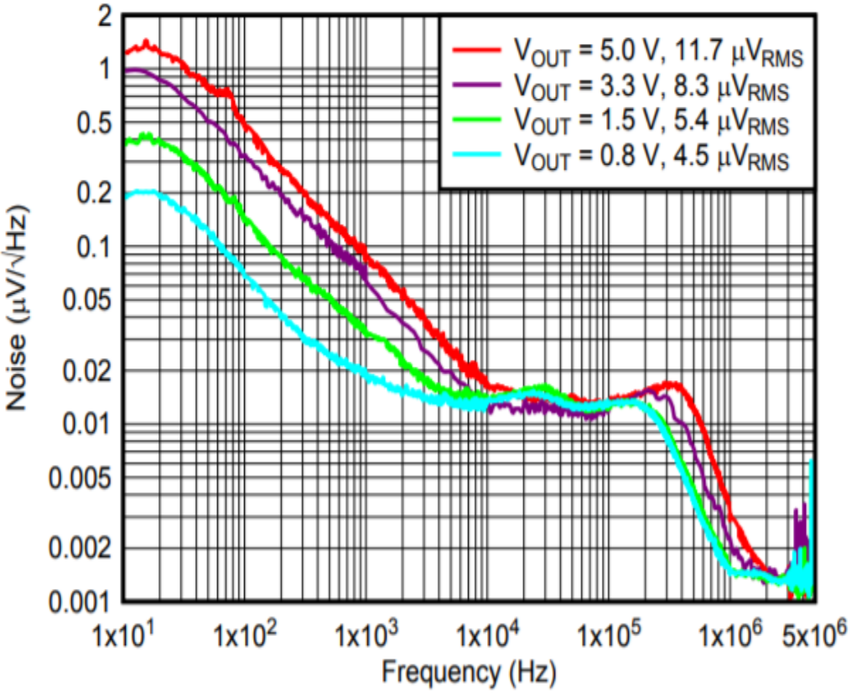


Figure 10. Output Noise vs Frequency and Output Voltage

The next thing that effects noise is the noise reduction capacitor

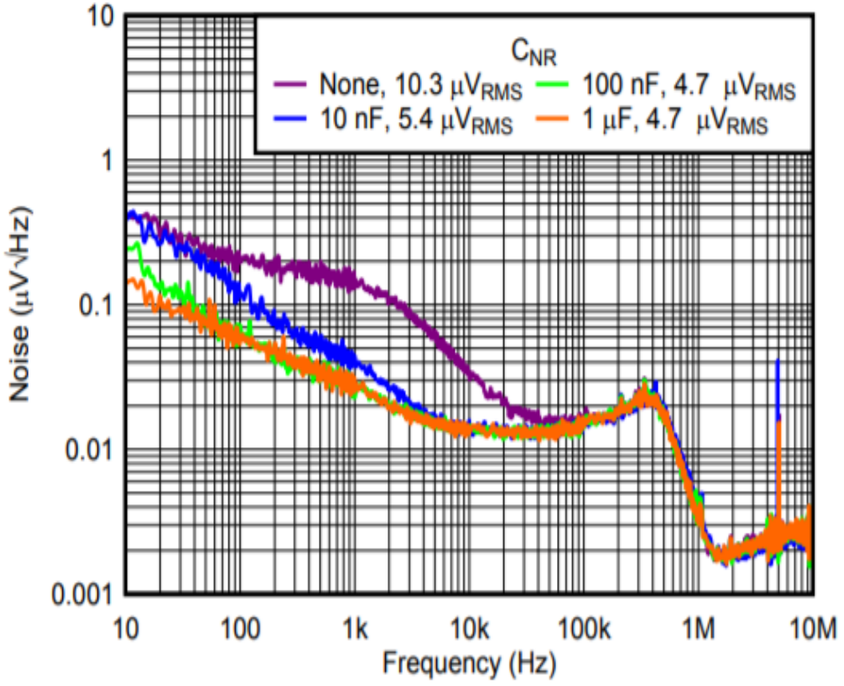


Figure 9. Spectral Noise Density vs Frequency and $C_{NR/SS}$

And the final thing that effects noise to a large degree is the feedforward capacitor

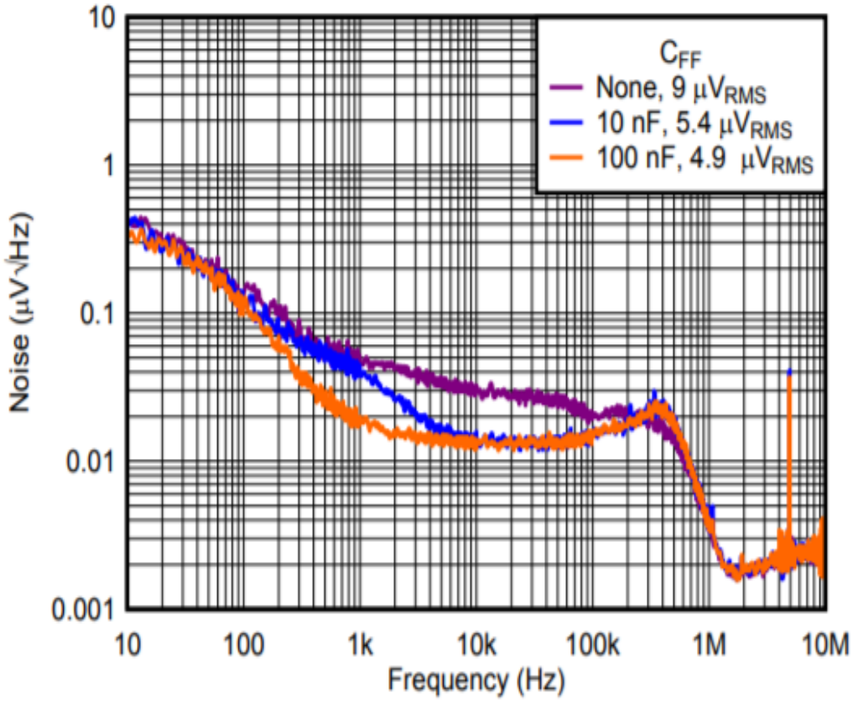


Figure 10. Spectral Noise Density vs Frequency and C_{FF}

What Conditions Do Not Effect Noise

TECH DAYS
Texas Instruments

Number one thing that has almost no effect on noise is output current

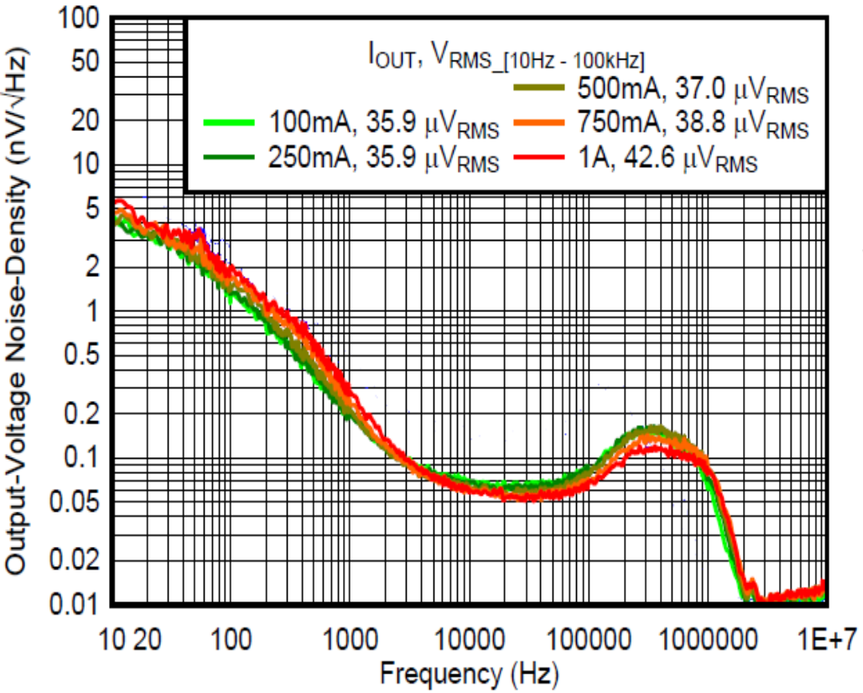


Figure 11. Noise Density vs Frequency and I_{OUT}

The next thing that has very little effect on noise is Vin

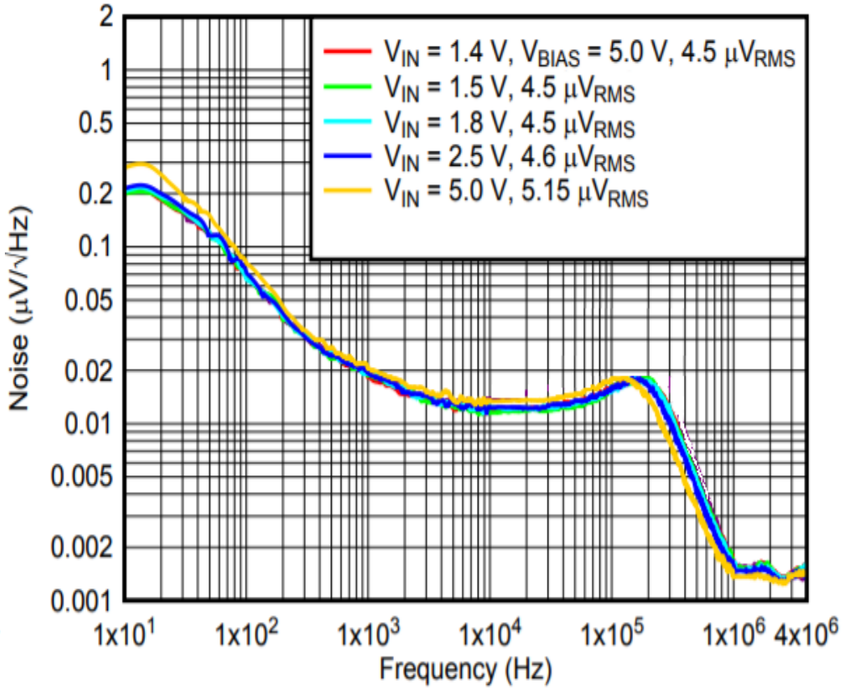


Figure 11. Output Noise vs Frequency and Input Voltage

The final thing is output capacitor
(very large Cout can show some difference)

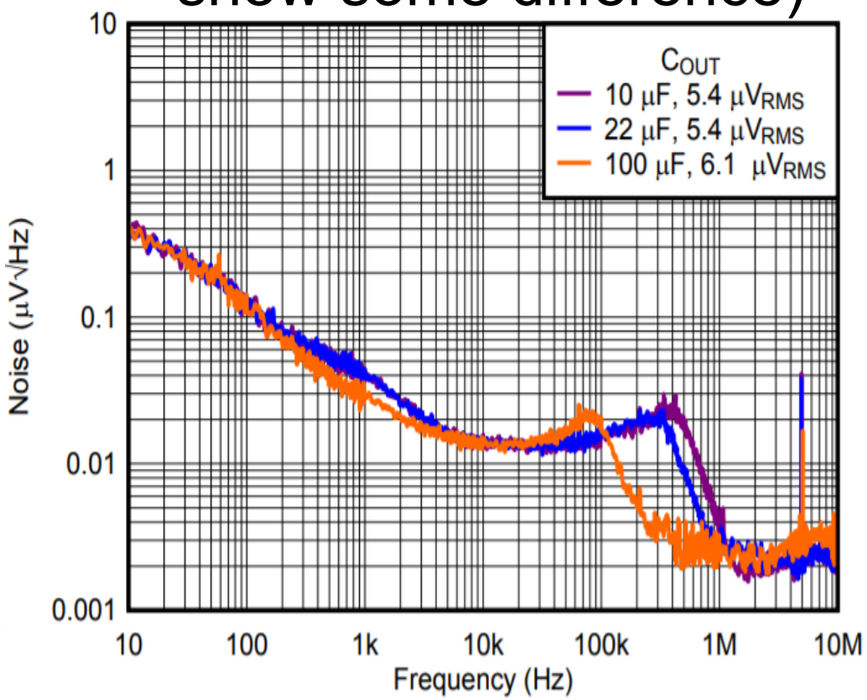


Figure 11. Spectral Noise Density vs Frequency and C_{OUT}

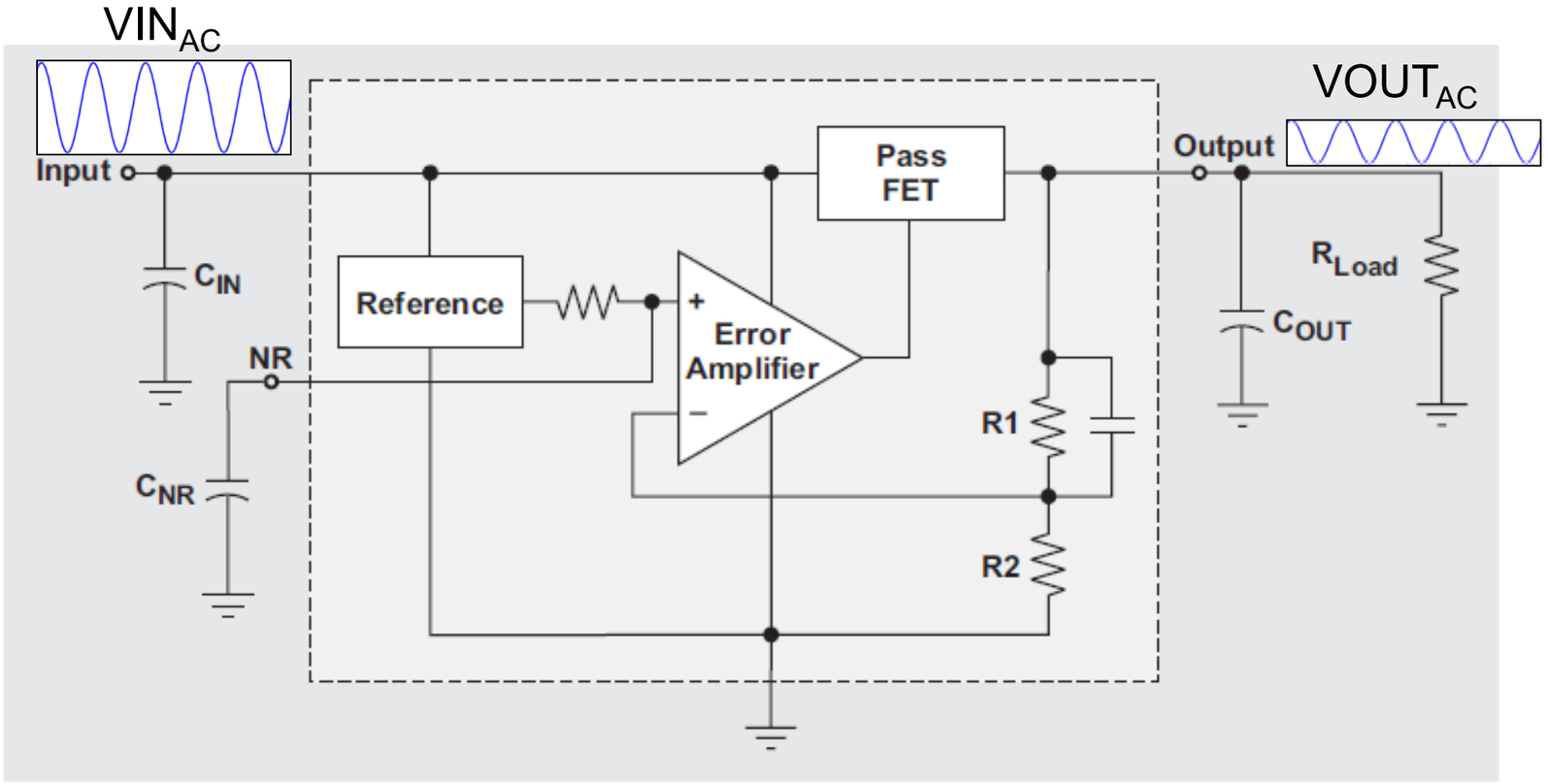
Topics

- Noise
- PSRR
- Thermal Performance
- Capacitor vs Capacitance
- Getting Answers to Your LDO Questions ASAP

PSRR

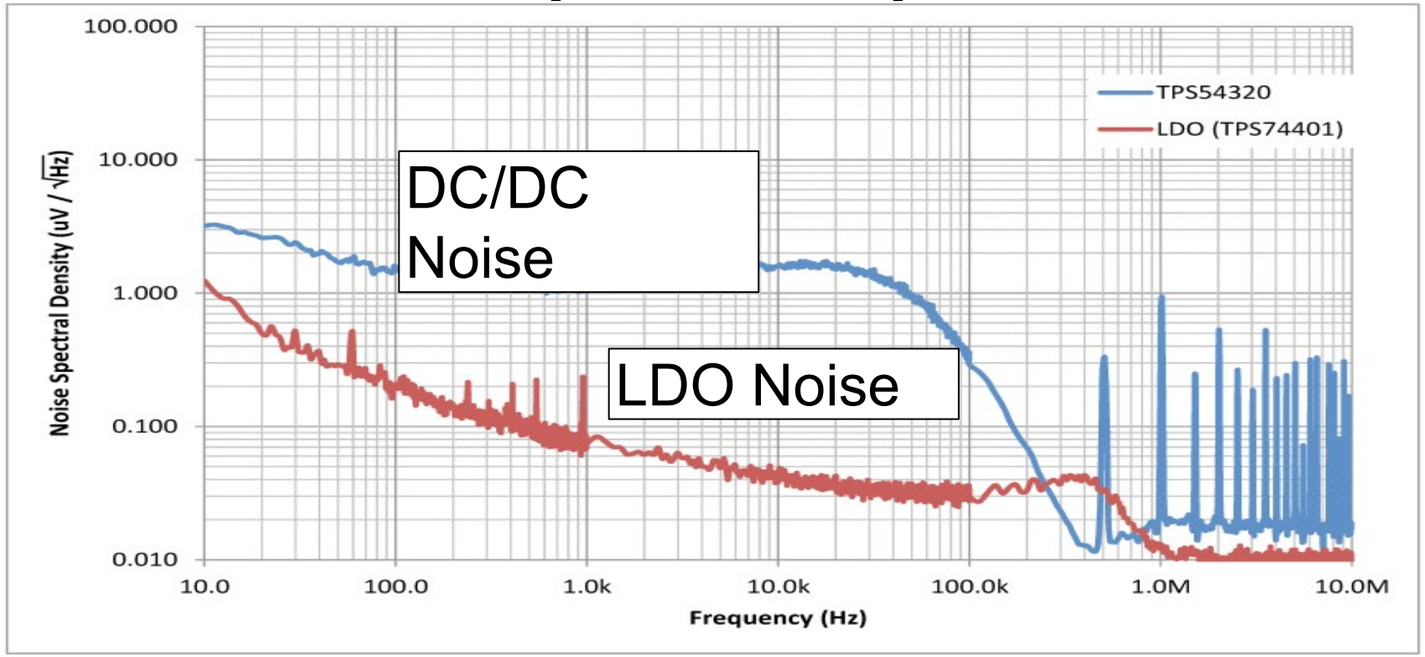
PSRR (Power Supply Rejection Ratio) represents the ability of the LDO to filter input voltage changes. This is critical for low-noise applications.

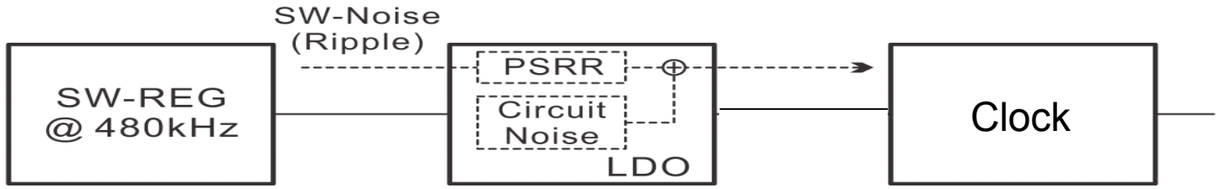
$$PSRR = 20 * \log\left(\frac{VIN_{AC}}{VOUT_{AC}}\right)$$



The Importance of LDO PSRR

- DC/DC (switching) converters are necessary for efficiency, however they are very noisy
  - Many devices are very sensitive to power supply noise
  - DC/DC converters are commonly followed by an LDO to clean the supply





Typical PSRR Curve

Region 1 is determined by:

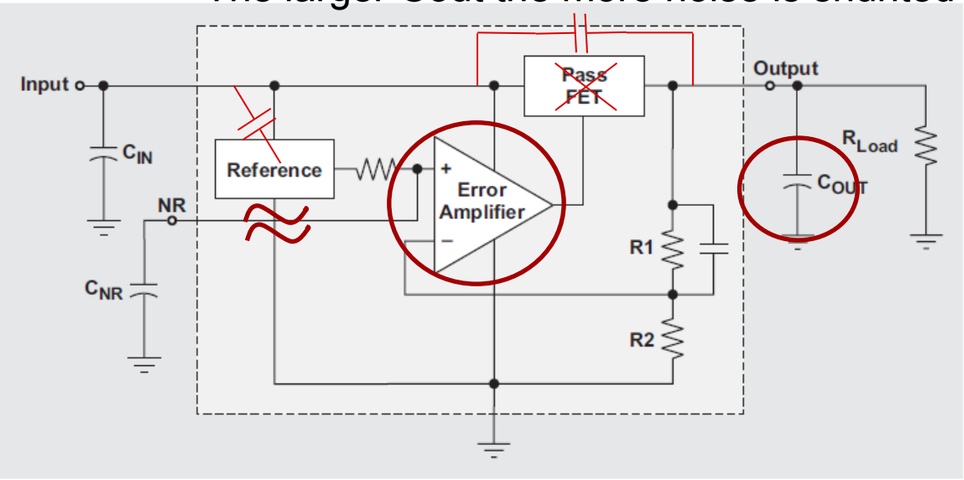
- PSRR of the Reference and the effectiveness of the RC filter

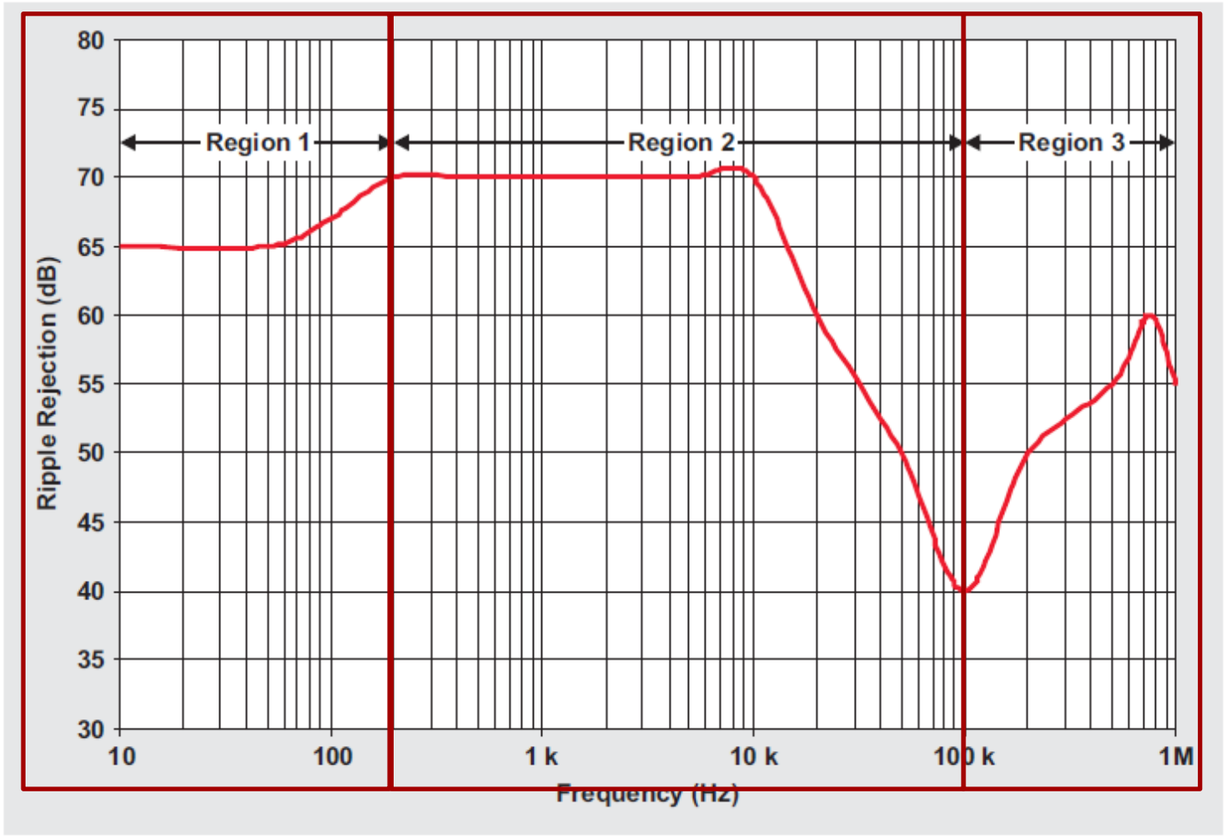
Region 2 is determined by:

- Open-Loop Gain of Error Amplifier

Region 3 is determined by:

- Parasitic capacitance of the FET and the output capacitor (capacitive divider)
  - The smaller the parasitic cap the less the Vin is AC coupled to Vout
  - The larger Cout the more noise is shunted to GND

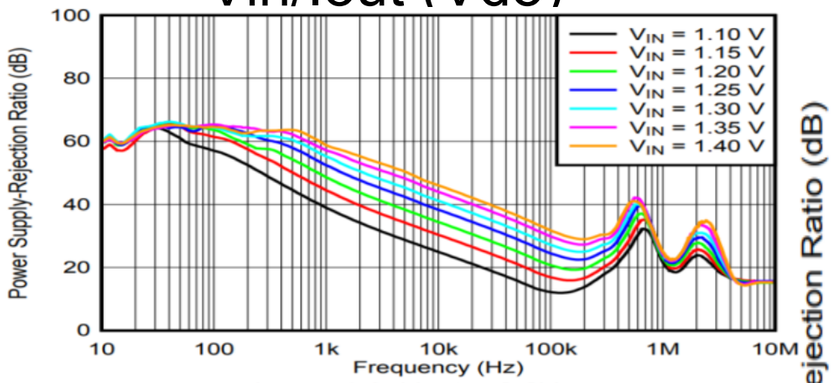




What Conditions Effect PSRR

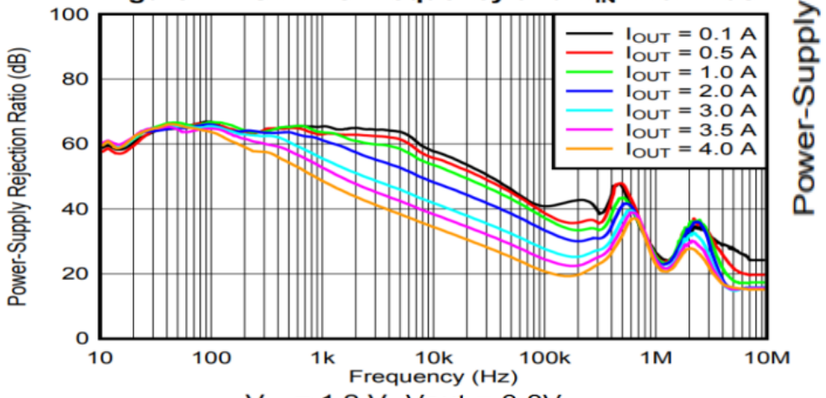
TECH DAYS
Texas Instruments

#1 thing that effects PSRR performance is the Combo of Vin/Iout (Vdo)



I_{OUT} = 4 A, Vout = 0.8V

Figure 2. PSRR vs Frequency and V_{IN} With Bias



V_{IN} = 1.2 V, Vout = 0.8V

Figure 1. PSRR vs Frequency and I_{OUT}

The next thing that effects PSRR is the noise reduction capacitor

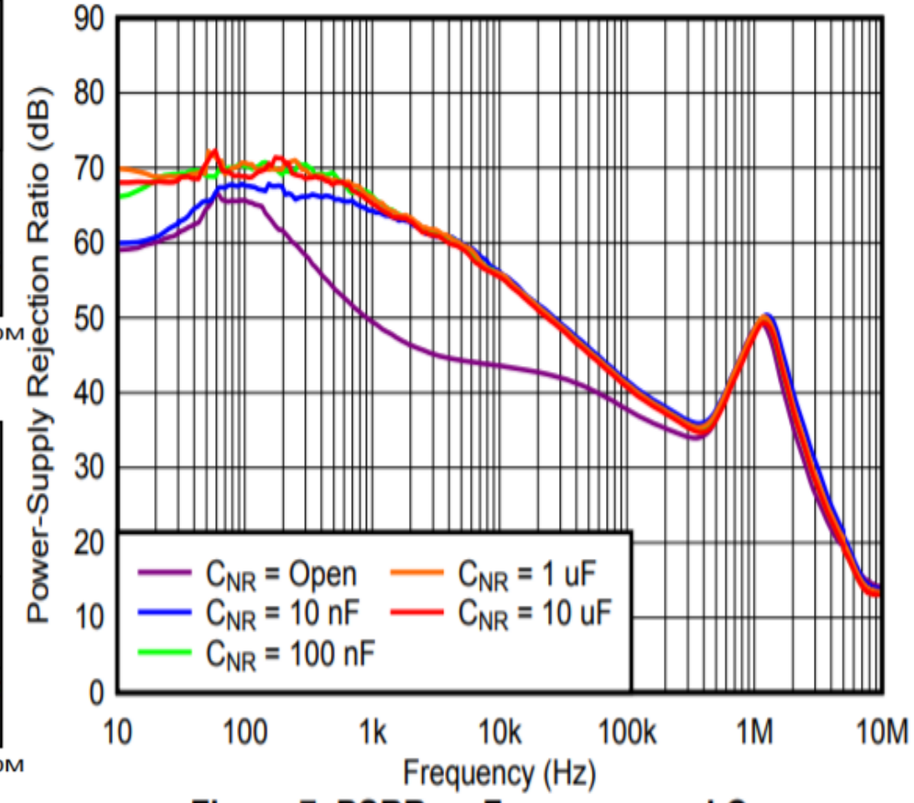


Figure 7. PSRR vs Frequency and $C_{NR/SS}$

The final thing that effects PSRR is the feedforward capacitor

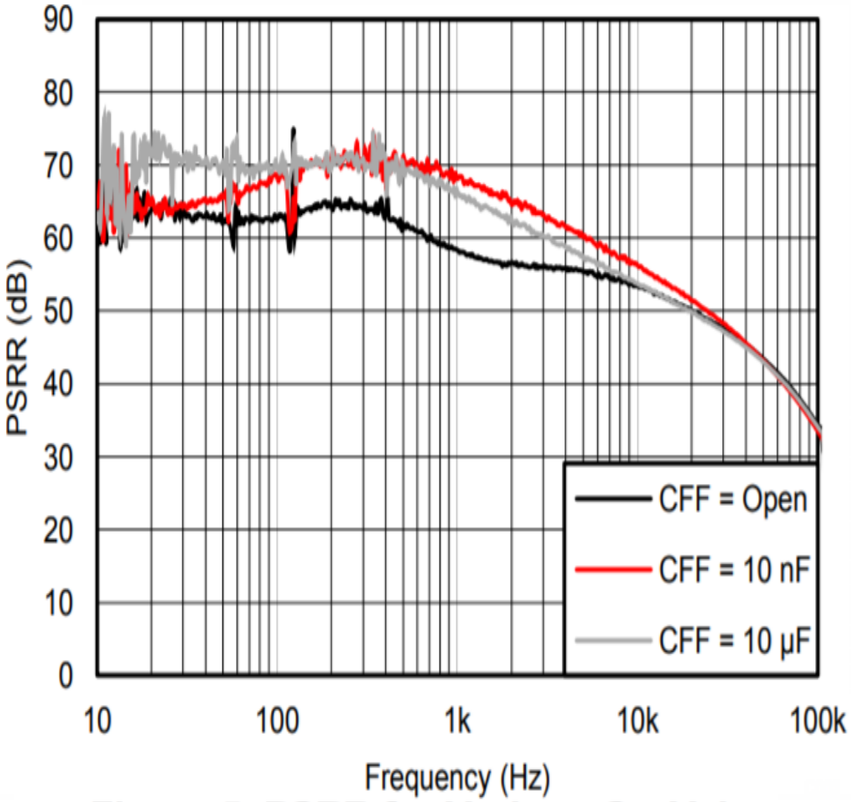


Figure 5. PSRR for Various C_{FF} Values

What Conditions Do Not Effect PSRR

TECH DAYS
Texas Instruments

Number one thing that has almost no effect on PSRR is Vbias>min

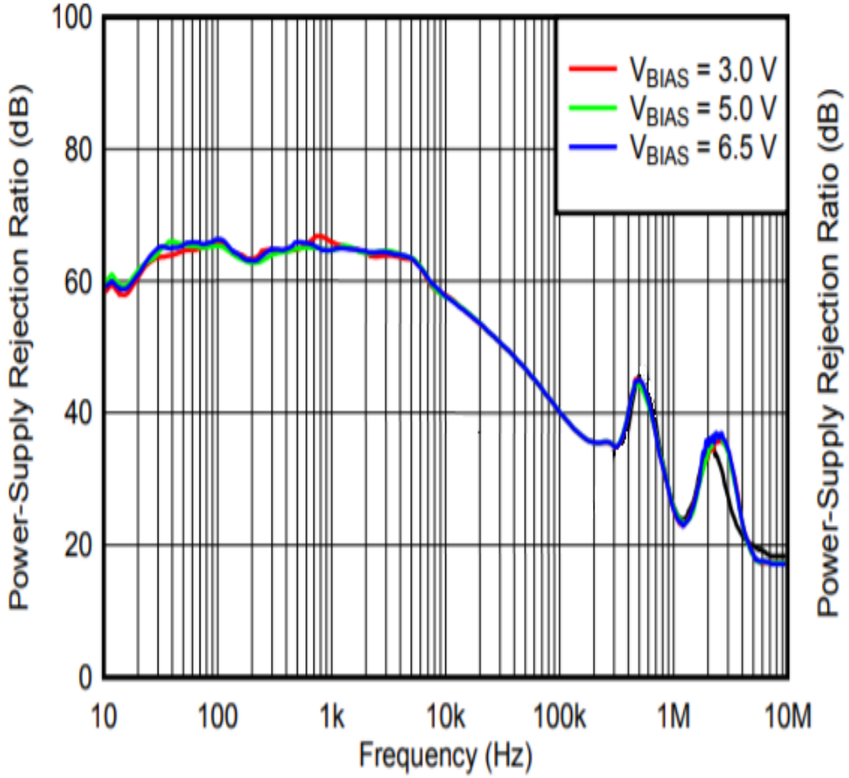


Figure 3. PSRR vs Frequency and V_{BIAS}

The next thing that only has a small effect on PSRR is Vout

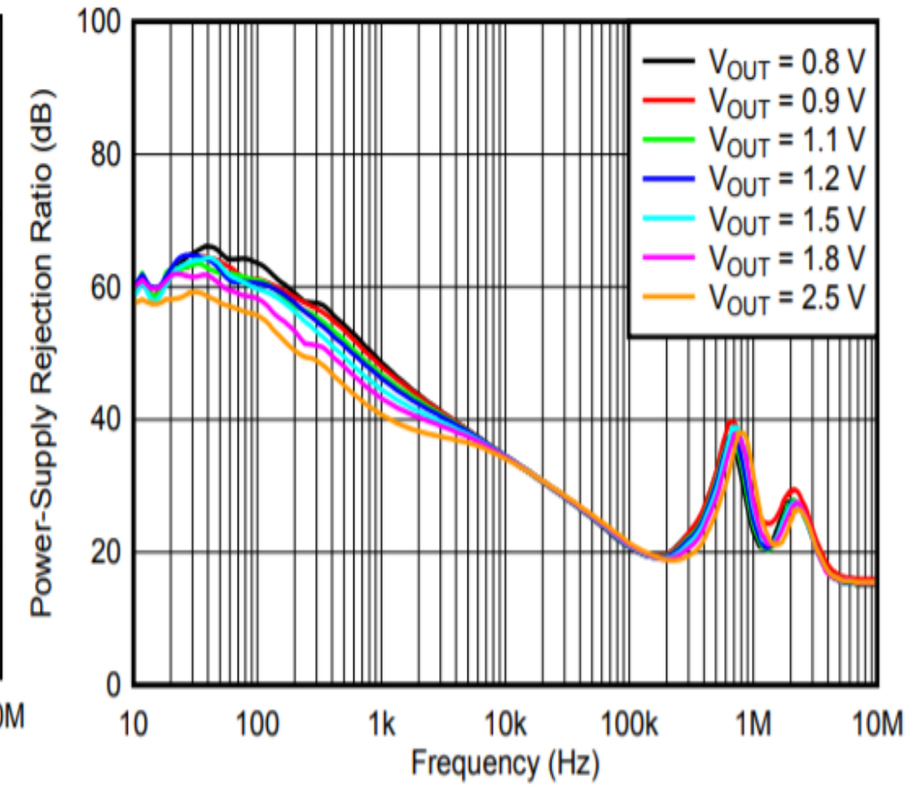


Figure 5. PSRR vs Frequency and V_{OUT} With Bias

The final thing that has some effect (but only at high freq) is output capacitor

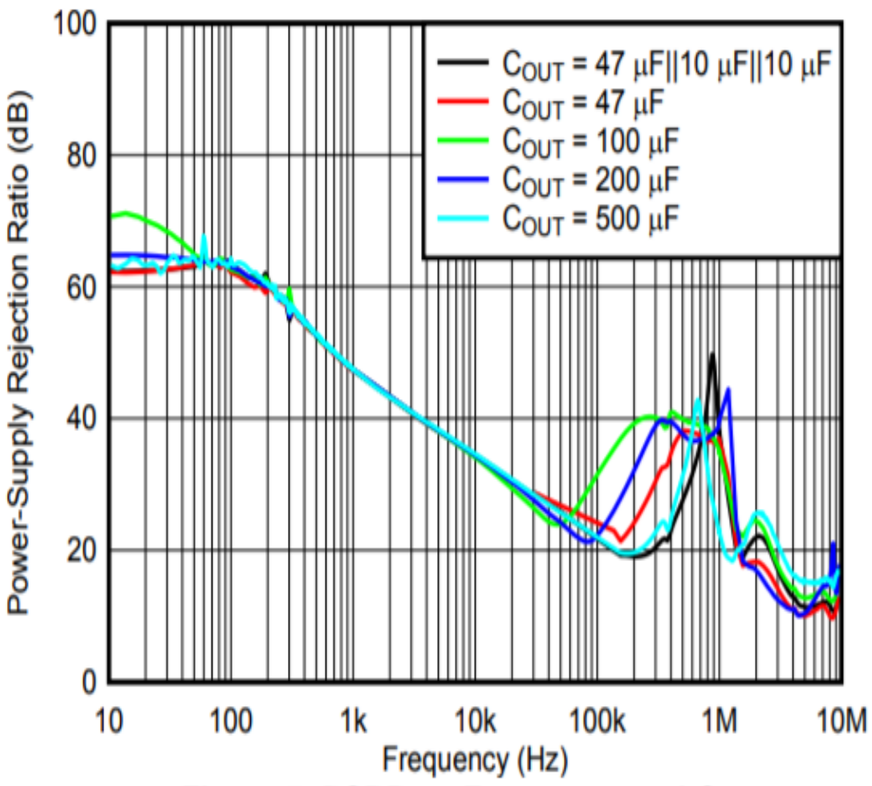


Figure 7. PSRR vs Frequency and C_{OUT}

Topics

- Noise
- PSRR
- Thermal Performance
- Capacitor vs Capacitance
- Getting Answers to Your LDO Questions ASAP

JEDEC Thermals

- Because an IC's thermal dissipation is subject to many variables we use the JEDEC standard (JESD51) for all thermal modeling.
- The JEDEC standard is used so that devices can be easily compared on a similar basis.
  - if a competitor is not reporting the JEDEC standard the customer should consider why they don't want to be directly compared to other devices.
- Common thermal metrics: θ_{JA}, θ_{JB}, $\theta_{JC(top)}$, $\theta_{JC(bot)}$

TI Datasheet

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS732[3] DRB [SON] 8 PINS	TPS732[3] DCQ [SOT223] 6 PINS	TPS732[3] DBV [SOT23] 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.3	53.1	205.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	35.2	119	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.8	7.8	35.4	
ψ_{JT}	Junction-to-top characterization parameter	2.7	2.9	12.7	
ψ_{JB}	Junction-to-board characterization parameter	25	7.7	34.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator*.
(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3 × 2 thermal via array.

Competitor Datasheet

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
DPAK 5-PIN PACKAGE			
	Min Pad Board (Note 3)	**1" Pad Board** (Note 4)	
Junction-to-Tab (psi-JLx, ψ_{JLx})	4.2	4.7	C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	100.9	46.8	C/W
D²PAK 5-PIN PACKAGE			
	0.4 sq. in. Spreader Board (Note 5)	**1.2 sq. in. Spreader Board** (Note 6)	
Junction-to-Tab (psi-JLx, ψ_{JLx})	3.8	4.0	C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	74.8	41.6	C/W

3. 1 oz. copper, 0.26 inch² (168 mm²) copper area, 0.062" thick FR4.
4. 1 oz. copper, 1.14 inch² (736 mm²) copper area, 0.062" thick FR4.
5. 1 oz. copper, 0.373 inch² (241 mm²) copper area, 0.062" thick FR4.
6. 1 oz. copper, 1.222 inch² (788 mm²) copper area, 0.062" thick FR4.

28mm x 28mm area on the top side dedicated to only thermal dissipation?

θ_{JA}: Understanding Usage and Limitations

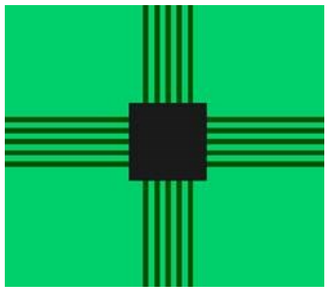
TECH DAYS
Texas Instruments

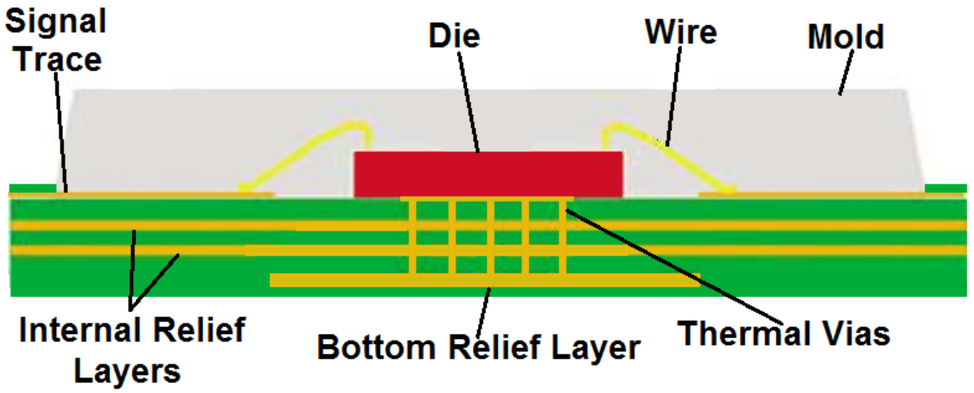
- The junction-to-ambient thermal resistance, θ_{JA}, is the most commonly used thermal metric.
  - θ_{JA} is a measure of the thermal performance of an IC mounted on a PCB.
- θ_{JA} is used since the ambient temperature is one of the few temperatures that designers have accurate data on. $T_J = T_A + (\theta_{JA} * P_D)$
  - The board acts as the main heat sink for any IC attached to it
  - If the actual application board is significantly different from the JEDEC High-K board this can result in an estimate that is unrealistic

Factors Affecting θja	Strength of Influence (rule of thumb)	Relation to θja
PCB design	Very Strong	The more metal connected to the IC the lower θja due to larger thermal mass
Chip or pad size	Strong	The larger the chip and thermal pad the lower θja due to heat spreading
Altitude	Medum	The lower the altitude the lower θja due to increased cooling efficiency of air
External ambient temperature	Weak	The higher the ambient temp the lower θja due to increased radiative heat transfer
Power dissipation	Very Weak	The higher the junction temp the lower θja due to increased heat transfer

JEDEC High-K Board

- TI LDO thermal metrics are modeled using the JEDEC High-K Board (2s2p)
- The JEDEC High-K board has:
  - Two internal layers which have ~5500mm^2 of 1oz copper (1 GND & 1 PWR plane)
  - Bottom layer (opposite the IC) thermal relief layer which has ~1100mm^2 of 2oz copper
  - Internal GND plane and bottom GND plane are connected to the thermal pad using as many thermal vias as can be fit within the power pad dimensions.
  - The top layer only has traces running straight to the pins.
- The JEDEC high-k board is good but not 100% optimized for maximum thermal dissipation





TEST BOARD DESIGN	JEDEC HIGH-K 2s2p	JEDEC LOW-K 1s0p
Trace thickness	0.0028 in	
Trace length	0.98 in	
PCB thickness	0.062 in	
PCB width	4 in	
PCB length	4.5 in	
Power/ground plane thickness	0.0014in (2 planes)	No internal copper planes

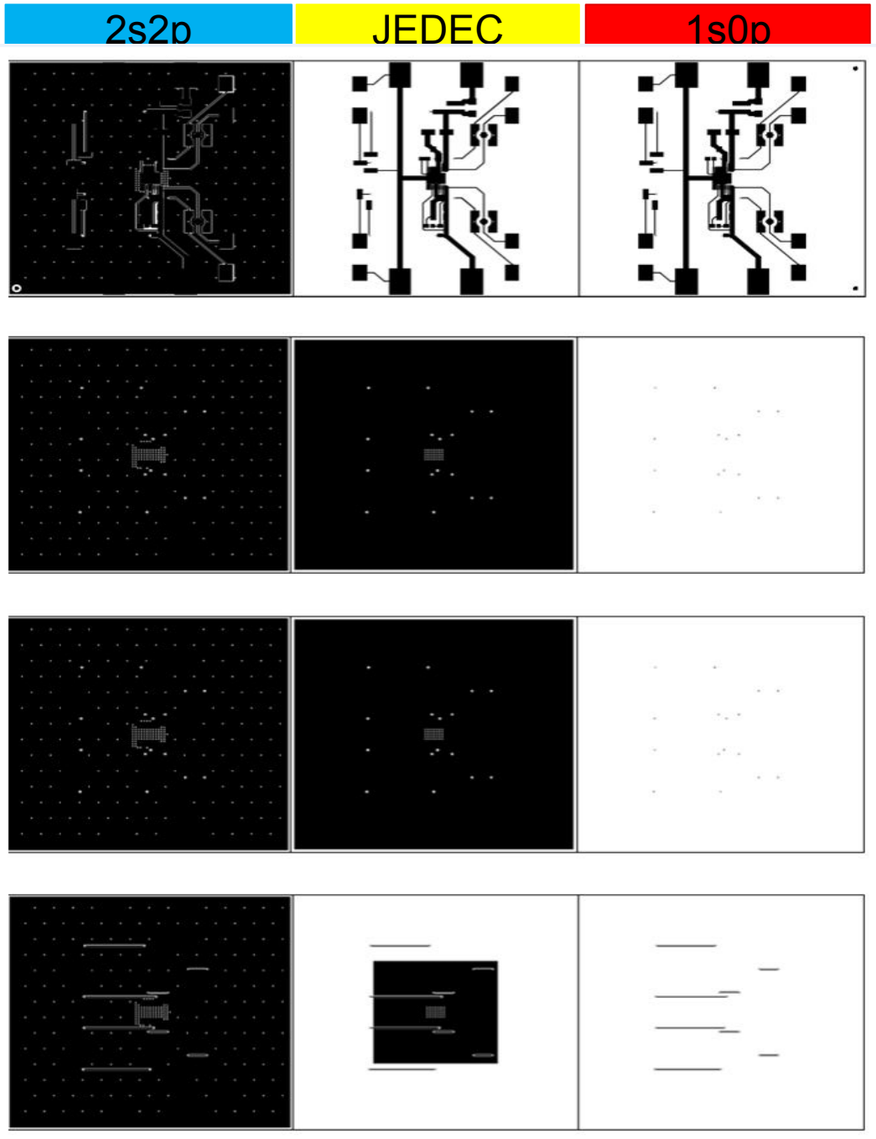
Guidelines For Maximum Thermal Relief

TECH DAYS
Texas Instruments

✓Have as much metal as possible in the areas around the device (both on the same layer and the layers below it)
- 2oz copper is better than 1oz copper simply because there is extra metal
- The more thermal vias the better spreading the heat between the different layers

✓The largest array of thermal vias in the thermal pad maximizes the amount of heat which can be transferred from the LDO to the internal and bottom layers.
- A 6x6 array allows the internal layers to dissipate heat almost as well as the top layer which is often crowded with other components.
- Vias should be as small as possible to decrease the amount of open space in the via hole (this maximizes the amount of metal)
- If the power pad is too small to put many vias in, then placing extra vias as close as possible to the power pad is still helpful

✓If the board is large, there is a lot of metal, and the thermal vias are maximized then it is possible to reduce the θja by 25-50%.



Other Thermal Considerations

- Nearby heat sources on the PCB can reduce the ability of the LDO to shed heat to the board
  - This is because those other heat sources increase the local board temperature decreasing the temperature differential between the board to the LDO in question
- Load pulses can still heat the die significantly if the duty cycle isn't low
  - A step increase in power dissipation will cause the die temp to stabilize on the order of hundreds of milliseconds to 1 second
    - For ~1 second pulses the LDO should reach a similar internal temp as if the load was on constantly
  - Pulses of tens of milliseconds don't heat the die nearly as much
- Forced convection and board level heatsinks can help significantly, though they are rarely a consideration for many applications which have to rely on passive cooling only
  - The thermal models in our datasheets assume natural convection (no forced air).

AEC-Q100 Grade 1 vs Grade 0

TECH DAYS
Texas Instruments

- Most of TI's commercial LDOs are designed such that they can be qualified to the Q100 Grade 1 standards
- There can be challenges when taking some of our LDOs through the Grade 0 qualification.
  - Package: Leaded vs Leadless packages
  - Materials used: IC's top level metal and bond wire materials must be chosen appropriately

- **Due to complexity of designing for Grade 0 it is best to design and plan for Grade 0 qualification at the beginning of a new design**

ACCELERATED ENVIRONMENT STRESS TESTS	
STRESS	**ADDITIONAL REQUIREMENTS**
Temperature Cycling	PC before TC for surface mount devices. **Grade 0:** -55ºC to +150ºC for 2000 cycles or equivalent. **Grade 1:** -55°C to +150°C for 1000 cycles or equivalent.
Power Temperature Cycling	PC before PTC for surface mount devices. Test required only on devices with maximum rated power ≥ 1 watt or $\Delta T_J \geq$ 40ºC or devices designed to drive inductive loads. **Grade 0:** T_a of -40ºC to +150ºC for 1000 cycles. **Grade 1:** T_a of -40ºC to +125ºC for 1000 cycles.
High Temperature Storage Life	**Plastic Packaged Parts** **Grade 0:** +175ºC T_a for 1000 hours or +150ºC T_a for 2000 hours. **Grade 1:** +150ºC T_a for 1000 hours or +175ºC T_a for 500 hours.
ACCELERATED LIFETIME SIMULATION TESTS	
STRESS	**ADDITIONAL REQUIREMENTS**
High Temperature Operating Life	For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005. **Grade 0:** +150ºC T_a for 1000 hours. **Grade 1:** +125°C T_a for 1000 hours. **Grade 2:** +105ºC T_a for 1000 hours. **Grade 3:** +85ºC T_a for 1000 hours. HTOL NOTES: If Tj is used to set the HTOL conditions, the minimum stress of 1000 hours at the Ta of the device is to be shown using activation energy of 0.7ev or other value technically justified.

AEC-Q100 Grade 1 vs Grade 0

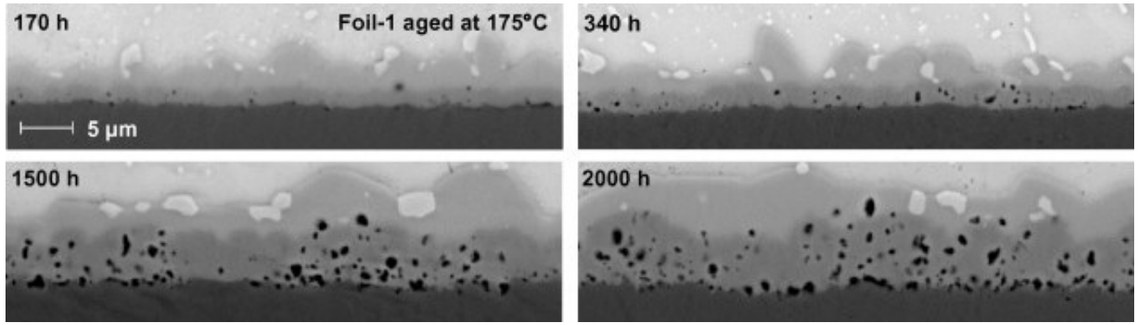
- TC and PTC: Leadless packages struggle to pass Grade 0 standards due to the different coefficients of thermal expansion (CTE) of the IC and the PCB.
  - Solder joints often break due to different rates of expansion
  - The CTE changes significantly when you surpass the glass transition temperature (Tg) ~130C-160C
  - The metal leads on leaded packages can move as the IC and PCB expand at differing rates which puts less stress on the solder attaching the IC to the PCB.

ACCELERATED ENVIRONMENT STRESS TESTS	
STRESS	**ADDITIONAL REQUIREMENTS**
Temperature Cycling	PC before TC for surface mount devices. **Grade 0:** -55ºC to +150ºC for 2000 cycles or equivalent. **Grade 1:** -55°C to +150°C for 1000 cycles or equivalent.
Power Temperature Cycling	PC before PTC for surface mount devices. Test required only on devices with maximum rated power ≥ 1 watt or $\Delta T_J \geq$ 40ºC or devices designed to drive inductive loads. **Grade 0:** T_a of -40ºC to +150ºC for 1000 cycles. **Grade 1:** T_a of -40ºC to +125ºC for 1000 cycles.
High Temperature Storage Life	**Plastic Packaged Parts** **Grade 0:** +175ºC T_a for 1000 hours or +150ºC T_a for 2000 hours. **Grade 1:** +150ºC T_a for 1000 hours or +175ºC T_a for 500 hours.
ACCELERATED LIFETIME SIMULATION TESTS	
STRESS	**ADDITIONAL REQUIREMENTS**
High Temperature Operating Life	For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005. **Grade 0:** +150ºC T_a for 1000 hours. **Grade 1:** +125°C T_a for 1000 hours. **Grade 2:** +105ºC T_a for 1000 hours. **Grade 3:** +85ºC T_a for 1000 hours. HTOL NOTES: If Tj is used to set the HTOL conditions, the minimum stress of 1000 hours at the Ta of the device is to be shown using activation energy of 0.7ev or other value technically justified.

AEC-Q100 Grade 1 vs Grade 0

TECH DAYS
Texas Instruments

- HTSL: Chemical interactions that take place between bond wires and metal layers are sped up due to increased temperature which can cause failures
  - HTSL usually causes Kirkendall Voiding failures
    - Kirkendall Voiding is caused by the diffusion of one metal into another metal. This chemical reaction increases as the temperatures increases.



  - To reduce the likelihood of failure at the increased temperatures Grade 0 qualification requires the selection of the proper materials

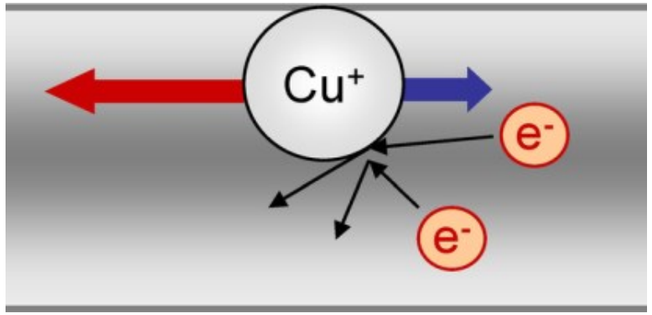
ACCELERATED ENVIRONMENT STRESS TESTS	
STRESS	**ADDITIONAL REQUIREMENTS**
Temperature Cycling	PC before TC for surface mount devices. **Grade 0:** -55ºC to +150ºC for 2000 cycles or equivalent. **Grade 1:** -55°C to +150°C for 1000 cycles or equivalent.
Power Temperature Cycling	PC before PTC for surface mount devices. Test required only on devices with maximum rated power ≥ 1 watt or $\Delta T_J \geq$ 40ºC or devices designed to drive inductive loads. **Grade 0:** T_a of -40ºC to +150ºC for 1000 cycles. **Grade 1:** T_a of -40ºC to +125ºC for 1000 cycles.
High Temperature Storage Life	**Plastic Packaged Parts** **Grade 0:** +175ºC T_a for 1000 hours or +150ºC T_a for 2000 hours. **Grade 1:** +150ºC T_a for 1000 hours or +175ºC T_a for 500 hours.

ACCELERATED LIFETIME SIMULATION TESTS	
STRESS	**ADDITIONAL REQUIREMENTS**
High Temperature Operating Life	For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005. **Grade 0:** +150ºC T_a for 1000 hours. **Grade 1:** +125°C T_a for 1000 hours. **Grade 2:** +105ºC T_a for 1000 hours. **Grade 3:** +85ºC T_a for 1000 hours. HTOL NOTES: If Tj is used to set the HTOL conditions, the minimum stress of 1000 hours at the Ta of the device is to be shown using activation energy of 0.7ev or other value technically justified.

AEC-Q100 Grade 1 vs Grade 0

TECH DAYS
Texas Instruments

- HTOL: physical interactions that take place in bond wires and metal layers are sped up due to increased temperature which can cause failures
  - HTOL usually causes Electromigration failures
    - **Electromigration** is the physical movement of metal atoms caused by electrons running into those metal atoms. The higher the temperature the more collisions there are, eventually causing an open circuit due to missing metal atoms



  - To reduce the likelihood of failure at the increased temperatures Grade 0 qualification requires the selection of the proper materials

ACCELERATED ENVIRONMENT STRESS TESTS	
STRESS	**ADDITIONAL REQUIREMENTS**
Temperature Cycling	PC before TC for surface mount devices. **Grade 0:** -55ºC to +150ºC for 2000 cycles or equivalent. **Grade 1:** -55°C to +150°C for 1000 cycles or equivalent.
Power Temperature Cycling	PC before PTC for surface mount devices. Test required only on devices with maximum rated power ≥ 1 watt or $\Delta T_J \geq$ 40ºC or devices designed to drive inductive loads. **Grade 0:** T_a of -40ºC to +150ºC for 1000 cycles. **Grade 1:** T_a of -40ºC to +125ºC for 1000 cycles.
High Temperature Storage Life	**Plastic Packaged Parts** **Grade 0:** +175ºC T_a for 1000 hours or +150ºC T_a for 2000 hours. **Grade 1:** +150ºC T_a for 1000 hours or +175ºC T_a for 500 hours.
ACCELERATED LIFETIME SIMULATION TESTS	
STRESS	**ADDITIONAL REQUIREMENTS**
High Temperature Operating Life	For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005. **Grade 0:** +150ºC T_a for 1000 hours. **Grade 1:** +125°C T_a for 1000 hours. **Grade 2:** +105ºC T_a for 1000 hours. **Grade 3:** +85ºC T_a for 1000 hours. HTOL NOTES: If Tj is used to set the HTOL conditions, the minimum stress of 1000 hours at the Ta of the device is to be shown using activation energy of 0.7ev or other value technically justified.

HTOL Grade 1 vs Grade 0

- Mission Profiles
  - We can use mission profiles which have temperature (ambient or board) and power dissipation profiles to calculate how it compares with the AEC-Q100 HTOL profile.

- Grade 1 vs Grade 0
  - Grade 1 assumes average Tj=~55C for approximately 9 years
  - Grade 0 assumes average Tj=~70C for approximately 9 years

Device Name:	TLV702-Q	Arrhenius calculations					
Package	DBV	units	$AF \equiv e^{-\frac{Ea}{k}\left(\frac{1}{T1}-\frac{1}{T2}\right)}$				
EA	0.7	ev					
K	8.63E-05	constant					
Power	0.2618	W					
θjb	69.3	C/W					
Delta C	18.14274	C					
Oven Stress Temp	150	C	Orange cells can be changed.				
T_b Customer Requirments	T_j Customer Requirments	Hrs Customer Requirements	T_{oven} C HTOL	Hrs HTOL Conditions	AF	°K (T1)	°K (T2)
-40	**-21.86**	316.00	150	0.0	503545.09	251.14	423
-20	**-1.86**	316.00	150	0.0	46431.60	271.14	423
23	**41.14**	0.00	150	0.0	771.69	314.14	423
30	**48.14**	0.00	150	0.0	439.42	321.14	423
40	**58.14**	3.00	150	0.0	204.85	331.14	423
50	**68.14**	276.00	150	2.8	99.87	341.14	423
60	**78.14**	600.00	150	11.8	50.72	351.14	423
70	**88.14**	1196.00	150	44.7	26.74	361.14	423
80	**98.14**	3268.00	150	223.9	14.60	371.14	423
90	**108.14**	2493.00	150	303.1	8.22	381.14	423
100	**118.14**	1385.00	150	290.3	4.77	391.14	423
110	**128.14**	576.00	150	202.5	2.84	401.14	423
125	**143.14**	105.00	150	76.5	1.37	416.14	423
Total hours needed for Multiple T-=Hr requirements				1155.6			

Topics

- Noise
- PSRR
- Thermal Performance
- Capacitor vs Capacitance
- Getting Answers to Your LDO Questions ASAP

Capacitor & Capacitance Defined

- Capacitor: a **device** used to store an electric charge, consisting of one or more pairs of conductors separated by an insulator.
- Capacitance: the **ability** to store an electric charge.

- In an Ideal world the value written on a capacitor would be exactly the same as the amount of capacitance it provides when inserted into a system.
  - (Un)Fortunately we do not live in a world with ideal components
    - The existence of an ideal components would leave me without a job!

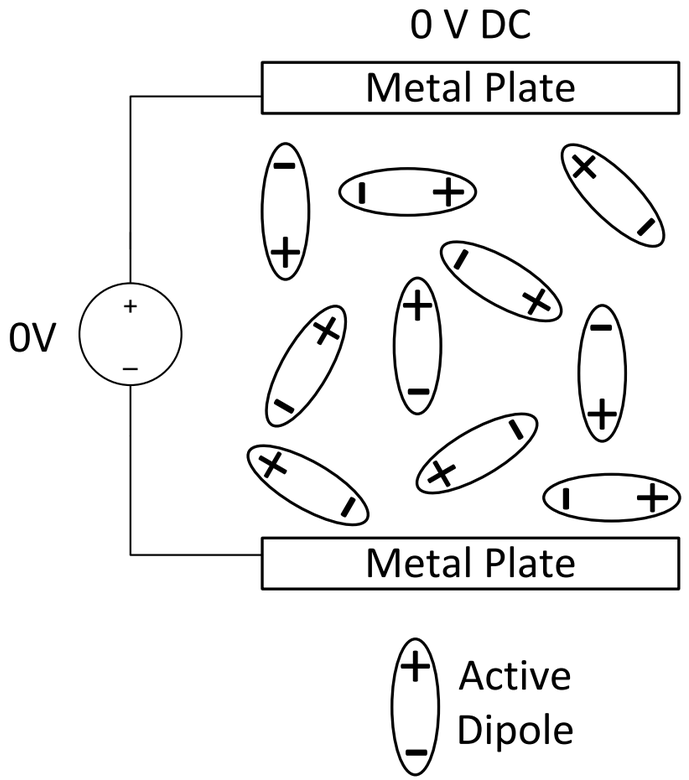
Capacitor vs Capacitance Explained

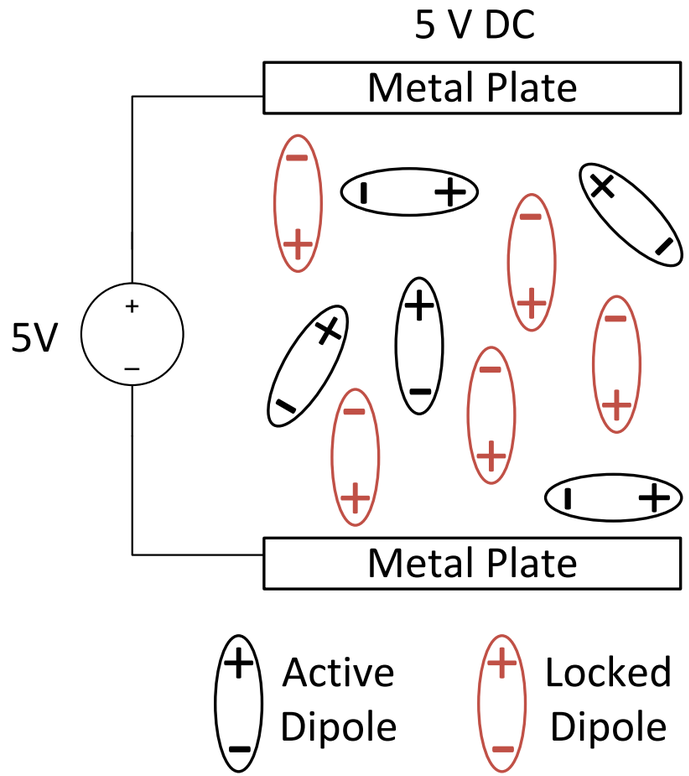
- There are three main reasons why the capacitance of a capacitor isn't always what it says on the label

1. Derating due to being biased with a DC Voltage
2. Derating due to changes in temperature
3. Manufacturing tolerances
   - This is called out specifically in the specs and is usually ±10% or ±20%

DC Voltage Derating Explained

- When a DC Voltage is applied to a capacitor it creates an E-field which “locks” some of the atomic dipoles into place.
  - These “locked” dipoles do not react to AC voltage transients which is why the effective capacitance decreases.



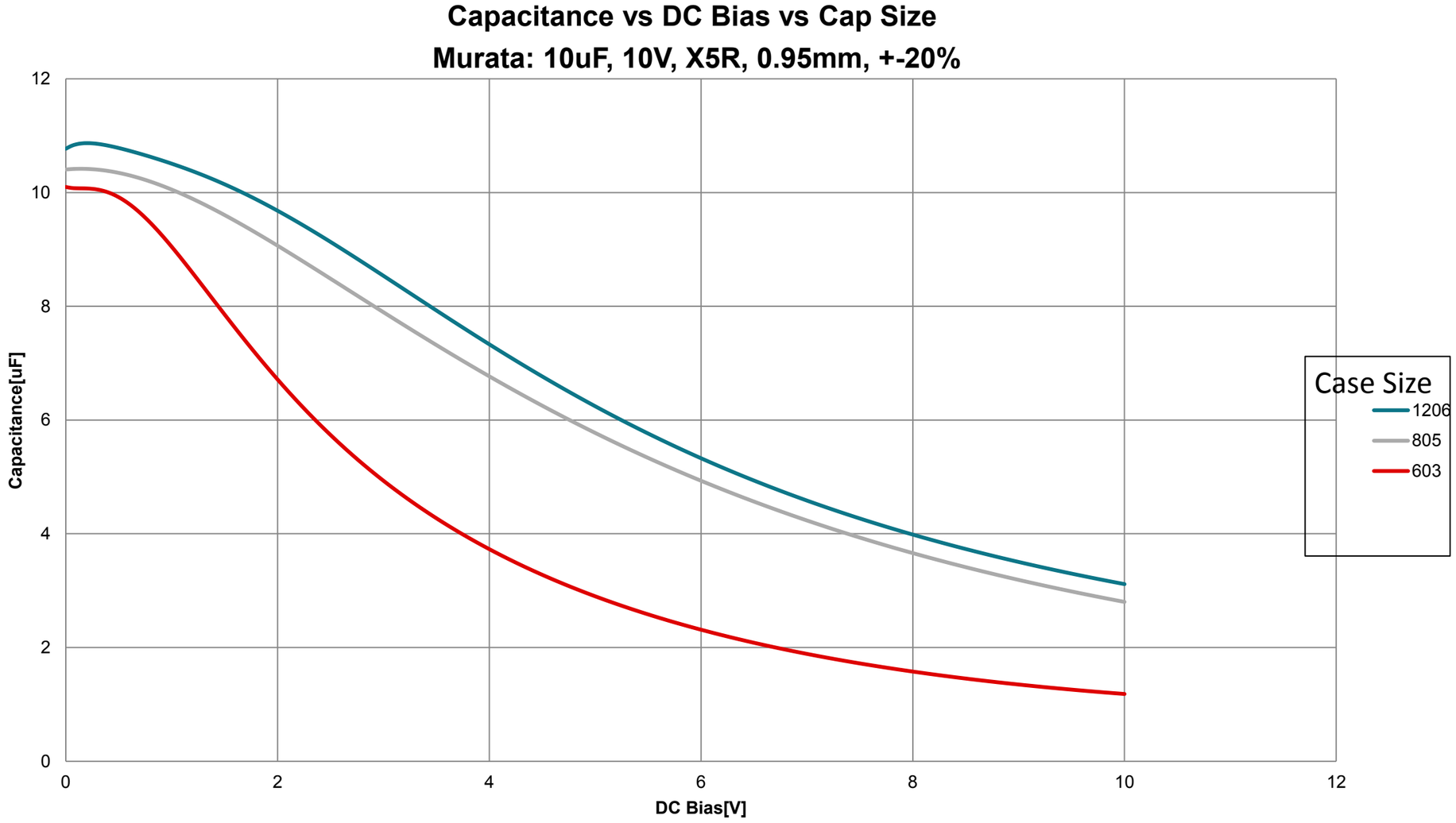


Capacitance vs DC Bias

TECH DAYS
Texas Instruments

Key Take Away

The same voltage applied across a thicker dielectric results in a lower E-Field which will “lock in” less dipoles and cause less derating



Capacitance vs Temperature Decoder Ring

TECH DAYS
Texas Instruments

Like all electronics capacitors have a temperature rating over which their performance is specified

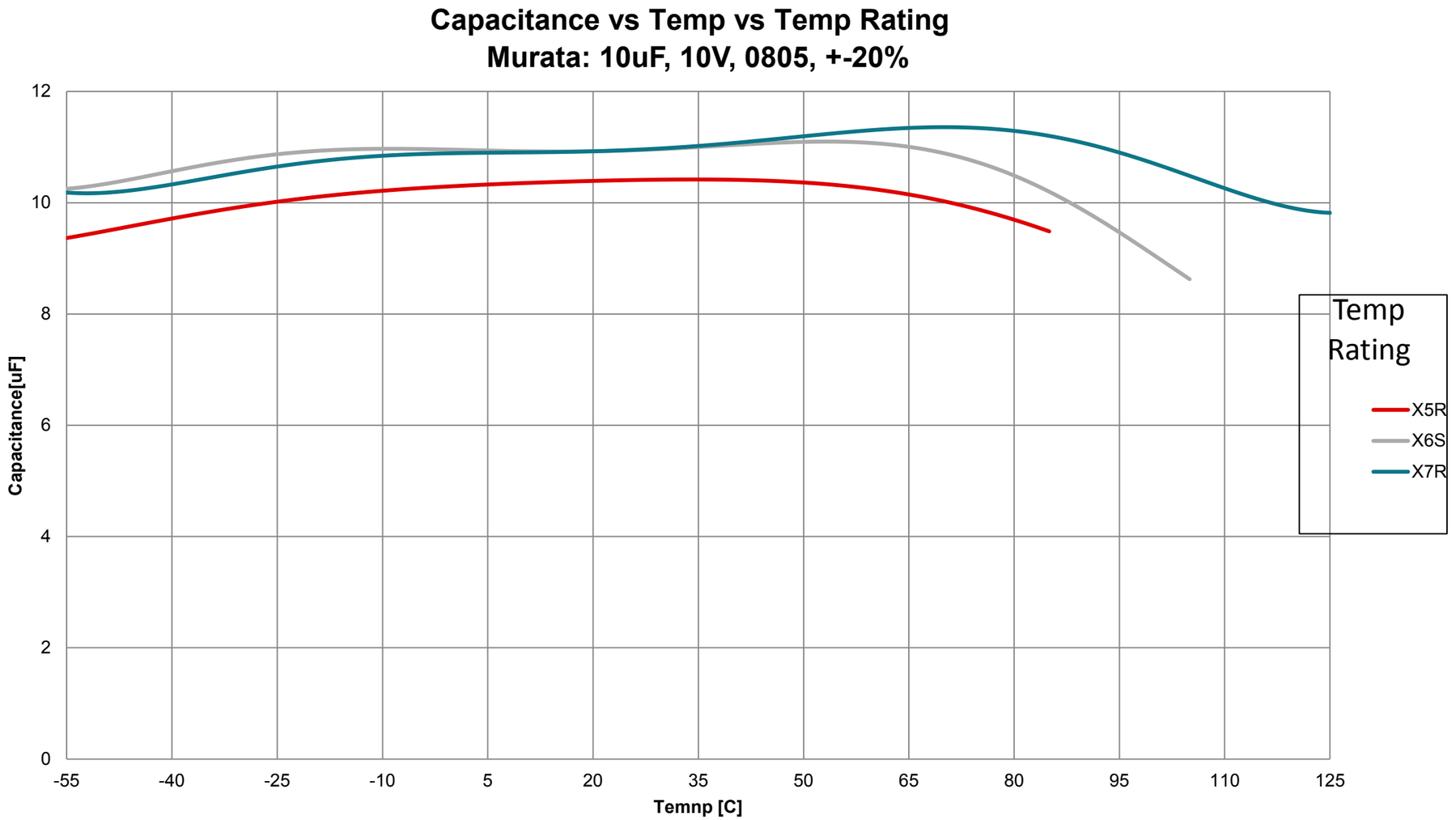
Majority of LDO junction temperatures are usually specified from -40C to 125C.

1st Character: Low Temp		2nd Character: High Temp		3rd Character: Max Change over Temp	
Char	Temp (°C)	Char	Temp (°C)	Char	Change (%)
Z	10	2	45	A	±1.0
Y	-30	4	65	B	±1.5
X	-55	5	85	C	±2.2
		6	105	D	±3.3
		7	125	E	±4.7
		8	150	F	±7.5
		9	200	P	±10
				R	±15
				S	±22
				T	+22, -33
				U	+22, -56
				V	+22, -82

So we usually recommend X5R or X7R caps

Capacitance vs Temperature Graph

Temperature affects the capacitance much less than the DC Bias which can reduce the capacitance by 90%



Topics

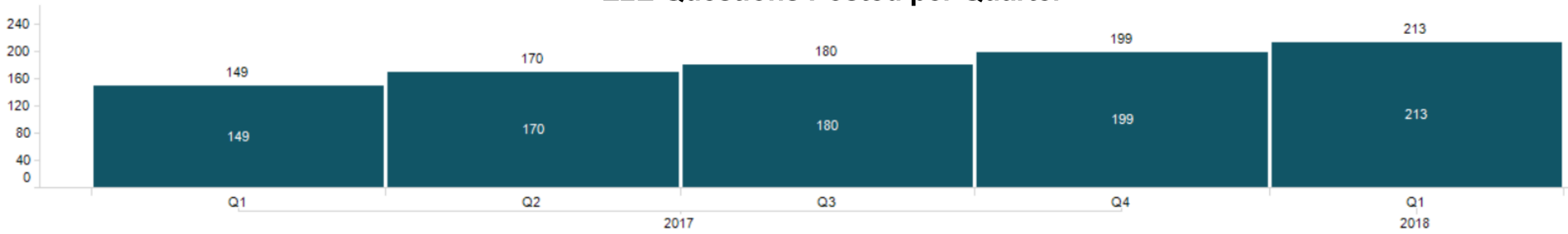
- Noise
- PSRR
- Thermal Performance
- Capacitor vs Capacitance
- Getting Answers to Your LDO Questions ASAP

Fastest Way to Get Answers

TECH DAYS
Texas Instruments

- The fastest way to get an answer to a question regarding LDOs is to post it on E2E
  - We know many people think that sending an email directly to one of the Apps Engineers (or better yet the Apps Manager!) will get them the fastest response.
    - However, this is **not** effective because like you each day we come in to inboxes full of emails which we must dig through to find the customer questions.
    - Instead we prioritize questions posted on E2E

Starting around Q4 of last year we started informing the field that E2E was the most effective way of submitting questions and as you can see it's working with E2E threads going up by almost 20%



Why Use E2E?

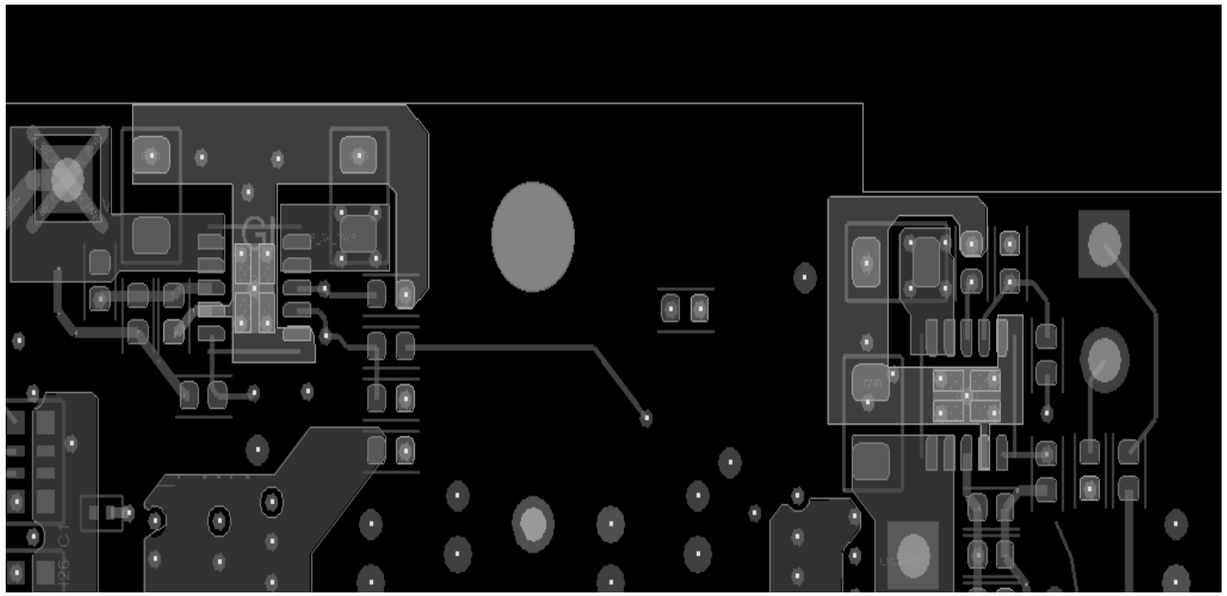
TECH DAYS
Texas Instruments

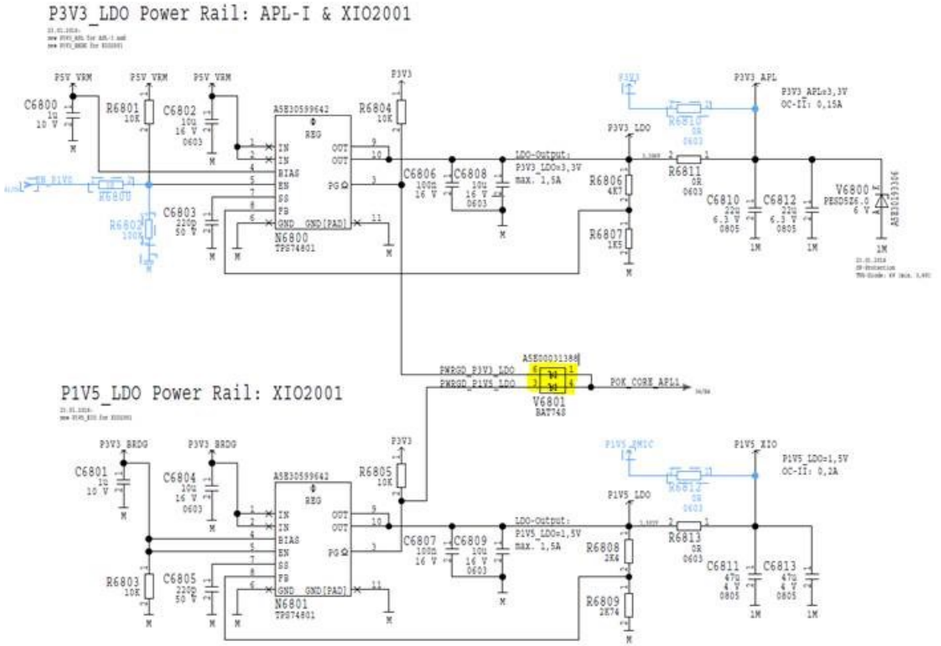
- It's faster because we have multiple people dedicated to monitoring and responding to all of the questions that are posted on E2E.
- Posting on E2E allows us to effectively track customer support metrics which can help us to justify dedicating even more resources to customer support.
  - Email has no effective way of tracking customer support metrics
- Posting on E2E also enables anybody to easily search for the answers to similar questions.
  - An email in another person's inbox isn't searchable by any one else on the team

Questions with Customer IP

TECH DAYS
Texas Instruments

- We understand that some customers may have sensitive IP in their questions and **those should not go on E2E, please send those requests to your field rep or myself** and I'll see that they are handled appropriately.
  - Examples of Customer IP include schematics or board layouts





Troubleshooting Questions

- If you are working through an issue and need our help please provide as many of the following as possible

In order of importance

1. Scope Shots
   - Scope shots are the best way for us to evaluate what is happening without being with the customer
   - They should include Vin, Ven, Vout and Iout if possible
     - If Vbias present or if PG is part of the issue include these

With these two items we can debug ~75% of issues remotely

2. Schematics
3. Input and output conditions
   - Vin, Vout (nominal), Cin, Cout, Cnr, Cff, Iout (is the load constant or changing?), what is driving Ven?
4. Board Layout
   - Not always needed immediately unless the problem seems related to: thermals, EMI, or PSRR/noise that is worse than expected