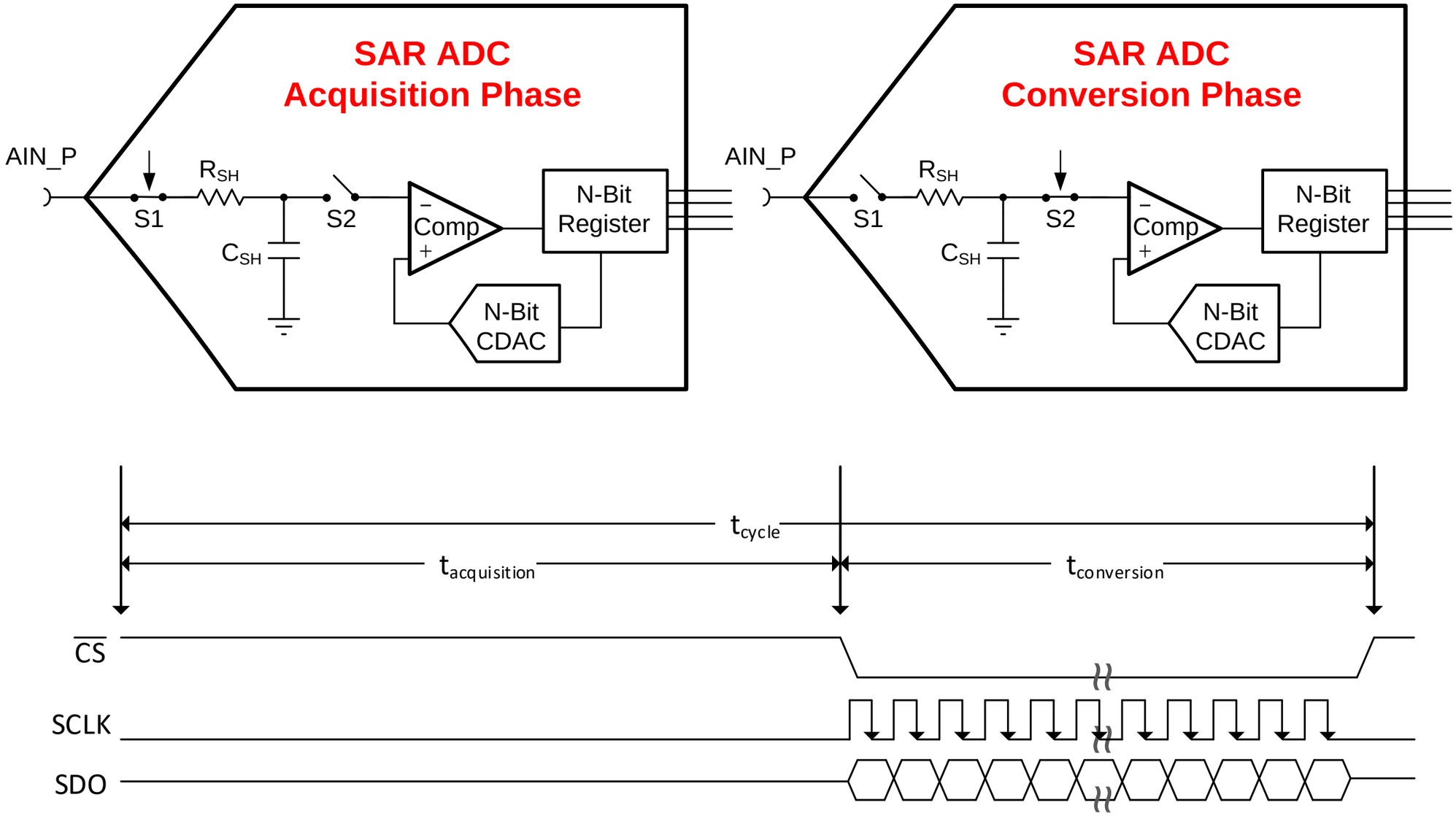
SAR ADC Power Scaling

TIPL 4601
TI Precision Labs – ADCs

Created by Reed Kaczmarek and Peggy Liska

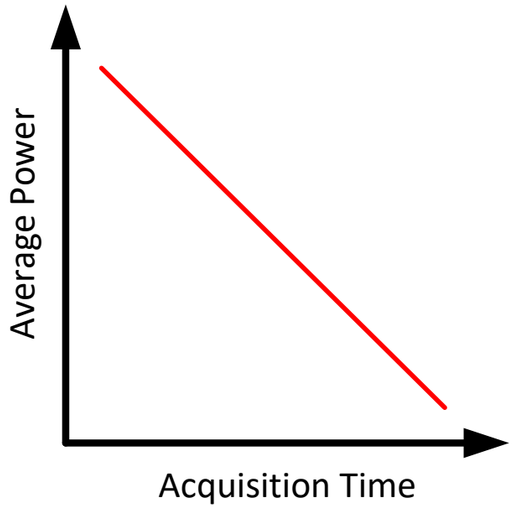
Presented by Peggy Liska

Acquisition Phase vs. Conversion Phase

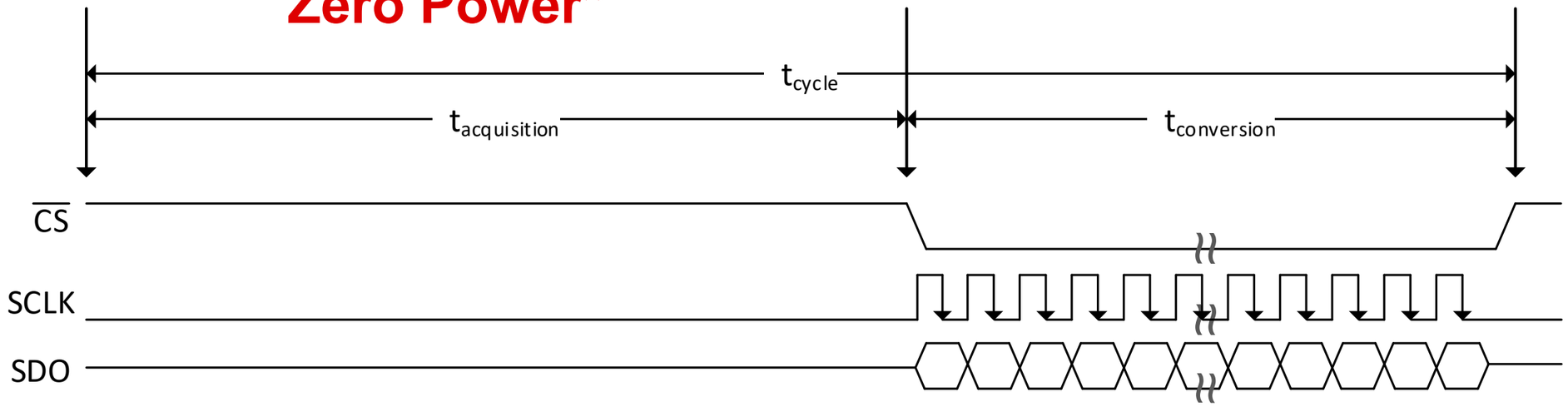


Power: Acquisition Phase vs. Conversion Phase

- The majority of the power is consumed during the conversion phase
- Note that not all SAR ADCs will support power scaling

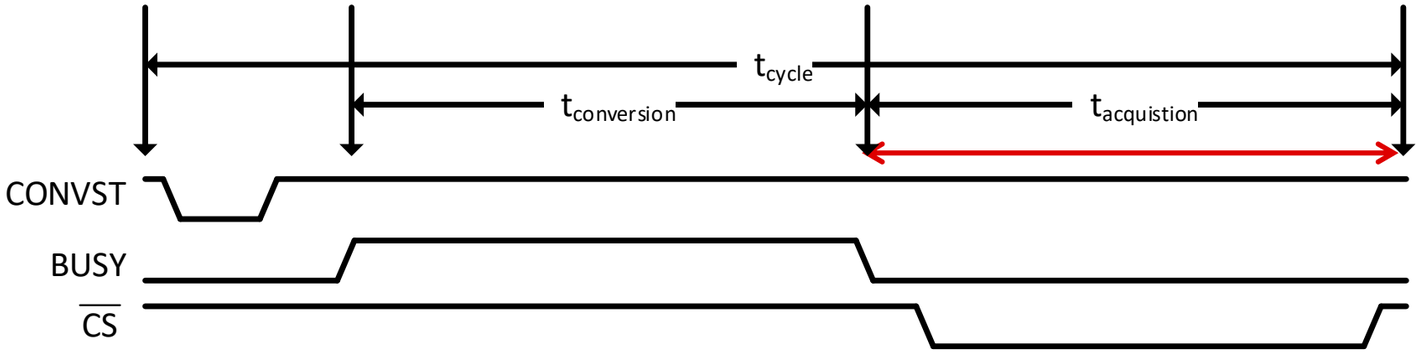


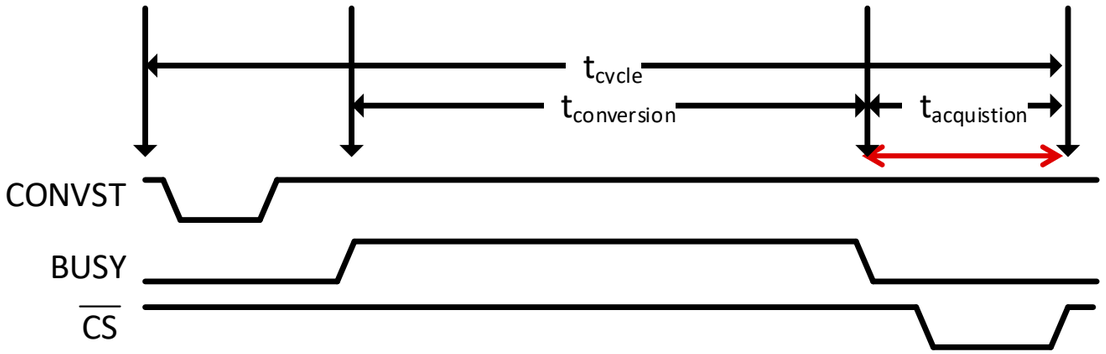
“Zero Power”



Acquisition Time: Internal Conversion Clock

- Conversion time is fixed due to internal conversion clock
- SCLK sets data output speed only, doesn't effect conversion / acquisition time
- Slower sampling rate directly adds more time for acquisition



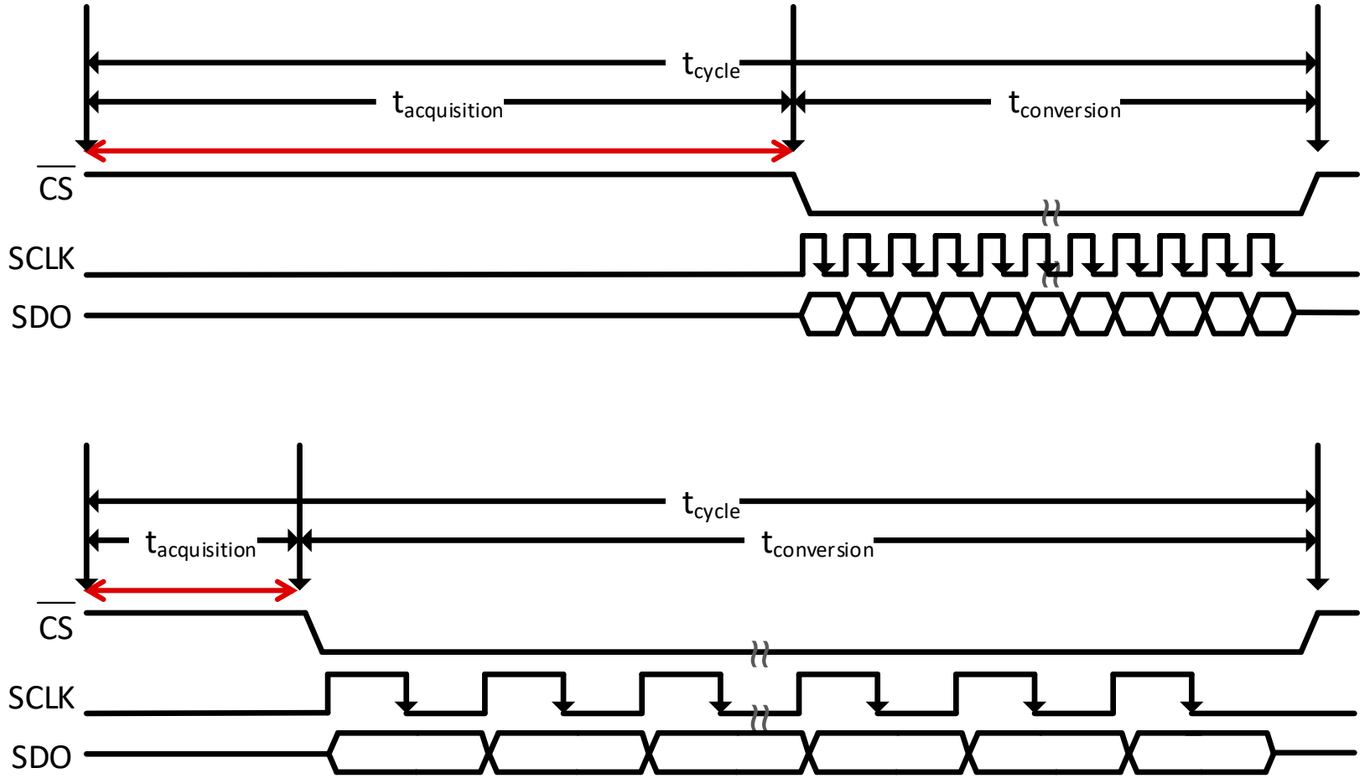


Examples:

ADS8881
ADS8332

Acquisition Time: External Conversion Clock

- SCLK sets data output speed and conversion time
- Increasing SCLK frequency increases acquisition time for same sampling rate
- Slower sampling rate with the same SCLK frequency increases acquisition time

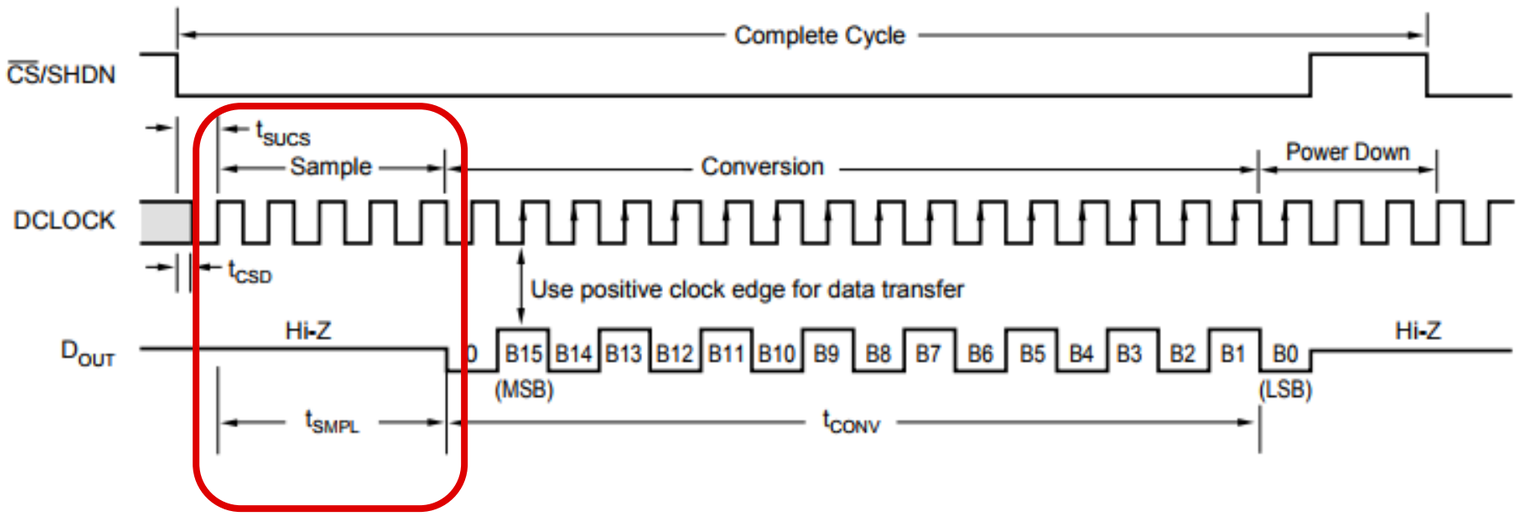


Examples:

ADS7042
ADS7056

Acquisition Time: Other

- I2C
- Fixed Acquisition
- Always check the datasheet for timing diagram

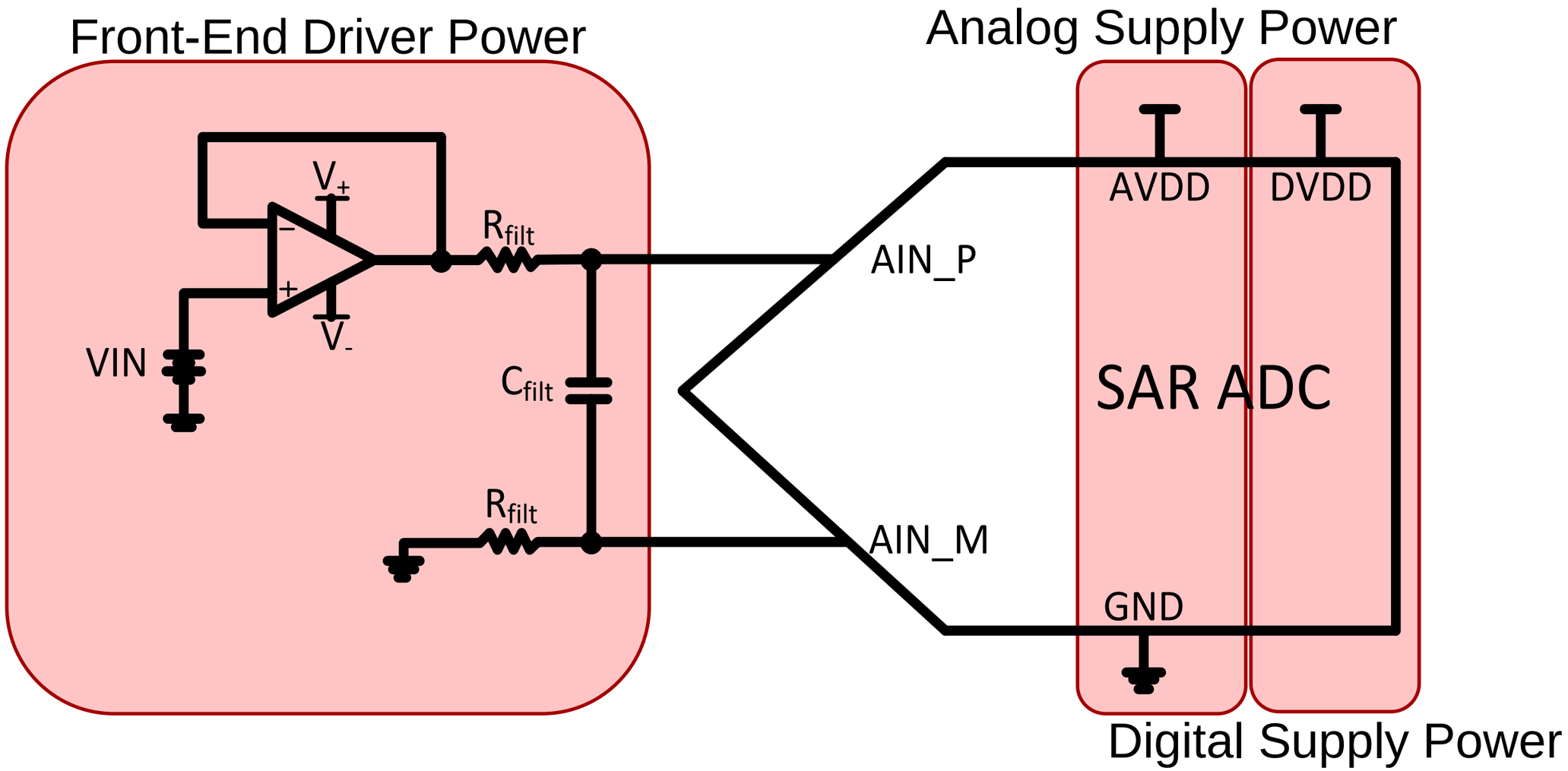


Fixed Acquisition Time

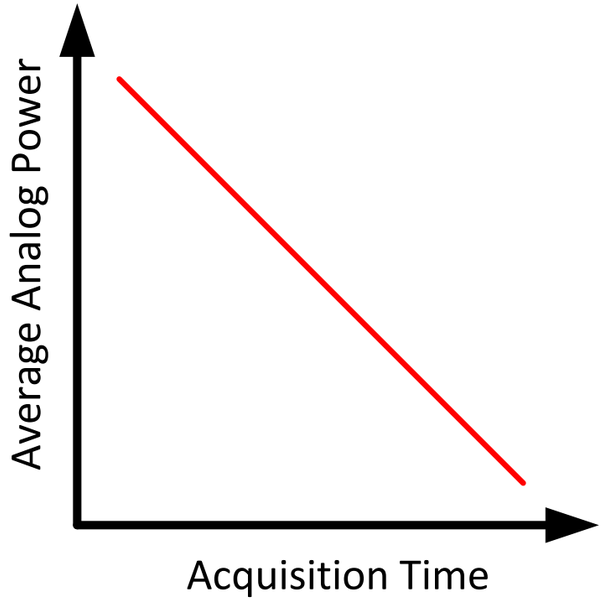
Examples:

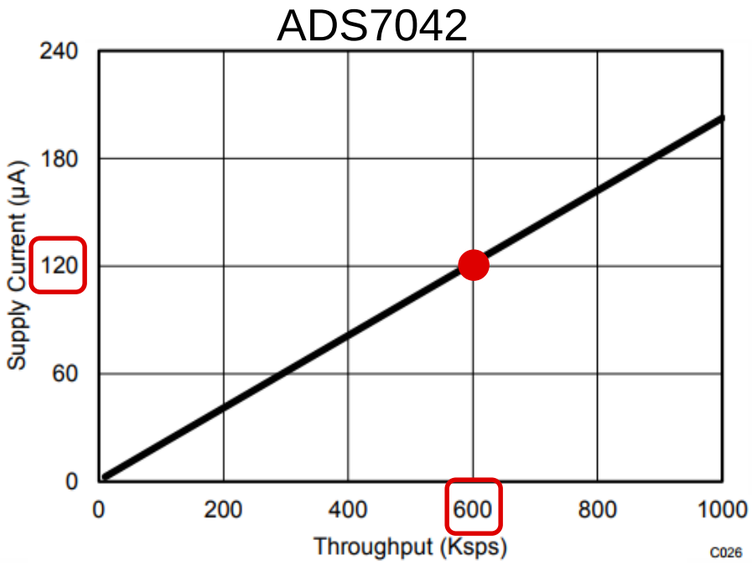
ADS7924 – I2C
ADS8321 – Fixed Acquisition

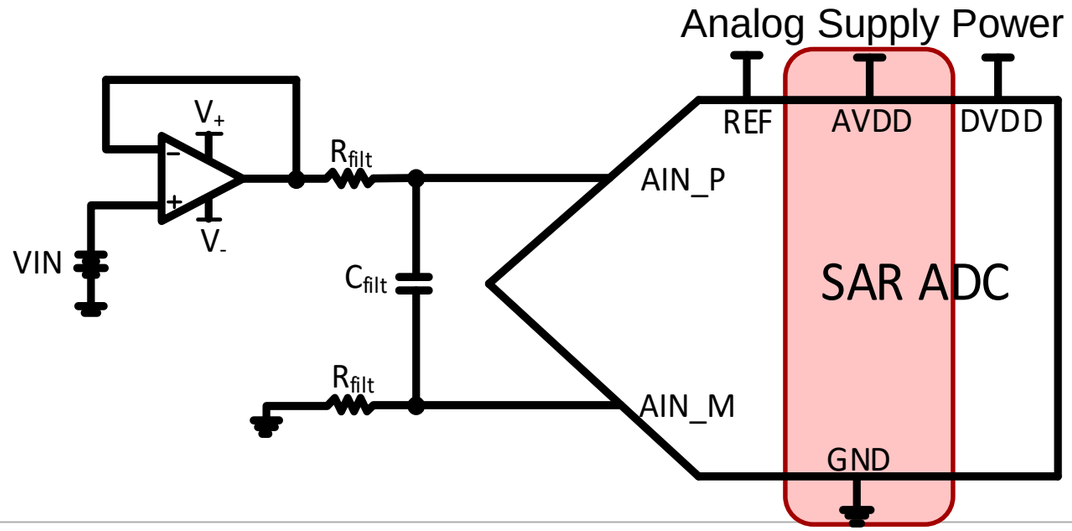
Power of a SAR ADC



Analog Supply (AVDD) Power Consumption







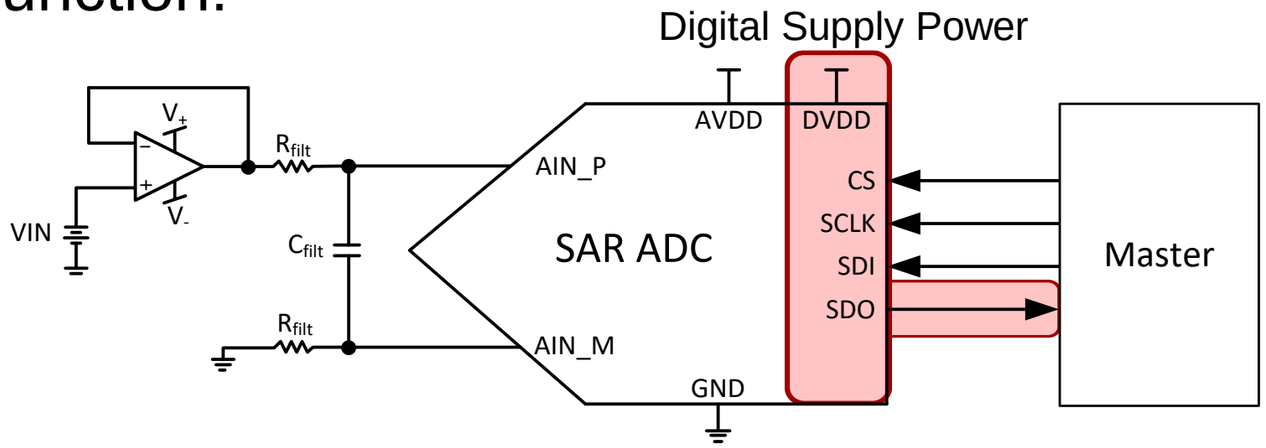
AVDD Example Calculation:

$$P = AVDD \cdot I_{AVDD}$$

$$P = 3.3V \cdot 120\mu A = 396\mu W$$

Digital Supply (DVDD) Power Consumption

- Digital supply power consumption is a function:
  - DVDD Voltage
  - Sampling rate
  - Digital output code
  - Capacitance
    - Trace + Pin + External



$$I_{DVDD} = C_{SDO} \cdot DVDD \cdot f$$

Where

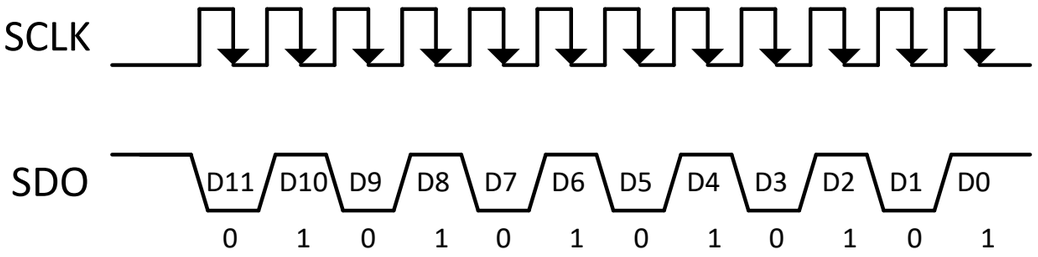
I_{DVDD} *is the DVDD supply current*

C_{SDO} *is the load capacitance on SDO*

$DVDD$ *is the digital supply voltage*

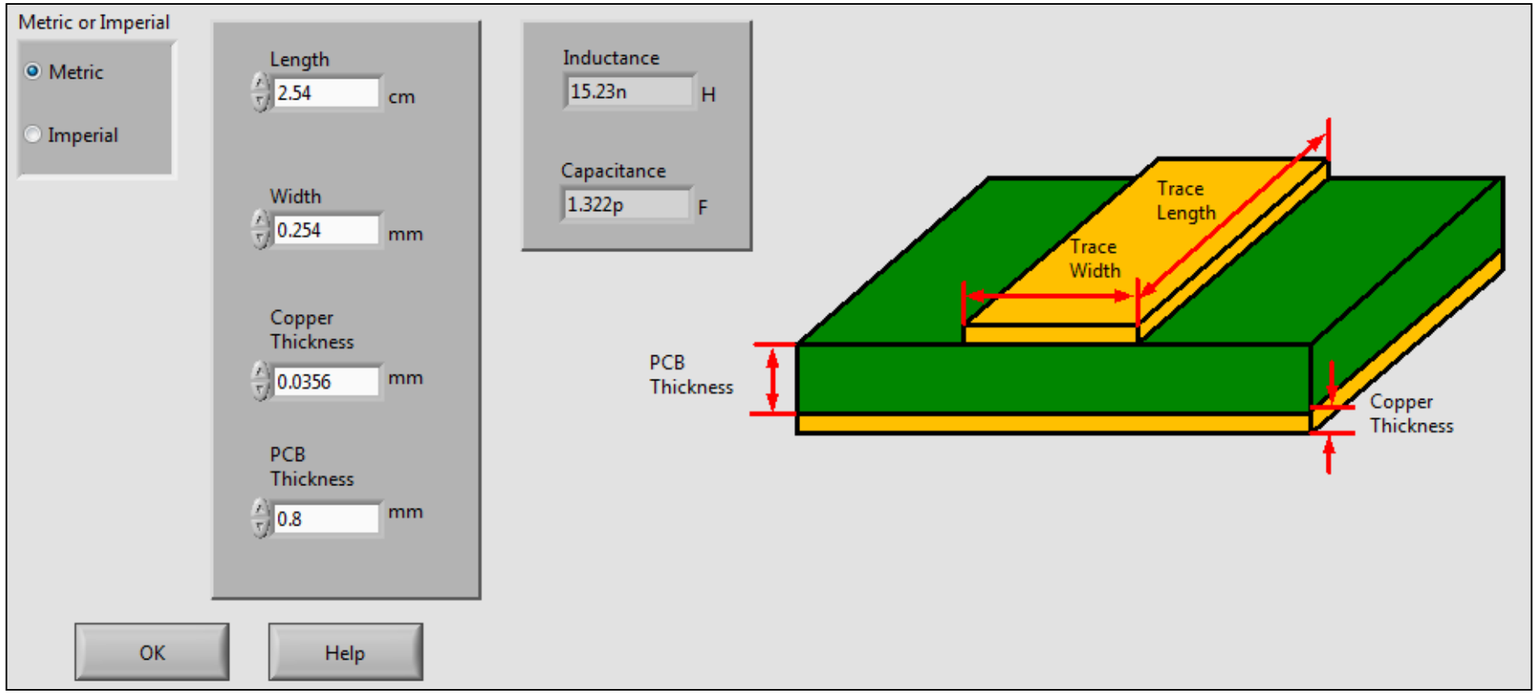
f *is the frequency of transitions on the SDO output*

Maximum SDO Transitions for 12-bit SAR



Minimizing Digital Supply Power Consumption

- Use a lower digital voltage (ex. use 1.8V logic instead of 3.3V logic)
- Run the device at lowest applicable throughput
- Reduce the trace capacitance of SDO line
  - Analog Engineer's Calculator can be used to determine PCB capacitance



ti.com/tool/analog-engineer-calc

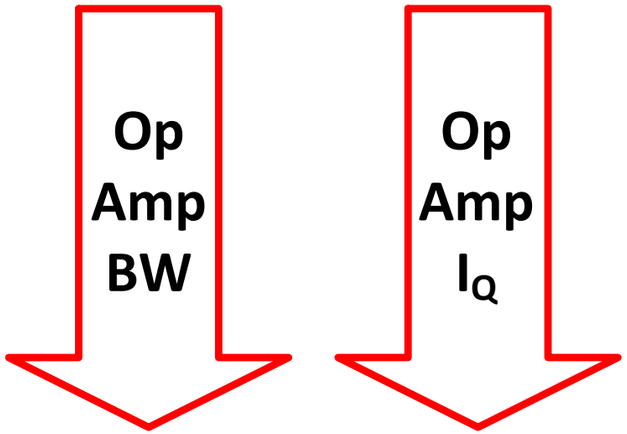
DVDD Supply Power: Example Calculation

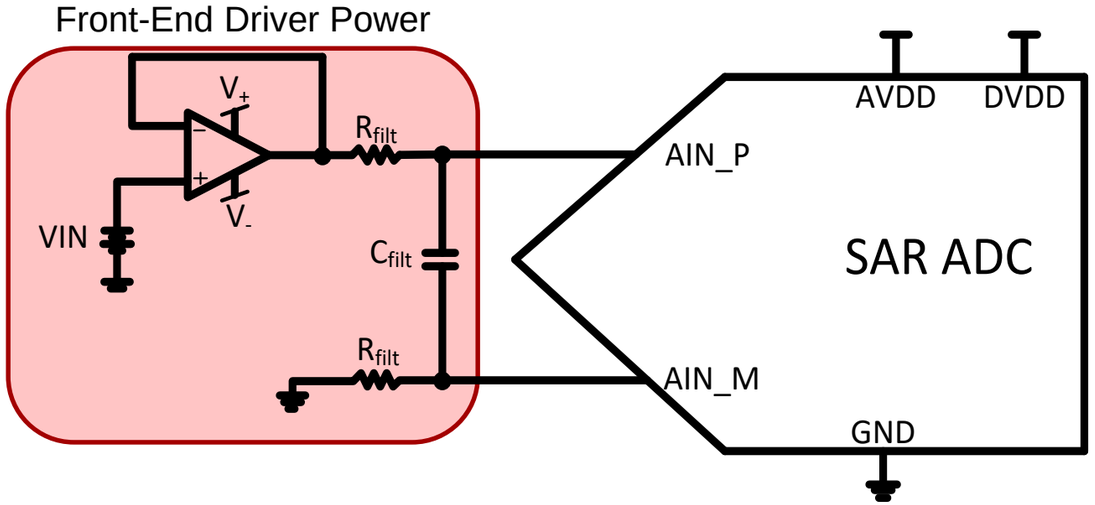
- DVDD Voltage = 3.3V
- Pin Capacitance = 3 pF for both ADC and Master
- SDO Trace Capacitance (2.54 cm long, 0.254 mm wide) = 1.322 pF
- Sampling rate = 1 MSPS
- Frequency of SDO Transitions (12 bit transitions, 1µs cycle time)

$$\boldsymbol{P_{DVDD} = DVDD \cdot I_{DVDD} = \mathrm{DVDD} \cdot (C_{SDO} \cdot DVDD \cdot f)}$$
$$\boldsymbol{= 3.3V \cdot \left((1.322pF + 3pF + 3pF) \cdot 3.3V \cdot \frac{12\ bit}{1\mu s}\right) = 956.8\mu W}$$

Where
P_{DVDD} *is the total DVDD supply power*
I_{DVDD} *is the DVDD supply current*
C_{SDO} *is the load capacitance on SDO*
$DVDD$ *is the digital supply voltage*
f *is the frequency of transitions on the SDO output*

Front-End Driver Power Consumption



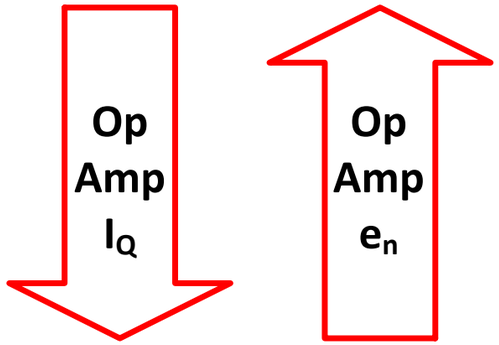


Amplifier	Bandwidth	I_Q
OPA365	50 MHz	5 mA
OPA211	45 MHz	3.6 mA
OPA320	20 MHz	1.45 mA
TLV313	1 MHz	65 µA
LPV811	8 kHz	450 nA

$$\boldsymbol{P = I_Q \cdot ((V_+) - (V_-))}$$

Where
P is the amplifier power consumption
I_Q is opamp quiescent current
V_+ is positive opamp power supply
V_- is negative opamp power supply

Front-End Driver Tradeoffs

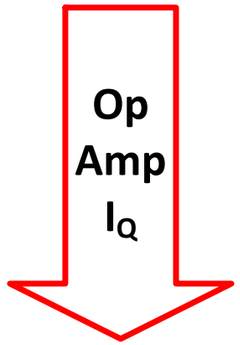


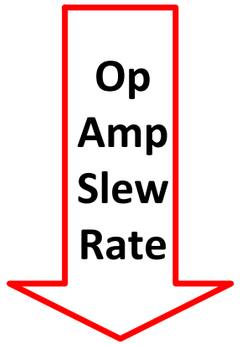
$$e_n \propto 1/\sqrt{I_Q}$$

$Where$

e_n $is\ opamp\ noise\ density$

I_Q $is\ opamp\ quiescent\ current$





- Large feedback resistors will act as a small load and result in less power consumption but add more noise

- A good rule of thumb is to keep the Op Amp noise dominant

$$e_{n_{opa}} \geq 3 \cdot e_{n_{res}}$$

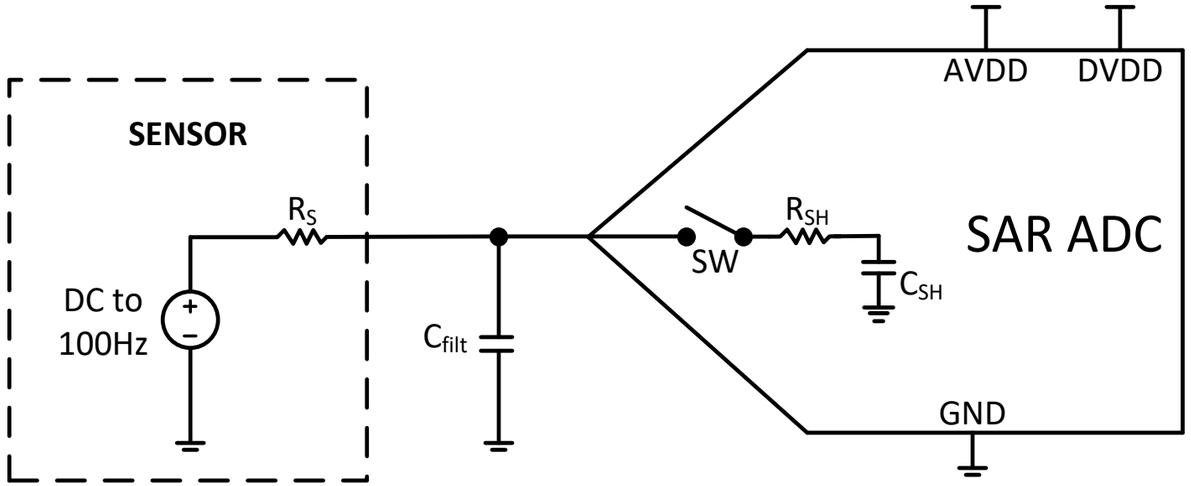
$Where$

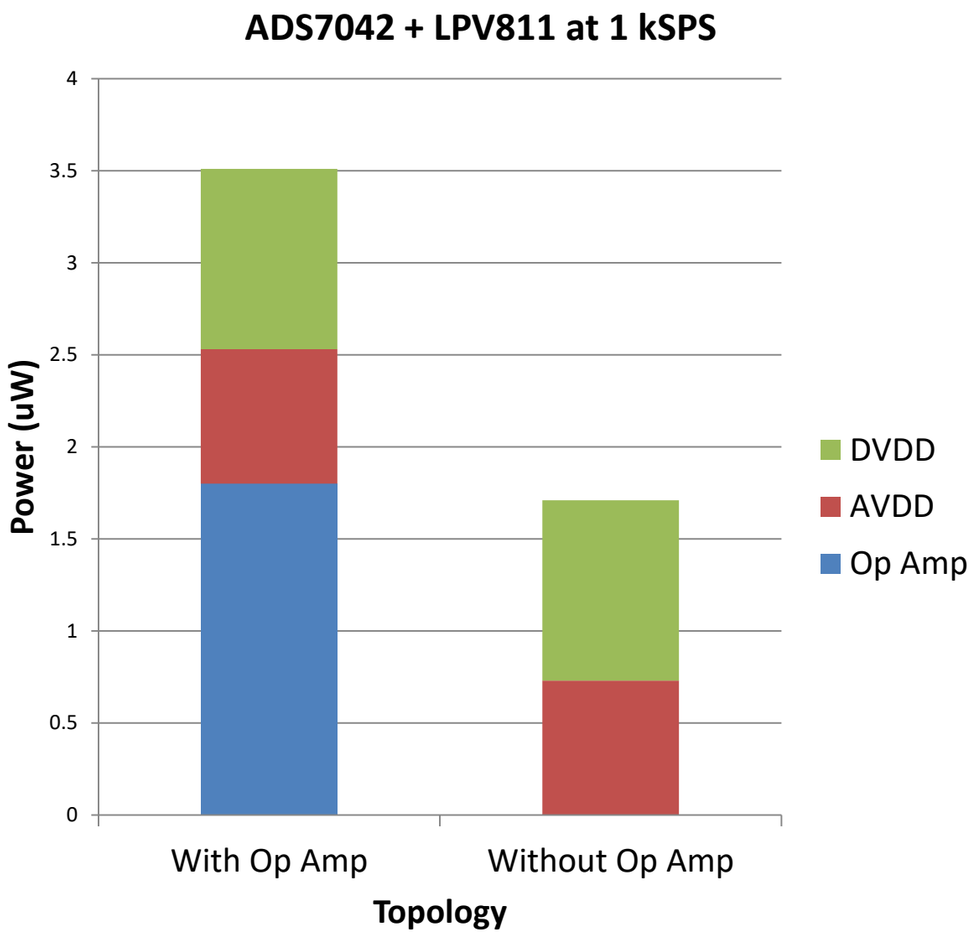
$e_{n_{opa}}$ $is\ opamp\ noise\ density$

$e_{n_{res}}$ $is\ resistor\ noise\ density$

Driving a SAR ADC without a Driver Amplifier

- Low frequency voltage inputs can be connected directly to the SAR ADC
- Applicable for low sampling rates (<20 kSPS)



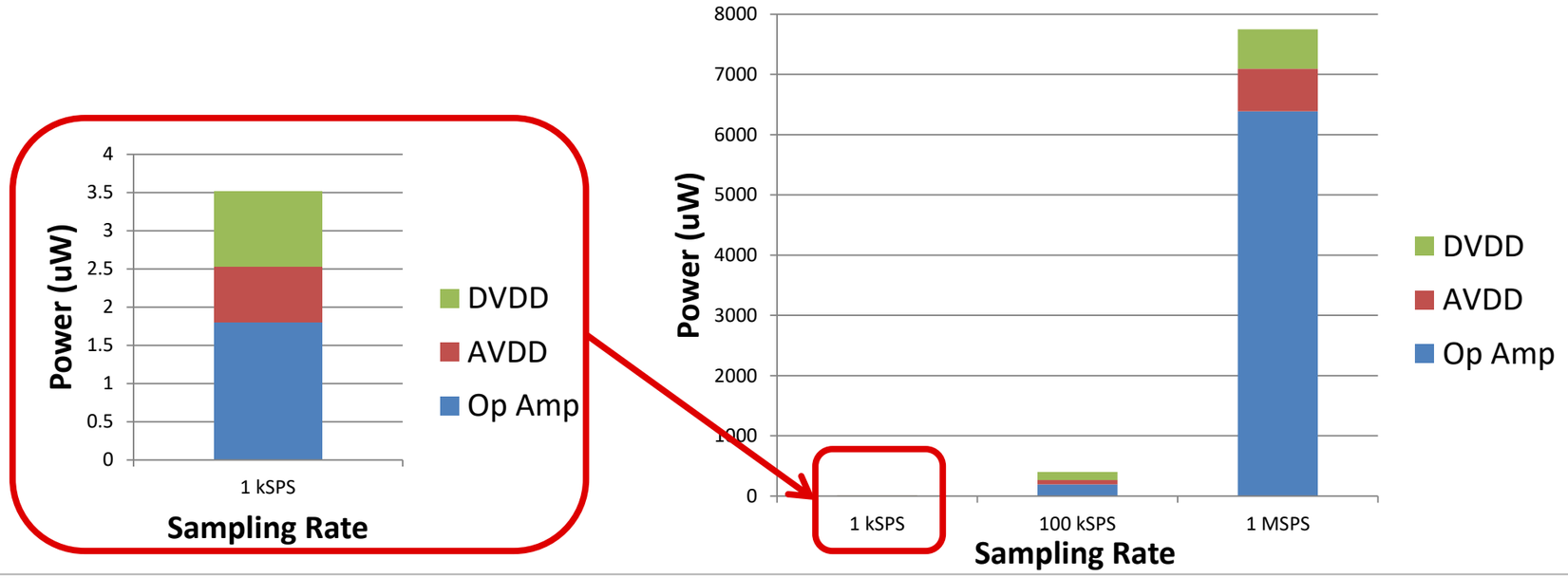


ti.com/lit/pdf/sboa206

Power Scaling Example

ADS7042
AVDD = 3.3V, DVDD = 3.3V, Op Amp Supply = 4.5V

Power Level	Amplifier	Sampling Rate	Measured Amplifier Power	Measured Analog Power	Measured Digital Power	Total System Power
Low	LPV811	1 kSPS	1.8 µW	0.737 µW	0.988 µW	3.5 µW
Medium	TLV313	100 kSPS	192.7 µW	73.1 µW	135.8 µW	401.7 µW
High	OPA320	1 MSPS	6386 µW	708.3 µW	655.2 µW	7750 µW



Thanks for your time!
Please try the quiz.

SAR ADC Power Scaling

TIPL 4601

TI Precision Labs – ADCs

Created by Peggy Liska

SAR ADC Power Scaling

1. (T/F) Most of the power is consumed by the SAR ADC during the acquisition phase.
   a. True
   b. False

2. You can always reduce the overall power consumption of a SAR ADC by _____.
   a. Decreasing the acquisition time
   b. Increasing the acquisition time
   c. Decreasing the SCLK speed
   d. Increasing the SCLK speed

SAR ADC Power Scaling

3. Which of the following is NOT a way to reduce digital supply (DVDD) power consumption?
   a. Decrease the digital logic voltage level
   b. Increase the throughput of the ADC
   c. Reduce the trace capacitance of the SDI line
   d. Both a & c
   e. Both b & c

4. (T/F) Large feedback resistors on the front-end driver reduce power consumption but add noise.
   a. True
   b. False

SAR ADC Power Scaling

5. Calculate the digital supply power consumption using the following values:

   HINT: Use the Analog Engineer's Calculator.

- DVDD Voltage = 1.8 V
- SDO Trace Dimensions = 1000 mils long, 10 mils wide
- Copper Thickness = 1 oz
- PCB Thickness = 31 mils
- Sampling rate = 1 MSPS
- ADC Resolution = 12-bit

Solutions

SAR ADC Power Scaling

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- ADC Resolution = 12-bit

$$P = DVDD \cdot (C \cdot DVDD \cdot f)$$

$$P = 1.8V \cdot \left(1.33pF \cdot 1.8V \cdot \frac{12}{1\mu s}\right)$$

$$P = 51.7\mu W$$

L = 15.14nH
C = 1.328pF