Jitter vs SNR for ADCs

TIPL 4704

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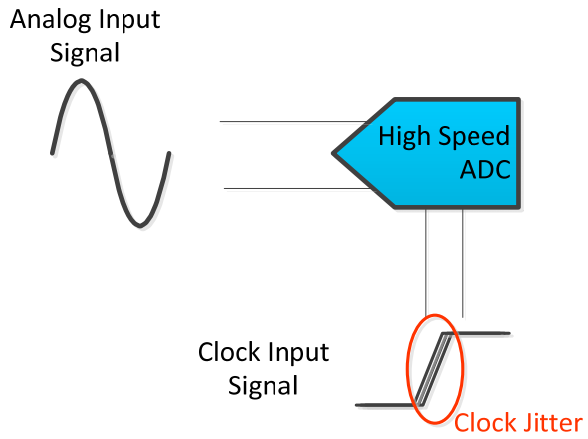
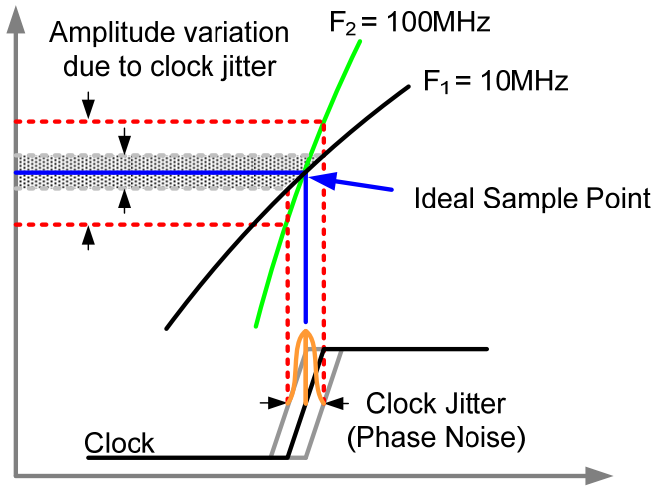
Sampling Theory

High-speed ADC uses external clock input to sample the analog input signal.



Higher input frequencies are more susceptible to timing uncertainty

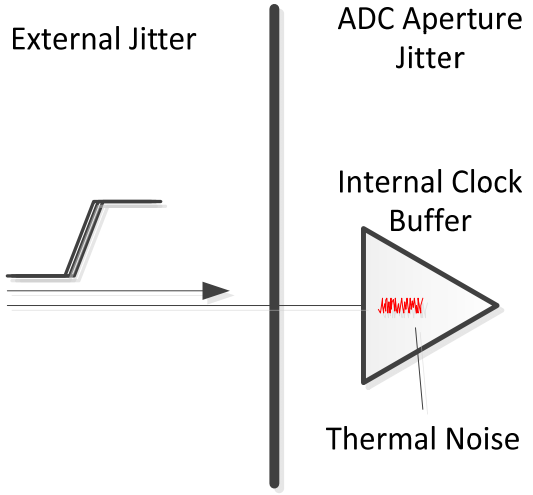


Sampling Clock Jitter

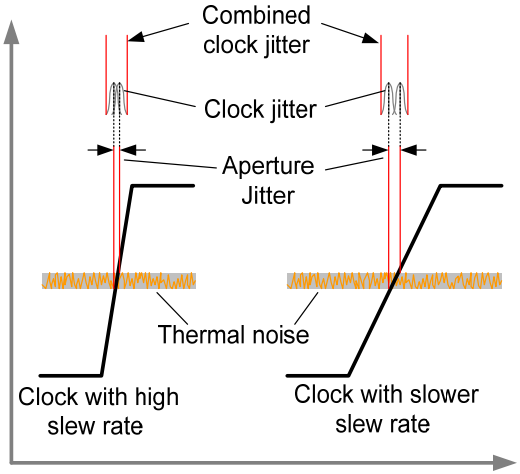
Sampling jitter is combination of:

- External jitter
- Internal ADC aperture jitter

$$T_{Jitter} = \sqrt{\left(T_{Jitter,ext}\right)^2 + \left(T_{Aperture\_ADC}\right)^2}$$



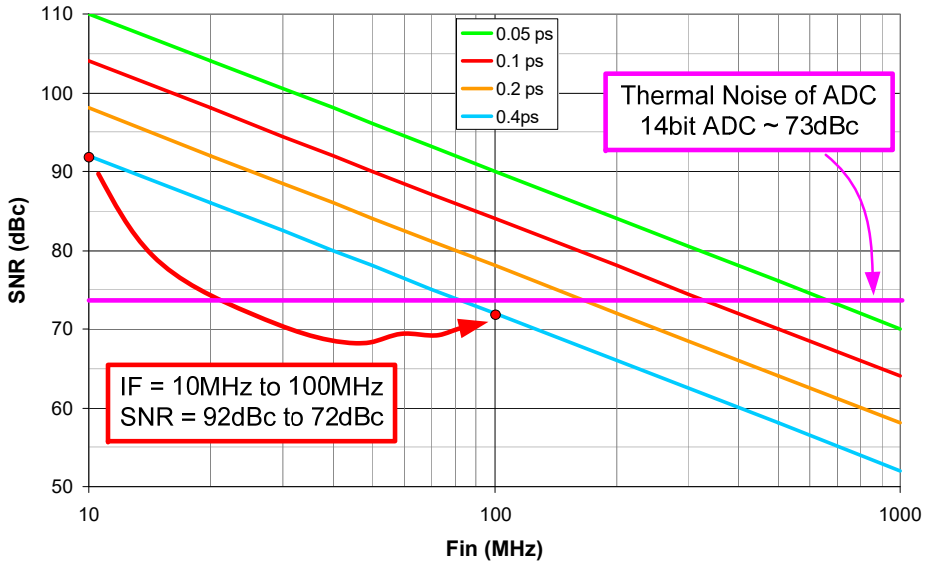
ADC Aperture Jitter
Clock amplitude dependent



SNR Impact of Jitter (1)

The ADC SNR degradation due to jitter (external + internal ADC aperture) can be calculated as:

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter})$$

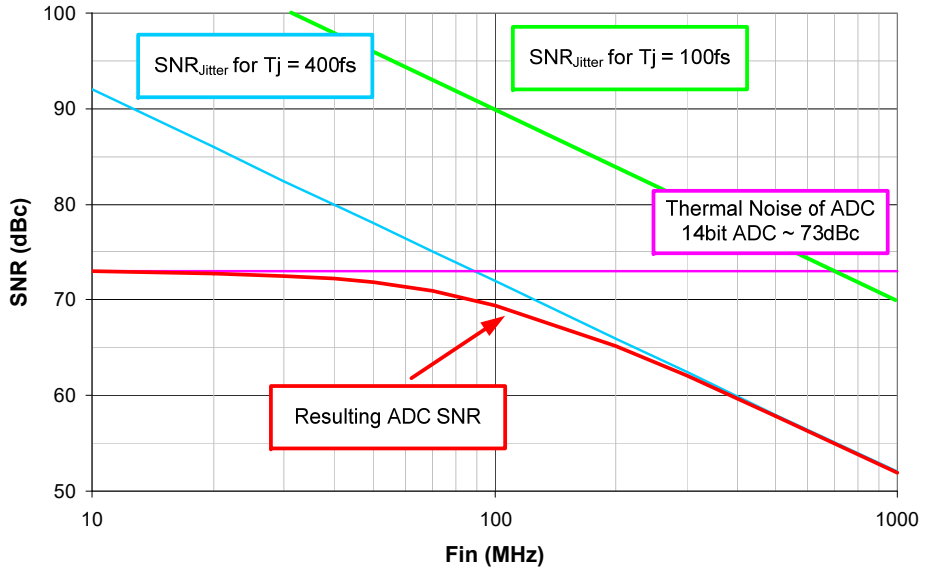


SNR Impact of Jitter (2)

The ADC noise floor (SNR) is basically set by 3 different contributors:

1. ADC Quantization Noise
2. ADC Thermal Noise
3. Jitter degradation

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{-\frac{SNR_{Quantizatoin\ \ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ \ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2}$$

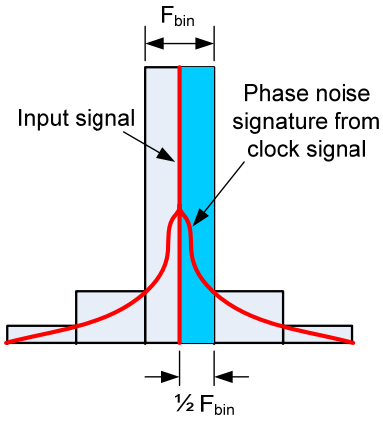


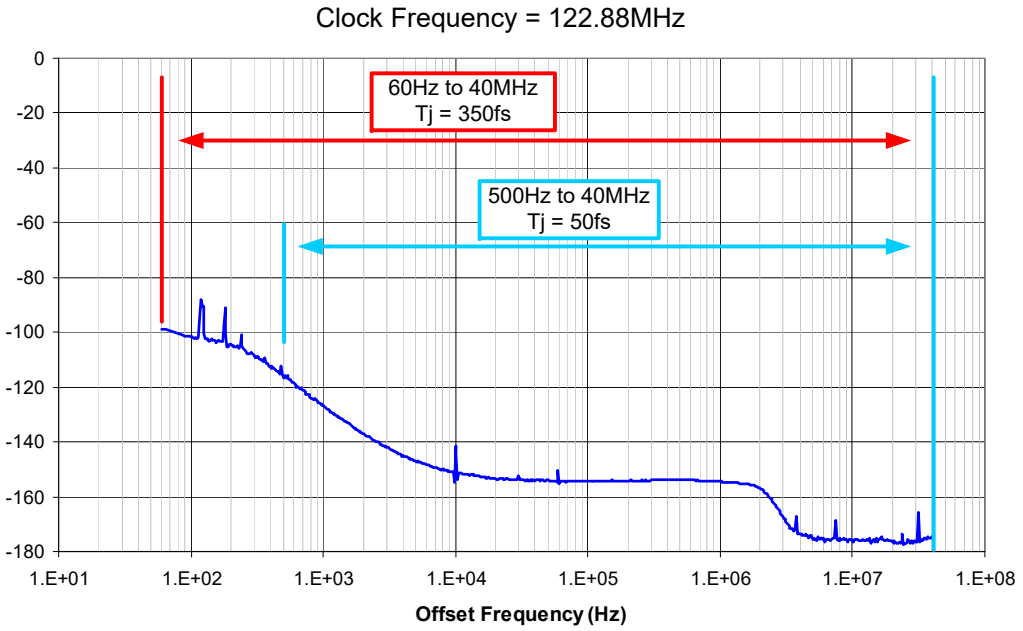
Calculating the jitter magnitude (1)

The clock jitter is calculated by integrating the phase noise of the clock signal.

Lower integration limit:

Typically application specific.



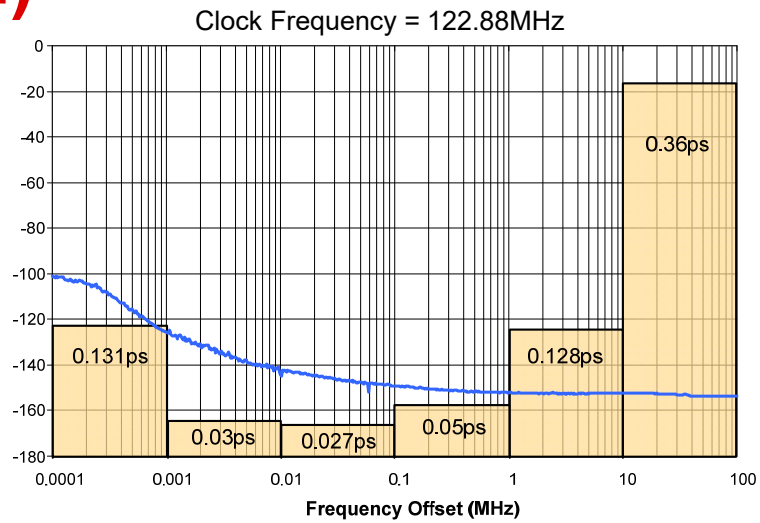


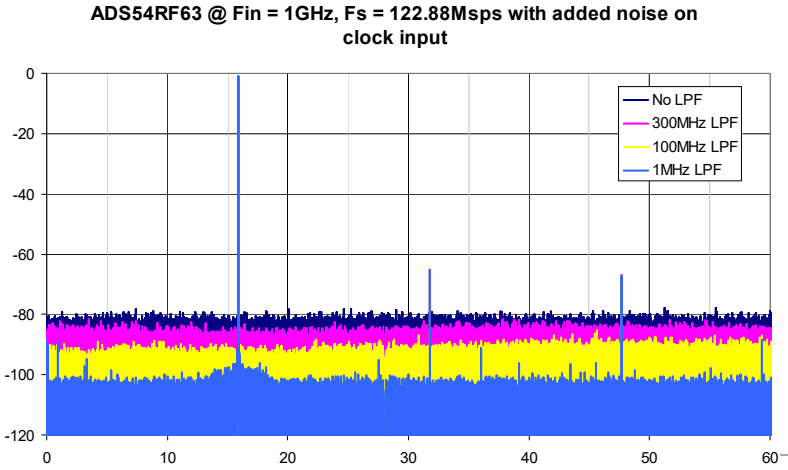
Calculating the jitter magnitude (2)

Upper integration limit:

The upper limit is set by factors like

- Clock filter bandwidth
- ADC clock input bandwidth
- ADC sampling rate

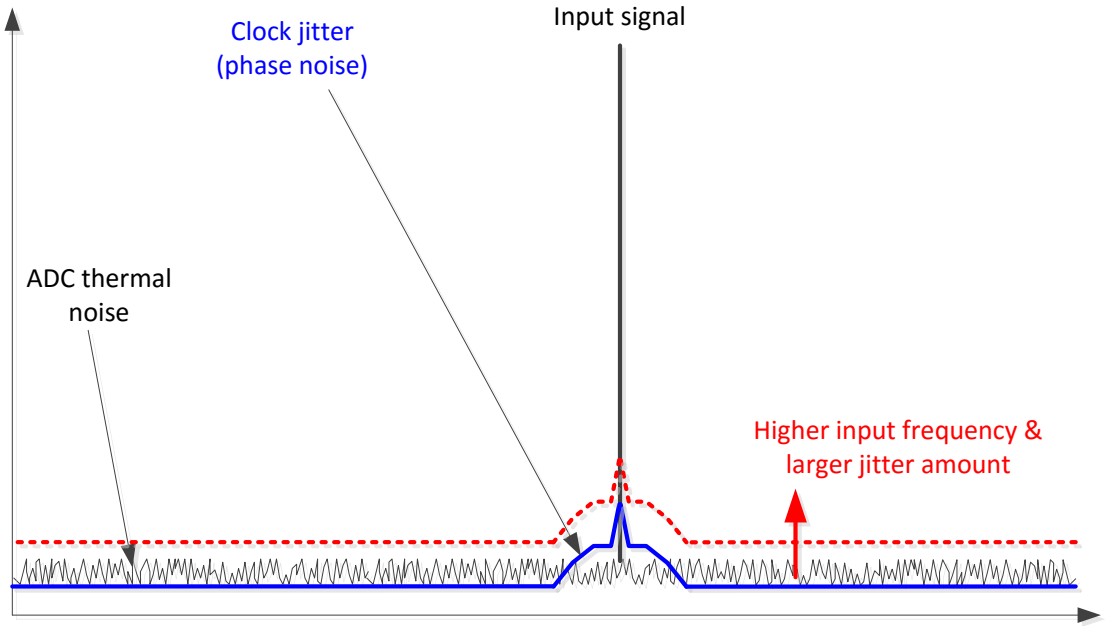




SNR impact in frequency domain

During the sampling process the clock signal phase noise gets added to the input signal.

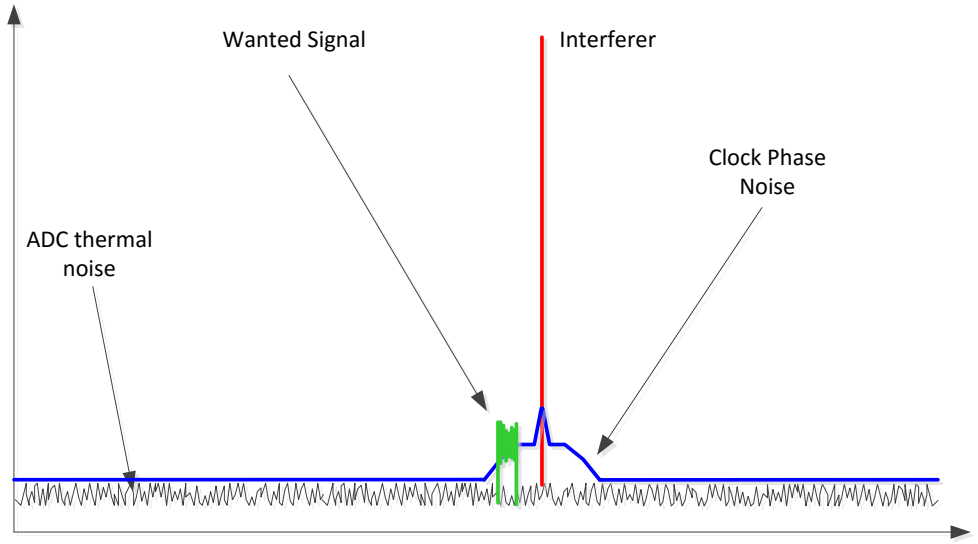
- The higher the input signal the larger the phase noise amplitude (scales by 20log (F_{IN}/F_S))
- The larger (worse) the clock phase noise, the worse the ADC noise floor degradation



Why is clock jitter/phase noise so critical?

A typical receiver use case is performance in a ‘blocking condition’

- The receiver needs to detect a small wanted signal
- There is a large in-band interferer that can’t be filtered out.



How to maximize the jitter performance?

There are several steps the system designer can take in order to maximize the SNR performance of a given ADC:

- Use low jitter/phase noise clock source
- Use bandpass filter with low insertion loss to limit broad band noise degradation
- Ensure clock amplitude is sufficient and doesn’t degrade ADC aperture jitter