LDO Architecture Review

How different LDO architectures influence performance

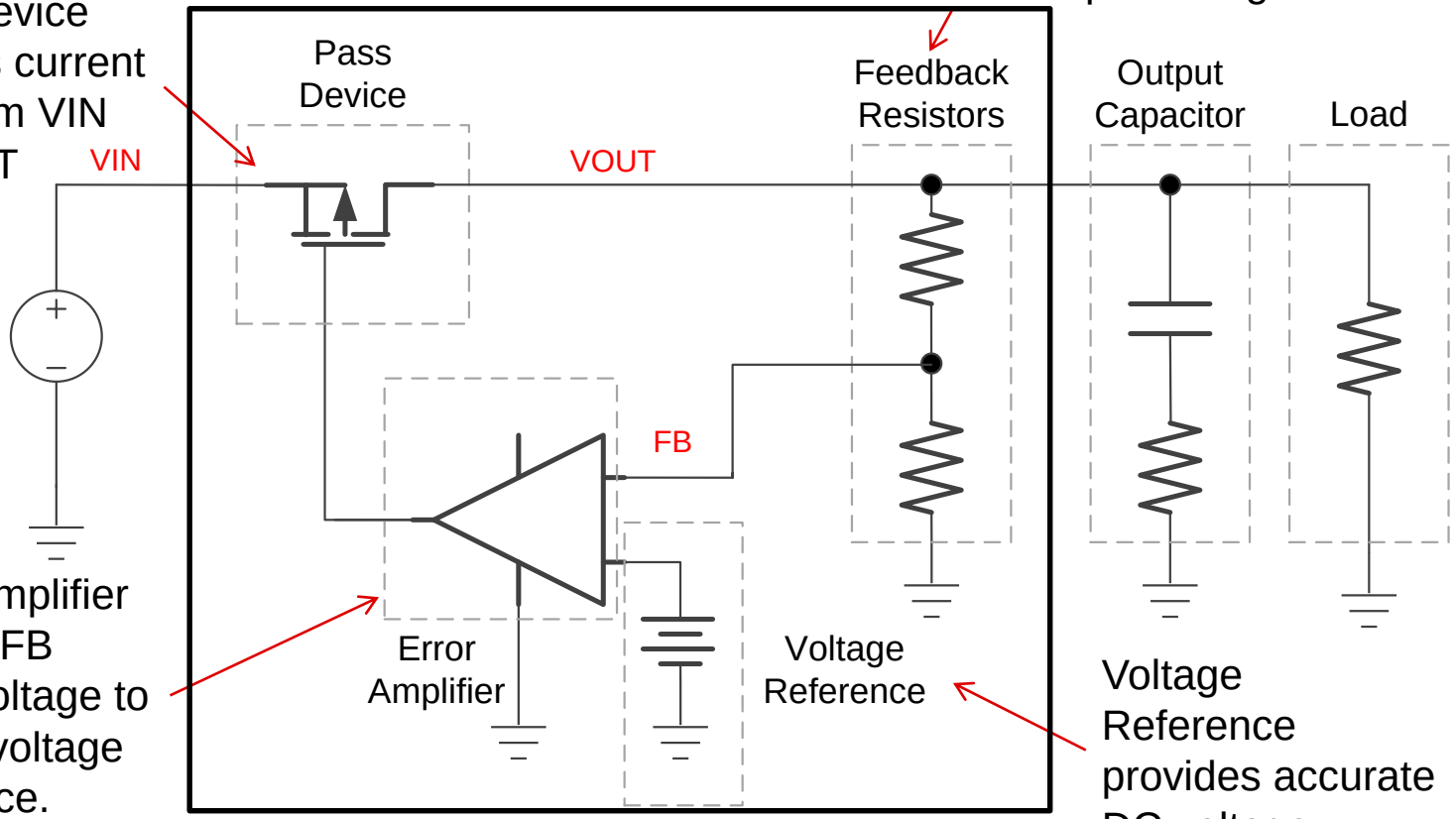
Overview

- General Block Diagram Review
- Small Signal Model
- LDO Pass Devices
  - PMOS
  - NMOS
  - BJT
- LDO Performance
  - Dropout
  - Noise
  - PSRR
  - Startup

Standard LDO Architecture

Feedback Resistors determine output voltage

Pass Device controls current flow from VIN to VOUT



Error Amplifier forces FB node voltage to match voltage reference.

Voltage Reference provides accurate DC voltage.

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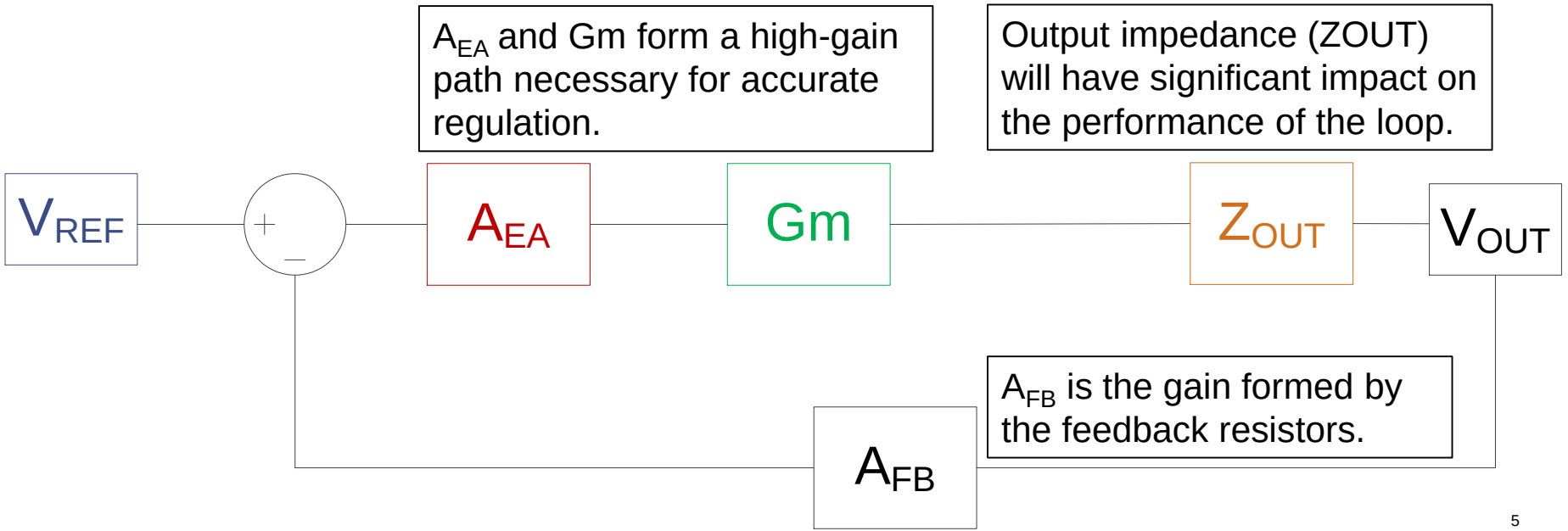
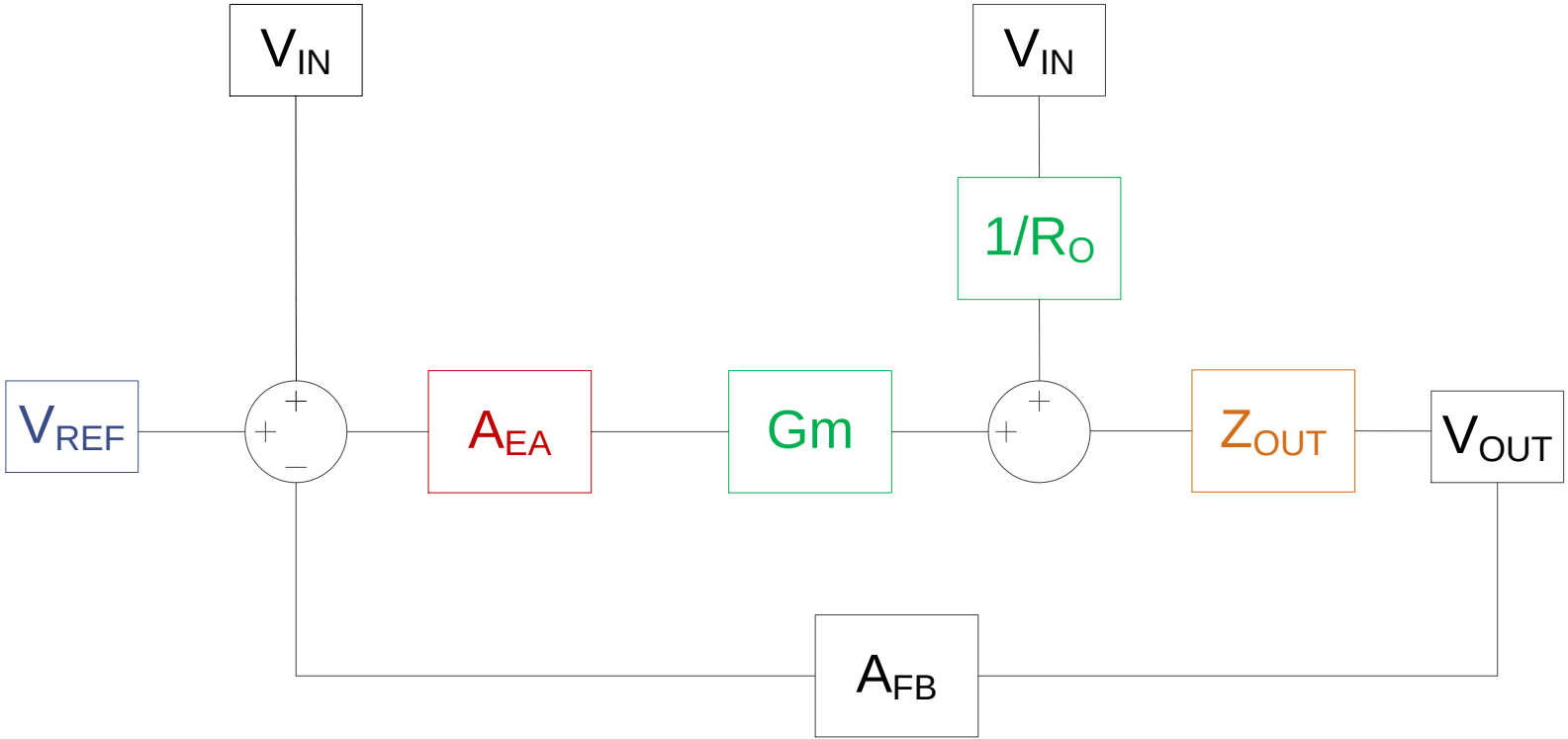
Simplified AC Model

- This system block diagram represents a simplified small-signal AC model of a typical LDO.
- Ideally, V_{IN} has no impact on the loop.

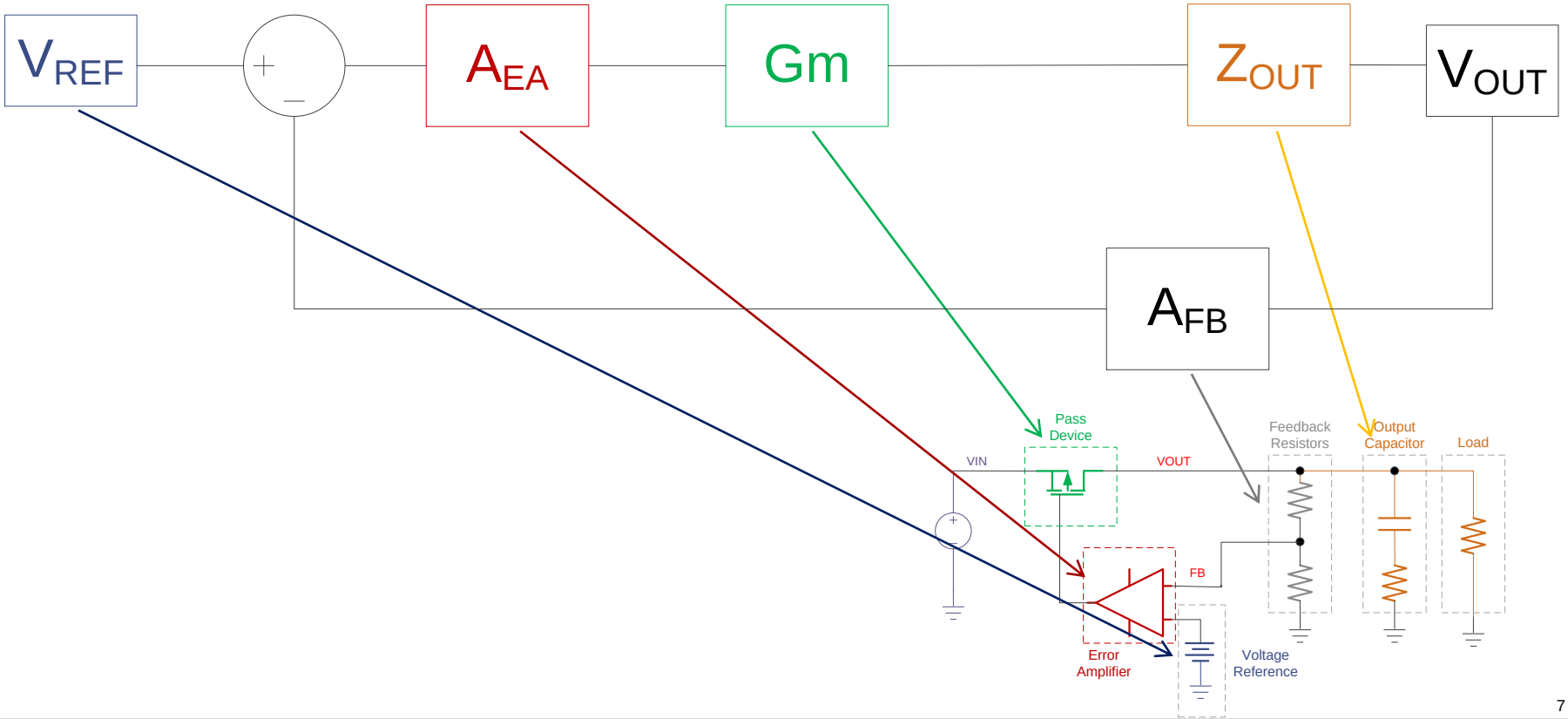


Simplified AC Model With Input Coupling

- In the real world, V_{IN} will couple into the loop and degrade loop performance.



Simplified AC Model



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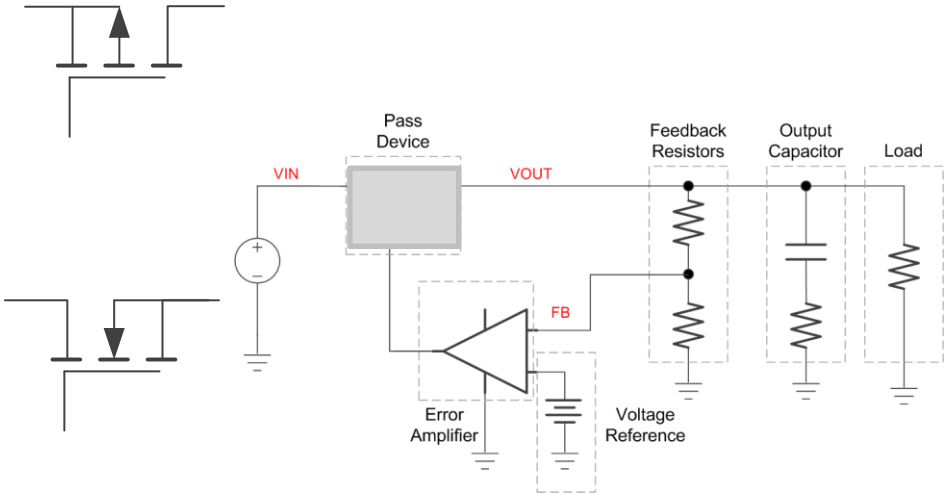
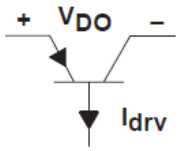
MOSFET Pass Devices

- P-Type MOS (PMOS):
  - Very common. Low VDO, low Iq, no charge pump or bias rail requirements.
- N-Type MOS (NMOS):
  - Lowest VDO possible, however, error amplifier needs higher voltage than VIN to drive it.
- PNP:
  - Can achieve higher voltage depending on process capability.



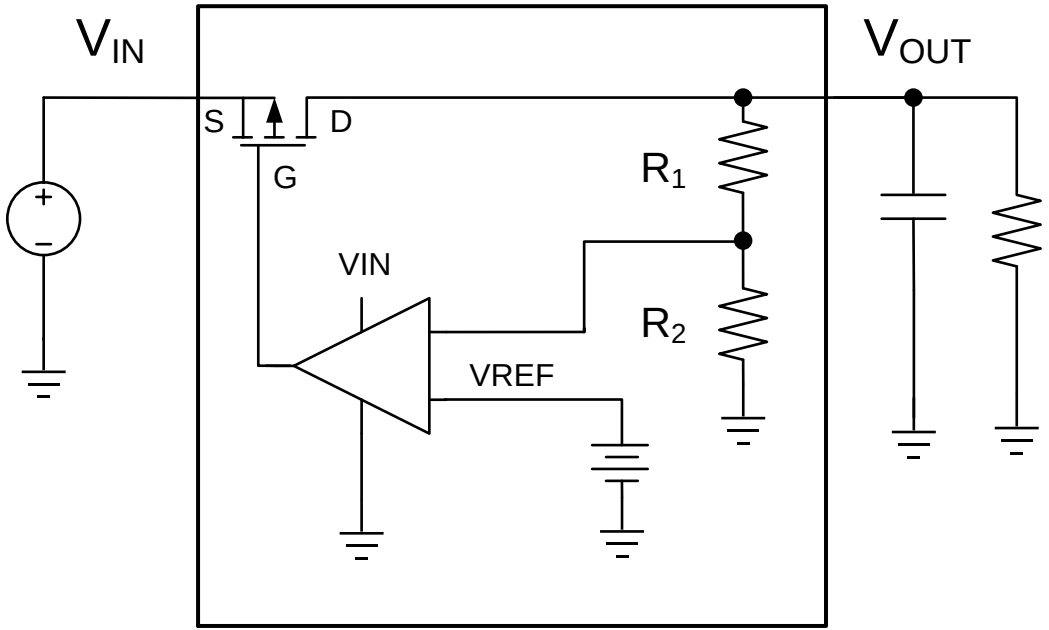


(c) PNP

PMOS Pass Device

PMOS Advantages:
- Simple
- Lowest cost structure

PMOS Disadvantages:
- R_{DSON} is higher vs. NMOS
- Common-drain structure gives higher output impedance



NMOS Pass Device

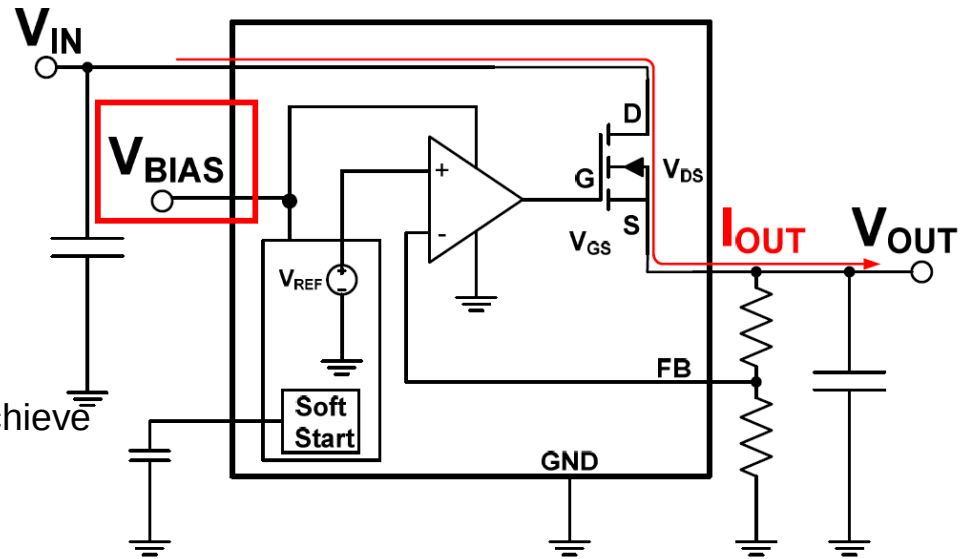
NMOS Advantages:

- Better $R_{DS(on)}$ per unit area
  - smaller die size

- Common Drain Structure gives low output impedance
  - Wide range of stability vs C_{OUT}
  - Low output impedance

Disadvantages:

- Needs a charge pump or external bias rail to achieve low $\mathbf{V_{IN} - V_{OUT}}$



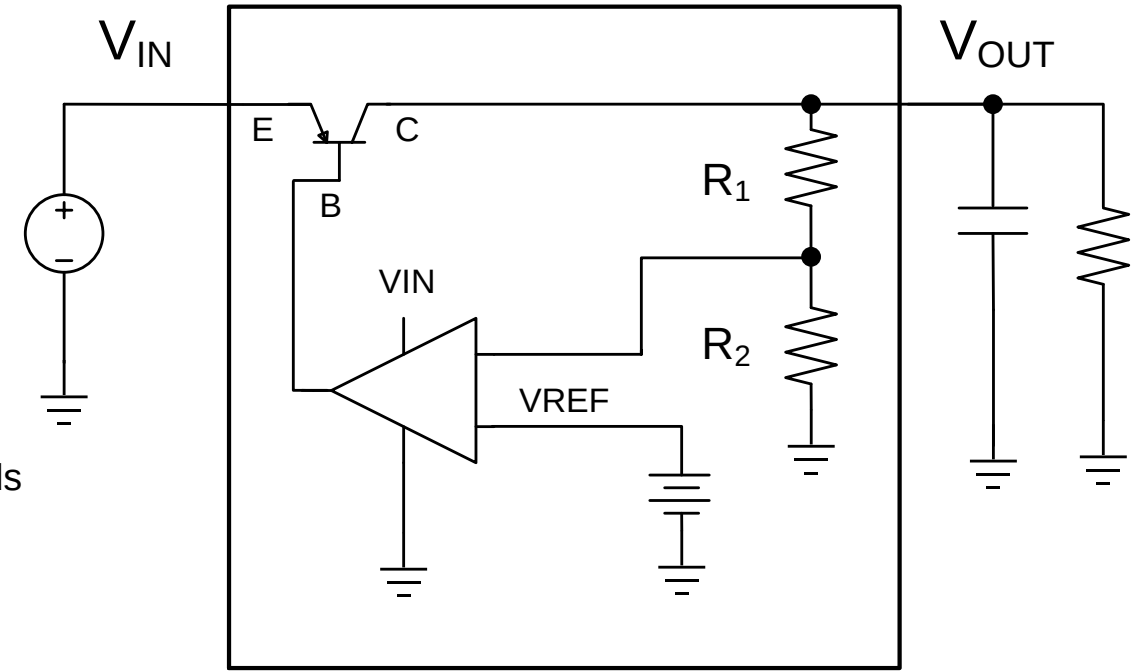
PNP Pass Device

PNP Advantages:

- Can achieve higher VIN voltages
- Error amplifier design in bipolar process can achieve low noise

Disadvantages:

- Difficult to design for low Iq
- Dropout can be higher for light loads



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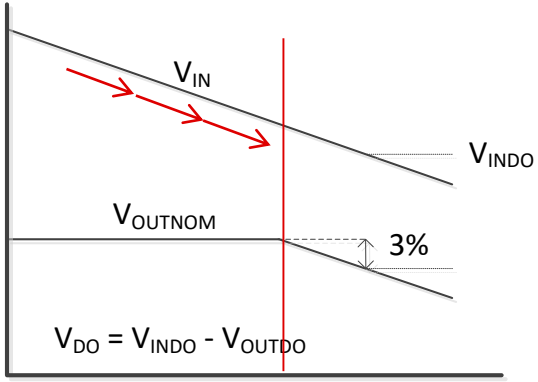
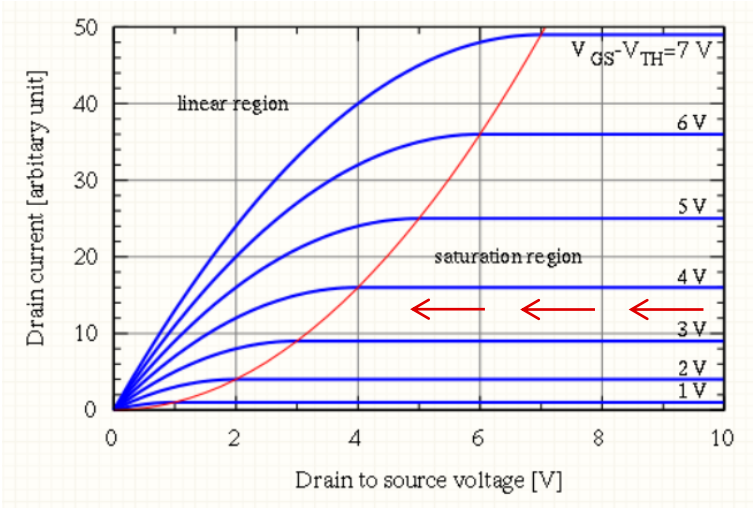
Dropout

- Dropout, or VDO, is the minimum voltage necessary from VIN to VOUT to maintain regulation.
- PSRR, noise, load regulation and transient response are all significantly worse when device is in dropout.
- Dropout -> VDO = $V_{IN} – V_{OUT}$ when V_{OUT} drops from nominal regulation voltage





- For a MOSFET pass element, pass device enters linear region when the LDO goes into dropout.
- In dropout, VDO is proportional to load current

Dropout Dependancies For MOS

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

TLV73318
VDO vs. IOUT

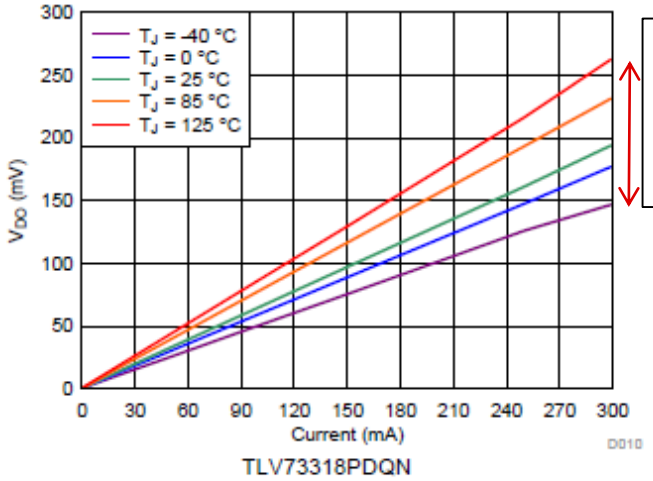


Figure 10. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

Dropout vs. Temperature increases because mobility of pass device is reduced.

Dropout vs. VOUT decreases because V_{GS} voltage is higher.

TLV73333
VDO vs. IOUT

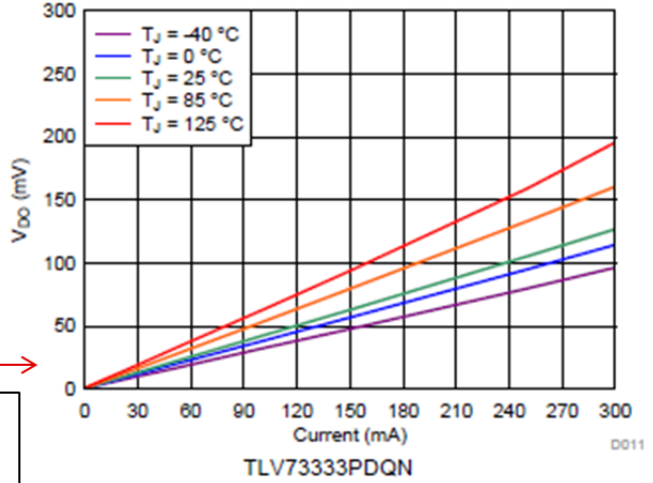


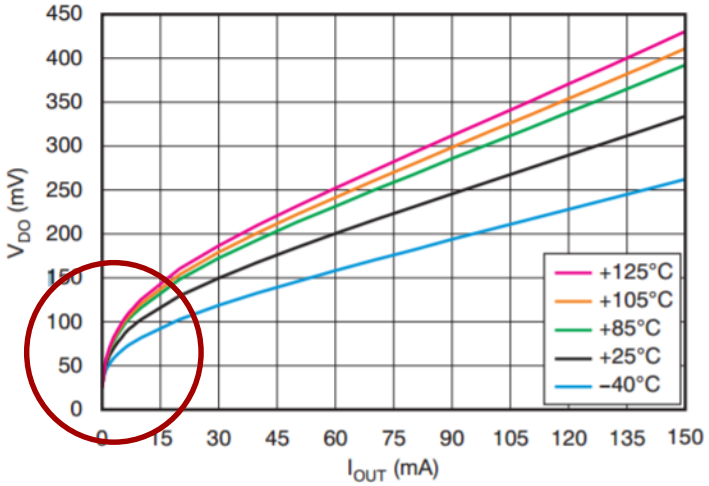
Figure 12. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

Dropout For PNP

- For a PNP pass device, when V_{CE} is low, the device is in “saturation”. In this state, the voltage is not directly proportional to the output current.

- Many devices, such as the TPS7A49, use an anti-saturation circuit to improve recovery time out of saturation.

TPS7A49
VDO vs. IOUT



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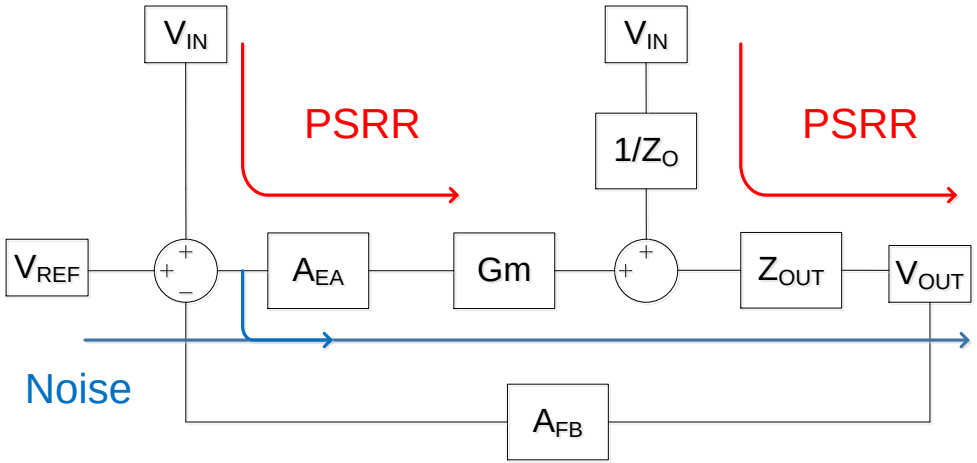
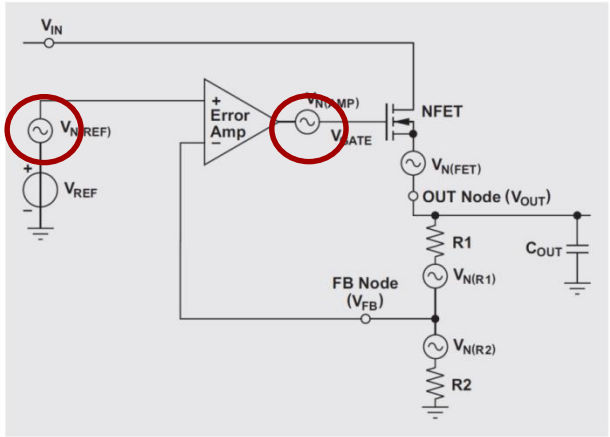
Intrinsic Noise VS Input Signal Coupling

- LDO output voltage disturbances that are not load-related are composed of **Input Signal Coupling** that is coupled through the pass device, as well as **Intrinsic Noise** that comes from primarily the reference and error amplifier.
  - **Power Supply Rejection Ratio** (PSRR) determines how much noise from the input couples into the output.
  - **Intrinsic Noise (**or simply **“Noise”)** is generated primarily from the internal reference and error amplifier.



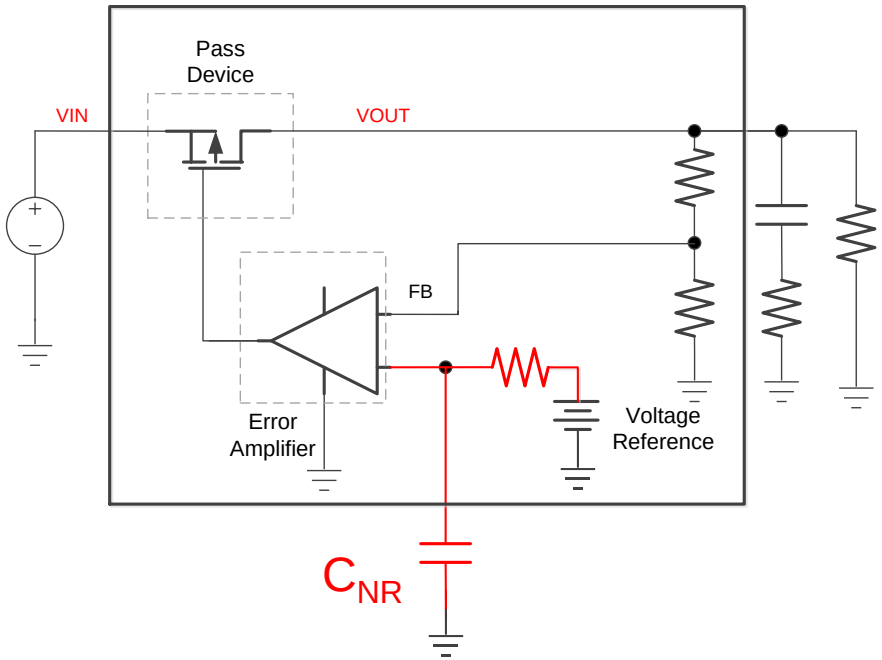
LDO Noise, Dominant Noise Sources

- Noise is combined into total output noise for the noise specification.
- Typically noise is specified in total RMS noise from 10 Hz to 100 kHz
- Dominant noise sources are the **voltage reference** and **error amplifier**.

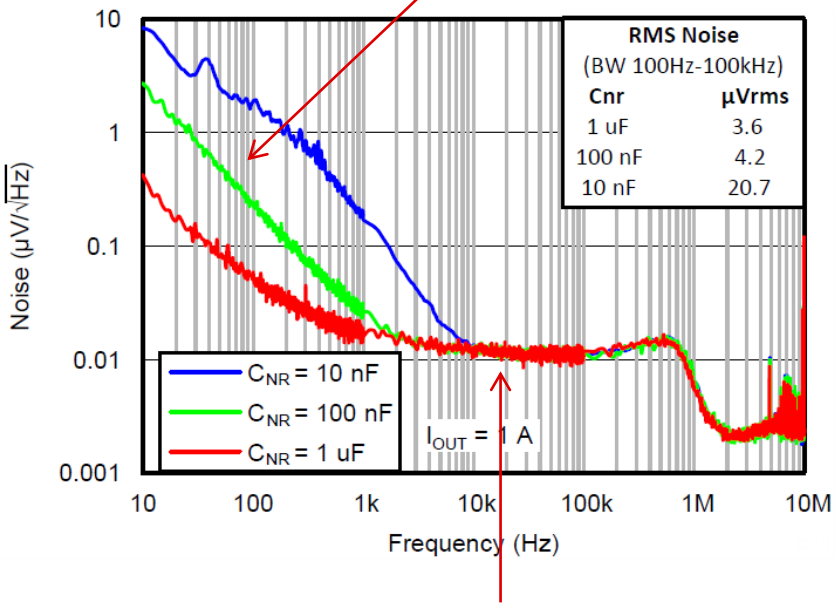


Noise Reduction (NR) with Bandgap RC Filter

- The Reference Voltage noise can be filtered with an RC filter. This can be external or internal. On external devices, add a capacitor to the NR pin.



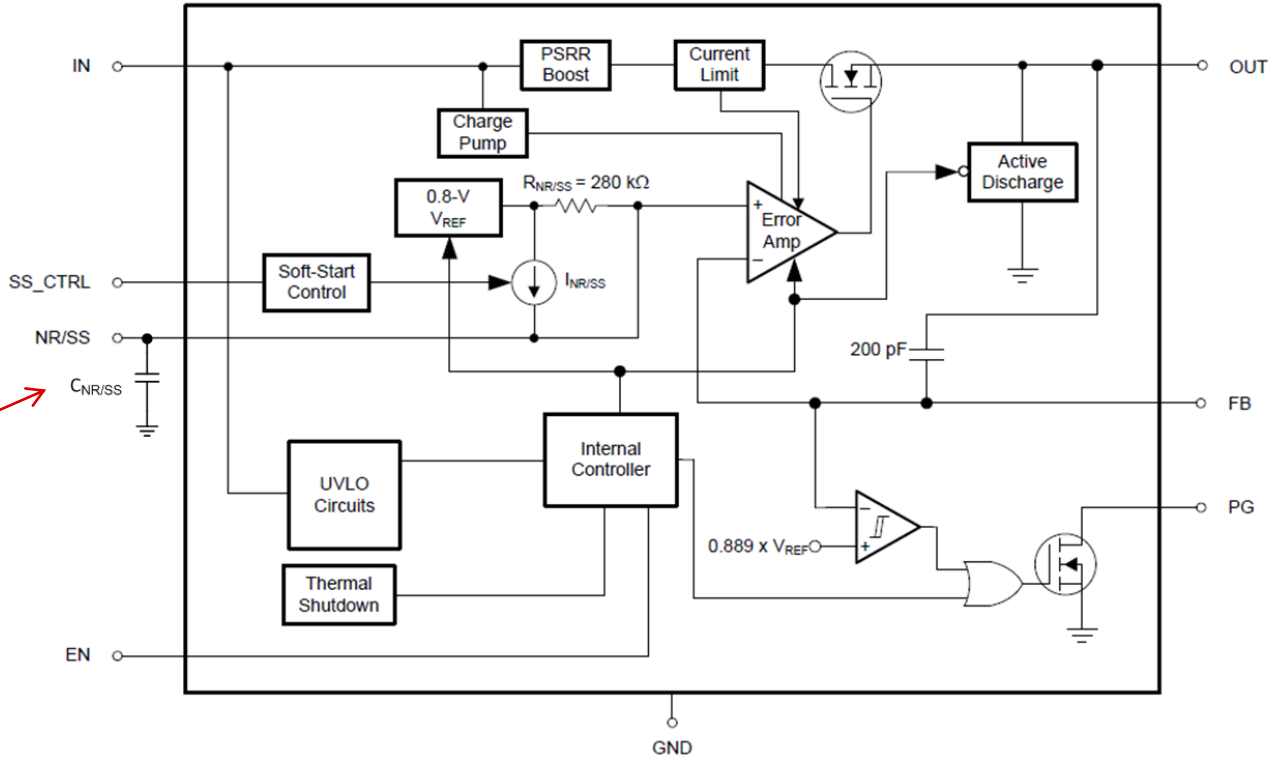
Increasing C_{NR} pushes noise lower.



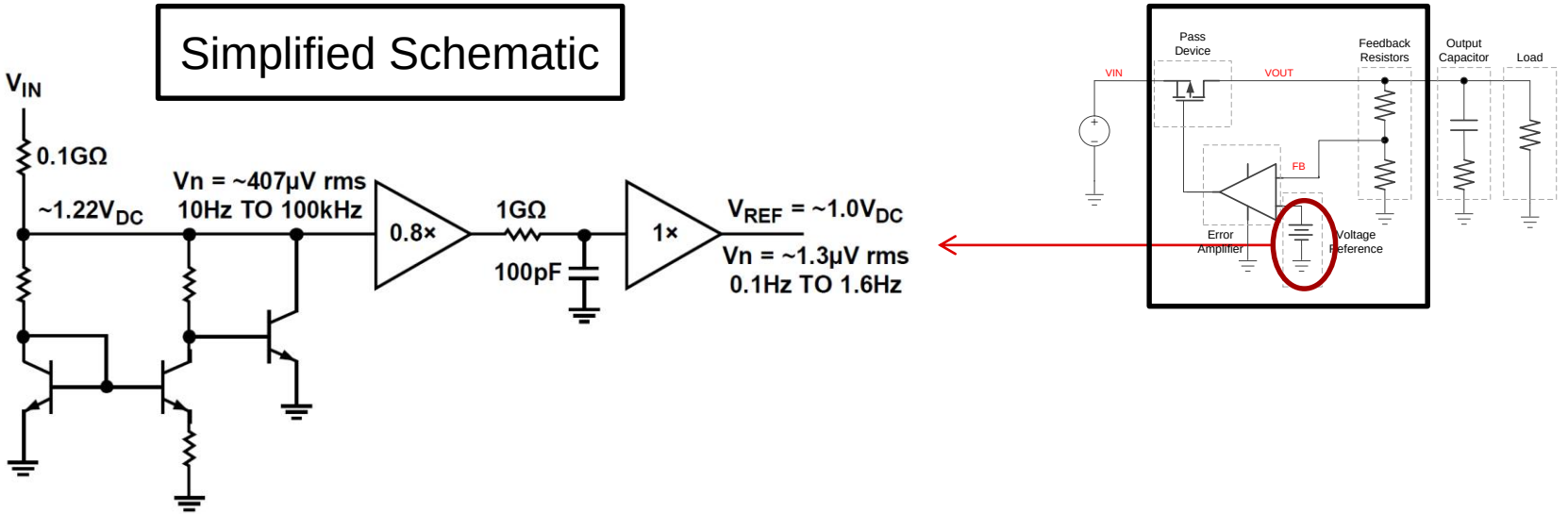
However, noise in this region is limited by thermal noise from the error amplifier.

Low Noise C_{NR} and Error Amplifier Example – TPS7A91

C_{NR} reduces reference voltage noise



Noise Reduction (NR) with Internal Bandgap RC Filter - LP5907

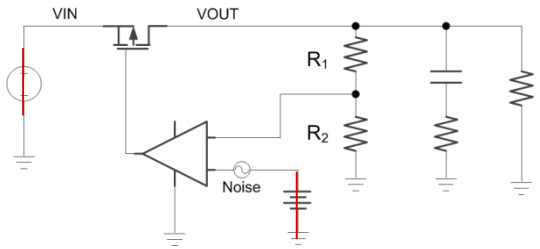


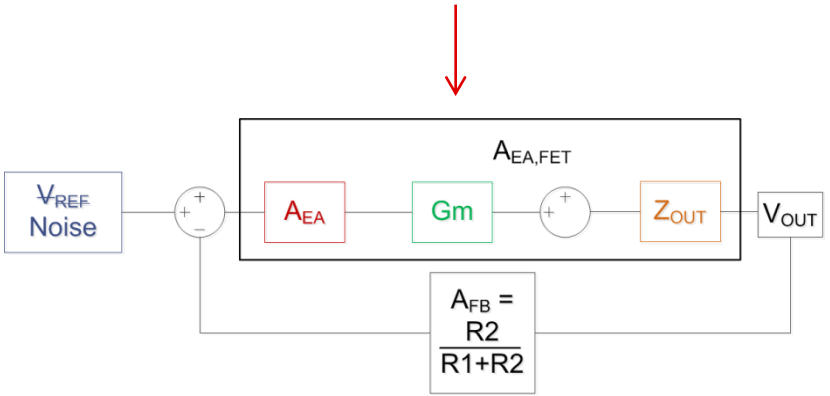
- NR filter is integrated with very large (1 GΩ) filter resistor
- No C_{NR} necessary

Feedback Resistor's Effect on Noise

- LDO Intrinsic noise is dominated by noise from the reference and the error amplifier.
- In a standard LDO, decreasing A_{FB} (feedback resistor attenuation) will result in higher noise at the output.
- Higher output voltages (lower A_{FB}) will have higher noise gain.

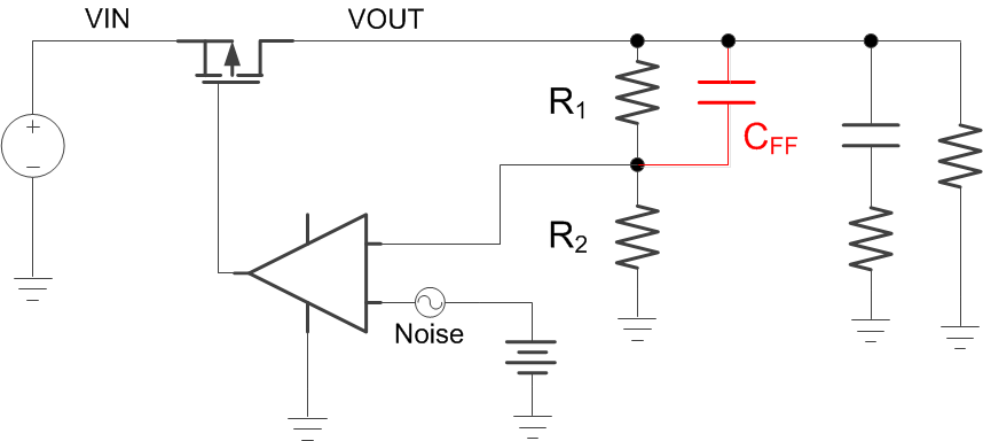
Assume:
input noise = 0 DC
voltages = 0

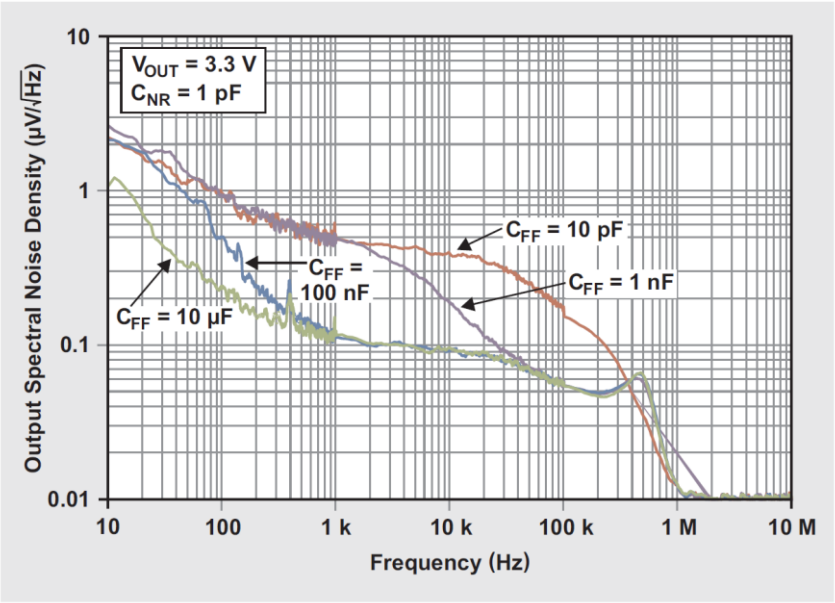




$$\frac{V_{OUT}}{Noise} = \frac{A_{EA,FET}}{1 + A_{EA,FET} * A_{FB}} \cong \frac{1}{A_{FB}}$$

Adding a C_{FF} reduces Closed-Loop Gain





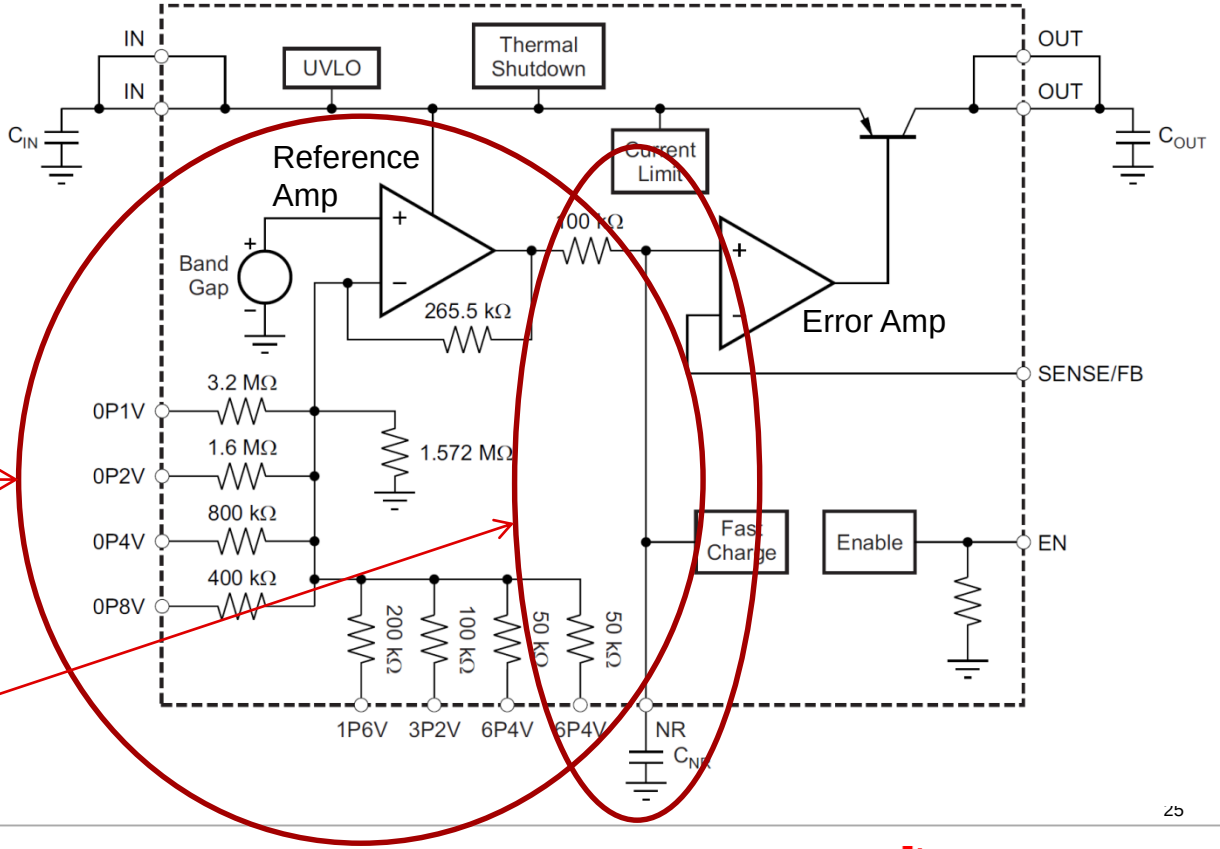
- C_{FF} brings resistor attenuation (A_{FB}) to 1 at high frequency
- C_{FF} can also improve transient response

Low Noise Example: TPS7A4700 36V 1A 4μVrms

- To reduce closed-loop gain, and therefore noise, some devices gain up the reference, and then use the RC filter.

The bandgap voltage reference is gained up with internal resistors.

The effective reference voltage is then filtered after the reference amplifier.



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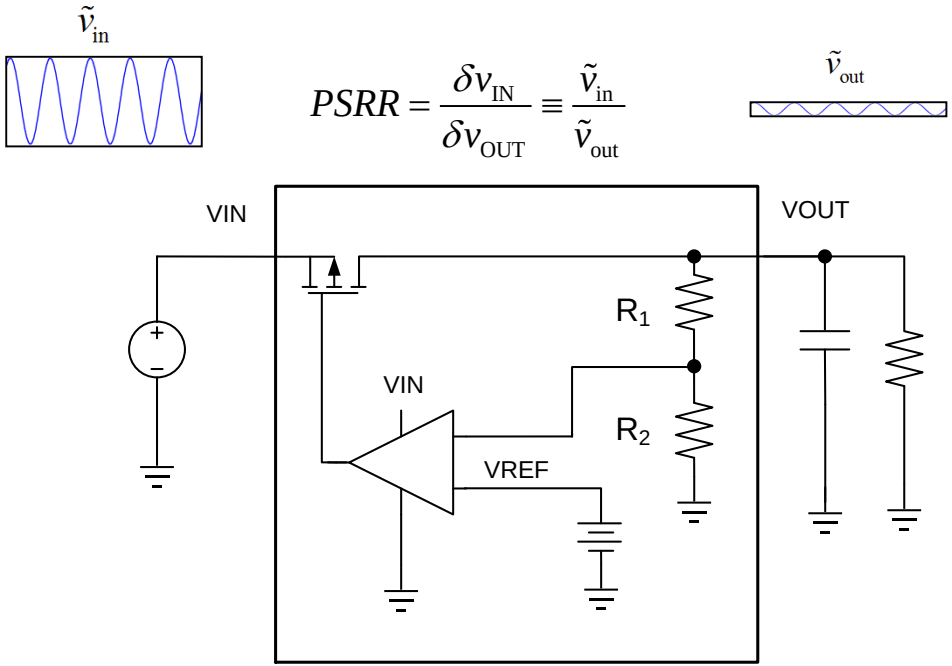
PSRR

- PSRR (Power Supply Ripple Rejection) represents the ability of the LDO to filter input voltage changes. This is critical for low-noise applications.



Typical PSRR Curve

Region 1 is determined by:

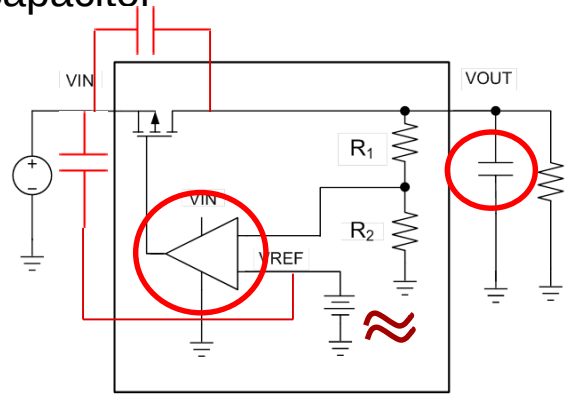
- PSRR or Thermal Coupling into Reference

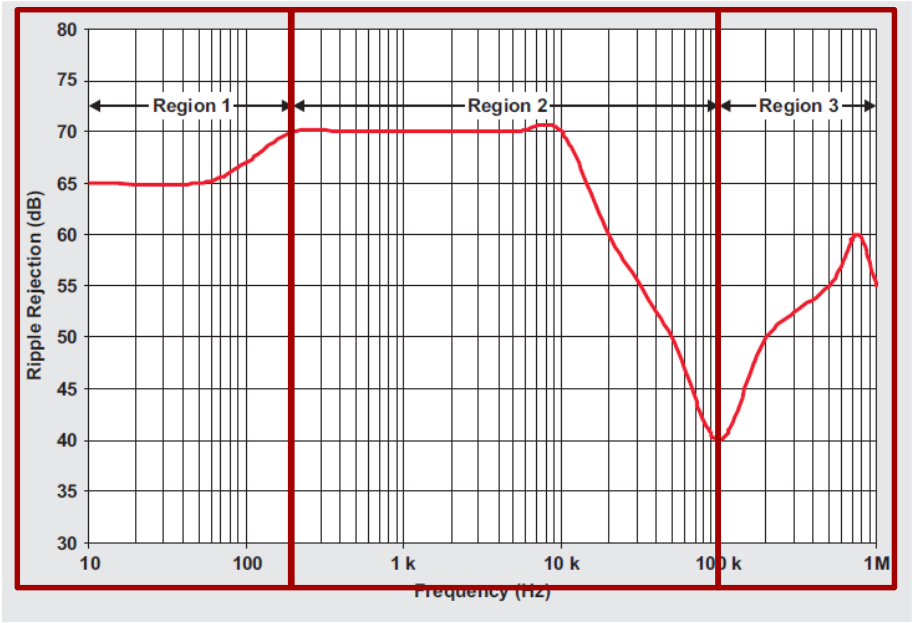
Region 2 is determined by:

- Open-Loop Gain of Error Amplifier

Region 3 is determined by:

- Parasitic capacitance and output capacitor

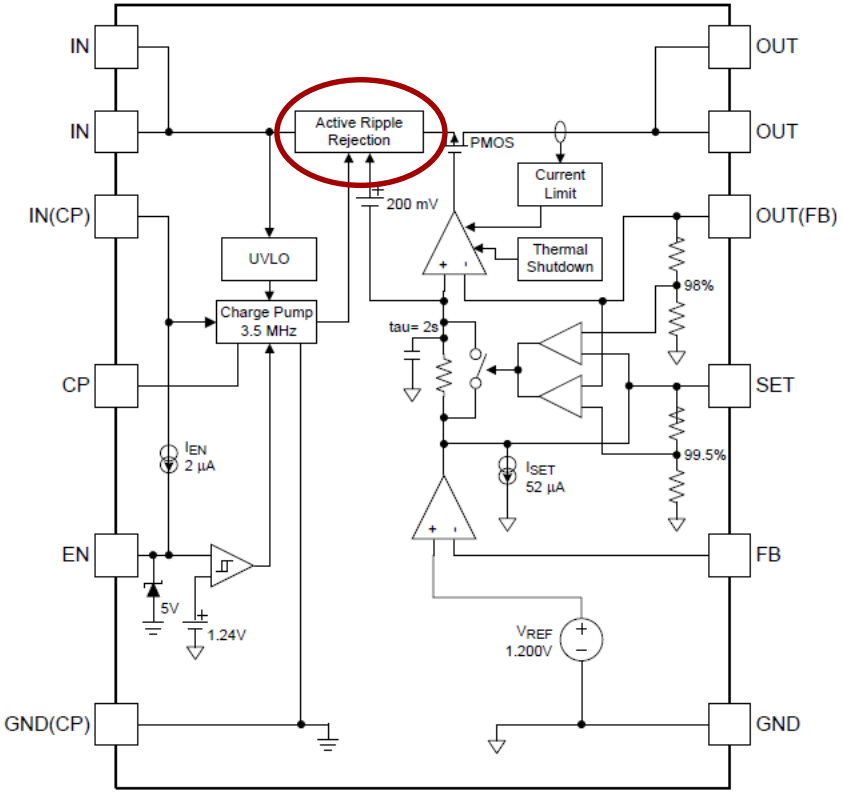




High PSRR with Additional Pass Device

Some devices use an additional pass element, connected as a “cascode” device. Using a cascode pass device can improve the pass device output impedance, and therefore, the PSRR.

Examples of this are the LP38798 (shown), TPS7A81 and TLV707.



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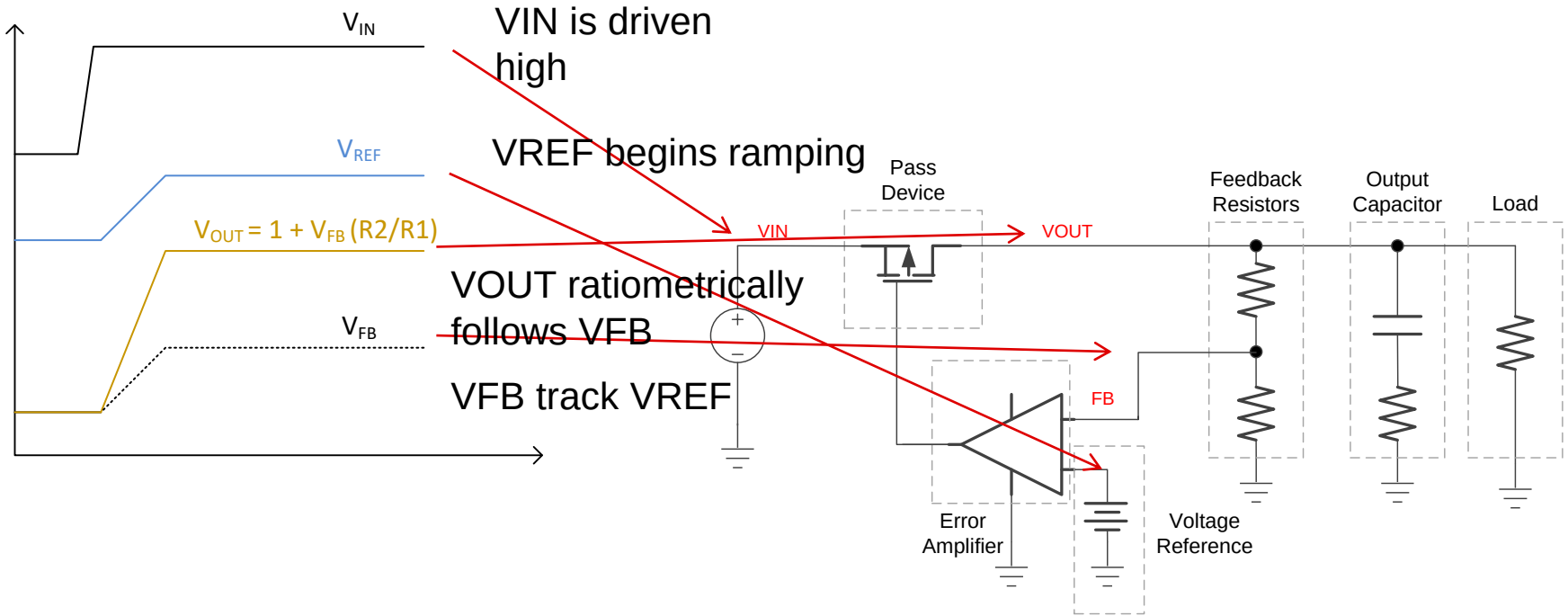
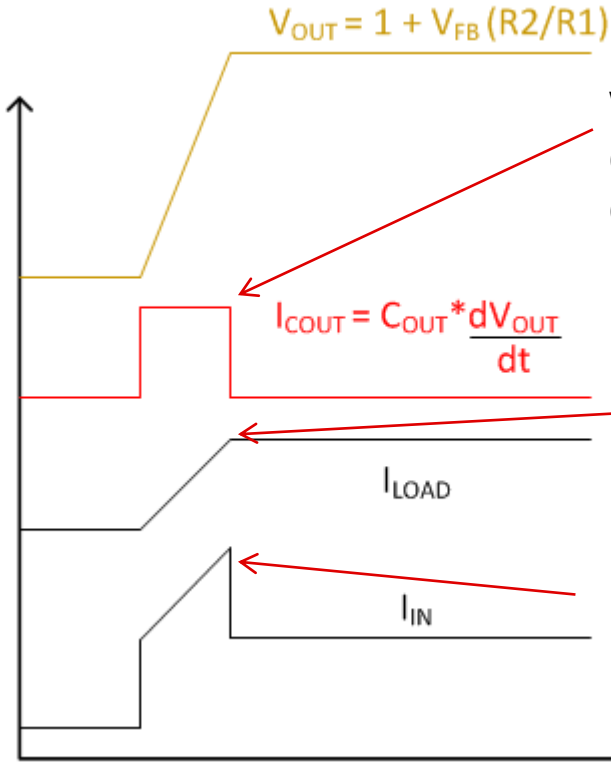
How Startup Works (ideally)

Ideal LDO startup behavior occurs when VFB tracks the reference from 0 V to the final value.



Inrush Current During Startup

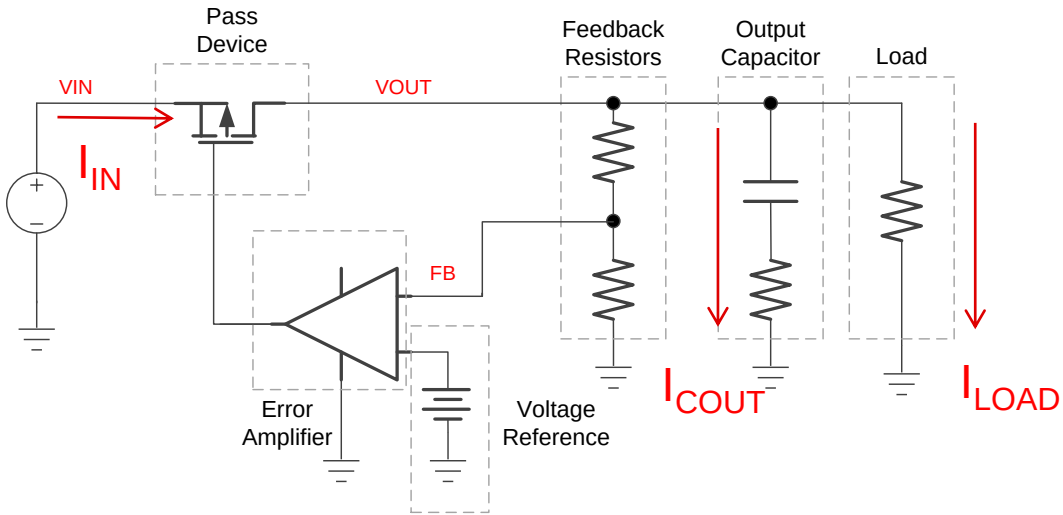
For an ideal startup, the current through the load capacitor is constant.



When the output ramps, current is supplied to both the output capacitor

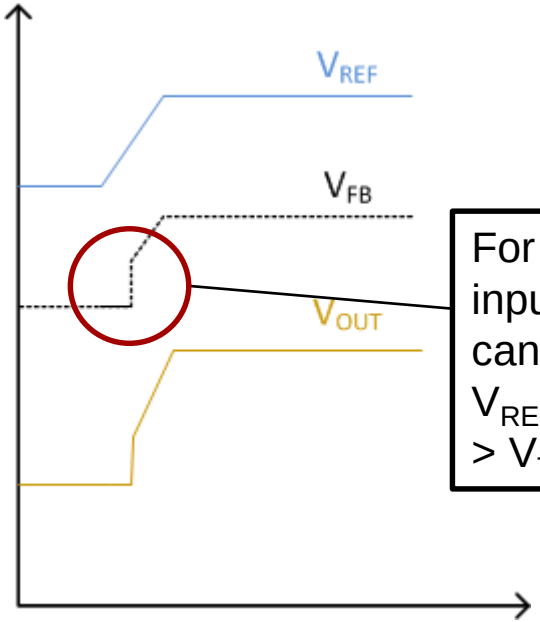
And the load.

Leading to a high current ramp.

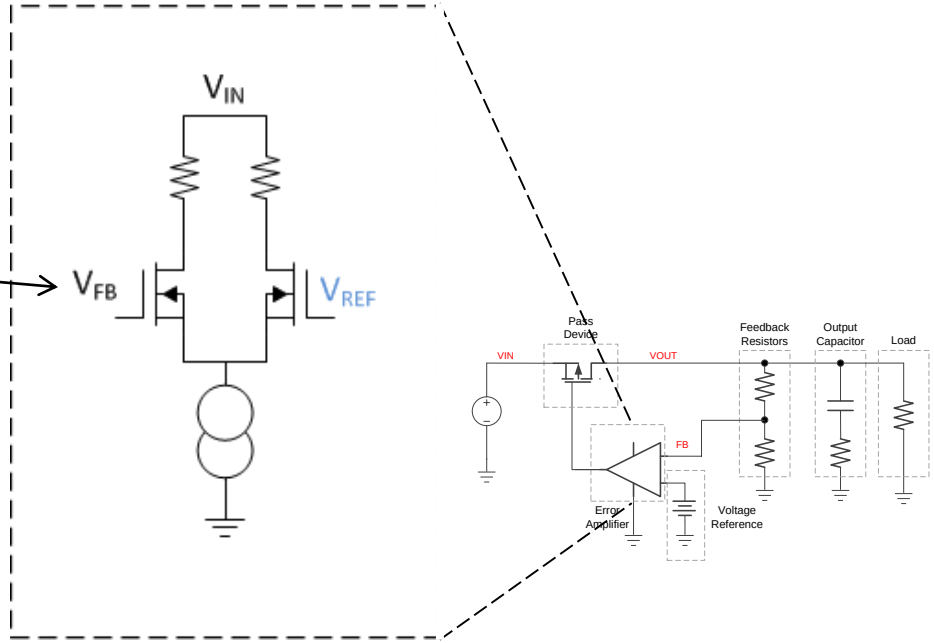


Non-ideal Startup

Many LDOs have a high dV/dT, or "jump" at startup. This is commonly due to limited common mode range of the error amplifier.



For an NMOS input pair, V_{FB} cannot track V_{REF} until $V_{REF} > V_{TH} + V_{OV}$



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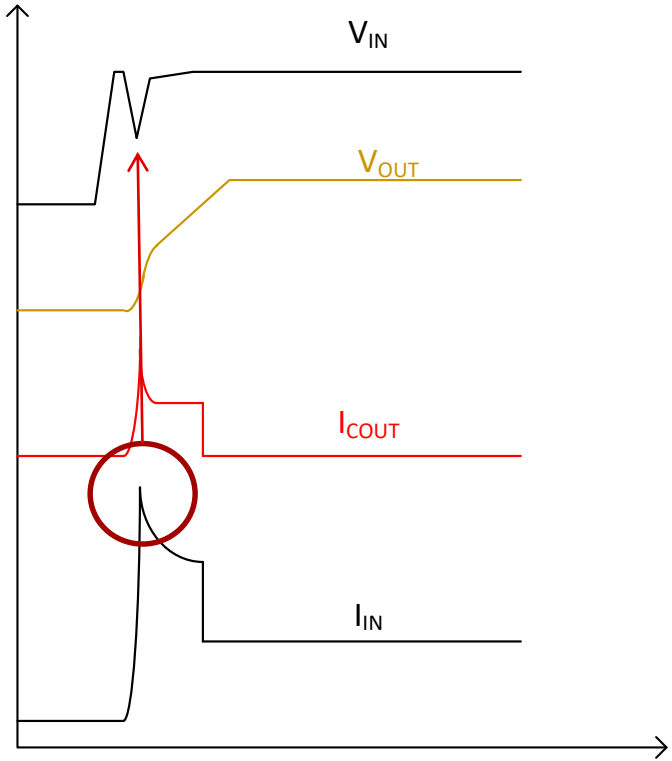
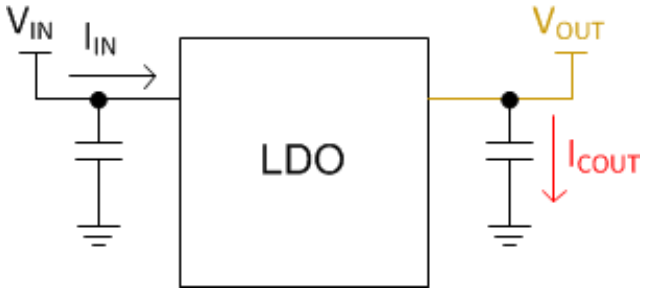


The high dV/dt change on the output will result in a peak of current into the output capacitor.

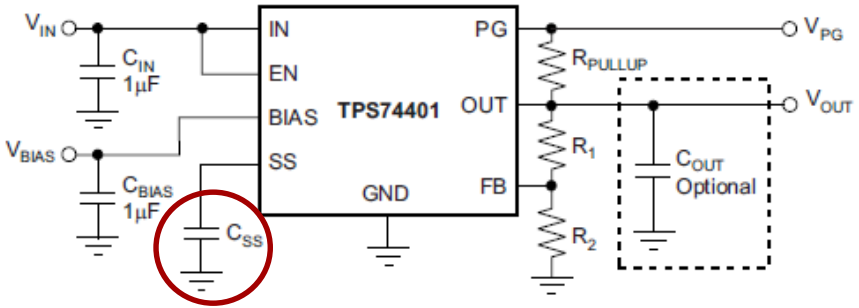
Output capacitor current will flow from the input, causing a peak of current at the input.

The input current will lead to a drop in the input voltage, which can create problems on the input rail.



Ideal Startup example: TPS74X

The TPS74X family has constant-current soft-start capacitor charging, leading to well-controlled startup behavior.



$$R_1 = \left[\frac{V_{OUT}}{V_{REF}} - 1\right] \times R_2$$