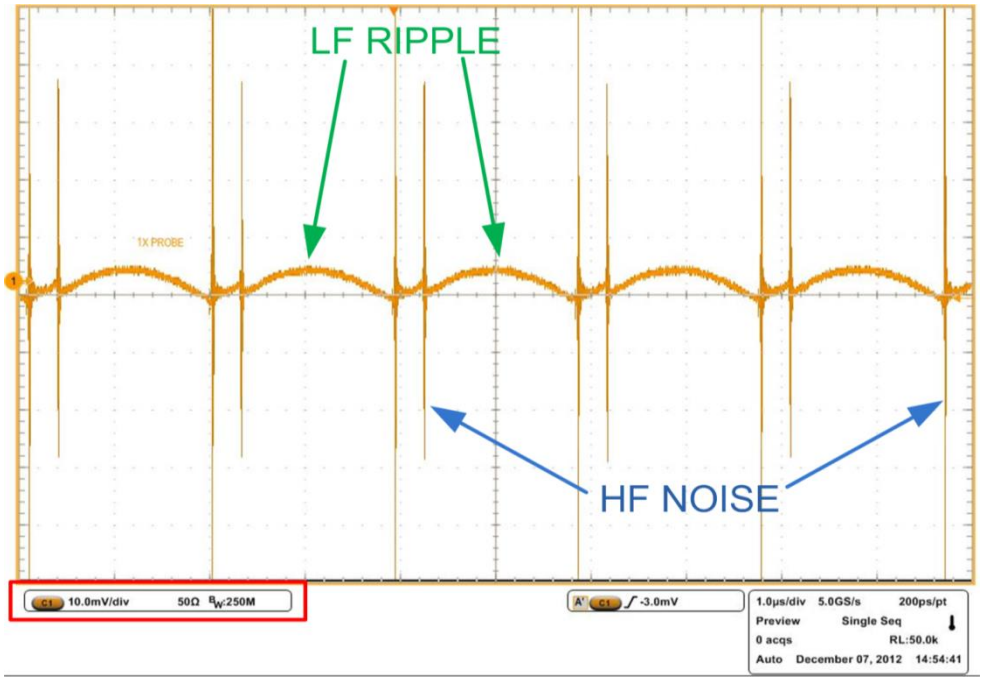
Mixed-Type Output Capacitors & Noise Mitigation

Akshay Mehta

Texas Instruments

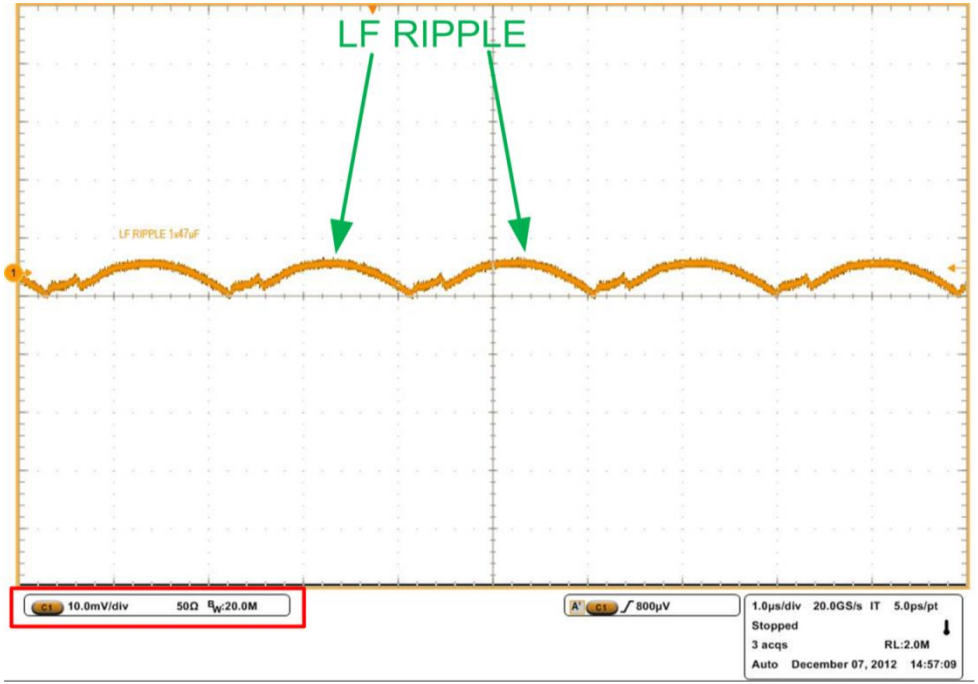
Output ripple components

- **Low Frequency (LF) “Ripple” & High Frequency (HF) “Noise”**



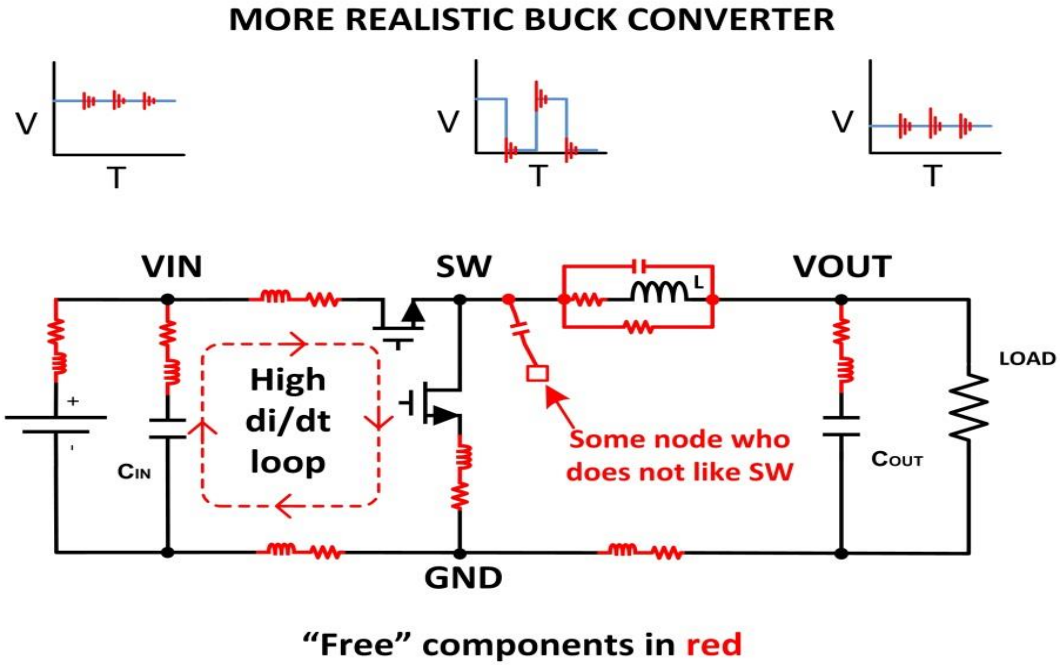
LF ripple

- **Low Frequency (LF) “Ripple”**



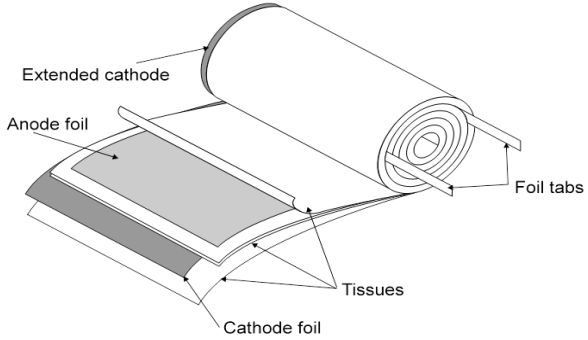
LF ripple: Origin

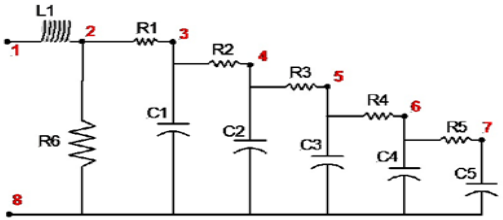
- **A function of the inductor ripple current & the output capacitor impedance (formed by C, ESR, and ESL)**



Aluminum electrolytics - Overview

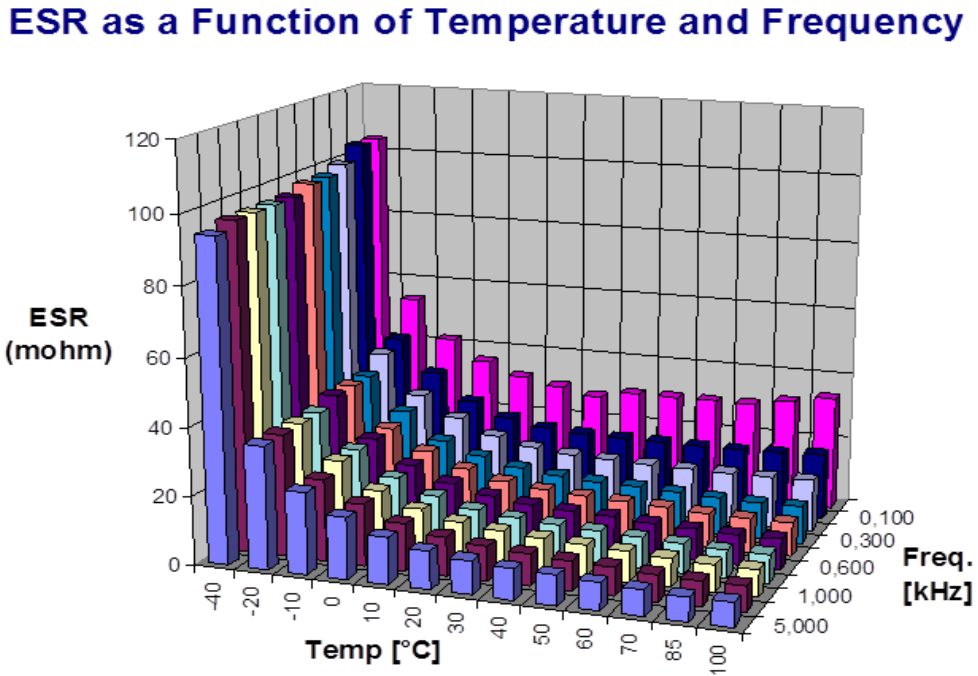
- Low cost
  - Mature technology with low cost materials
- Long history
  - Industry started in the 1930's
- Many manufacturers to choose from
- High capacitance values available
- Only choice for SMPS that need high voltage & high capacitance
- **Highest ESR**
- Low frequency capacitance roll off due to higher ESR



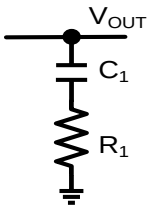


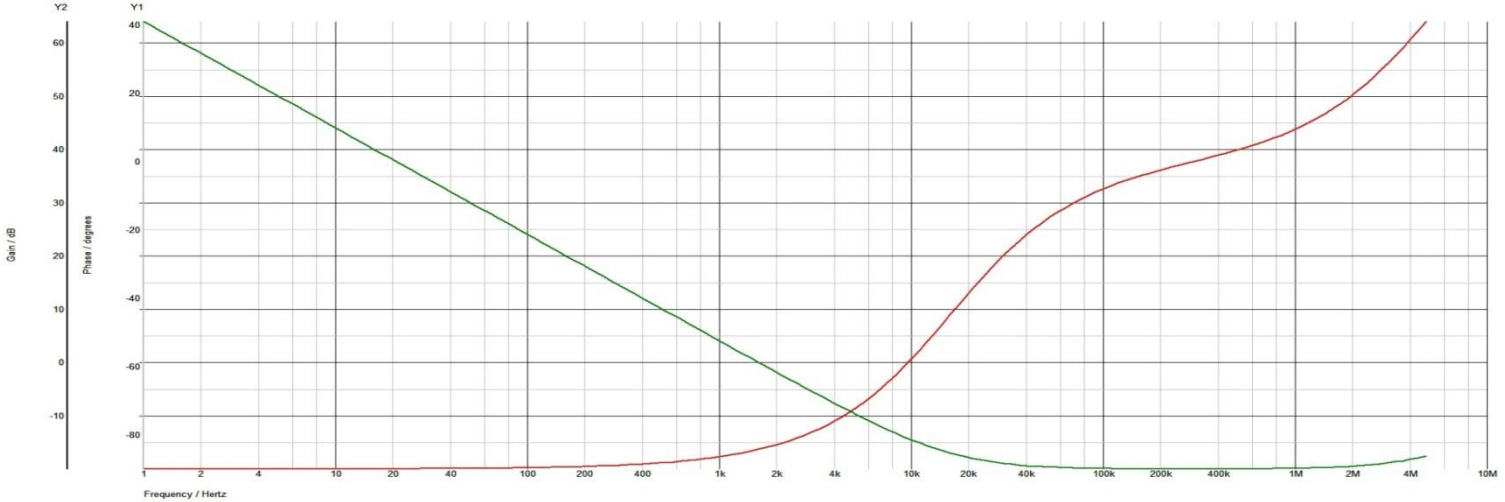
Aluminum electrolytics - Disadvantages

- Large swings in ESR vs. temperature
  - Cold temps have 4-8x higher ESR than at room temperature



Frequency response of a 100µF electrolytic capacitor with 100mΩ ESR

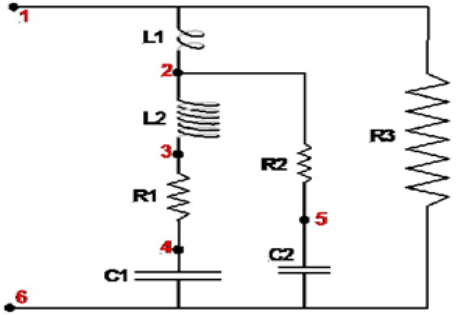


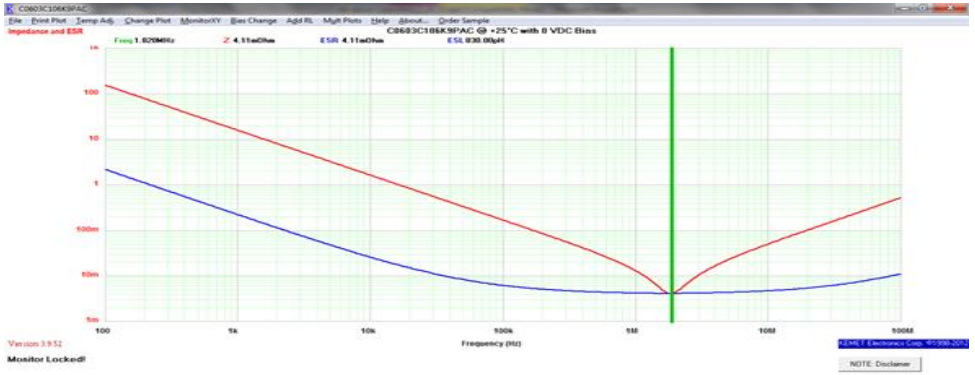


- **High ESR at low frequencies**
- **The high ESR introduces a zero at low frequencies which may cause instabilities during a transient if not properly compensated for**
- **The high ESR will also increase the steady state ripple**
- **To mitigate this & reduce LF ripple, parallel ceramic caps can be added.**

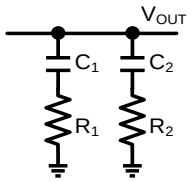
Ceramics - Overview

- Lowest cost devices
- Best choice for local bypassing
- Not polarized
- Low series resistance (Low ESR)
- Low effective series inductance (Low ESL)
- Significant effects for Class 2 dielectrics i.e. X5R, X7R
  - **Voltage bias effect**
  - Temperature effects
  - High Q
    - Frequency selective





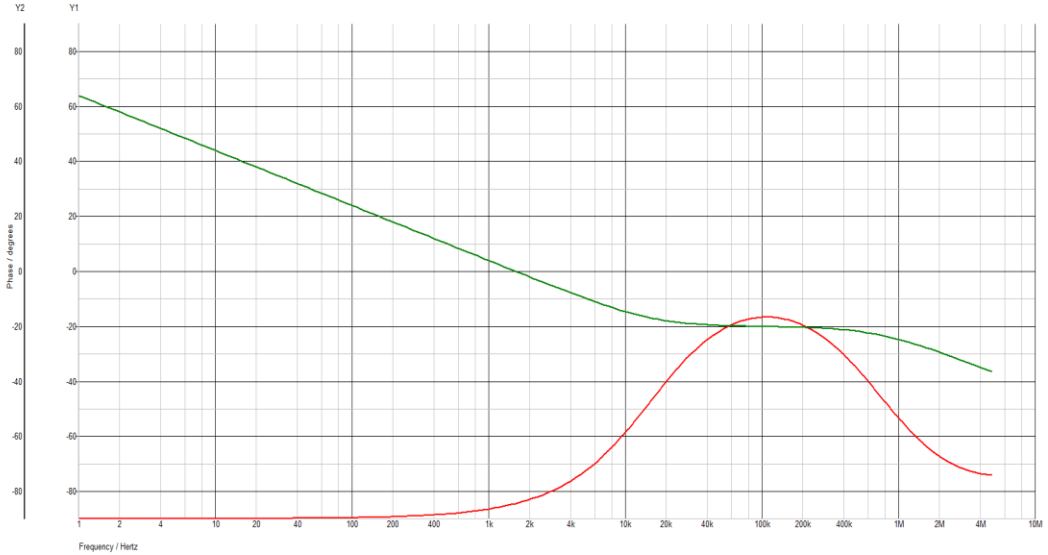
Adding a parallel 2.2µF ceramic capacitor to the 100µF electrolytic



$$Z = \frac{(1 + sR_1C_1)(1 + sR_2C_2)}{sC_t(1 + sR_tC_s)}$$

$$C_t = C_1 + C_2 \qquad C_s = \frac{C_1 * C_2}{C_t}$$

$$R_t = R_1 + R_2$$



- **Ceramic capacitor ESR is at a very high frequency**
- **Addition of ceramic cap introduces a pole at low frequencies**
  - **This will reduce the effect of the ESR zero of the electrolytic cap**
- **Effective ESR of the parallel combination reduces, thus reducing the steady state ripple**

How much is enough?

- **Addition of a single 2.2µF ceramic cap introduced a pole, but was it at a low enough frequency?**
- **How much was the ripple reduced by? Was it enough?**
- **Is the design stable?**

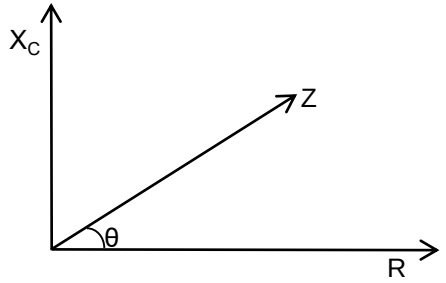
These are some questions that can be answered after doing some analysis on the parallel combination of the mixed type capacitors.

Reducing LF ripple with mixed type output caps for buck topology

Impedance of a capacitor with ESR can be visualized as shown

- **It is defined as:**

$$Z = |Z|e^{j\theta(Z)} \text{ where } |Z| = \sqrt{R^2 + {X_C}^2} \text{ and } \theta(Z) = atan\left(\frac{X_C}{R}\right)$$



For two capacitors in parallel, the magnitude & phase can be written as follows:

$$|Zc| = \frac{\sqrt{{R_1}^2 + {X_{c1}}^2} * \sqrt{{R_2}^2 + {X_{c2}}^2}}{\sqrt{(R_1 + R_2)^2 + (X_{c1} + X_{c2})^2}} \text{ and } \theta(Z_C) = atan\left(\frac{X_{c1}}{R_1}\right) + atan\left(\frac{X_{c2}}{R_2}\right) - atan\left(\frac{X_{c1} + X_{c2}}{R_1 + R_2}\right)$$

The effective ESR and capacitance can then be estimated as:

$$\boldsymbol{R_{eff} = |Z_C| * cos(\theta(Z_C))}$$

$$\boldsymbol{C_{eff} = \frac{1}{2 * \pi * f * |Z_C| * sin(\theta(Z_C))}}$$

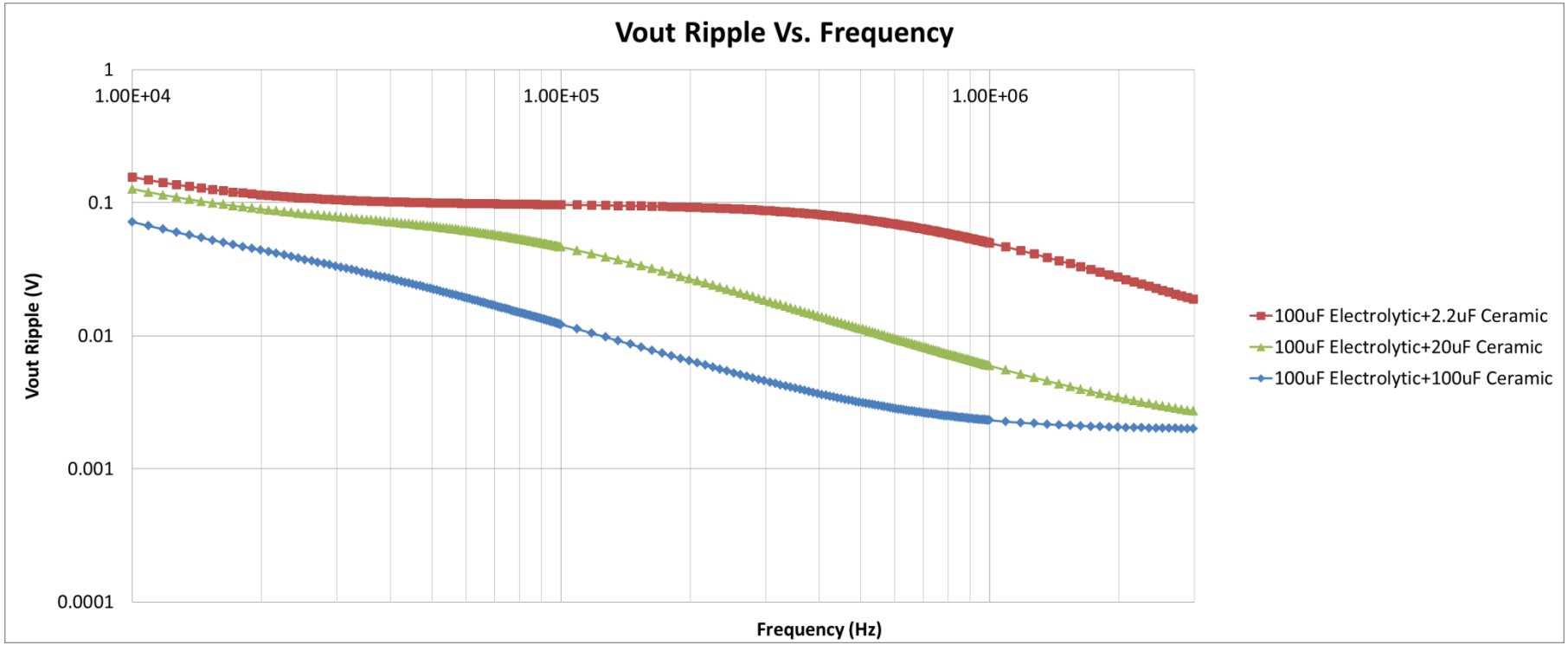
C_{eff} and R_{eff} are dependent on frequency, f

Output voltage ripple for buck: $\boldsymbol{V_{O_{ripple}} \approx \sqrt{(I_{Lpp} * R_{eff})^2 + \left(\frac{I_{Lpp}}{8 * f * C_{eff}}\right)^2}}$

Microsoft Excel Worksheet

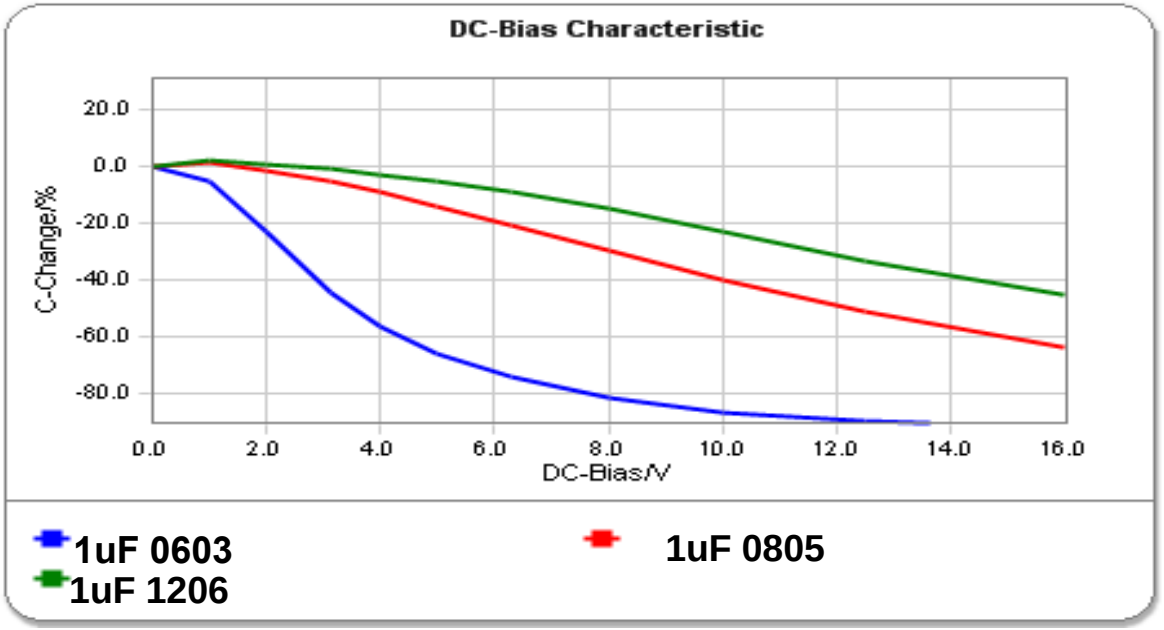
Spreadsheet to estimate output ripple

LF output voltage ripple with 1A ripple current



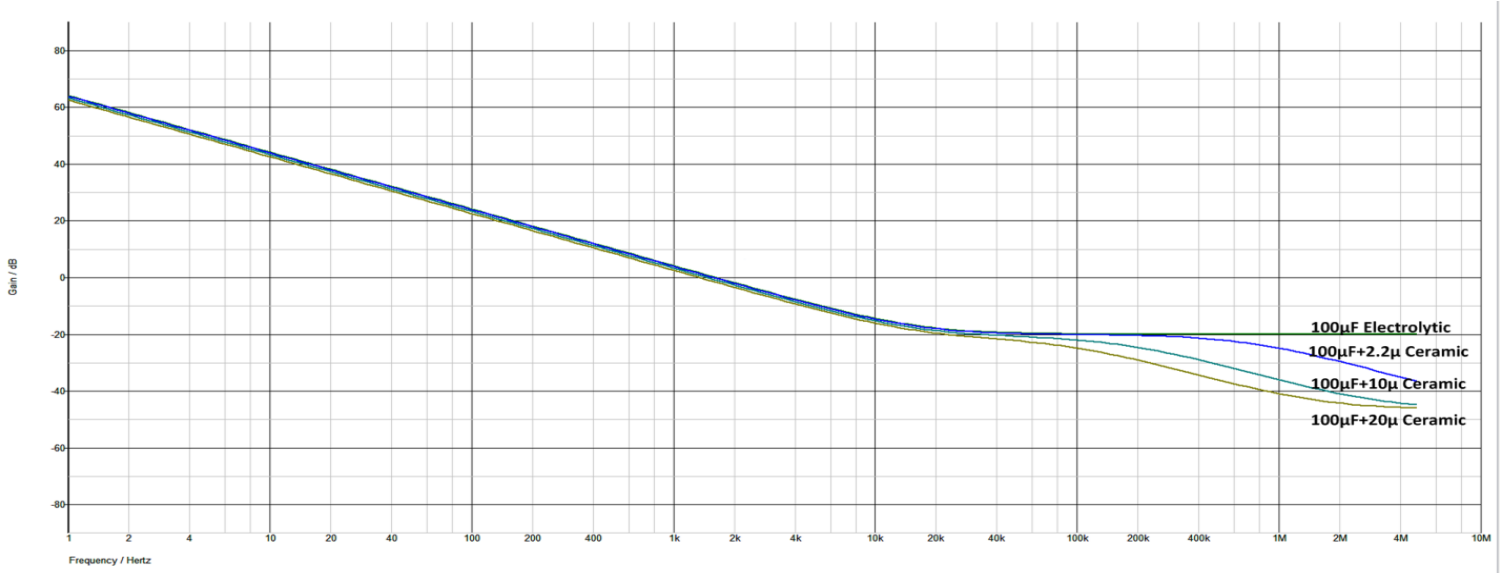
Ceramic cap: Voltage bias effect including case size

X5R, 16V Rated Capacitors



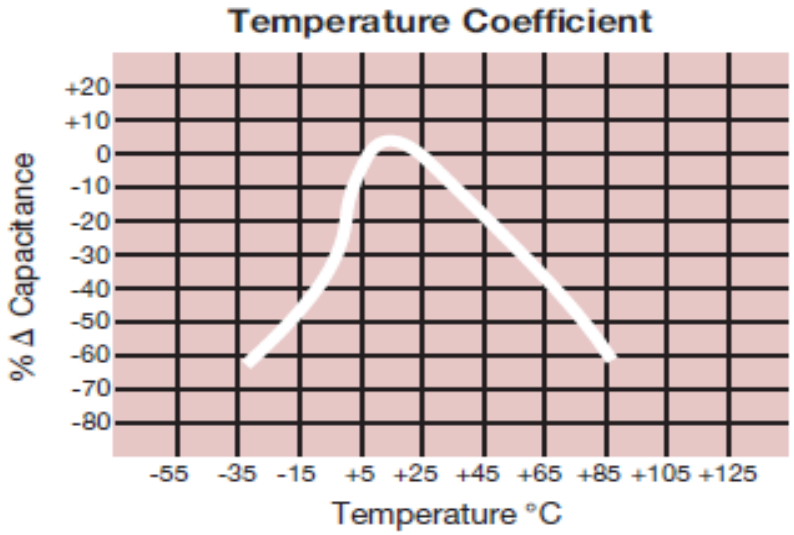
Capacitance decreases more quickly with smaller Case sizes

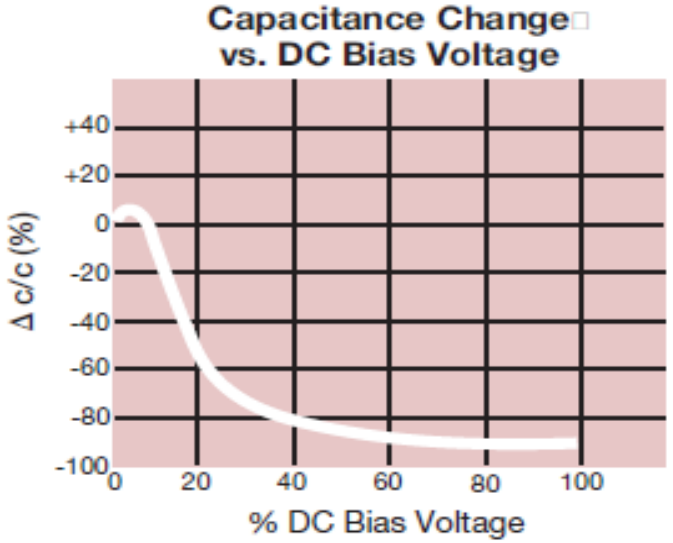
Ceramic caps: Choose the right rated component



- **If chosen cap has rated voltage close to applied voltage, the capacitance derates**
- **This will push the pole out to higher frequencies & will not be as effective in terms of compensating for the ESR of the electrolytic cap**

Ceramic caps: Y5V dielectric characteristics

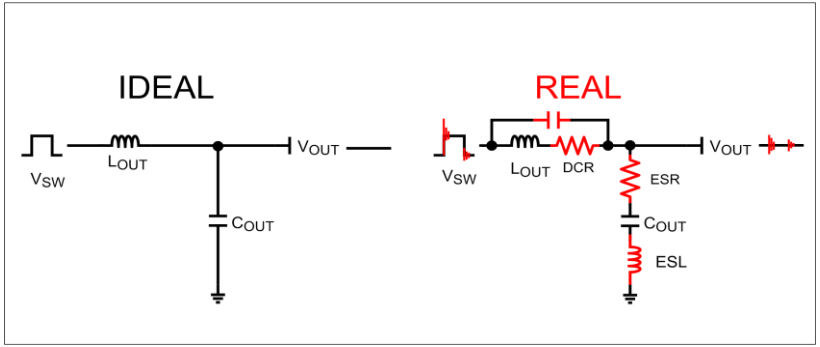




DO NOT USE! Y5V & Z5U ceramic dielectrics for power supply designs

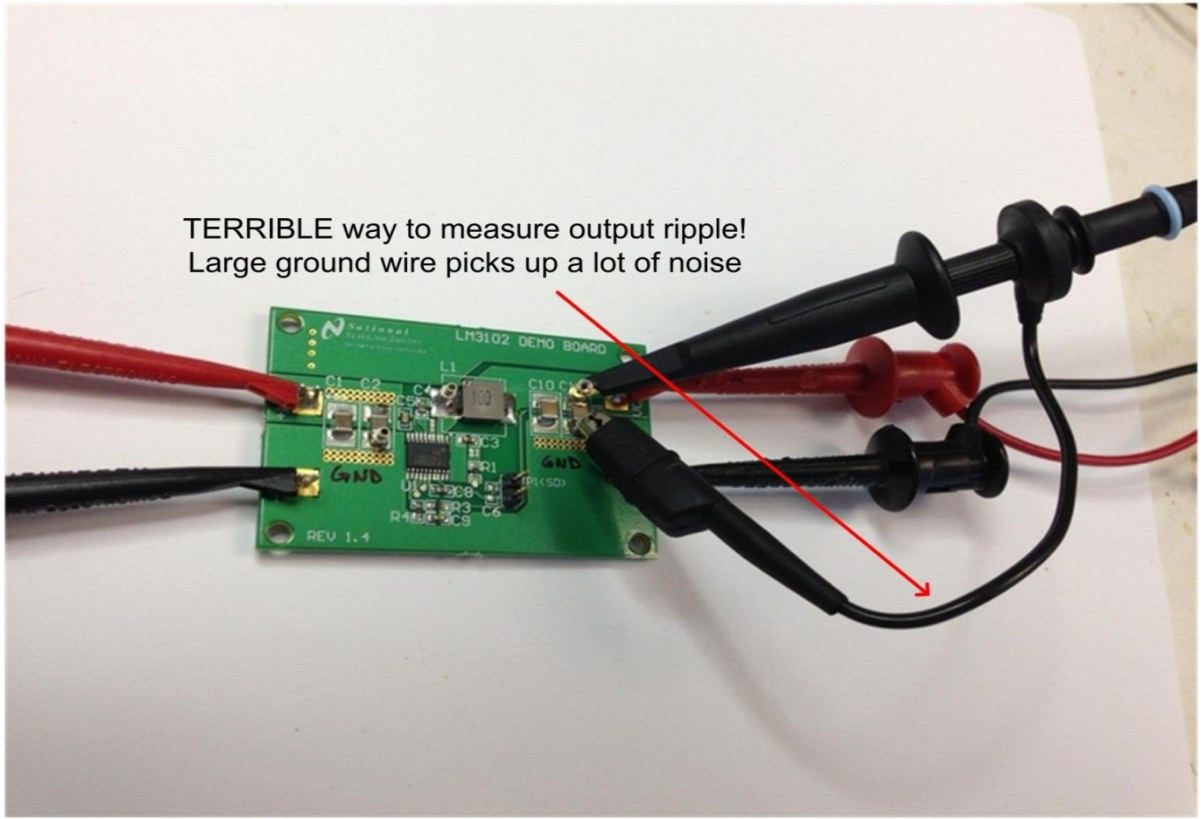
HF noise: Origin

- **Fast edge of switch node voltage couples right through the inductor parasitic capacitance**

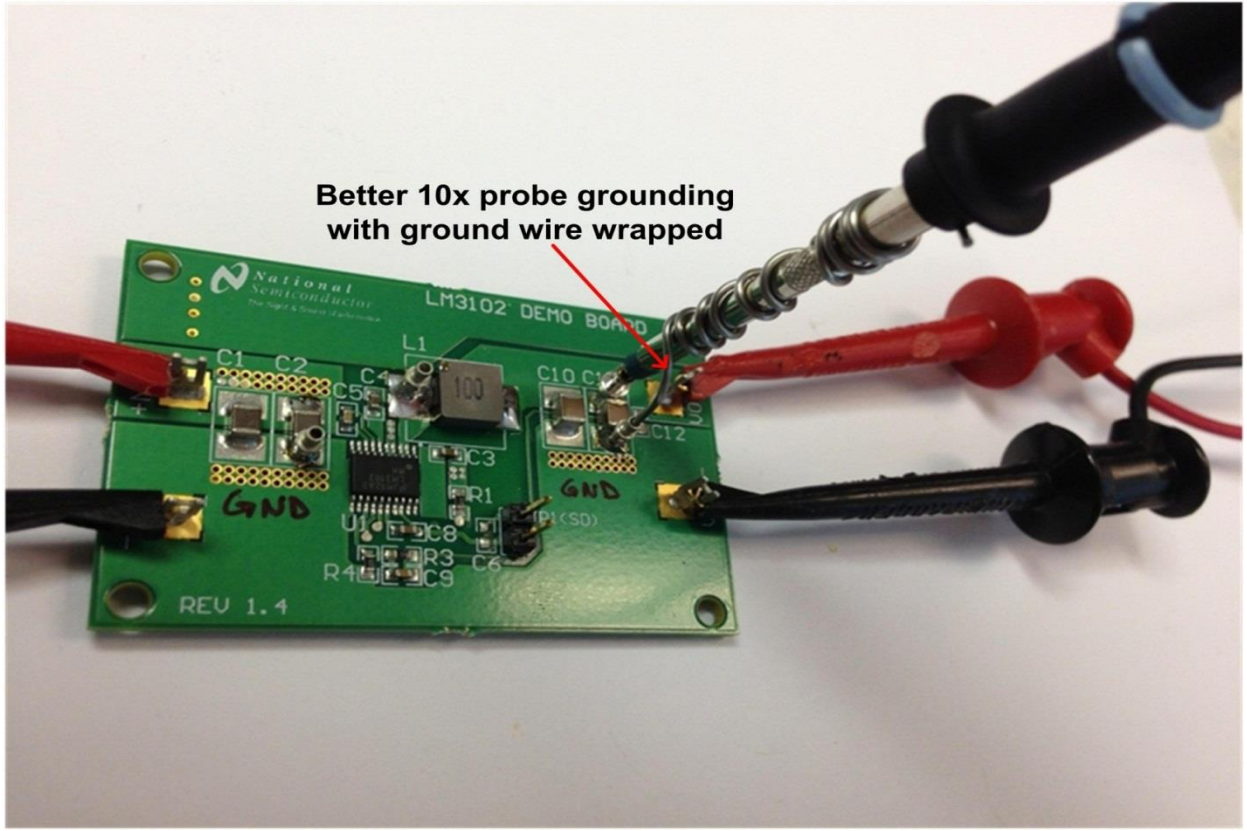


- **Ringing frequency in 100's of MHz, modulated by the inductor & output cap parasitics**

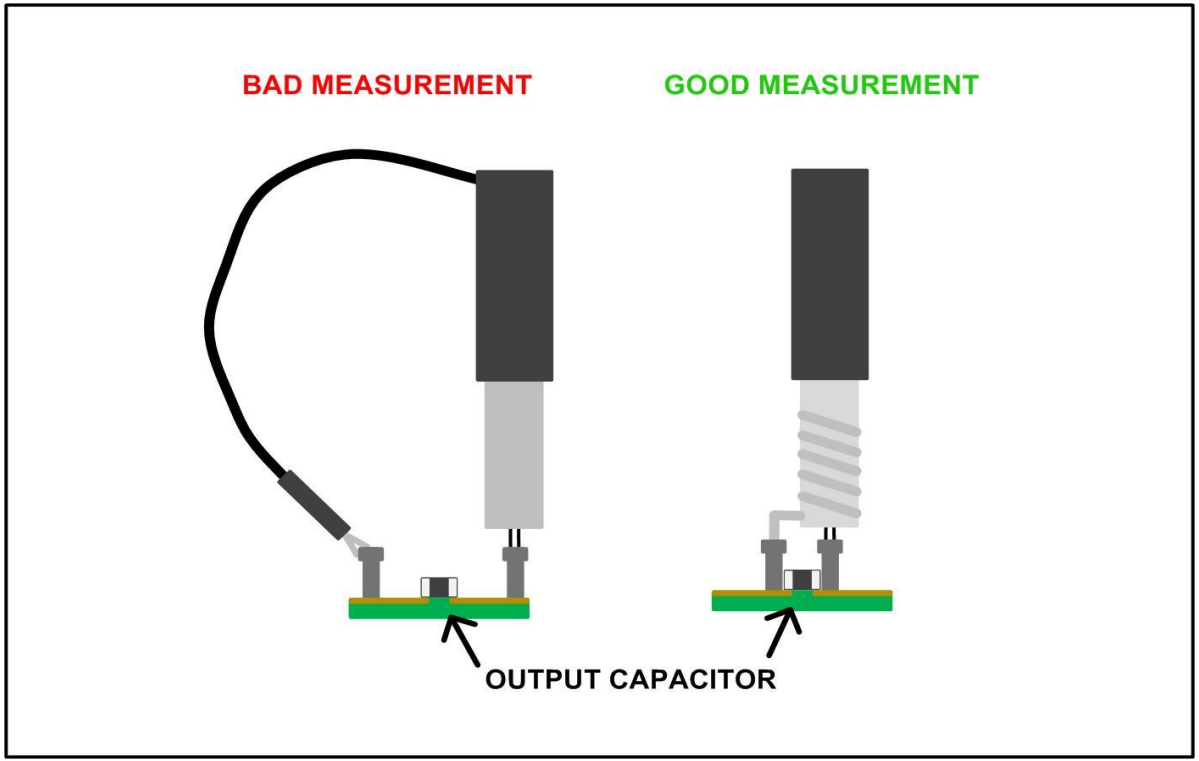
Measuring output ripple



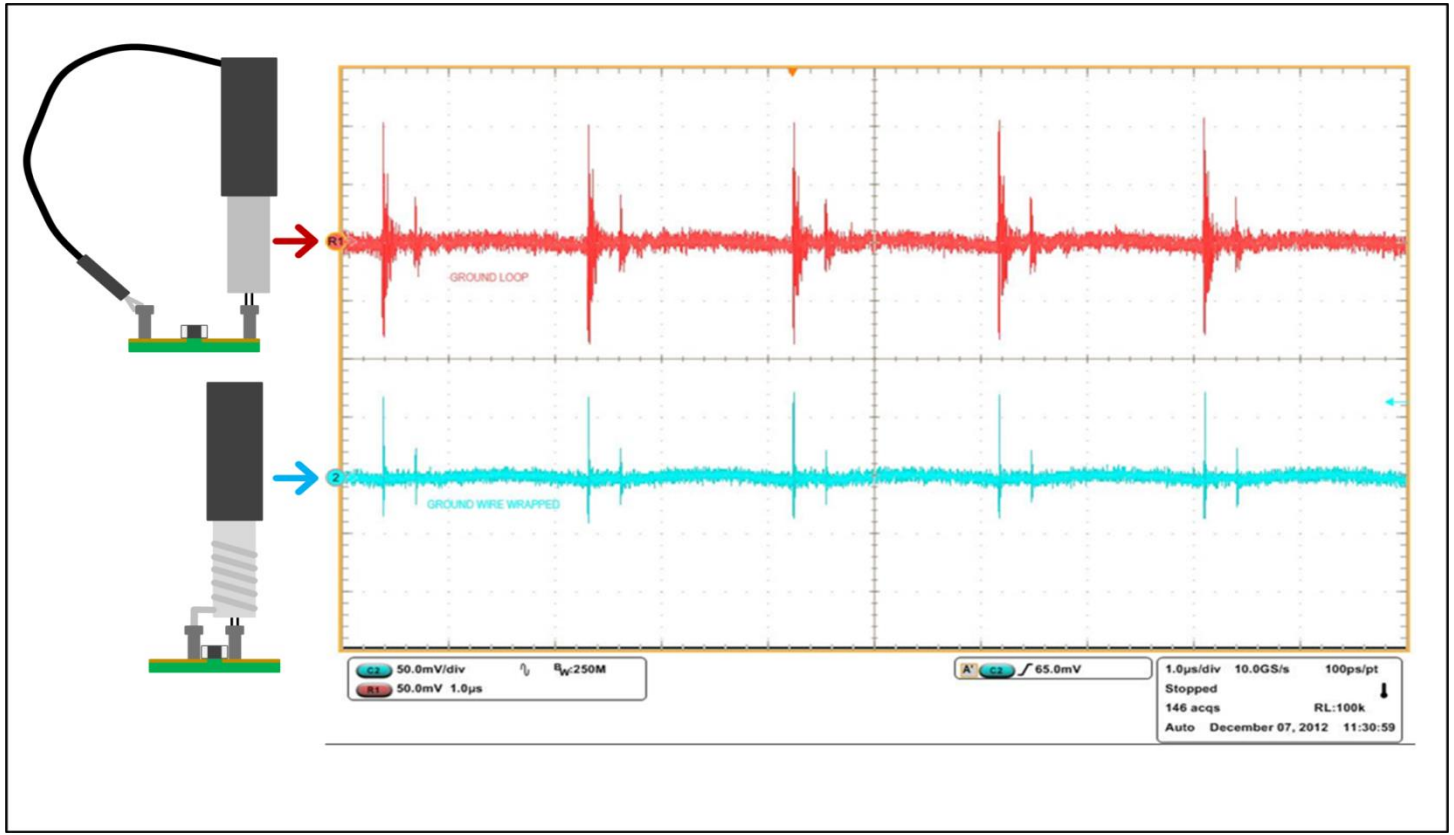
Measuring output ripple



Measuring output ripple

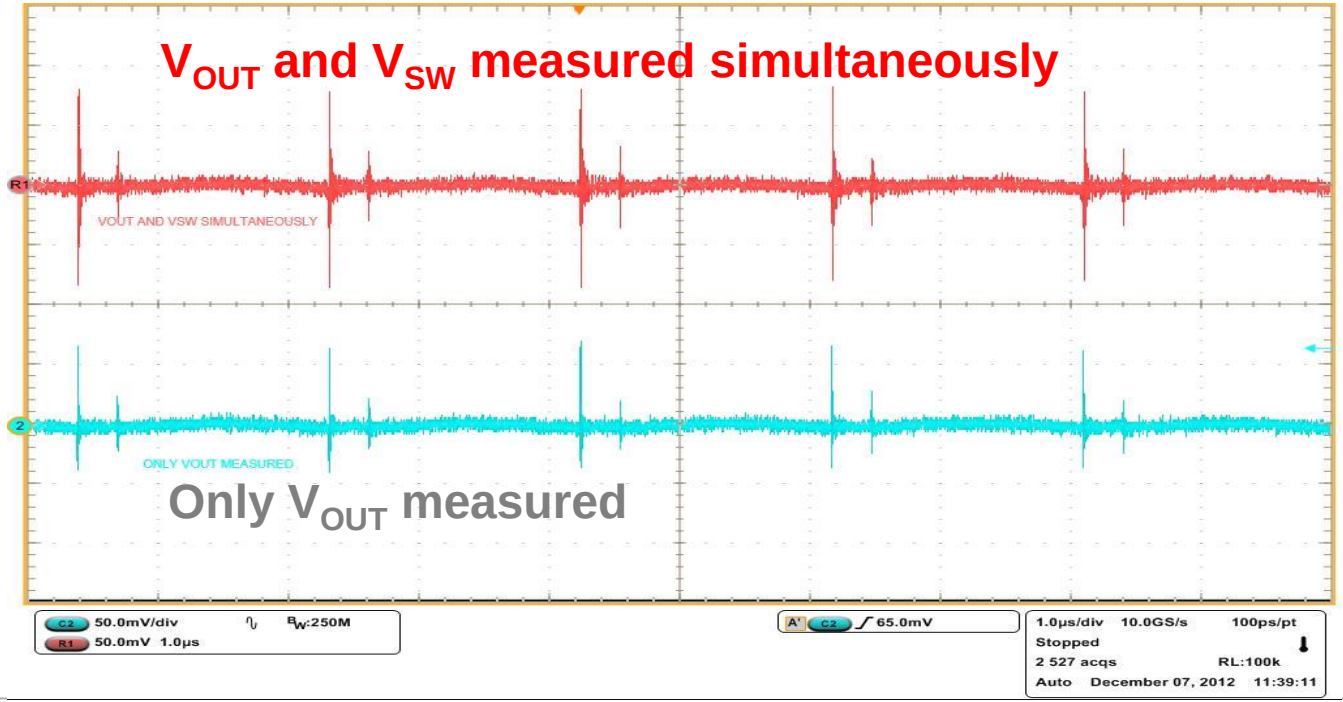


Measuring output ripple



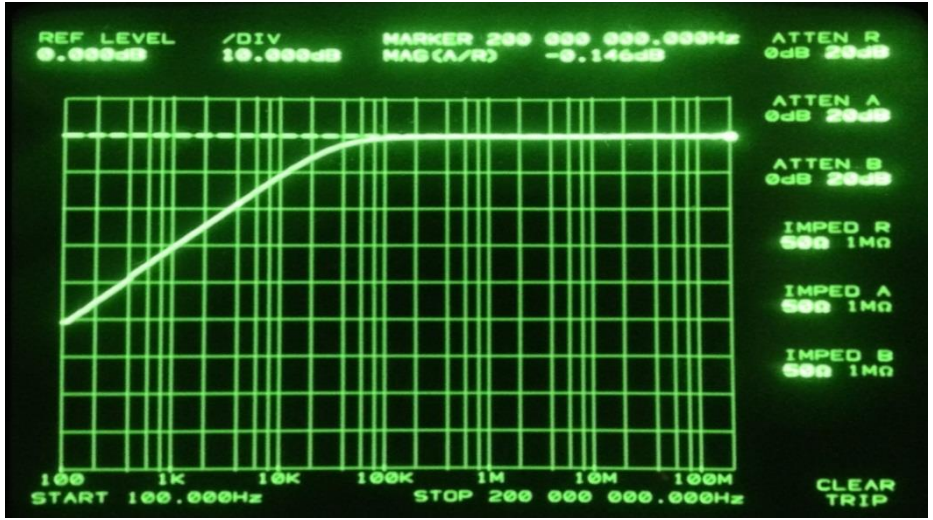
Measuring output ripple

- **When taking V_{OUT} measurements, don't probe any other noisy nodes (e.g. SW) with the scope**

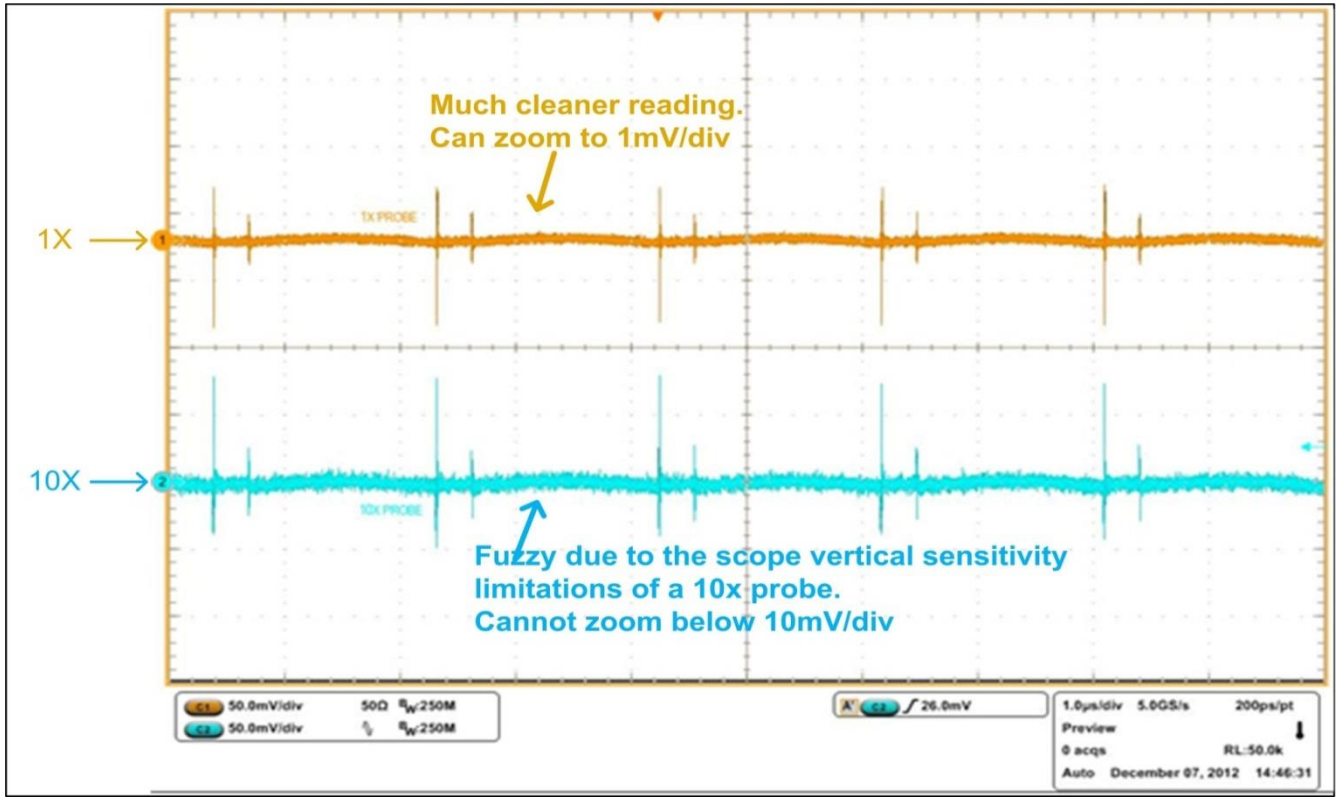


Measuring output ripple – Custom 1x probe

- 0.1µF AC coupling (DC blocking) capacitor & external (or internal) 50Ω termination at the scope
- High Pass cutoff frequency at 1 / (2πRC) = 32kHz
  - This simple probe is suitable for use for up to 250MHz BW setting on the scope

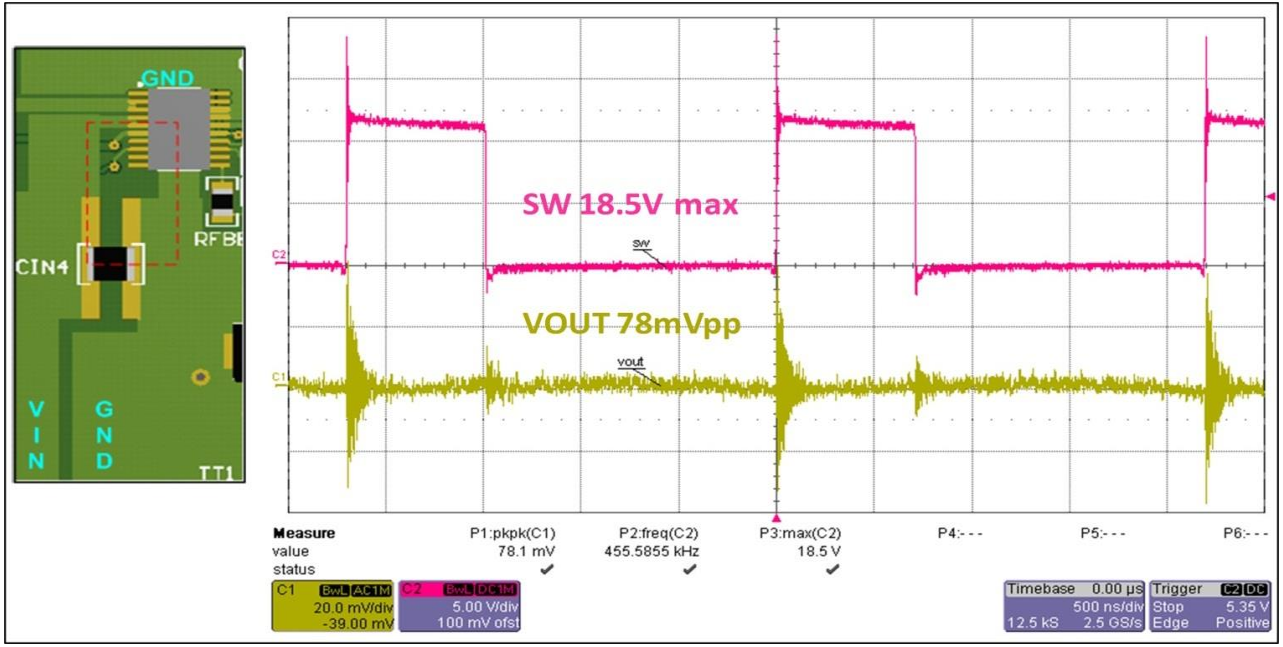


Measuring output ripple – Custom 1x probe



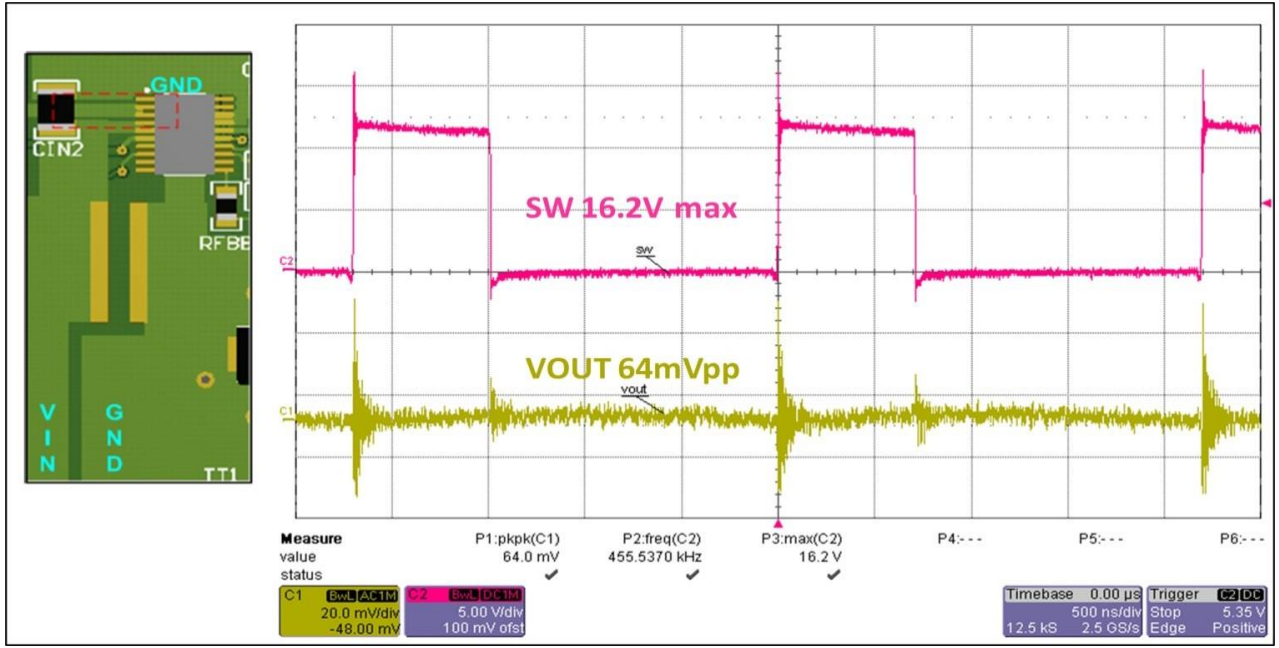
Reducing output ripple (HF)

- Buck **input capacitor** placement – reduce source of ringing



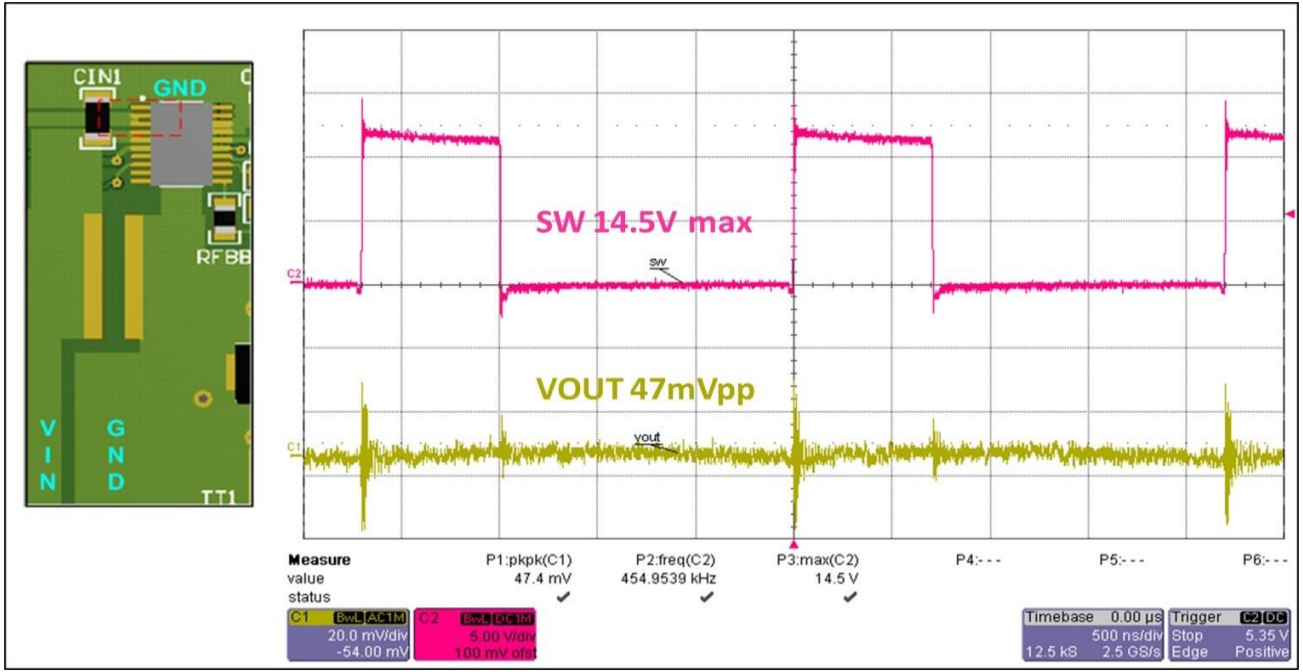
Reducing output ripple (HF)

- Buck **input capacitor** placement – reduce source of ringing



Reducing output ripple (HF)

- Buck **input capacitor** placement – reduce source of ringing FREE!

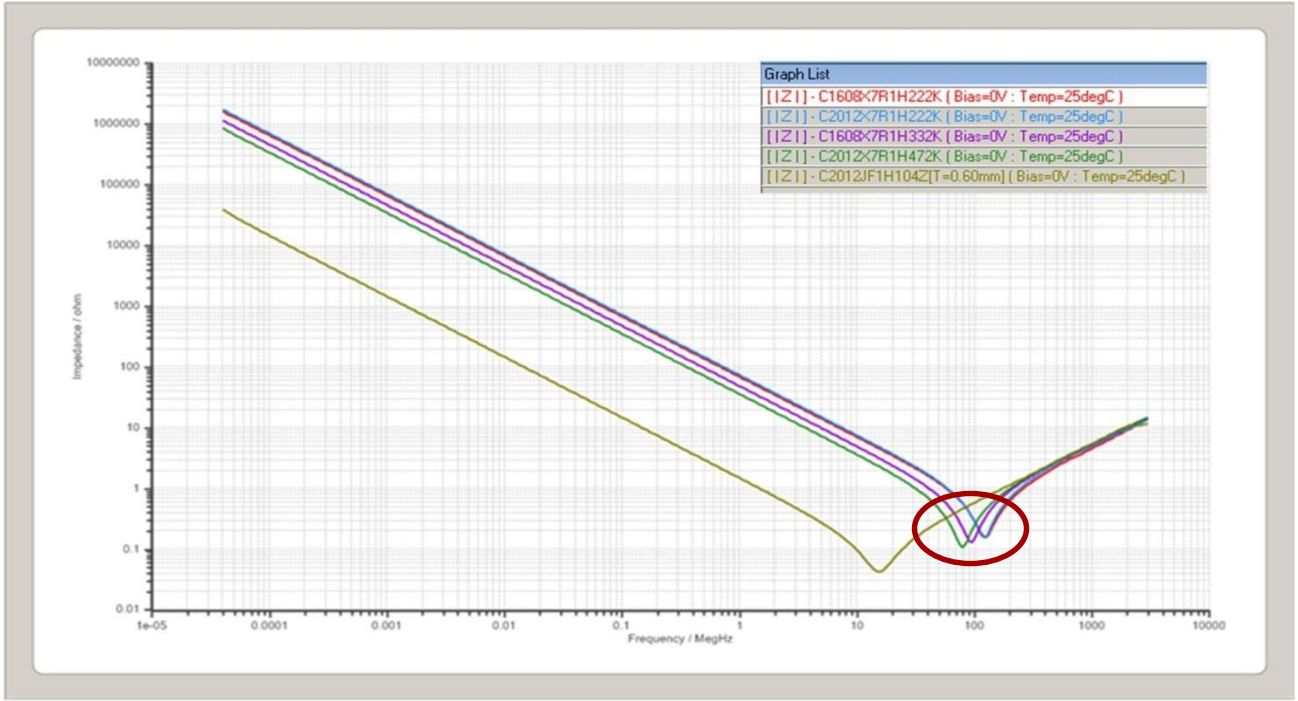


Reducing output ripple (HF)

- After careful input capacitor placement, we get what we get
  - There is still some HF noise on the output
- Now we need to filter the left over HF spike
- We need to provide “low” impedance path at the frequency of interest
- Method with capacitors only:
  - Leave empty small capacitor footprint(s) in your layout
  - When the hardware arrives, measure the HF ringing frequency with high BW scope setting
    - Remember, the ringing frequency is a result of the inductor parasitics, PCB layout, output capacitor, so knowing the frequency before getting hardware is difficult
  - Once the frequency is known from measurement, pick a small ceramic capacitor with a “notch” or ”null” at the frequency of interest
    - Place 1-2 small capacitors in parallel to reduce the HF noise

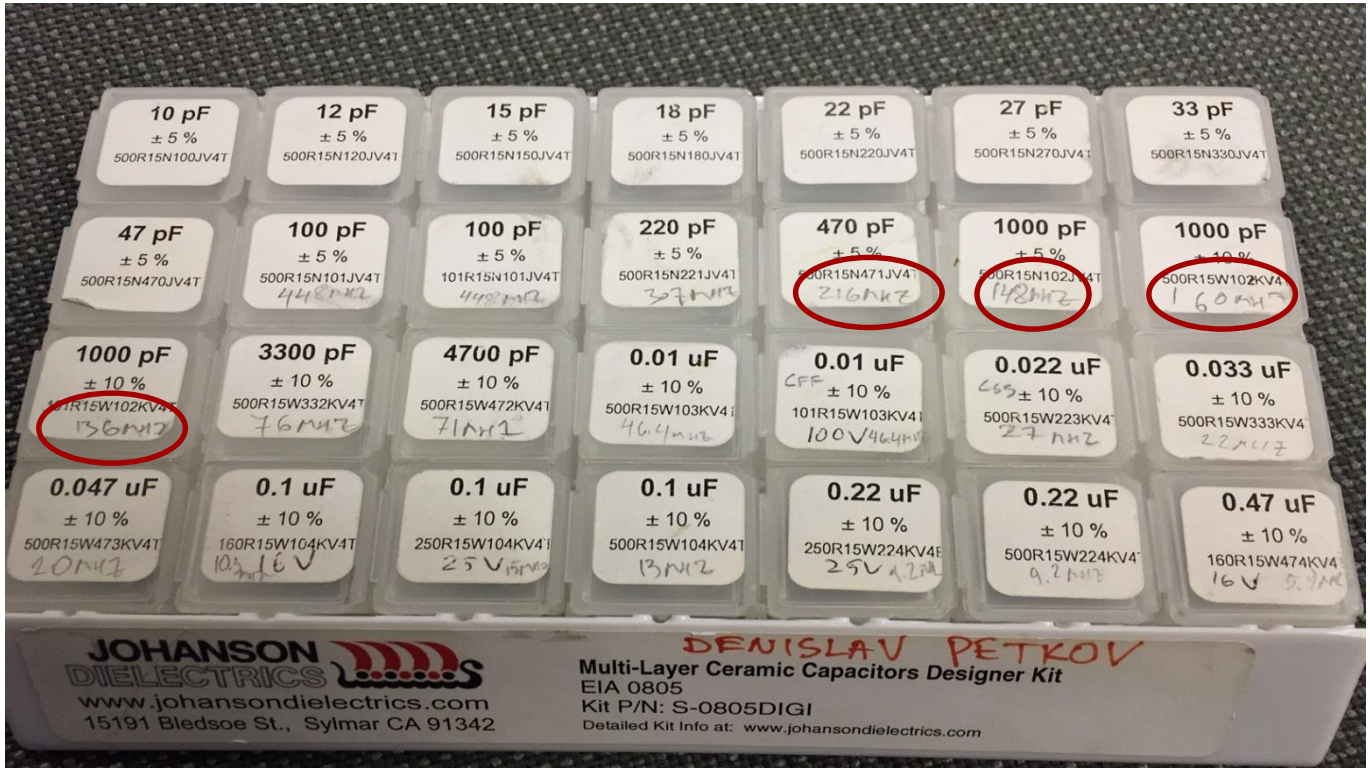
Reducing output ripple (HF)

- **Ceramic capacitor impedance (plot from manufacturer software)**

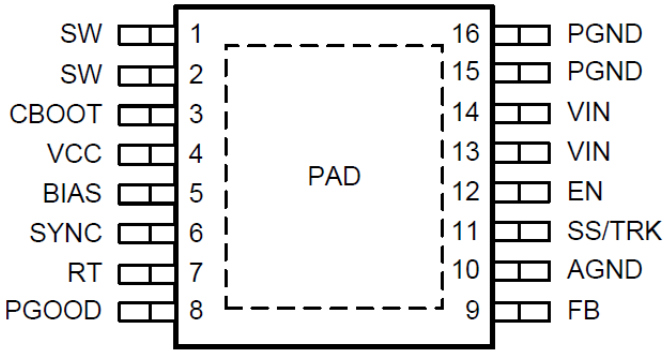


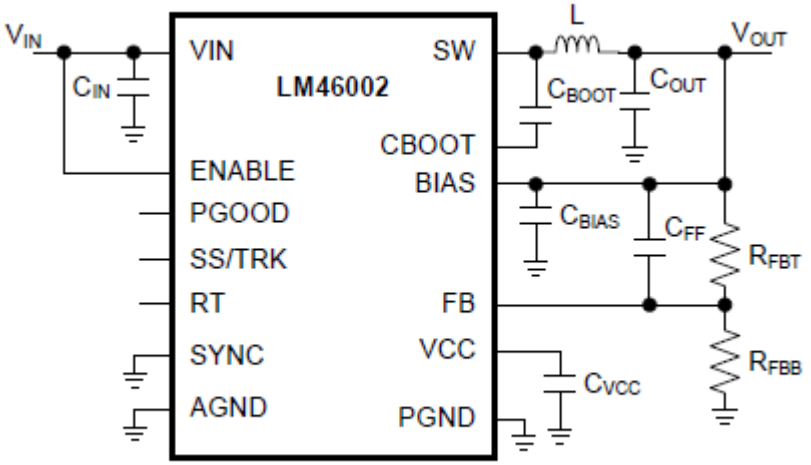
Reducing output ripple (HF)

- **Measure your caps**
- **Mark up your capacitor kit!**



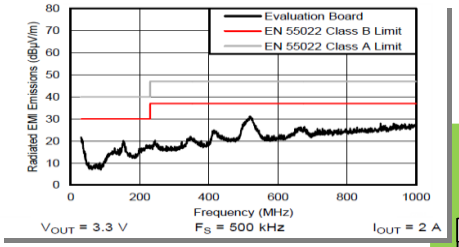
Gen6 SIMPLE SWITCHER®
easy-to-use pin out & schematic



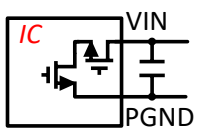


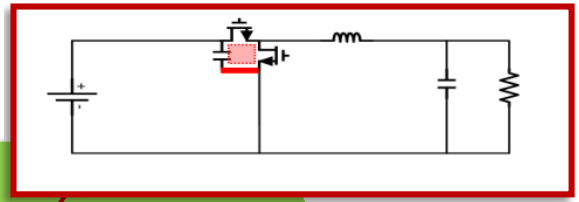
- Wide V_{IN} range 3.5V to 36V or 60V
- Low BOM count
- Good light load efficiency with DCM / PFM
- 27 µA operating quiescent current
- Full-featured: Soft Start, Tracking, Sync, Fs, PGOOD, UVLO, OCP, TSD

Pin-out optimized for EMI performance



Passes CISPR22 class B without filter





VIN Bypass

GND

GND

V_{OUT}

V_{IN}

COUT

L

CB

Cbias

CIN

CIN

SW
SW
CBOOT
VCC
BIAS
SYNC
RT
PGOOD

PGND
PGND
VIN
VIN
EN
SS/TRK
AGND
FB

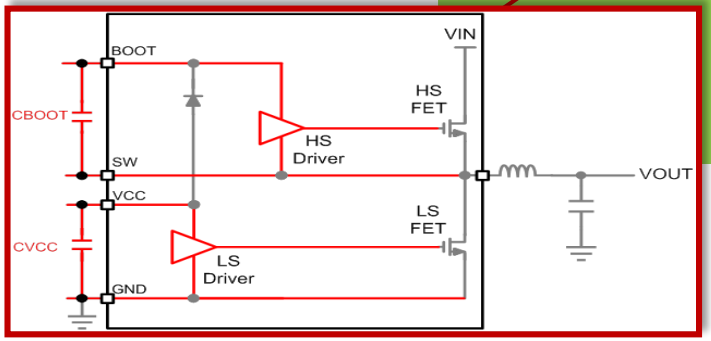
Rfb-bot

Rfb-top

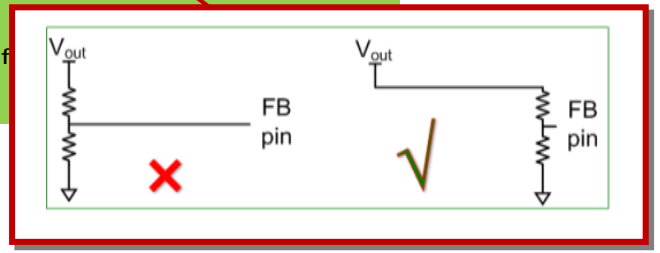
To Vout

Unbroken GND copper for thermal pef

Gate Drive



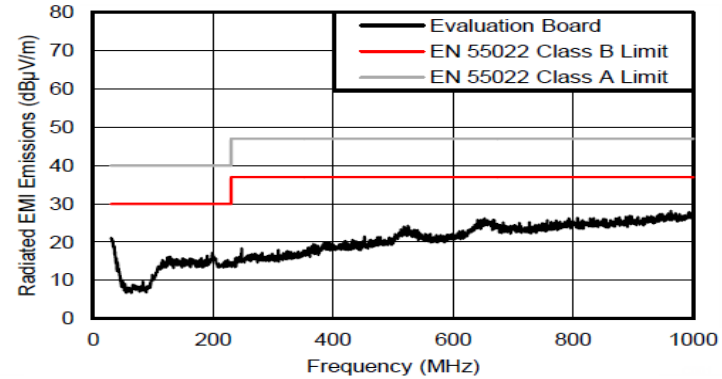
FB



LM43603 EMI performance

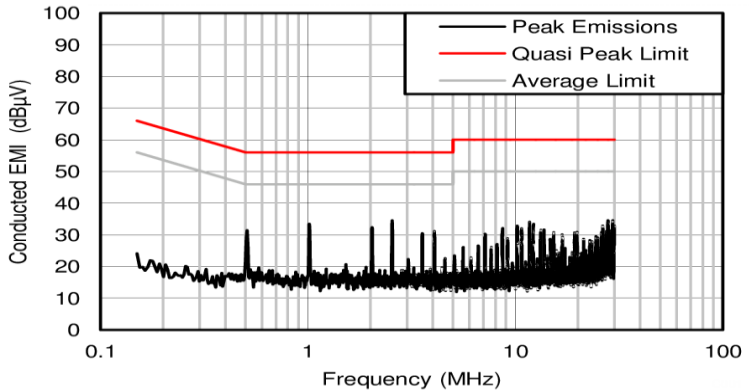
EMI curves on all 7 datasheets

Radiated

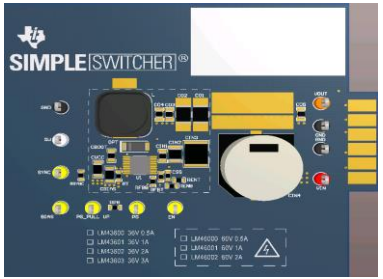


V_{OUT} = 3.3 V F_S = 500 kHz I_{OUT} = 3 A

Conducted



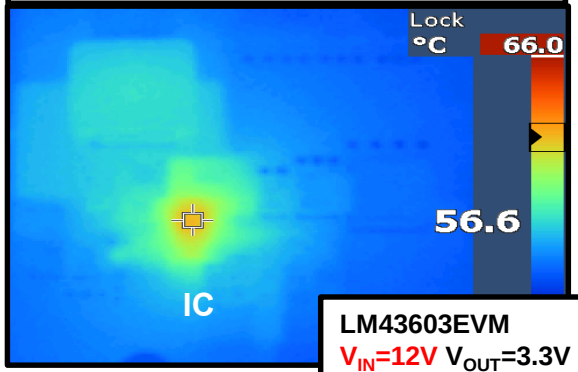
Measured on the LM43603PWPEVM with default BOM
No input filter used.



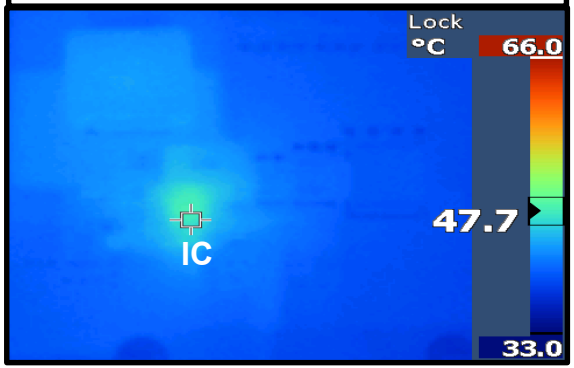
Measured on the LM43603PWPEVM with default BOM
Input filter: L_{IN} = 1 µH
C_d = 47 µF $C_{IN}4$ = 68 µF

LM43603 – 36V_{IN} 3A synchronous buck
Ta=25°C, EVM, 500kHz

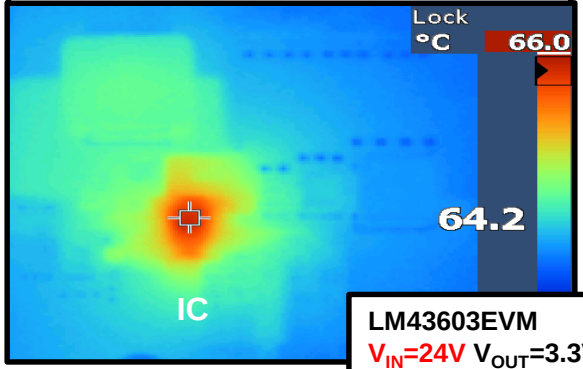
LM43603EVM
V_{IN}=12V V_{OUT}=3.3V I_{OUT}=3A



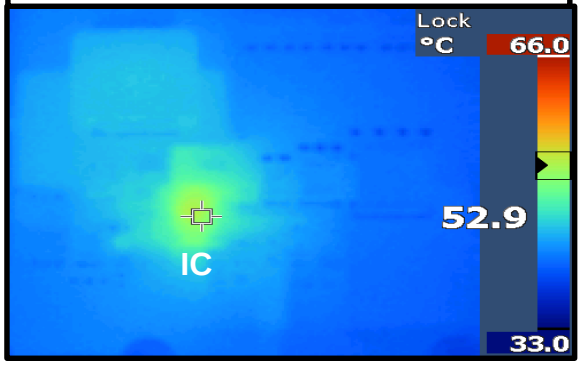
LM43603EVM
V_{IN}=12V V_{OUT}=3.3V I_{OUT}=2A



LM43603EVM
V_{IN}=24V V_{OUT}=3.3V I_{OUT}=3A

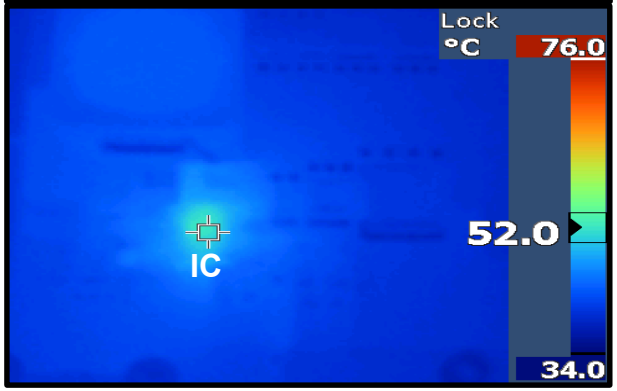


LM43603EVM
V_{IN}=24V V_{OUT}=3.3V I_{OUT}=2A

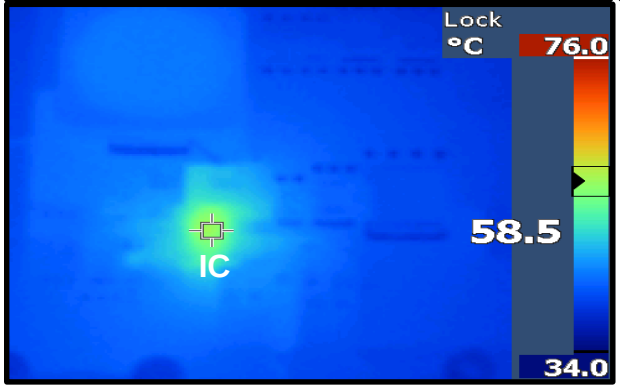


LM46002 – 60V_{IN} 2A synchronous buck
Ta=25°C, EVM, 500kHz

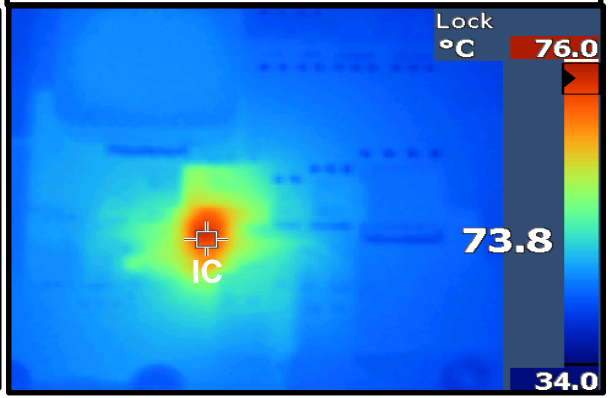
LM46002EVM
V_{IN}=12V V_{OUT}=3.3V I_{OUT}=2A



LM46002EVM
V_{IN}=24V V_{OUT}=3.3V I_{OUT}=2A



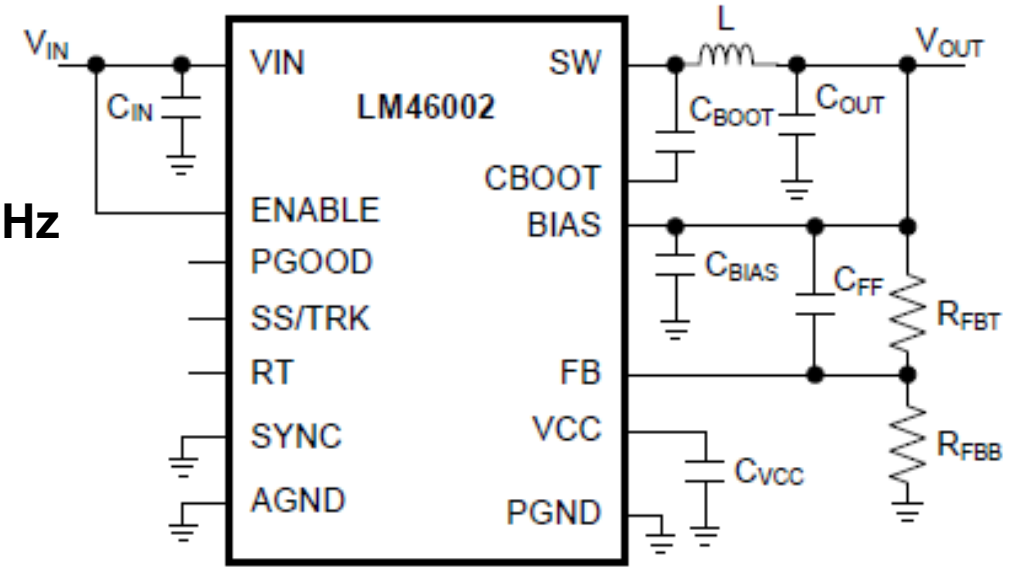
LM46002EVM
V_{IN}=48V V_{OUT}=3.3V I_{OUT}=2A



Flexible features for broad-market applications

- **Enable / UVLO**
- **PGOOD**
- **SS / Tracking / Prebias**
- **Programmable f_S: 200kHz to 2.2MHz**
- **Frequency synchronization**
- **Internal Compensation**
- **OCP / SC / TSD**
- **HTSSOP package**

- *EVM tested under EN55022/CISPR22 EMI standards*



Thanks!

Fore more information:

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