Debugging a Current Shunt Monitor Circuit - Layout

TI Precision Labs – Current Sense Amplifiers

Presented and Prepared by Patrick Simmons

Hello, and welcome to the TI precision labs series on current sense amplifiers. My name is Patrick Simmons, and I’m an applications engineer in the Current & Position Sensing product line. In this video, we will broach the topic of debug, beginning with board layout.

Sources of Error

Device Errors:

$$\varsigma_{RSS}(\%) \approx \sqrt{e_{Vos}{}^2 + e_{CMRR}{}^2 + e_{PSRR}{}^2 + e_{Gain\_error}{}^2 + e_{Linearity}{}^2 + e_{Shunt\_tolerance}{}^2 + e_{Bias\_current}{}^2 + e_{Other}{}^2}$$

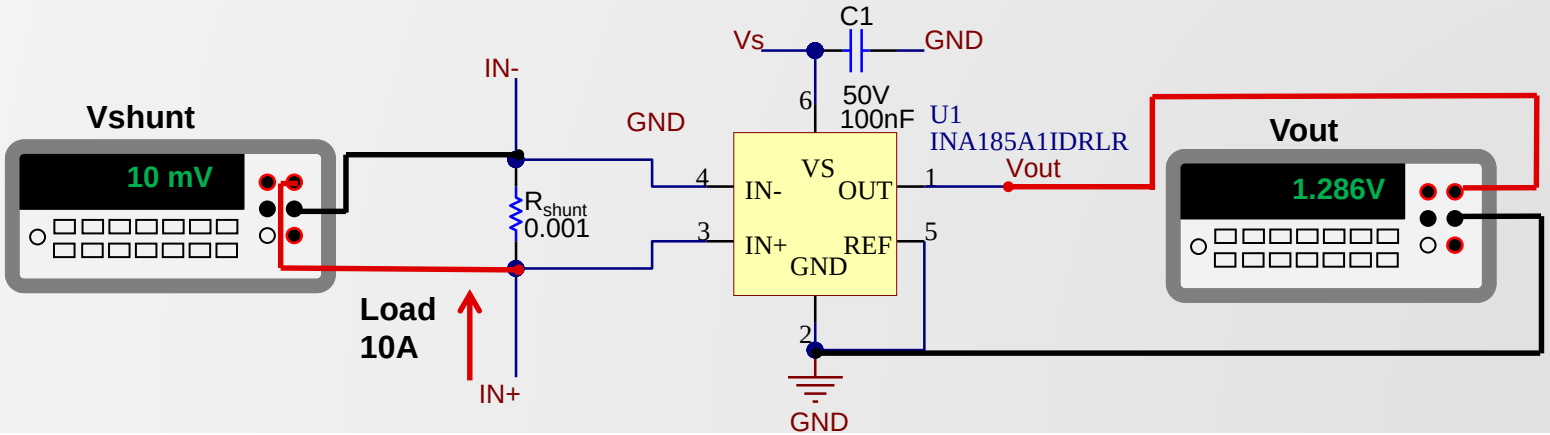
User Errors:

- Improper Layout
- Probe Placement
- Solder issues
- Overlooking device specifications
- Downstream circuitry
- Equipment and Settings
- Actual Fails

As you may have seen in our other videos, there are several sources of error that can make the measured output deviate from the ideal output. Aside from the shunt tolerance these are all inherent to the device and cannot be avoided. However, there is another set of errors that hinge on the user. These include improper layout, probe placement, solder issues, overlooking device specifications, downstream circuitry, equipment, and damaging the device. In the subsequent video series, we will cover a large yet non-exhaustive list of scenarios that lead to results that the untrained eye may overlook. We will then point out the source of error and provide a tip on how to avoid such an error. For this particular video, we will focus on errors related to improper layout.

Improper Layout: Case 1

Conditions



Calculations

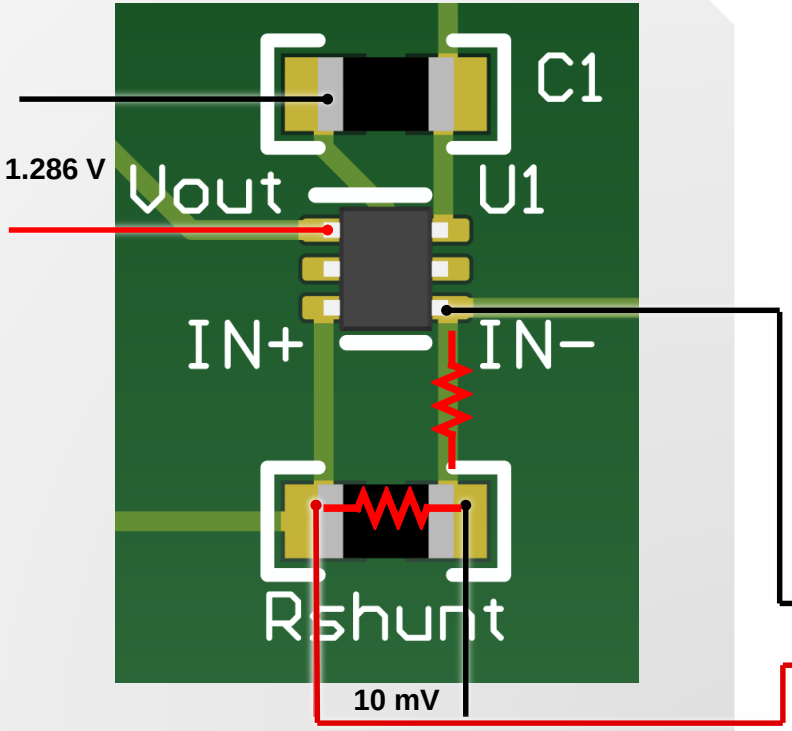
$$Vshunt = Load \times R_{shunt} = 10A \times 0.001\Omega = 10mV$$

$$\text{Expected } V_{out} = Vshunt \times Gain = 0.01V \times 20\frac{V}{V} = 200\text{mV}$$

Our first case study results from us trying to measure 10A across a 1mΩ shunt. Based off of our calculations, we expect the output should be roughly 200mV referenced to ground. However, when we take measurements with our multimeters, we observe something that defies expectation. While our input measurement is 10mV, our output is way off at 1.286V. What could be the issue here? Our schematic looks correct. Do we have a defective or damaged part?...Lets look at some more details.

Improper Layout: Case 1

Conditions



Source of Error

- Board Trace Resistance Neglected

$$R_{trace} = \frac{resistivity \times Length}{Thickness \times Width} = \frac{\rho_{Cu} \times L_{trace}}{T_{trace} \times W_{trace}}$$

$$\rho_{Cu} = 1.74 \times 10^{-8} \Omega m$$

$$L_{trace} = 0.00269m$$

$$T_{trace} = T_{1oz.\,Cu} \times number\ or\ oz. = 0.0000347m \times 1 = 0.0000347\text{m}$$

$$W_{trace} = 0.000254\text{m}$$

$$R_{trace} = \frac{(1.74 \times 10^{-8} \Omega m) \times (0.00269m)}{0.0000347\text{m} \times 0.000254\text{m}} = 5.43m\Omega$$

$$R_{tot} = R_{Shunt} + R_{trace} = 6.43m\Omega$$

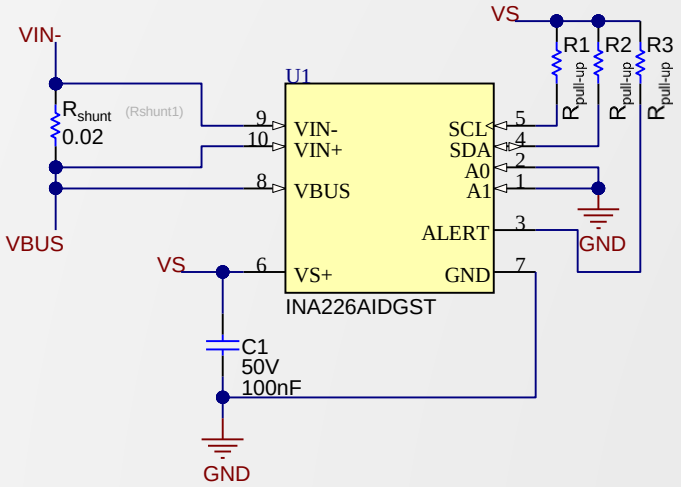
$$V_{Sense} = Load \times R_{tot} = 10A \times 6.43m\Omega = 64.3\text{mV}$$

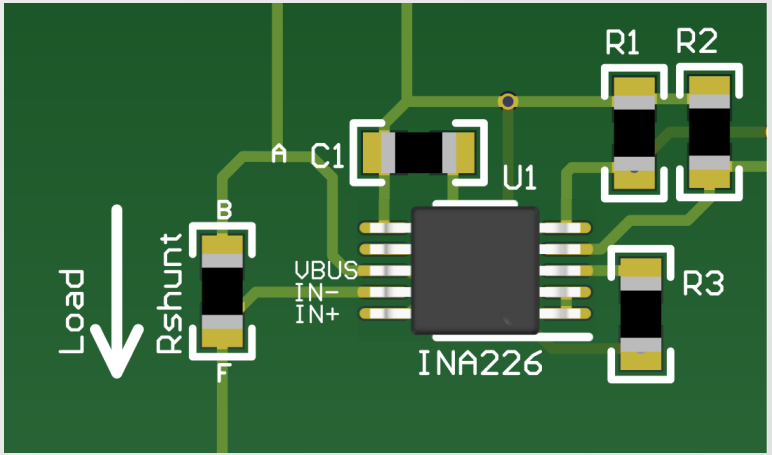
$$V_{out} = V_{Sense} \times Gain = 64.3mV \times 20\frac{V}{V} = 1.286V$$

Here is the board layout along with where we are probing. Now we can see the source of our error, the board trace. The IN- board trace is actually in the direct path of the load, and therefore is in series with Rshunt. As shunts typically have small resistances, any series trace resistance can significantly increase the differential sense voltage detected by the current shunt monitor and therefore increase the output of the device. In this particular case, we calculate the series trace resistance to be 5.43mΩ, which leads to 64.3mV being measured by the INA185, thereby making the INA185 output 1.286V.

Improper Layout: Case 2

Conditions



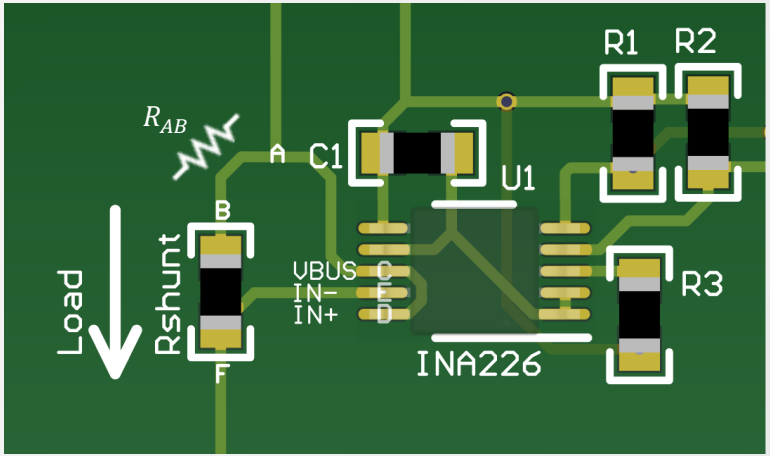


$$V_{shunt} \neq V_{shunt}\ Register\ Value$$

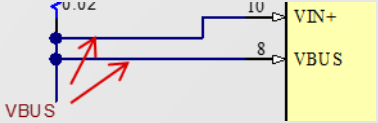
Now lets look at another case. Here we have one of our digital power monitor devices, the INA226, measuring some load. Yet again, we are getting a discrepancy between the measured input and the expected output. As the schematic yet again looks flawless, we decide to take a closer look at the board layout. Based off the prior case, can you see what the issue might be?

Improper Layout: Case 2

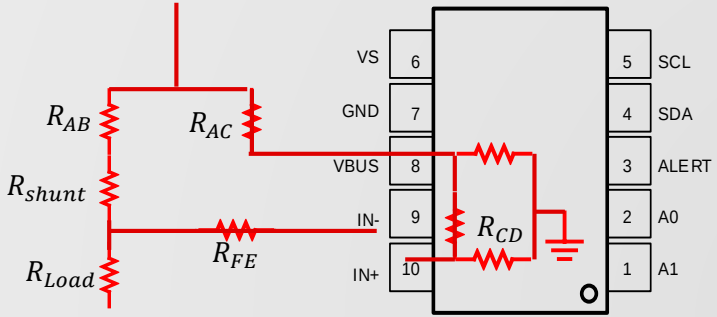
Source of Error



- Parasitic Series Resistor
- Connected IN+ through VBUS pin
  - Can happen if you are connecting according to trace net names



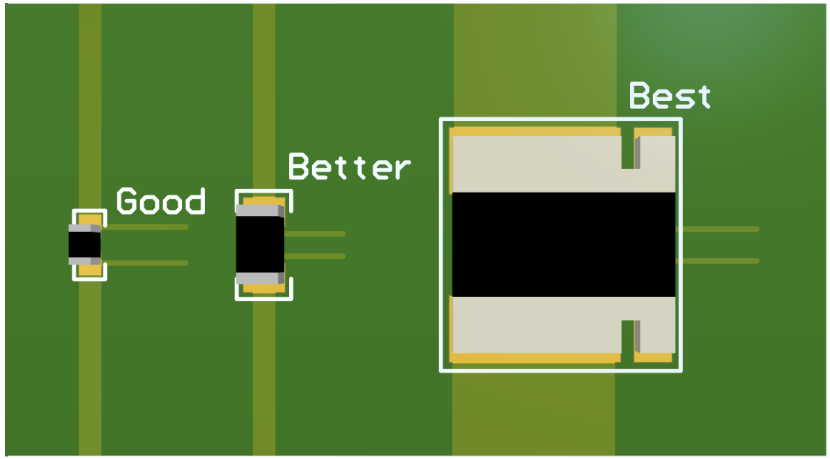
- Asymmetric input Traces, $R_{AC}+R_{CD} \neq R_{FE}$

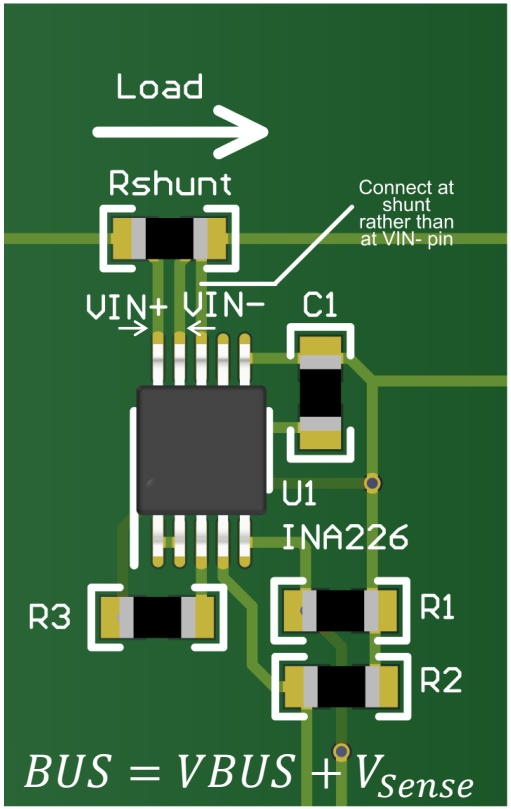


If you guessed this trace from node B to node A would contribute error because it is in series with Rshunt and contributes to the sensed voltage potential, you are correct, however, there are some other details to consider. The paths from the shunt to the input pins are not equal. This imbalance in trace lengths can contribute error due to the input bias current sunk into the device input pins, especially as the traces get longer and the difference in their lengths becomes greater. Also, the impedance from VBUS to GND is not equivalent to IN+ to GND, thereby pulling more input bias current across the unequal input traces. To avoid these issues when doing your layout, use differential pair routing for your sense inputs as this should inherently maintain equal resistance for both traces. Also do not route your sense input trace through VBUS.

So having seen two instances of improper layout, you might ask, what does good layout look like?

Good Layout Examples





Check precision resistor data sheets to see if the manufacturer calls out where the resistance is measured.

Here on the left we show three different ways to layout shunt traces. On the left we have a relatively small shunt, where the input traces tap directly at the shunt pads. In the middle example we have a slightly bigger shunt, which allows us to tap into the shunt pad side, facing into the shunt. The last approach on the right shows a resistor with dedicated sensing connection pads. You may hear these pads referred to as kelvin connections. The basic goal of a Kelvin connection is to remove the sensing connection from the main path of current flow, which is what all of these recommended layouts do. Dedicated Kelvin sense connections become extremely important for high current/low-Rshunt applications because the solder can add resistance to conduction path.

As for the traces between the shunt and the current monitor, we recommend that both traces be symmetric. Additionally for high-side sensing with power monitors that are not preceded by an input filter, we recommend the Bus pin connected as such. This allows any current sunk through the bus pin to be detected in the current measurement. The actual Bus voltage can then be determined by summing both the vbus and vsense voltages.

Summary

- Layout can be source of error
- A schematic omits parasitic board components
- Traces in series with small resistors such as the shunt matter
- Be careful when wiring based off of net names
- Be sure to use Kelvin connections for measuring across the shunt

As stated in the opening, layout can be a source of error and may need to be assessed when performing debug. The layout is particularly important due to shunt resistors having resistance on an order of magnitude similar to board traces. The best way to eliminate any impact of board trace resistance is with kelvin connections and symmetric input traces, which requires vigilance when wiring based on board net names.

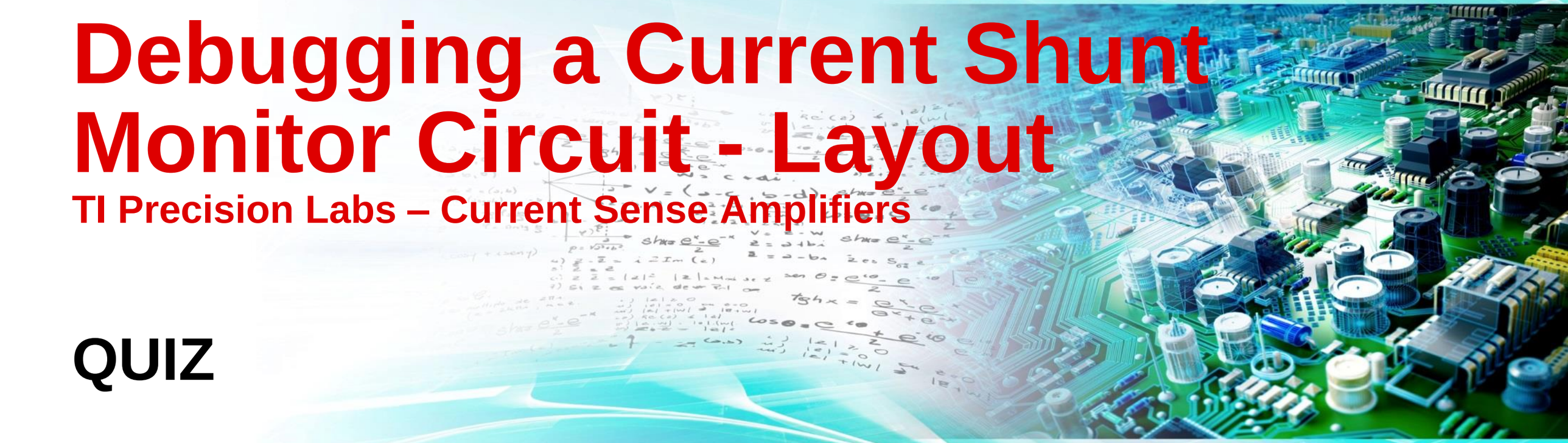
To find more current sense amplifier technical resources and search products, visit ti.com/currentsense

That concludes this video - thank you for watching! Please try the quiz to check your understanding of the content.

For more information and videos on current sense amplifiers please visit ti.com/currentsense.

Debugging a Current Shunt Monitor Circuit - Layout

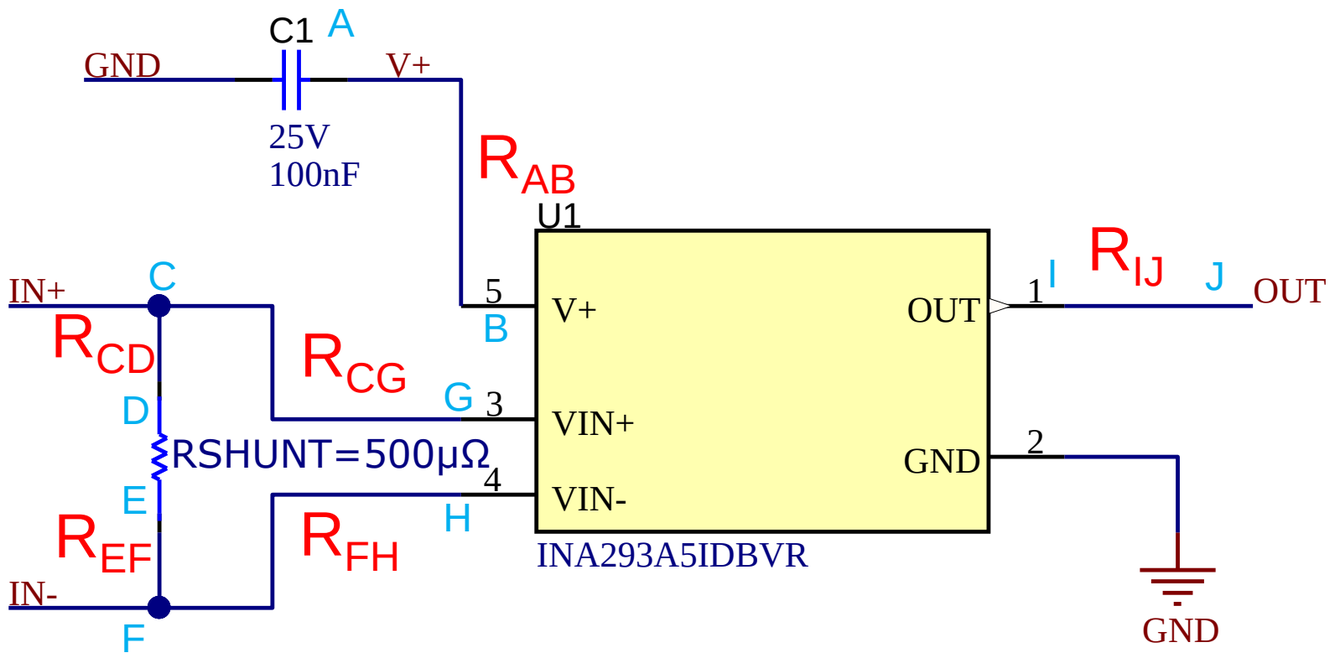
TI Precision Labs – Current Sense Amplifiers



QUIZ

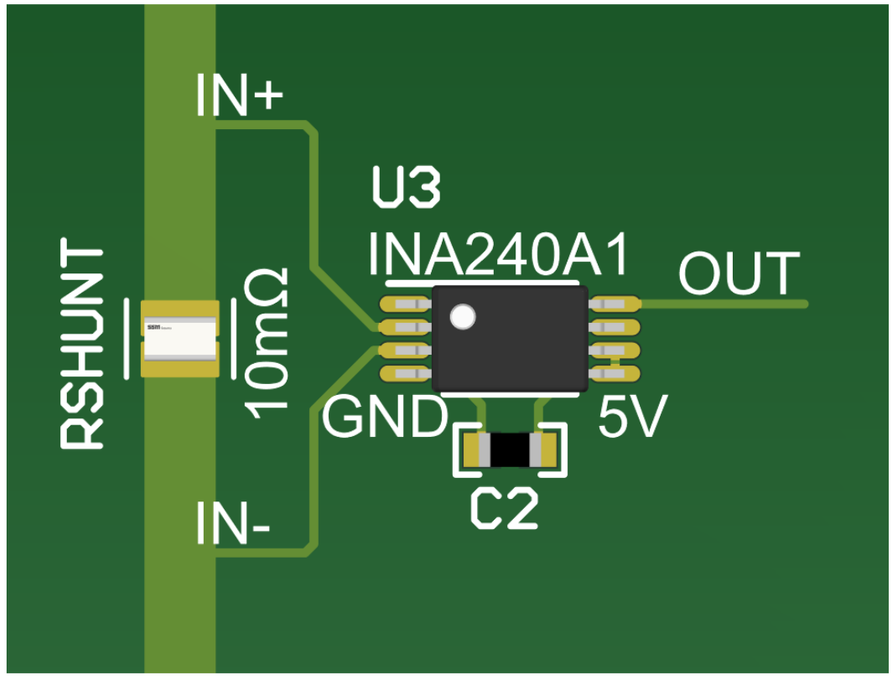
Debugging a Current Shunt Monitor – Layout – Quiz

1. For a DC measurement, what unaccounted resistances in this schematic are important?
   a) R_{AB}
   b) R_{CD} & R_{EF}
   c) R_{CG} & R_{FH}
   d) R_{IJ}
   e) None of the above
   f) R_{CD}, R_{EF}, R_{CG}, and R_{FH}



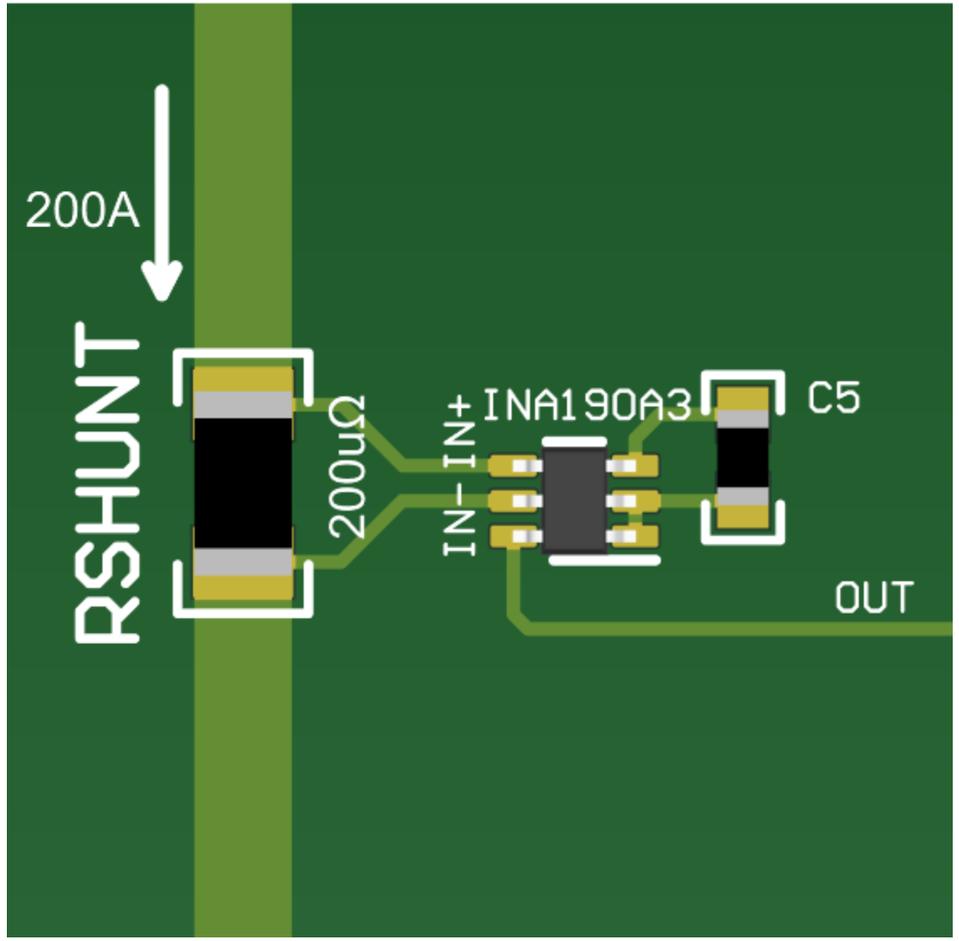
Debugging a Current Shunt Monitor – Layout – Quiz

2. What might the error from this layout look like?
   a) Gain Error
   b) Offset Error
   c) An open between the input pins
   d) All of the Above
   e) None of the above



Debugging a Current Shunt Monitor – Layout – Quiz

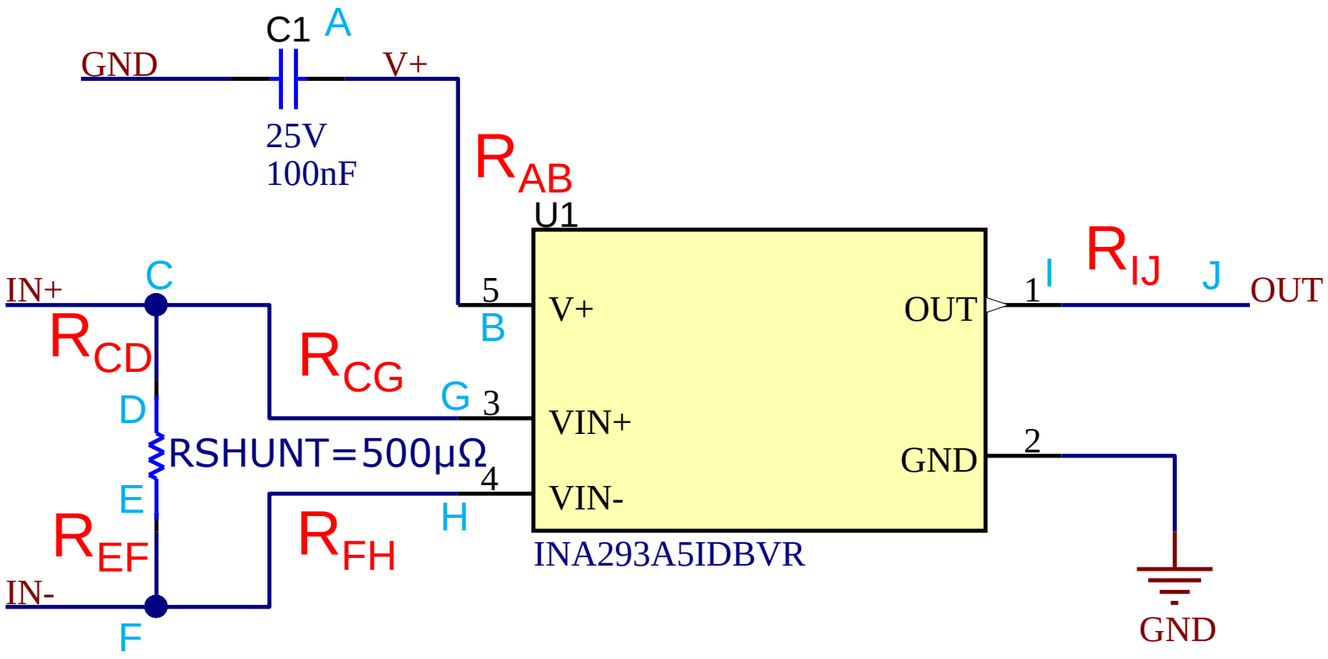
3. Is this shunt layout optimized?
   a) Yes
   b) No



Answers

Debugging a Current Shunt Monitor – Layout – Quiz

1. For a DC measurement, what unaccounted resistances in this schematic are important?
   a) R_{AB}
   b) R_{CD} & R_{EF}
   c) R_{CG} & R_{FH}
   d) R_{IJ}
   e) None of the above
   f) R_{CD}, R_{EF}, R_{CG}, and R_{FH}

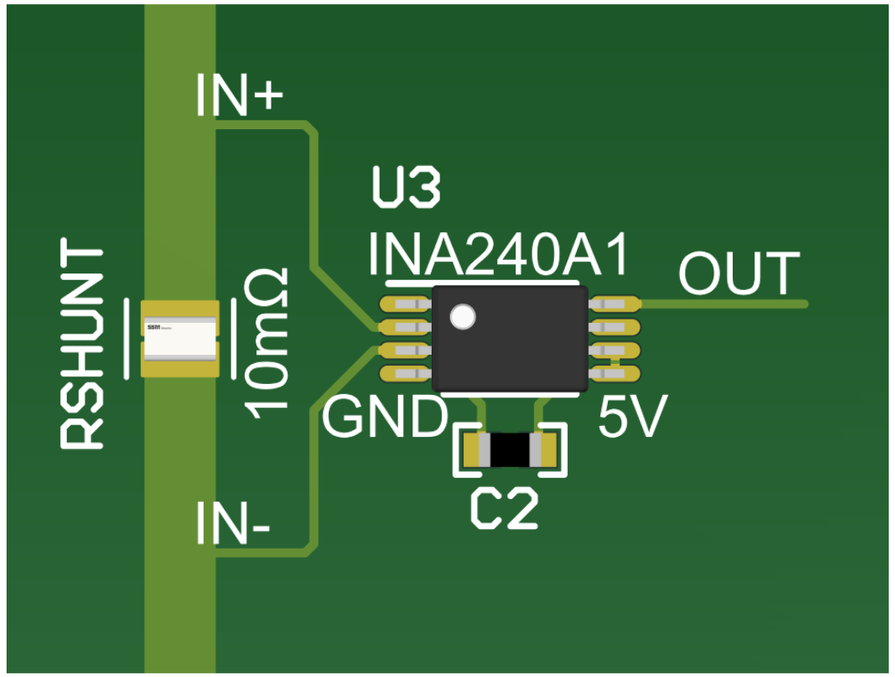


In this example Rshunt = 500uΩ, which may actually be lower than some of the trace resistances on you pcb board. Any series resistances found at R_{CD} and R_{EF} will have significant impact on your measurement error. Resistances R_{CG} and R_{FH} will also have impact, but it will likely only be relevant if you have long traces and or wires between the shunt and device. Typically, these paths only become important when you include input filter resistors. If R_{CG} and R_{FH} are large resistance this can introduce a noticeable gain error. Large mismatches in these resistances will further compound that error.

Debugging a Current Shunt Monitor – Layout – Quiz

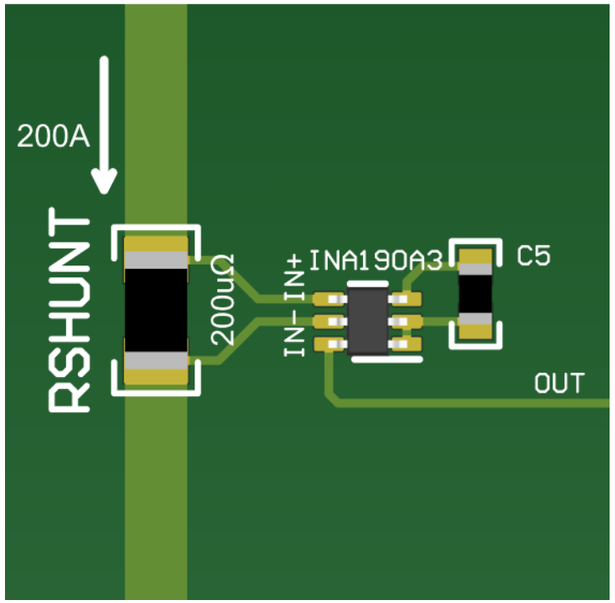
2. What might the error from this layout look like?
   a) Gain Error
   b) Offset Error
   c) An open between the input pins
   d) All of the Above
   e) None of the above

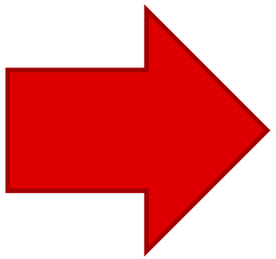
Gain error, is the most accurate answer. For a single measurement at low current, the trace resistance in series with the shunt will make the output look larger than it should. This may initially suggest an offset error. Additionally, if a single measurement is performed with sufficiently high load, the output might rail suggesting the shunt is open. However, further measurements will reveal that the output simply ramps up much quicker than ideal device gain specifications suggest, thereby indicating a gain error.

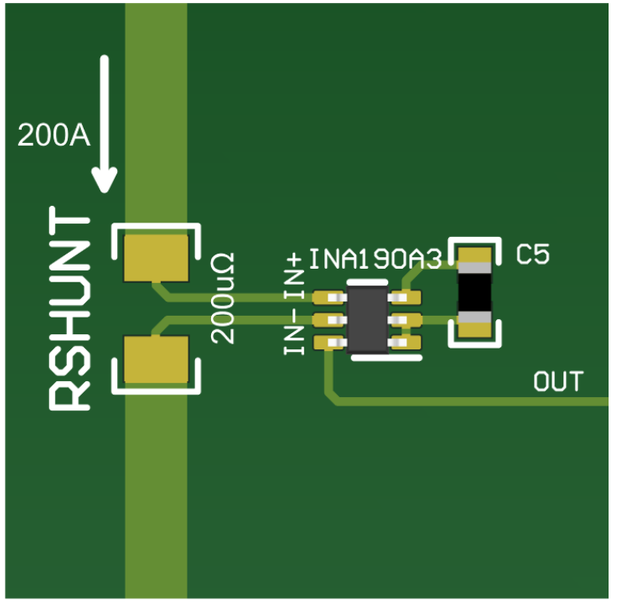


Debugging a Current Shunt Monitor – Layout – Quiz

3. Is this shunt layout optimized?
   a) Yes
   b) No







The connections to the shunt are ok for relatively small loads and large shunts. However, in this case we are measuring 200A with a 200uΩ shunt. For this type of shunt without dedicated Kelvin connections, it would be better to have the shunt to device input traces connecting to the inner facing pads of the shunt.