Demonstrating Simple Open Real-Time Ethernet Protocol (SORTE) Master & Slave on PRU-ICSS using Processor SDK RTOS

SORTE support

SORTE on PRU-ICSS		
Processor	Hardware	RTOS
AM572x	AM572x Industrial Development Kit (IDK)	✓
AM571x	AM571x Industrial Development Kit (IDK)	✓
AM437x	AM437x Industrial Development Kit (IDK)	✓
AM335x	AM335x Industrial Communications Engine (ICE)	✓
66AK2Gx	K2G Industrial Communications Engine (ICE)	✓

Agenda

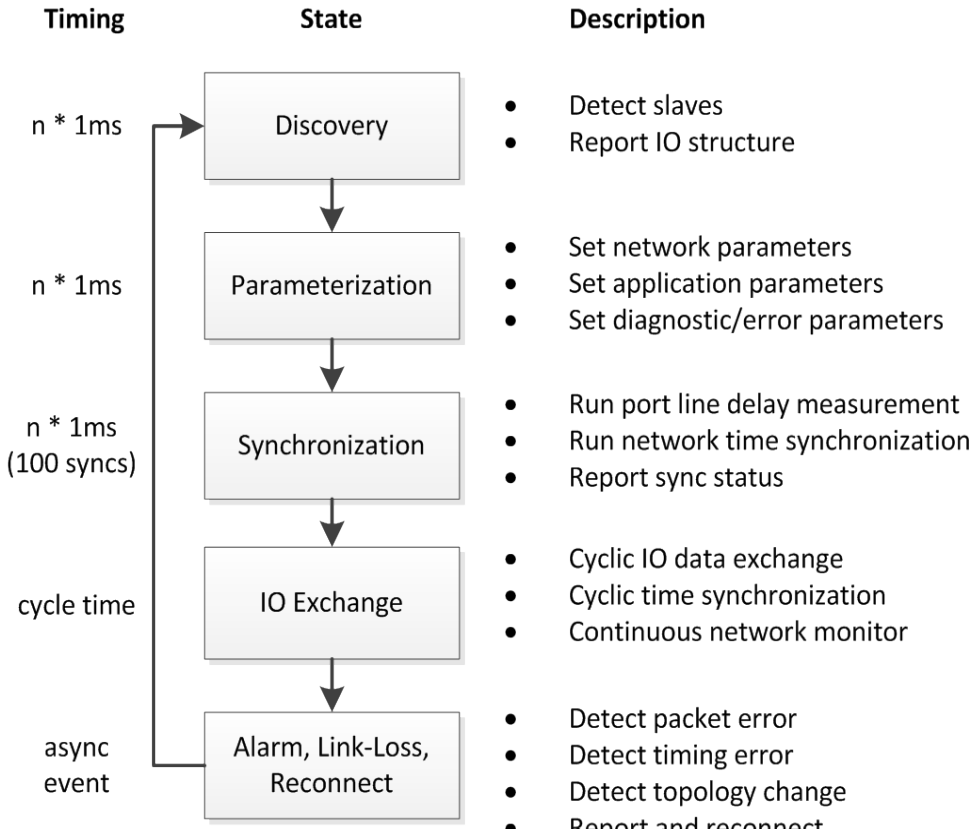
- SORTE Overview
- SORTE State Machine
- ARM Processor Overview

- SORTE Source Code

Simple Open Real-Time Ethernet (SORTE) overview

- Fast and efficient real-time Ethernet protocol implementation on PRU-ICSS:
  - Master and device(s) network line topology
  - 4µs cycle time for process data exchange with one master and up to four slave devices
  - 100 Mbit, full-duplex
- Removes external ASIC or FPGA support and integrates industrial Ethernet.
- Training and programming example for real-time Ethernet on PRU-ICSS:
  - Fully-customizable PRU firmware
  - PRU firmware provided in source code
  - Reference PRU firmware with User's Guide, PRU firmware, and ARM driver software.

SORTE state machine



ARM application overview

The SORTE master and slave applications running on the ARM support the following:

- Board level initialization
- Initialization of PRU-ICSS subsystem, which includes clearing PRU-ICSS shared memory and pru0/pru1 data RAM memory, configuration of PRU-ICSS registers, and initialization of the 8-bit CRC table
- Initiation of PRU shared memory with PRU-ICSS PHY addresses and enabling MDIO link interrupts for each PRU-ICSS PHY
- Downloading Master/Slave protocol firmware
- Displaying status information through the on-board UART console

SORTE demonstration: Hardware requirements

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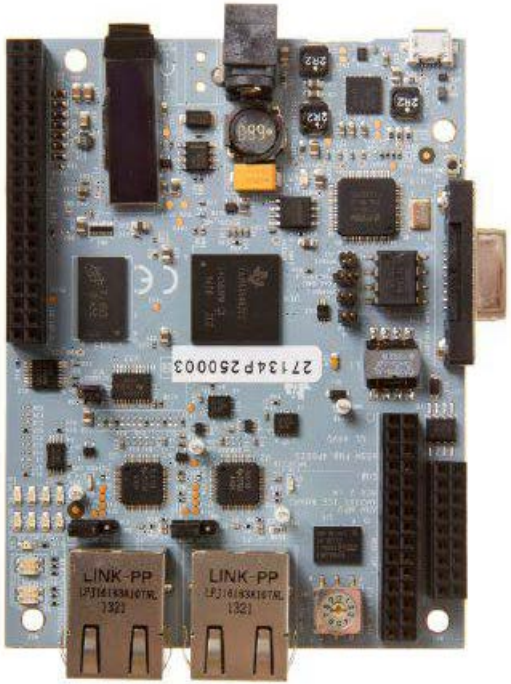
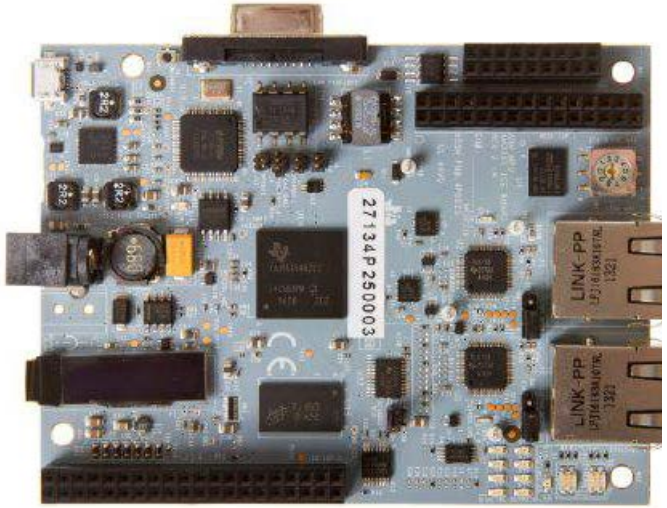
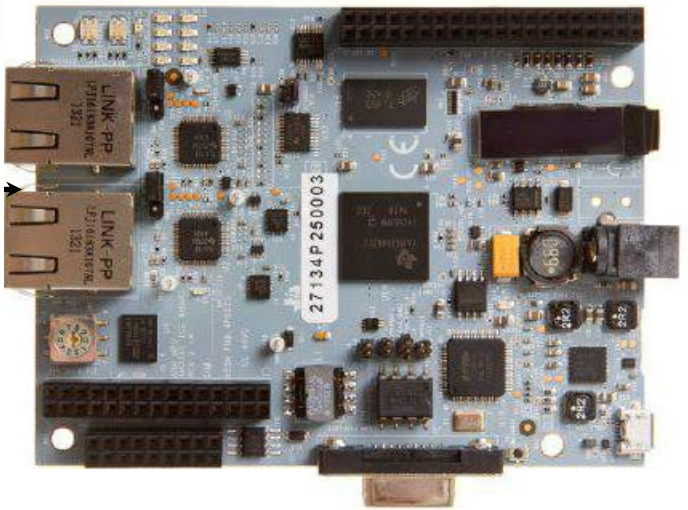
AM335x ICE



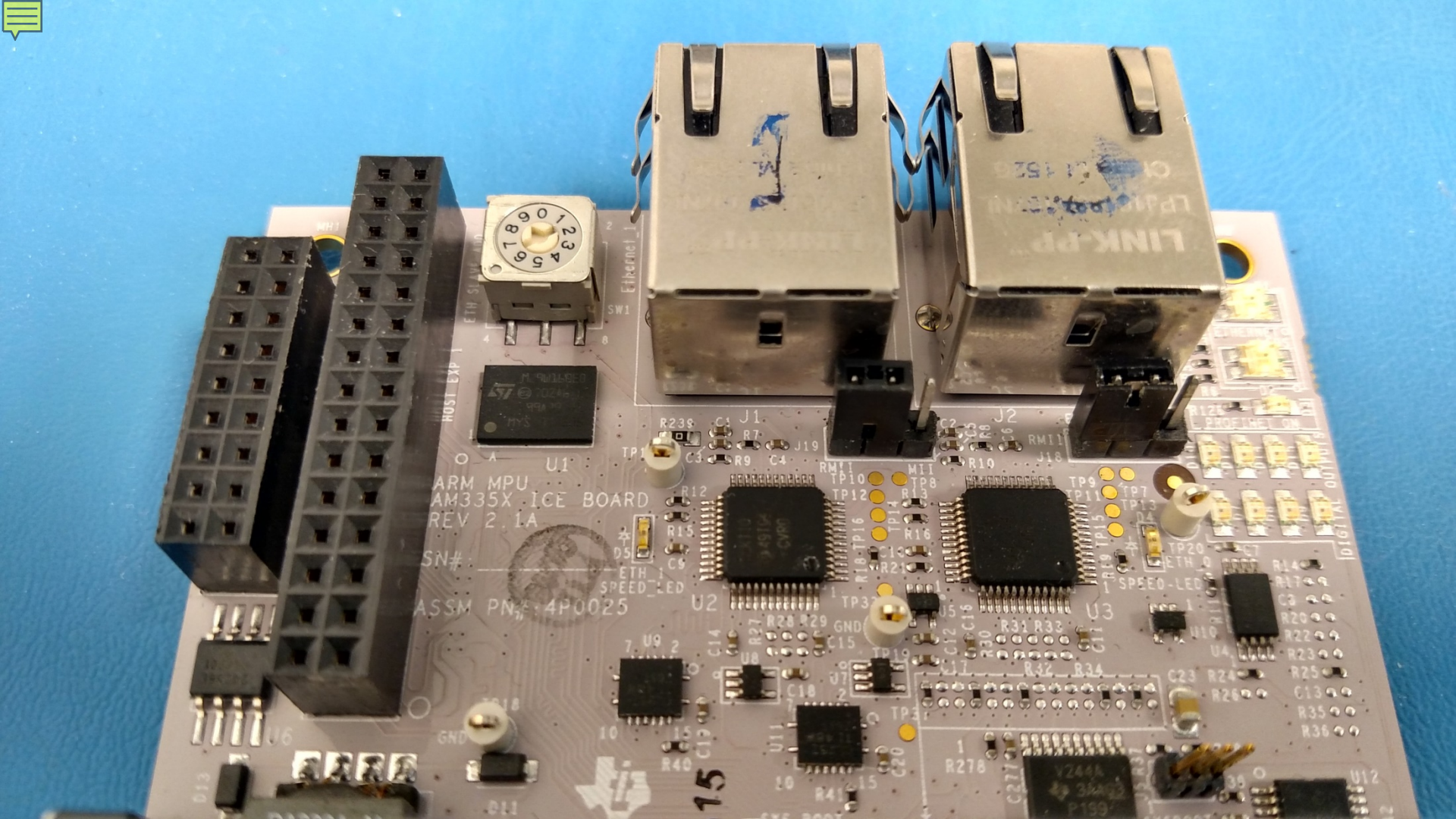
AM335x ICE



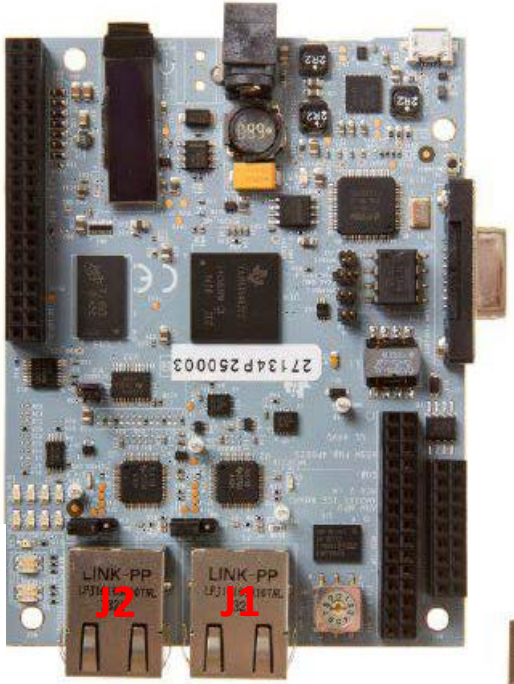
AM335x ICE



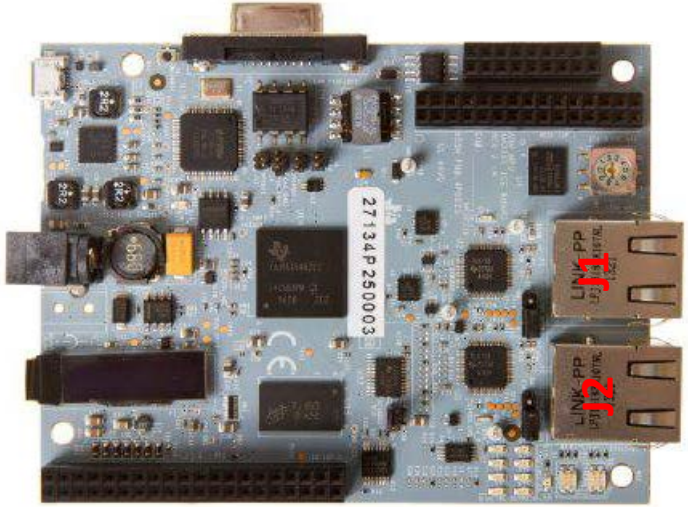
AM3359 Industrial Communications Engine (ICE): http://www.ti.com/tool/tmdsice3359


ARM MPU
AM335X ICE BOARD
REV 2.1A
SN#:
ASSM PN#: 4P0025
U1
U2
U3
J1
J2
SW1
Ethernet 1
Ethernet 2
HOST EXP 1
ETH SLAVE 1
ETH_1 SPEED_LED
ETH_2 SPEED_LED
LINK-PP
15

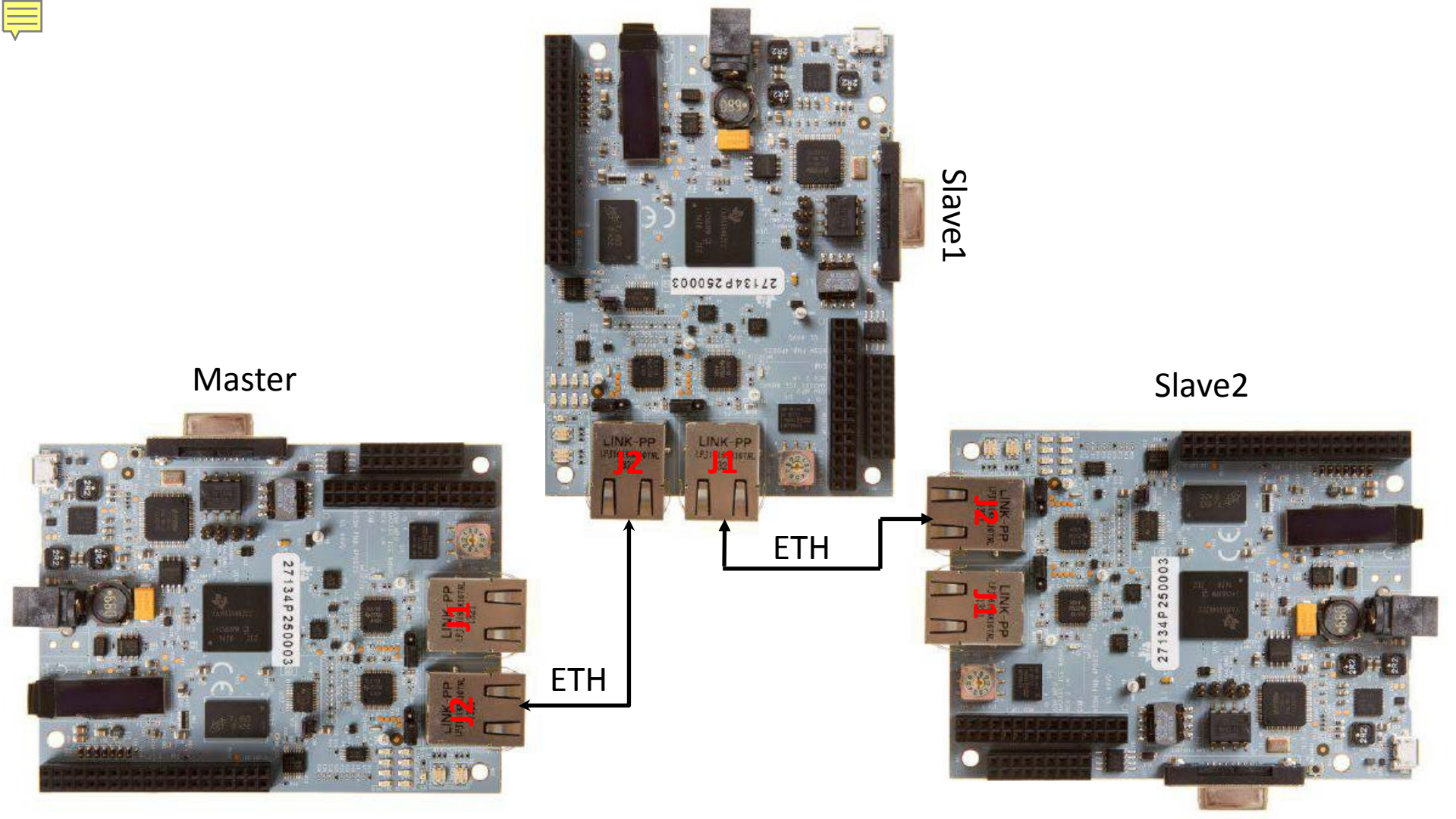
Slave1



Master



Slave2


Slave1
Master
Slave2
J2
J1
J1
J2
J2
J1
ETH
ETH

SORTE demonstration: Software requirements

Download Processor SDK: http://www.ti.com/tools-software/processor-sw.html

Processor SDK Developer's Guide - PRUSS SORTE:
http://processors.wiki.ti.com/index.php/Processor_SDK_RTOS_PRUSS_SORTE

SORTE demonstration: Build applications

Console:

Navigate to /packages

Run pdksetupenv.bat

Console: Build ARM Application for Master and Slave Devices

Navigate to /packages/ti/drv/pruss

Run gmake apps

SORTE demonstration: Load & run applications

CCS:

Launch target configuration

CCS:

Connect cores
Load gel
Load master binary
Load slave binary
Run the demo

SORTE demonstration: Verify SORTE functionality

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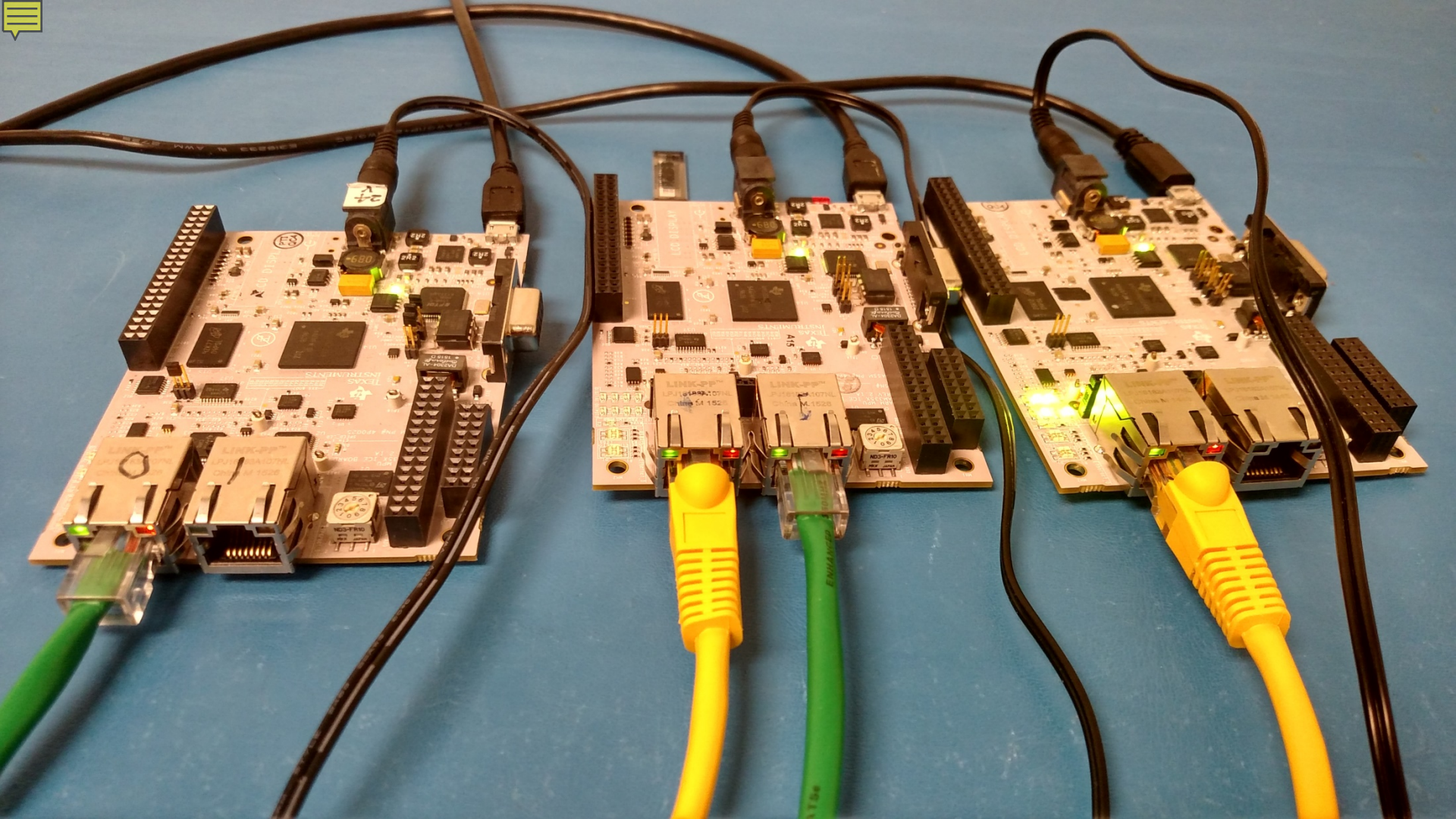

SORTE code organization

The SORTE ARM applications and firmware sources are located in the following directory:

<PDK>\packages\ti\drv\pruss\example\apps\sorte

The \sorte directory layout:

\firmware	
\bin	Pre-compiled SORTE firmware binaries
\src	
\include	SORTE firmware common header files
\master	README.txt, firmware sources, and header files for MASTER device
\slave	README.txt, firmware sources, and header files for SLAVE device
\master	SORTE makefile for MASTER application running on ARM
\slave	SORTE makefile for SLAVE application running on ARM
\src	SORTE ARM application source and build-related files
README.txt	Overview of protocol and directory structure.

Modify the source code

For more information

- Simple Open Real-Time Ethernet (SORTE) Master With PRU-ICSS Reference Design: http://www.ti.com/tool/tidep-0085
- Simple Open Real-Time Ethernet (SORTE) Slave With PRU-ICSS Reference Design: http://www.ti.com/tool/tidep-0086
- 4-Axis CNC Router with 250 kHz Control Loop with PRU-ICSS based on SORTE Reference Design: http://www.ti.com/tool/TIDEP0061
- PRUSS SORTE Wiki: http://processors.wiki.ti.com/index.php/Processor_SDK_RTOS_PRUSS_SORTE
- AM3359 Industrial Communications Engine: http://www.ti.com/tool/tmdsice3359
- Processor SDK for AM335x Sitara Processors: http://www.ti.com/tool/processor-sdk-am335x
- Download Code Composer Studio: http://processors.wiki.ti.com/index.php/Download_CCS
- Projects and Build Handbook for Code Composer Studio (CCS): http://software-dl.ti.com/ccs/esd/documents/users_guide/sdto_ccs_build-handbook.html
- For questions about this training, refer to the E2E Community Forums for Sitara Processors at http://e2e.ti.com/support/arm/sitara_arm/f/791/t/277411