Layer	Name	Material	Thickness	Constant	Flex Layer Stack
1	Top Overlay				
2	Top Solder	Kapton	2.00mil	3.5	
3	Top Layer	Copper	1.00mil		
4	Dielectric 1	Kapton	3.00mil	4.2	
5	Bottom Layer	Copper	1.00mil		
6	Bottom Solder	Kapton	2.00mil	3.5	
7	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 10 MIL
MIN. CLEARANCE: 7 MIL
MIN. VIA PAD SIZE: 16 MIL
MINIMUM ANNULAR RING 5.90 MIL EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER KAPTON
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER 10mil
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER _____

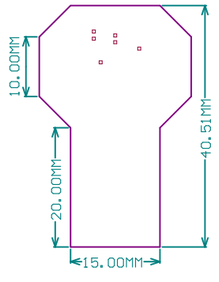
BOARD FINISH:
SILKSCREEN: [X] TOP [ ] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK



Symbol	Count	Hole Size	Plated	Hole Type
□	6	0.203mm (8.00mil)	PTH	Round
	6 Total			

Drill Table
FOR 8MIL DRILL +0/-8MIL

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-01614_TMP117
DESIGNED FOR: Public
FILE NAME: TIDA-01614_TMP117.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01614_TMP117	REV: EI	SVN REV: EI
LAYER NAME = Drill Drawing	TID #: TIDA-01614_TMP117		
PLOT NAME = Fabrication Drawing	GENERATED : 4/2/2019 4:35:57 PM	TEXAS INSTRUMENTS	

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:	LAYOUT BY:
S LENI	AVINASH
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1