

FABRICATION NOTES:

- FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2, PER IPC-6011.
PCB SHALL BE MANUFACTURED USING 1-SPEED OR EQUIVALENT.
2. MATERIALS:
1. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/128.
(MIN. TS 180)
 2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-M-99, UNLESS OTHERWISE SPECIFIED.
MINIMUM WEIGHT FOR INTER DIGITAL LAYERS AND INNER PLANE LAYERS TO BE 150M (1 OZ.).
FOR OUTER LAYERS 1.31 OZ. COPPER WEIGHT IS TO BE CONSIDERED "THINNEST".
THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012E TABLE NO.3-7 AND 3-8.
 3. ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION.
LAYERS TO LAYER REGISTRATION SHALL BE WITHIN 0.127MM.
 4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
 5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCREASE FOR MATCHING
INTEGRATION SHALL APPROVE THE MODIFIED WIDTHS AND SPACING.
TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
 6. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
 7. FINISHES:
 1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG,
ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-4 MICRONS, TYPICAL IMMERSION GOLD
THICKNESS SHALL BE 0.8-0.9 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
 2. APPLY LIQUID HOTPOT IMAGEABLE SOLDER MASK PER IPC-SM-845, CLASS R, TO BOTH SIDES OF THE BOARD OVER BARE COPPER.
VIA HOLES THAT HAVE MASK OPEN SHALL BE FILLED WITH NON CONDUCTIVE DIE AND CAP FLATTED.
IF THE SOLDER MASK FILLED WITH NON CONDUCTIVE DIE AND CAP FLATTED WITH SOLDER MASK,
ONLY SOLDERABLE IMAGES THAT ARE 0.08(0.003)" PER SIDE SHALL BE REDUCED IF REQUIRED.
OTHER OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN.
 3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE
NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED
IF THE SILK SCREEN FALLS ON SOLDERABLE AREA.
 4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 200M (0.00079)". INCREASE OF LAYER
VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 120M (0.00471)" AND BORED VIA'S SHALL NOT BE LESS THAN 150M (0.00471)".
 5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANT TO IPC6012, CLASS 2.
 8. MARKING:
 1. BOARD SHALL MEET THE REQUIREMENTS OF UL-7968 WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, UL FILE NUMBER,
MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTERS SHALL BE RENDERED IN SILKSCREEN.
 9. TEST REQUIREMENTS:
 1. 100% NET ELECTRICAL VERIFICATION USING METRAX SUPPLIED IPC-316 NET LIST FOR OPENS AND SHORTS.
 2. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
 3. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
 4. FINISHED PCB THICKNESS SHALL BE 0.085" +/-0.01.
 5. MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/0.003".
 6. ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.
 10. NA
 11. ALL UNCONNECTED VIA'S SHALL BE SOLDERED IN INTERNAL LAYERS.
 12. BACKDRILLING TO BE DONE FROM L61 TO L10.
 13. BACKDRILLING TO BE DONE FROM L16 TO L11.
 14. BACKDRILLING TO BE DONE FROM L16 TO L04.

BACKDRILL: TOP to L10-SIGNAL				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
	7.98	+3.0/-0.0	PLATED	64
START	TARGET	MUST CUT	MUST NOT CUT	
1.1	1.10	1.8	1.11	

NOTES:

- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- VENDOR IS REQUIRED TO SELECT TOOLING FOR OVERDRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER

BACKDRILL: BOTTOM to L11-GND4				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
	7.99	+3.0/-3.0	PLATED	128
START	TARGET	MUST CUT	MUST NOT CUT	
13.6	13.1	13.2	13.0	

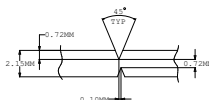
NOTES:

- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- VENDOR IS REQUIRED TO SELECT TOOLING FOR OVERDRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER.

BACKDRILL: BOTTOM to L4-GND2				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
	7.96	+3.0/-3.0	PLATED	18
START	TARGET	MUST CUT	MUST NOT CUT	
1.2	1.2	1.4	1.3	

NOTES:

- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- VENDOR IS REQUIRED TO SELECT TOOLING FOR OVERDRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER




DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	7.96	+3.0/-3.0	PLATED	18

7.	-	7.98	+3.0/+0.0	PLATED	64
8.	-	7.99	+3.0/+3.0	PLATED	121
	-	8.0	+3.0/+3.0	PLATED	234
	-	10.0	+3.0/+3.0	PLATED	980
	-	12.0	+3.0/+3.0	PLATED	57
	•	36.0	+3.0/+3.0	FLATED	3
	•	40.0	+2.0/-2.0	FLATED	6
	•	49.0	+3.0/+3.0	FLATED	2
	•	40.0	+3.0/+3.0	FLATED	12
	•	34.0	+1.0/-1.0	NON-PLATED	2
	■	42.0	+2.0/-2.0	NON-PLATED	6
	■	58.0	+3.0/+3.0	NON-PLATED	4
	▼	66.0	+3.0/+3.0	NON-PLATED	4
	▼	108.0	+3.0/+3.0	NON-PLATED	4
	▲	250.0	+3.0/+3.0	NON-PLATED	4

IMPEDANCE SPECIFICATIONS

S/L	TYPE	LAYER	FACEWIDTH (M118)	SPACING (M118)	IMPEDANCE (Ohms)	REF. LAYER
01	EDGE COUPLED MICROSTRIP	L1/L16	4.7	5.6	100	L2/L15
02	EDGE COUPLED MICROSTRIP	L16	6.3	5.7	90	L2/L15
03	EDGE COUPLED MICROSTRIP	L1/L16	7.4	5.8	85	L2/L15
04	EDGE COUPLED MICROSTRIP	L1	9	5	80	L2
05	EDGE COUPLED MICROSTRIP		NOT APPLICABLE			
06	MICROSTRIP	L1	18	-	33	L2
07	MICROSTRIP	L1	13	-	40	L2
08	MICROSTRIP	L1/L16	9	-	50	L2/L15
09	EDGE COUPLED STRIPLINE	L3,L5,L7, L10,L12,L14	3	5	100	L2/L4,L4/L6,L6/L8, L9/L11,L11/L13,L13/L15
10	EDGE COUPLED STRIPLINE	L10,L12,L14	3.8	5	90	L9/L11,L11/L13,L13/L15
11	EDGE COUPLED STRIPLINE	L12,L14	4.3	5	85	L11/L13,L13/L15
12	EDGE COUPLED STRIPLINE	L3,L5	5	5	80	L2/L4,L4/L6
13	EDGE COUPLED STRIPLINE	L7	7.3	5.4	66	L6/L8
14	EDGE COUPLED STRIPLINE	L3	3	15	132	L2/L4
15	STRIPLINE	L3,L5,L7, L10,L12,L14	3.8	-	50	L2/L4,L4/L6,L6/L8, L9/L11,L11/L13,L13/L15
16	STRIPLINE	L7	8	-	33	L6/L8
17	STRIPLINE	L3	3	-	66	L2/L4
18	STRIPLINE	L3,L5,L10	6	-	40	L2/L4,L4/L6,L9/L11

SIGNATURES	DATE		TEXAS INSTRUMENTS	PROC078E8
LAYOUT BY SW	211020			
REVIEWED BY ZA	211020			
APPROVED BY AMB	211020			
		J721EX SOM 941x PMIC BRD		
		SIZE D		Rev E8
		SCALE: NONE		SHEET 1 OF 23