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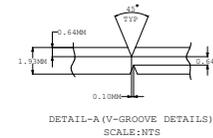
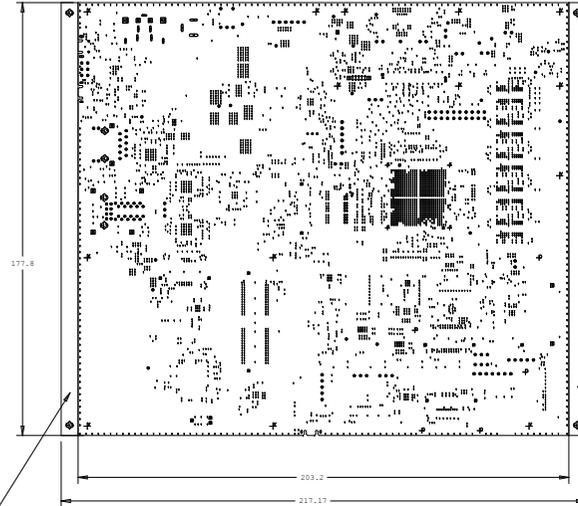
REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

FABRICATION NOTES:

- FABRICATE PCB IN ACCORDANCE WITH IPC-6012, CLASS 2) PER IPC-6011. PCB SHALL BE MANUFACTURED USING 1-SPEED OR EQUIVALENT WITH Et 3.34.
- MATERIALS:
  - LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126. (MIN.TC 180)
  - COOPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150, UNLESS OTHERWISE SPECIFIED. ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS TO BE 15UM (1 OZ.). FOR OUTER LAYERS 1.43 OZ. COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6015 TABLE NO. 3-7 AND 3-8.
- ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
- BOM AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
- CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCREASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
- AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
- FINISH:
  - ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG. ELECTROLESS NICKEL/IMMERSION GOLD. ELECTROLESS NICKEL SHALL BE +/- MICRONS. TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
  - APPLY LIQUID PHOTO IMAGABLE SOLDER MASK PER IPC-BM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES THAT HAVE MASK OPEN SHALL BE FILLED WITH NON CONDUCTIVE INK AND CAP PLATED. ALL OTHER VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK. ONLY SOLDERMASK IMAGES THAT ARE 0.08(1.00") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOR OF SOLDER MASK SHALL BE GREEN.
  - SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
  - SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM (0.00079"), INCREASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 120M (0.0047") AND BURIED VIA'S SHALL NOT BE LESS THAN 150M (0.0056").
  - ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANT TO IPC6012, CLASS 2.
- MARKING:
  - BOARD SHALL MEET THE REQUIREMENTS OF UL-798 WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, UL FILE NUMBER, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
- TEST REQUIREMENTS:
  - 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
- THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
- TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
- FINISHED PCB THICKNESS SHALL BE 0.0781" +/-10%.
- MIN TRACE WIDTH/SPACING ON BOARD IS 0.0033"/0.004".
- ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.
- DATA WITH 40MIL DRILL HAS A DUPLICATE HOLE AT ONE OF THE LOCATION, THIS SHALL BE IGNORED DURING FABRICATION. AND QUANTITY CAN BE CONSIDERED AS 11 HOLES.
- ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IN INTERNAL LAYERS.

DRILL CHART: TOP TO BOTTOM  
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
1	24.0	+3.0/-3.0	PLATED	10
2	32.0	+2.0/-2.0	PLATED	2
3	32.0	+3.0/-3.0	PLATED	5
4	36.0	+3.0/-3.0	PLATED	38
5	40.0	+2.0/-2.0	PLATED	34
6	40.0	+3.0/-3.0	PLATED	43
7	46.0	+2.0/-2.0	PLATED	18
8	46.0	+3.0/-3.0	PLATED	6
9	66.0	+3.0/-3.0	PLATED	8
10	86.0	+3.0/-3.0	PLATED	2
11	34.0	+2.0/-2.0	NON-PLATED	2
12	34.0	+3.0/-3.0	NON-PLATED	2
13	40.0	+3.0/-3.0	NON-PLATED	12
14	40.0	+3.0/-3.0	NON-PLATED	3
15	36.0	+3.0/-3.0	NON-PLATED	4
16	68.0	+3.0/-3.0	NON-PLATED	4
17	88.0	+3.0/-3.0	NON-PLATED	5
18	108.0	+3.0/-3.0	NON-PLATED	14
19	126.0	+3.0/-3.0	NON-PLATED	8
20	52.0x24.0	+3.0/-3.0	PLATED	2
21	52.0x24.0	+3.0/-3.0	PLATED	2
22	44.0x22.0	+3.0/-3.0	PLATED	2
23	86.0x24.0	+3.0/-3.0	PLATED	1
24	86.0x24.0	+3.0/-3.0	PLATED	2
25	98.0x24.0	+3.0/-3.0	PLATED	4
26	120.0x30.0	+3.0/-3.0	PLATED	1
27	120.0x30.0	+3.0/-3.0	PLATED	1
28	140.0x40.0	+3.0/-3.0	PLATED	1



IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH (Mils)	SPACING (Mils)	IMPEDANCE (Ohms)	REF LAYER
01	EDGE COUPLED STRIPLINE	L12	3.0	7.9	100	L11/L13
02	EDGE COUPLED STRIPLINE	L5	3.5	5.0	90	L4/L6
03	EDGE COUPLED STRIPLINE	L3	4.3	4.4	80	L2/L4
04	STRIPLINE	L10, L12	3.3	NA	50	L9/L14, L4/L6
05	STRIPLINE	L3, L5	5.0	NA	40	L2/L4, L4/L6
06	EDGE COUPLED MICROSTRIP	L1, L14	4.2	7.4	100	L2, L13
07	EDGE COUPLED MICROSTRIP	L1, L14	4.1	4.4	90	L2, L13
08	EDGE COUPLED MICROSTRIP	L1, L14	6.2	5.3	80	L2, L13
10	EDGE COUPLED MICROSTRIP	L1	10.5	5.0	85	L4
11	MICROSTRIP	L1, L14	5.2	NA	50	L2, L13
12	MICROSTRIP	L1, L14	8.2	NA	40	L2, L13

LAYER STACKUP

LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS [INCHES]
PRIMARY SIDE SILKSCREEN			
PRIMARY SIDE SOLDERMASK			
L01	PRIMARY SIDE		0.00320
L02	GROUND-PLANE-1		0.00400
L03	INNER-SIGNAL-1		0.00350
L04	GROUND-PLANE-2		0.00400
L05	INNER-SIGNAL-2		0.00350
L06	POWER-PLANE-1		0.00350
L07	POWER-PLANE-2		0.00350
L08	POWER-PLANE-3		0.00350
L09	GROUND-PLANE-3		0.00350
L10	INNER-SIGNAL-3		0.00400
L11	GROUND-PLANE-4		0.00350
L12	INNER-SIGNAL-4		0.00400
L13	GROUND-PLANE-5		0.00320
L14	SECONDARY SIDE		0.00320
SECONDARY SIDE SOLDERMASK			
SECONDARY SIDE SILKSCREEN			

SIGNATURES		DATE	TEXAS INSTRUMENTS	PROC062
LAYOUT BY	UAK	030918		
REVIEWED BY	ZA	030918		
APPROVED BY	AMB	030918		
AM654x EVM PROCESSOR BOARD				
SCALE: NONE			Rev 23	
				SHEET 1 OF 21

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