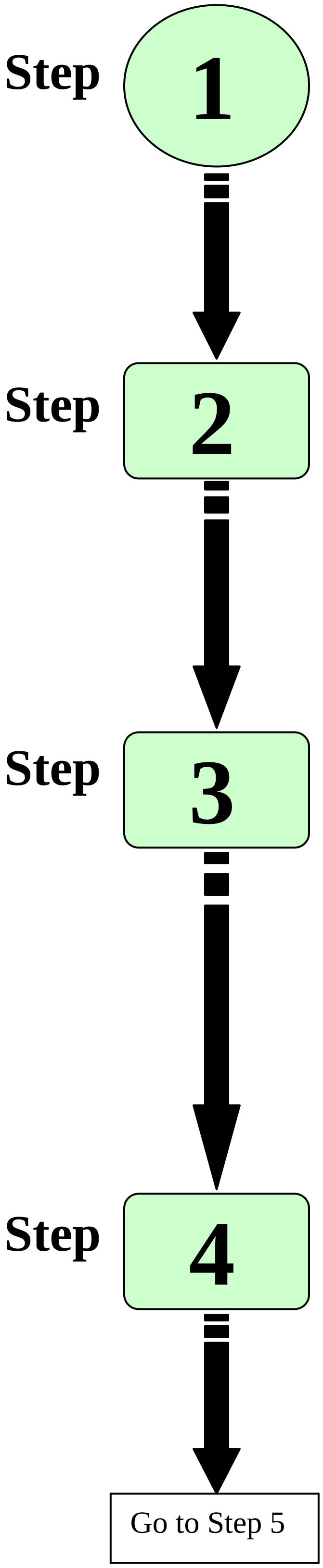
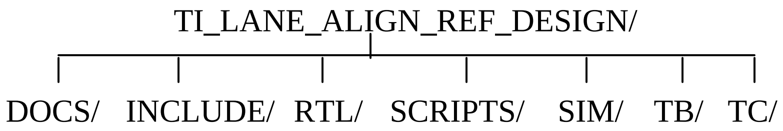
TLK10002 Lane Alignment FPGA Reference Design
Quick Setup Guide



Step 1: Install the package and check the desktop folder TI_HPA_ICP_TLK10002_FPGA for contents.



Step 2: Run the testcase with Cadence Incisive Simulator.

Go to SIM directory, to run simulation without MDIO, type:
../SCRIPTS/irun_REFDESIGN.pl TC_ReferenceDesignSim4Lanes
Or, to run simulation with MDIO, type:
../SCRIPTS/irun_REFDESIGNwmdio.pl TC_ReferenceDesignSimwmdio4Lanes

If you use a different simulator, the simulation script needs to be modified for your simulator.

Step 3: Check the simulation results.

Go to /SIM/TC_ReferenceDesignSim4Lanes directory (or /SIM/TC_ReferenceDesignSimwmdio4Lanes if you run the simulation with MDIO) and check the irun.log. The waveform is stored in the Waveform.shm directory. If you use a different simulator, please check your simulator's log files. If there is no error message in the simulation log files (indicated by **ERROR**), the package has been installed correctly and all files are correct.

Step 4: Create a top level FPGA design which instantiates the reference design.

Please refer to /DOCS/lane_alignment_fpga.pdf Chapter 3.0 on page 5 for a conceptual top level design. Please do NOT add your own code at this time.

Instantiate the /RTL/fpga_channel.v and /RTL/top_mdio.v in the top level. Please refer to /RTL/fpga_channel_wmdio.v for the connection between the top_mdio module and the fpga_channel module.

1) If you use Altera Arria II GX, please refer to /DOCS/arria2gx_lane_align.pdf for configuring the Transceiver macro in Quartus II MegaWizard.
OR
2) If you use Xilinx Spartan6, please refer to /DOCS/spartan6_gtp_withbuffer.pdf for the FPGA clocking structure and for configuring the GTP transceiver macro in Xilinx ISE CoreGen.

Continued from Step 4

Step 5

Step 5: Simulate the top level design.

1) Create your own top level testbench. You may refer to the files /TB/TB_TOP_ReferenceDesignwmdio.v and /TC/TC_ReferenceDesignSimwmdio4Lanes.v for examples of controlling the reference design through MDIO interface. Also see /DOCS/tlk10002_fpga_ref_design_regmap.pdf for details on MDIO interface.

2) Simulate your top level design and make sure it runs error free.

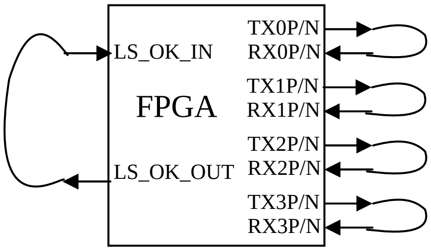
Step 6

Step 6: Implement the top level design.

Synthesize/map/place-route your top level FPGA design, and generate the bit map for programming the FPGA hardware.

Step 7

Step 7: Test the reference design in real FPGA hardware.
Externally loopback the FPGA’s transmit serial lines to its receive serial lines per lane and per channel. Also loopback the FPGA’s LS_OK_OUT to its LS_OK_IN per channel.



Run CRPAT Long test pattern to test TI lane alignment master and slave connectivity. Please refer to Appendix A in /DOCS/tlk10002_fpga_ref_design_regmap.pdf for test pattern verification procedures.

Step 8

Congratulations!

You have verified the reference design in your FPGA. Now, you can connect your own traffic core to the fpga_channel tx_data_ln0~3_in and rx_data_ln0~3_out. The tx_tpgen_64 and rx_tpver_64 blocks can be removed to save resources, but are recommended to keep in the design. You can also implement some of the MDIO registers in your own microprocessor interface. Then your FPGA is ready to interface with TLK10002!