 **TEXAS INSTRUMENTS**

Title

**SCH, TSW1418EVM**

Size

**B**

Document Number

**DC069**

Rev

**A**

Date:

Tuesday, August 14, 2018

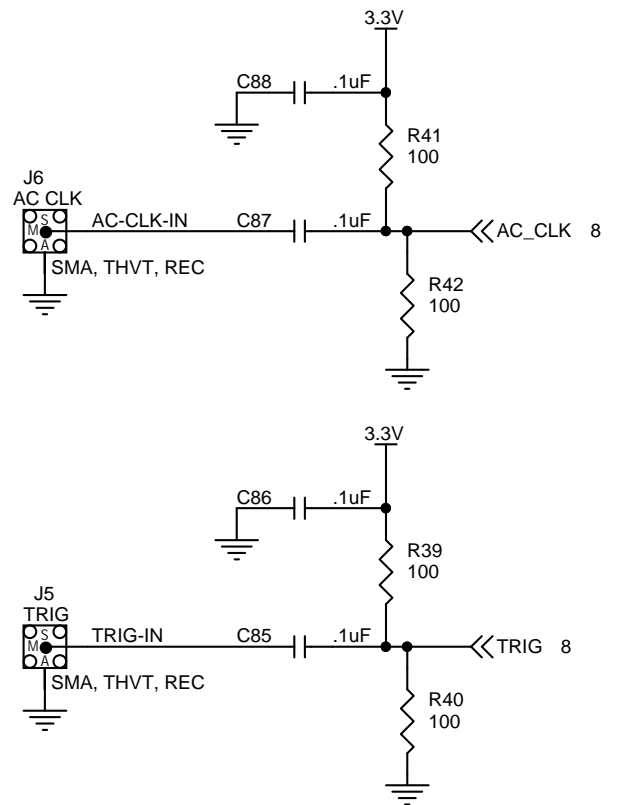
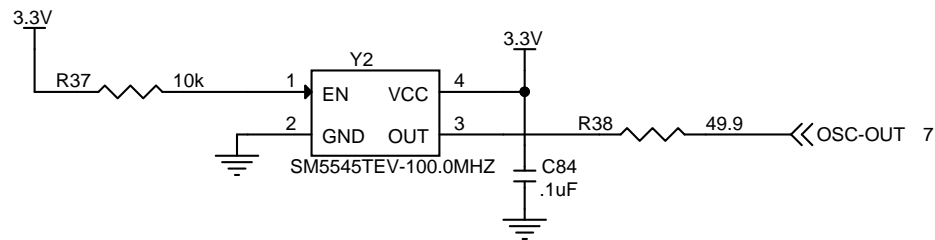
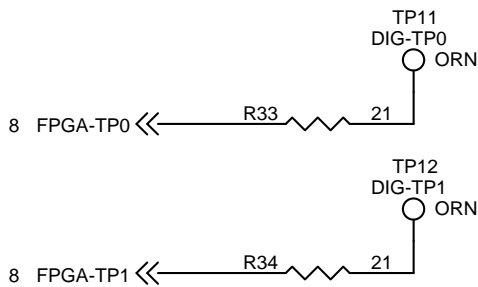
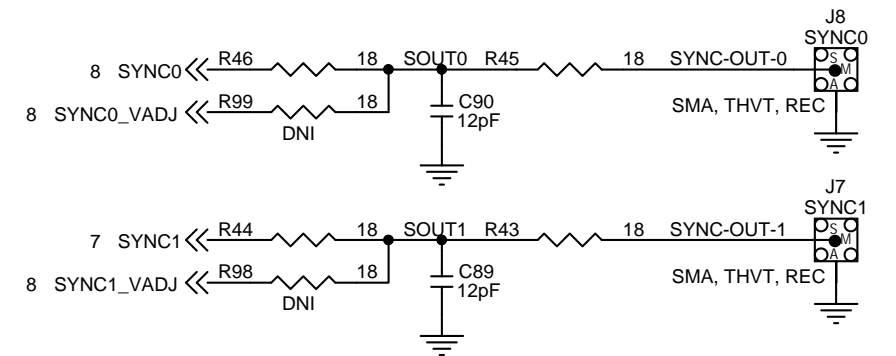
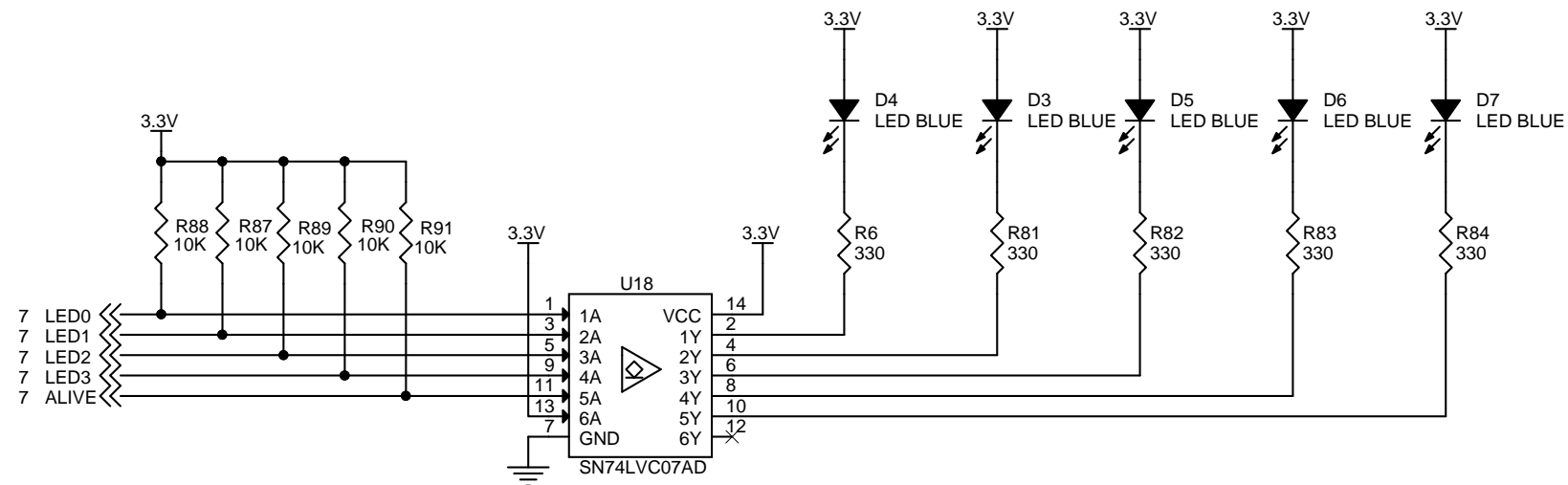
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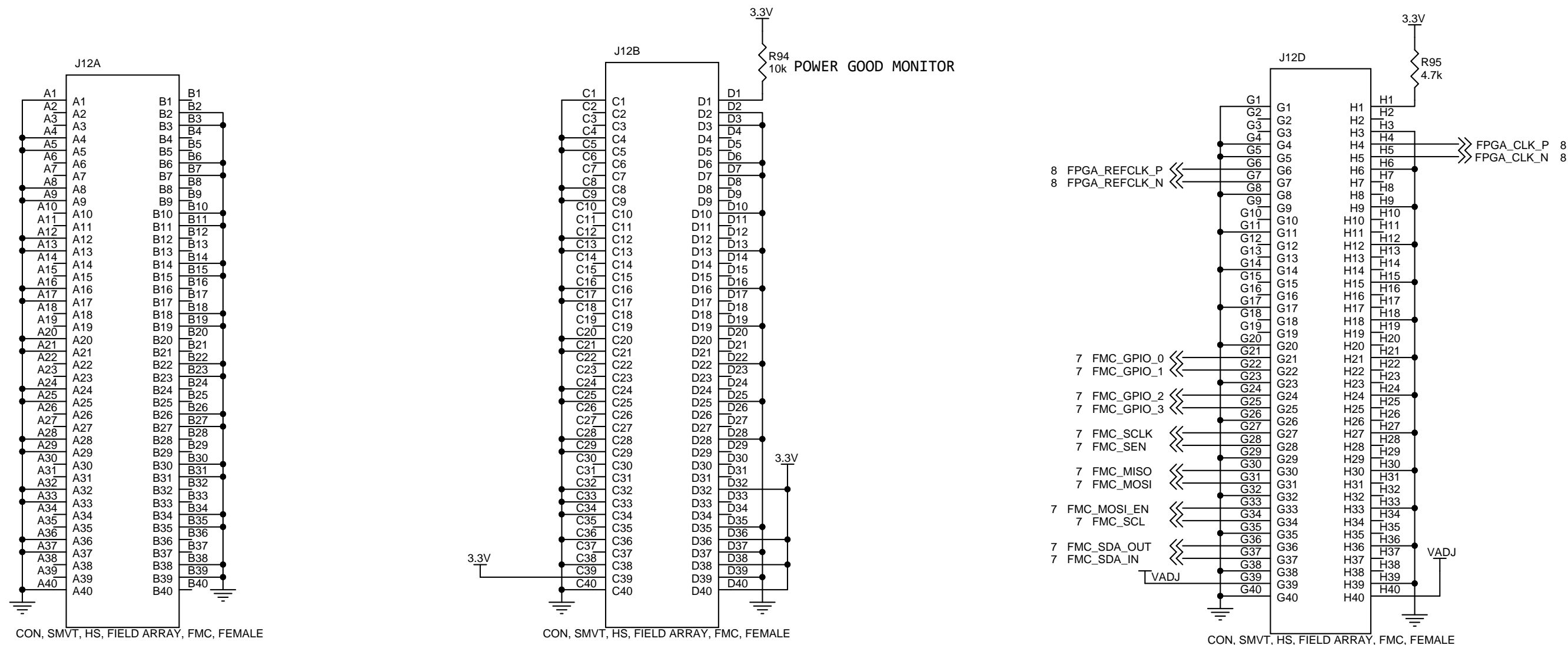
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Drawn:	JV SMITH	02/2018
Engineer:	B. KINCAID	02/2018



5 BS\_ENA << R92 0 >> JTAG\_BS\_EN 5  
CLOSED = USE FTDI  
OPEN = USE EXT JTAG

# ADC Interface



3.3V available on FMC

VADJ available on FMC

All routed I/O is based on VADJ

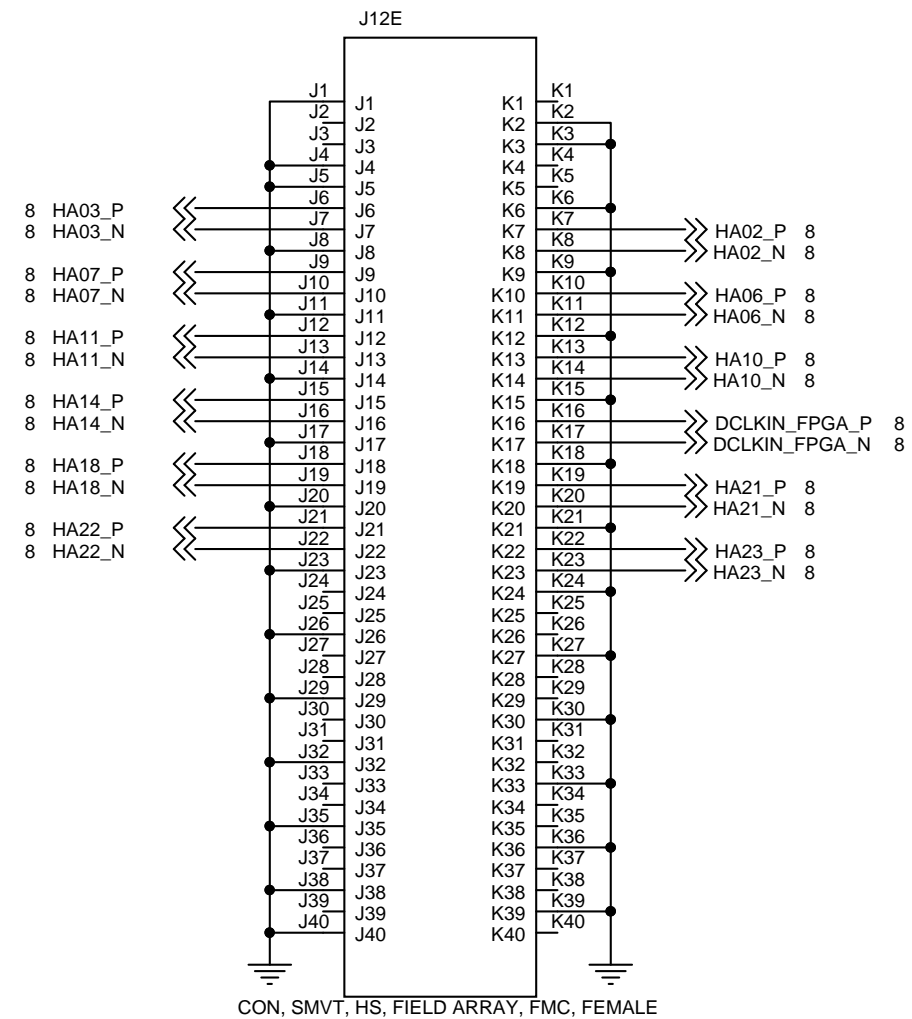
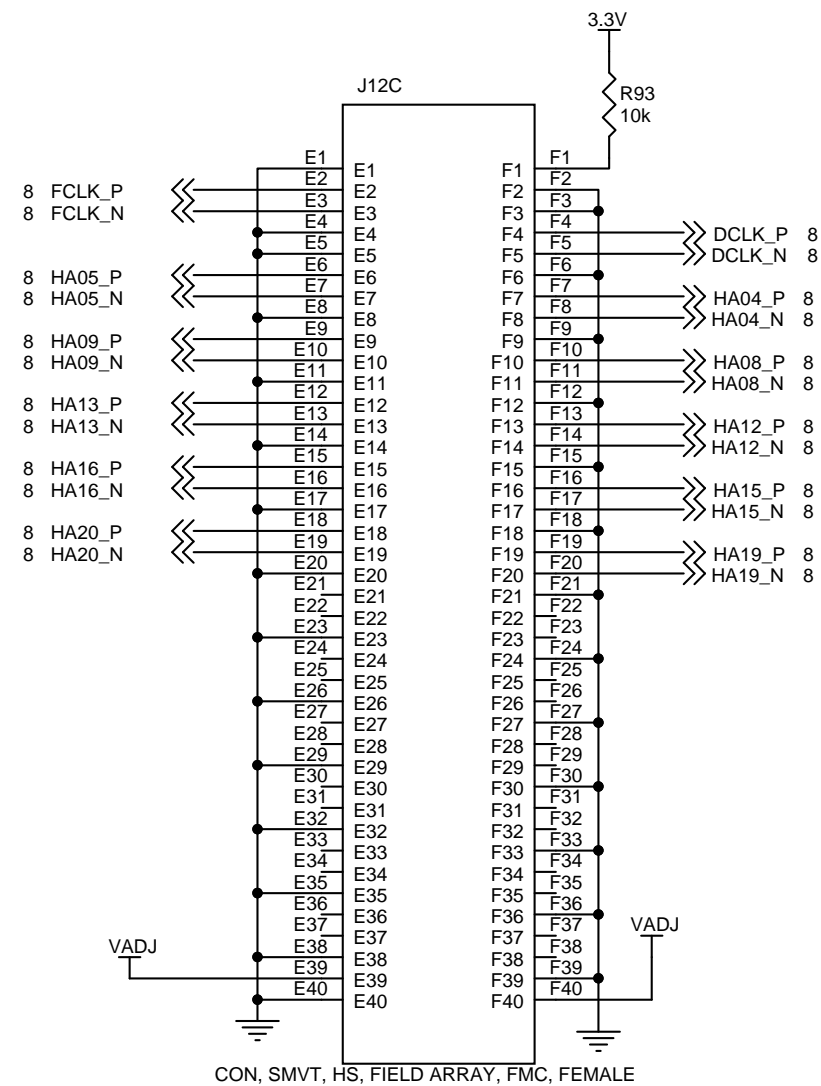
12V not available on FMC

Mates to male bottom side FMC on the ADC35\* EVMs.



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ADC Interface

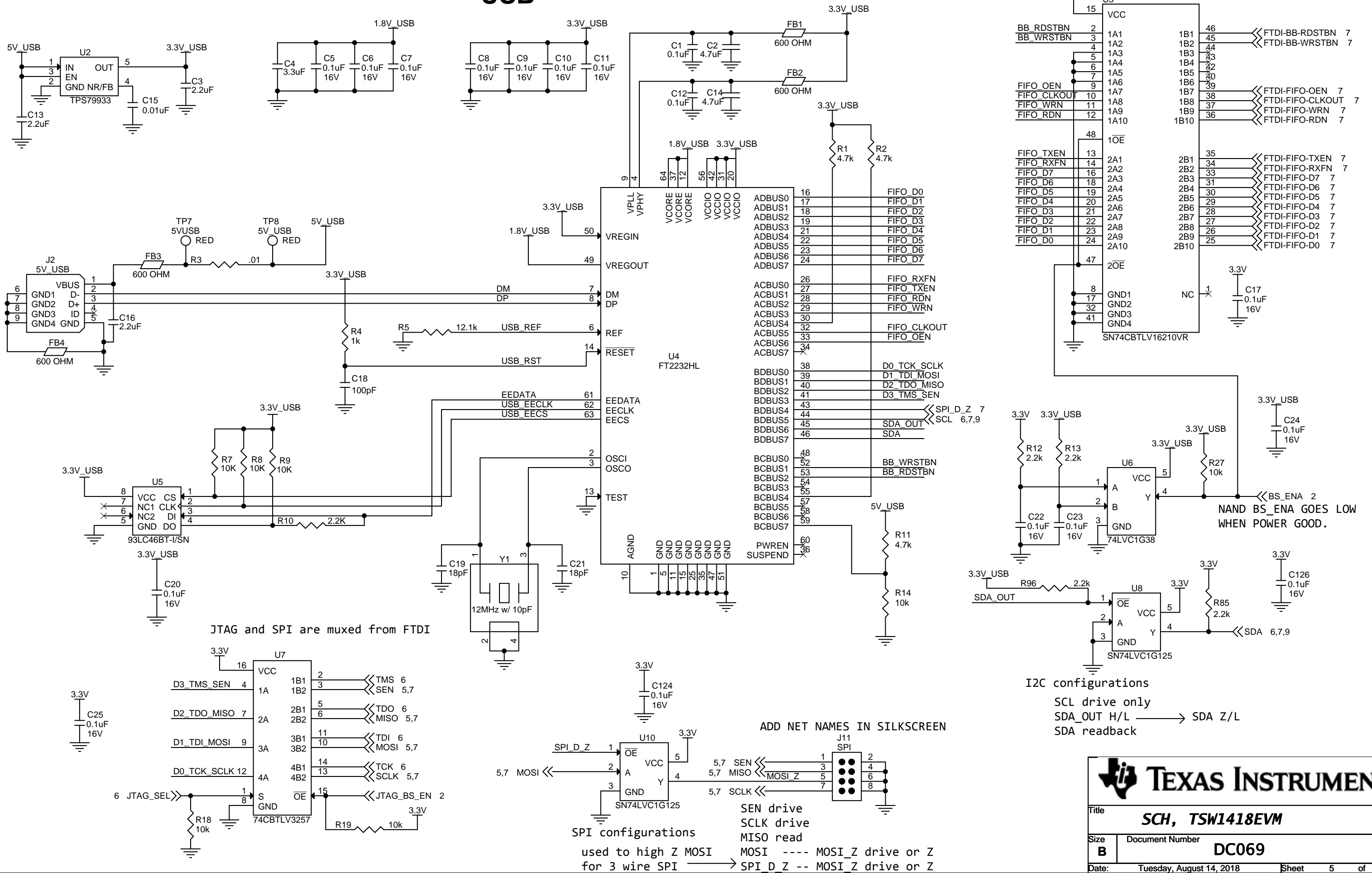


Mates to male bottom side FMC on the ADC35\* EVMs.

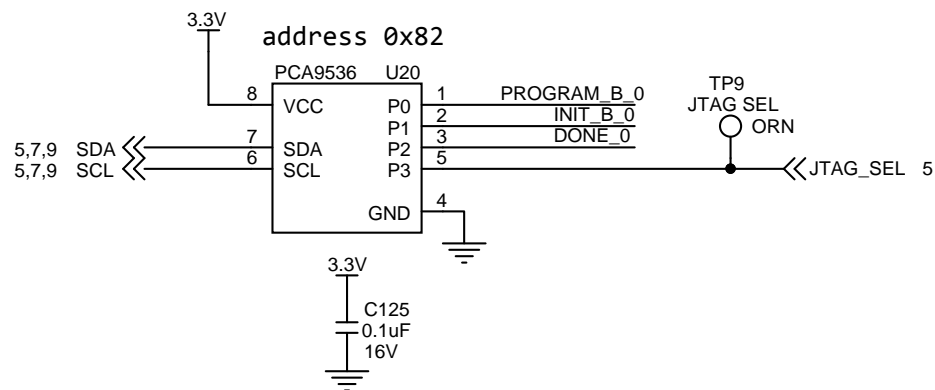
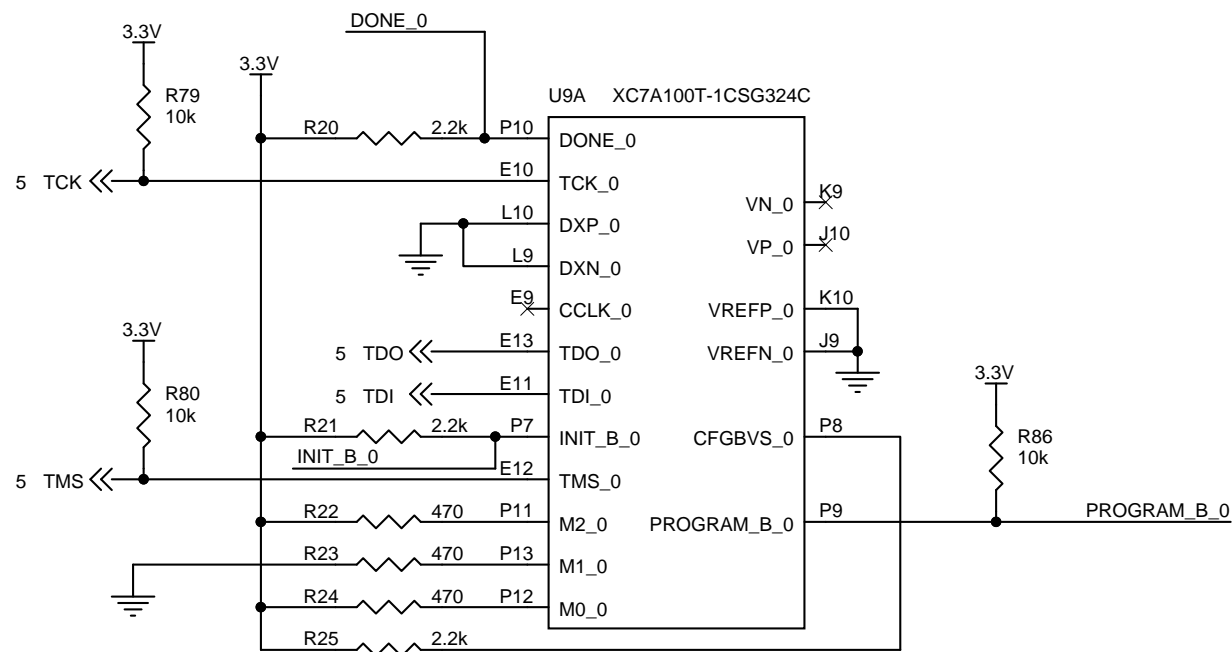
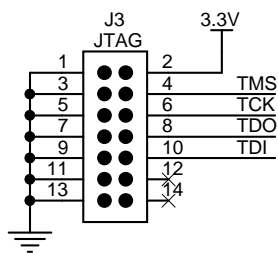


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# USB



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#### FPGA JTAG CONFIG

CFGBVS= 1(VCC\_0=3.3V)

M[2:0]= 101

TCK, TMS, TDI, TDO = from FTDI device through MUX

PROGRAM\_B=I2C expander P0, write, pulse low to enable configuration mode

INIT\_B= I2C expander P1, read only

DONE= I2C expander P2, read only

CCLK= no connect

PUDC\_B= 3.3V

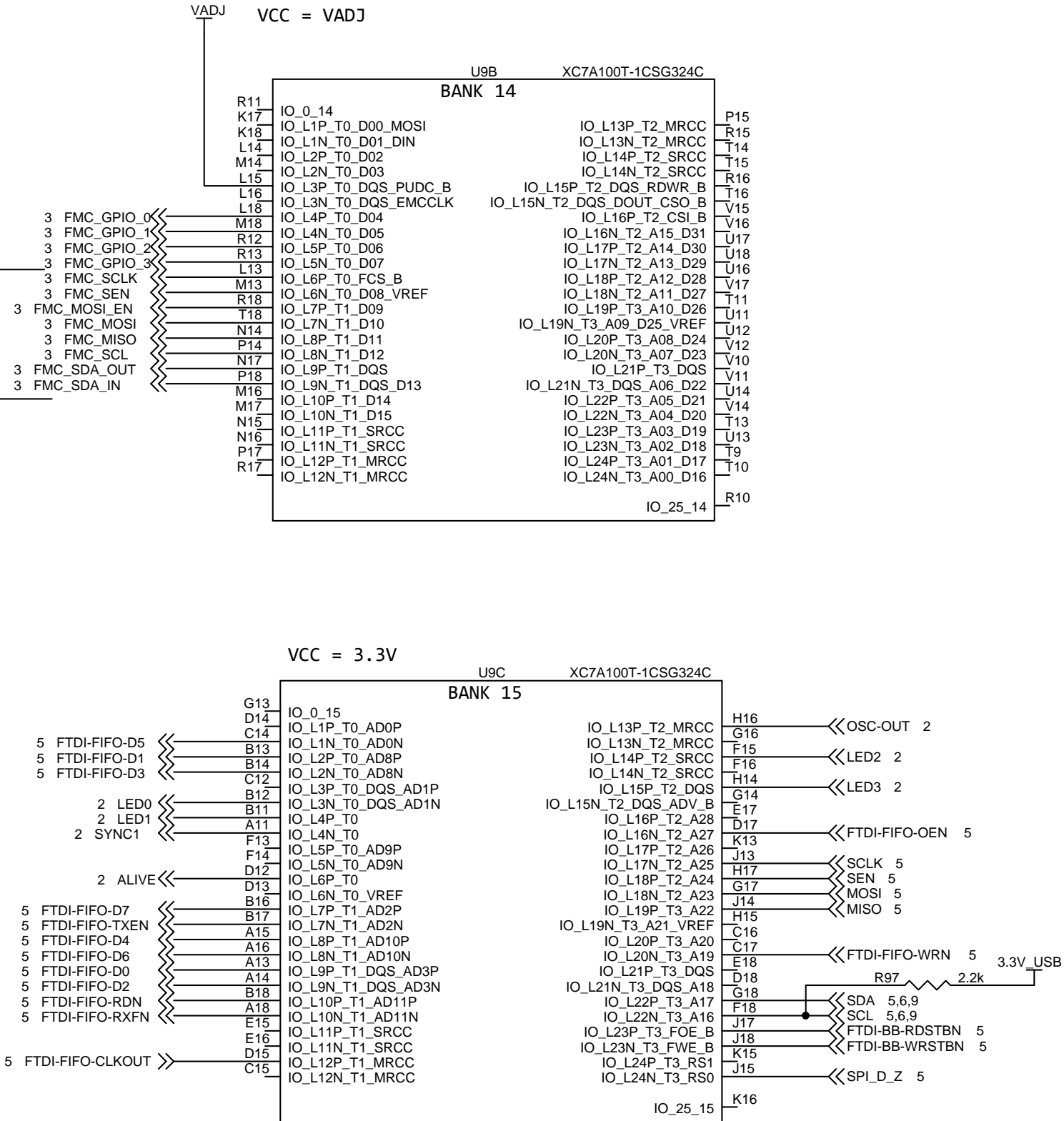
#### PCA9536 address 0x82

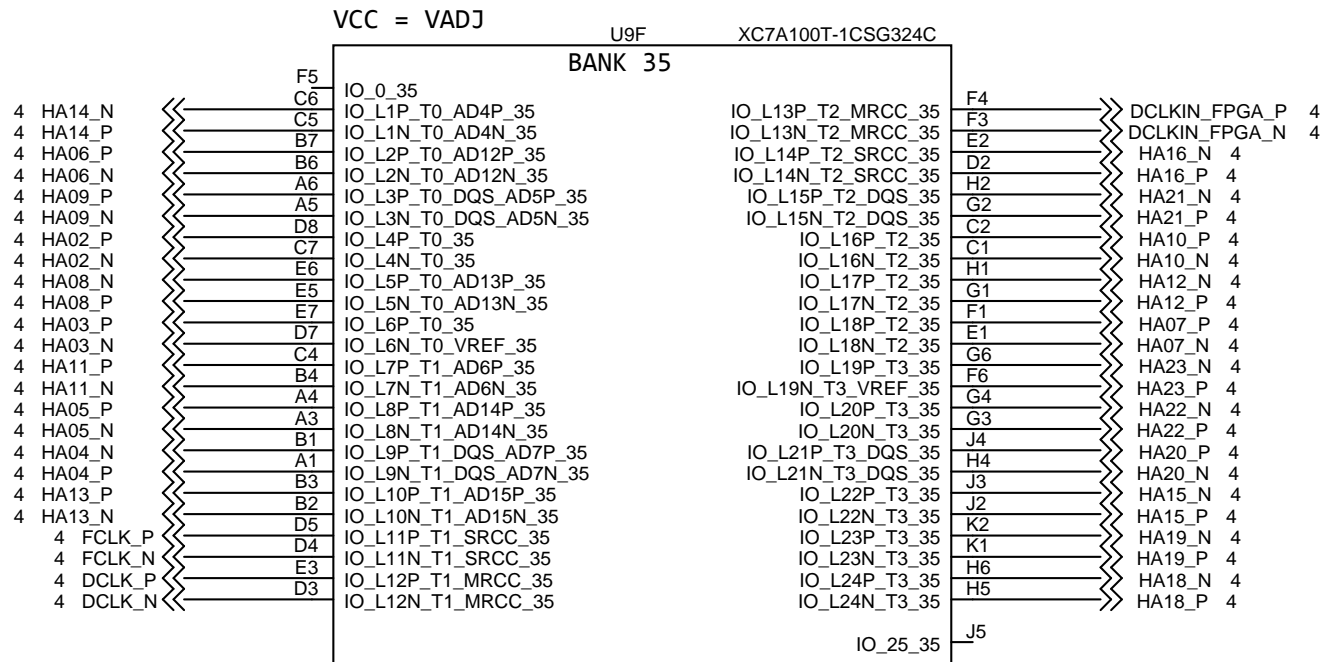
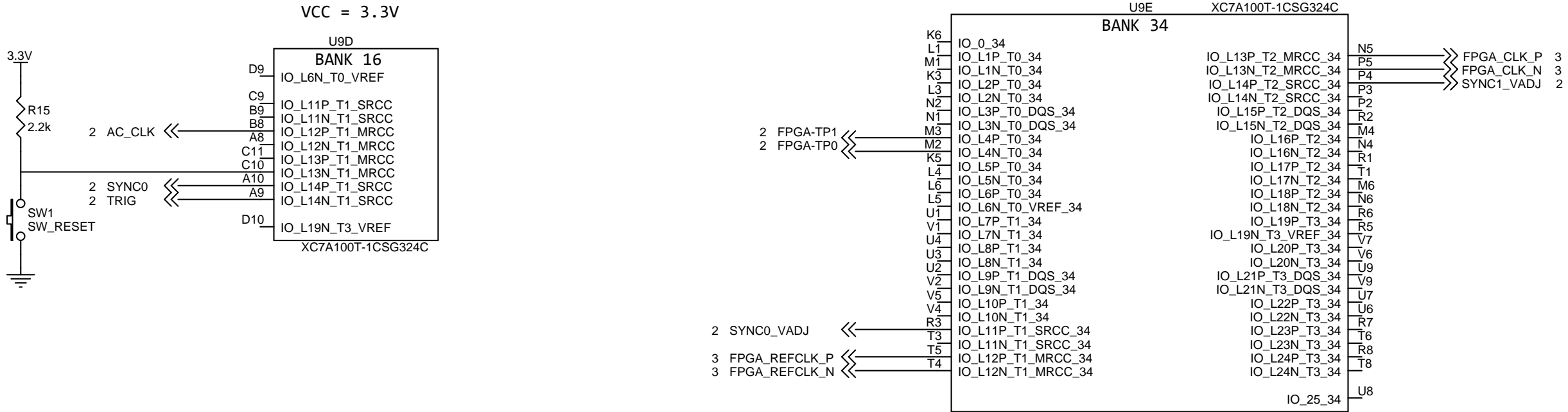
- All pins input at power up
- Configure 0x03 F6 (wrrw) at startup
- Read 0x00 [JTAG\_SEL DONE INIT\_B PROGRAM\_B]
- Write 0X01 [JTAG\_SEL X X PROGRAM\_B]



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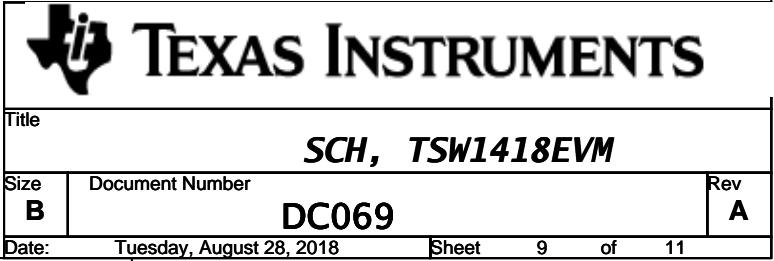
These signals are  
wired through FPGA  
to FMC





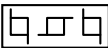
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MECHANICAL PARTS



BARE BOARD, TSW1418



STANDOFF, FEMALE, 4-40 X 1/2"



STANDOFF, FEMALE, 4-40 X 1/2"



STANDOFF, FEMALE, 4-40 X 1/2"



STANDOFF, FEMALE, 4-40 x 1/2"



SCREW PANHEAD 4-40 x 3/8"




SCREW PANHEAD 4-40 x 3/8"



SCREW PANHEAD 4-40 x 3/8"



SCREW PANHEAD 4-40 x 3/8"

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