

A

B

C

D

SEE 001svengprerelstackup18.pdf FOR CORRECT STACKUP INFORMATION

Layer Stack Up Detail for: SU600847A1.PcbDoc

Layer Name	Gerber Document	Copper Thickness	Dielectric Height	Dielectric Material	Dielectric Constant	Dielectric Type
Top Solder Mask	(.GTS)		0.4mil	Solder Resist	3.50	
Top Layer L1	(.GTL)	0.6mil	4mil	Rogers R04350	3.66	Core
Gnd-Plane - L2	(.GP1)	1.2mil	6.7mil	NP 4000-6	4.11	PrePreg
Signals - L3	(.G1)	0.6mil	6mil	NP 4000-6	4.11	Core
Gnd-Plane - L4	(.GP2)	1.2mil	4.1mil	NP 4000-6	4.11	PrePreg
Pwr Plane - L5	(.GP3)	1.2mil	6mil	NP 4000-6	4.11	Core
Signals - L6	(.G2)	0.6mil	6.7mil	NP 4000-6	4.11	PrePreg
Gnd-Plane - L7	(.GP4)	1.2mil	4mil	Rogers R04350	3.66	Core
Signals - L8	(.G3)	0.6mil	7.3mil	Rogers R04350	3.66	PrePreg
Gnd-Plane - L9	(.GP5)	1.2mil	4mil	Rogers R04350	3.66	Core
Bottom Layer - L10	(.GBL)	0.6mil				
Bottom Solder Mask	(.GBS)		0.4mil	Solder Resist	3.50	

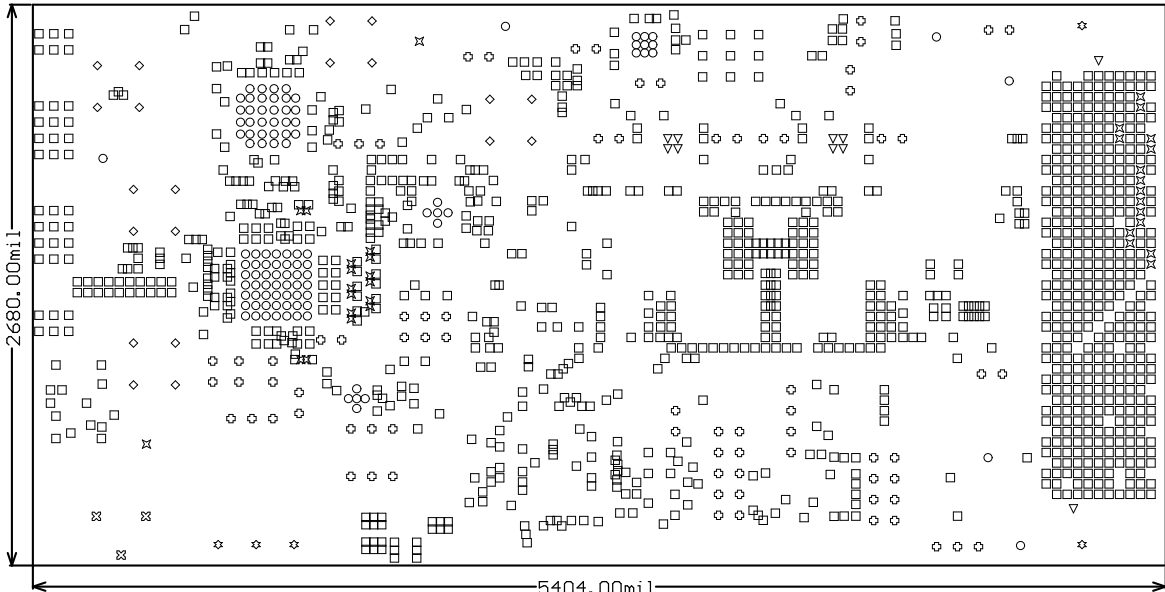
SEE 001svengprerelstackup18.pdf FOR CORRECT IMPEDANCE INFORMATION

Single ended tracks 50 ohms Top & Bottom Layers equal 8.0mil width.

Differential tracks 100 ohms Top & Bottom Layers equal 8.0mil width & 8.0mil spacing.

Differential tracks 100 ohms Inner Layers equal 4.0mil width & 4.0mil spacing.

Back Drill high speed lines 8.001 mil vias from Layer 1 to Layer 7, leaving the via connecting layer 8 to layer 10.



Symbol	Hit Count	Tool Size	Physical Length	Route Path Length	Plated	Hole Type
○	100	7.874mil (0.2mm)			PTH	Round
□	1147	8mil (0.203mm)			PTH	Round
×	32	8.001mil (0.203mm)			PTH	Round
▽	8	12.992mil (0.33mm)			PTH	Round
□	11	37.992mil (0.965mm)			PTH	Round
⊕	77	40mil (1.016mm)			PTH	Round
▽	2	50mil (1.27mm)			NPTH	Round
◇	20	59.055mil (1.5mm)			PTH	Round
○	6	63mil (1.6mm)			PTH	Round
*	3	64.961mil (1.65mm)			PTH	Round
*	2	106mil (2.692mm)			PTH	Round
×	2	125.984mil (3.2mm)			PTH	Round
⊗	3	39.37mil (1mm)	137.795mil (3.5mm)	98.425mil (2.5mm)	PTH	Slot
	1413 Total					

Slot definitions : Route Path Length = Calculated from tool start centre position to tool end centre position.
Physical Length = Route Path Length + Tool Size = Slot length as defined in the

Drill Table

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)

X

Number of Layers : 10

MIN. TRACK WIDTH: 4 MIL

MIN. CLEARANCE: 4 MIL

MIN. VIA PAD SIZE: 18 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:

☐ FR-4 ☐ FR-4 High Tg ☒ OTHER SEE LAYER STACK UP

THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

COPPER THICKNESS (FINISHED):

OUTER: ☒ 0.7MIL (0.5oz) ☐ 1.4MIL (1oz) ☐ 2.8MIL (2oz)

INNER SIGNAL: ☒ 0.7MIL (0.5oz) ☒ 2.8MIL (2oz) ☐ N/A

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES

PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR:

☒ GREEN ☐ BLUE ☐ OTHER

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG)

☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL:

☐ CUT AND TRIM PER MECH LAYER 1

☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3

☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

MANUFACTURER'S ID/LOGO: ☐ RAIL ☒ METAL ☐ SILK



PROJECT TITLE:
ADC12J4000 / LM15851 EVAL BOARD

DESIGNED FOR:
Internal Use Only

FILE NAME:
SU600847E3.PcbDoc

ENGINEER:
Marjorie Plisch

LAYOUT BY:
Bob Holtz

SCALE: 1.09

ALTUM DESIGNER VERSION:
10.0.0.27009

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: SU600847	REV: E3	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = 001svengprerelstackup18.pdf				
PLOT NAME = Fabrication Drawing	GENERATED : 11/26/2013 3:01:38 PM		TEXAS INSTRUMENTS	