

Pulser Output Stage

- Pulser of each channel can give out maximum of 1A current. When all the 32 channels are excited together, device takes 32A current from high voltage power supply.
- Figure shows simplified diagram of PMOS stage with layout parasitic.
- The internal Vgs of PMOS cant go above 5V. Therefore it is important that FLOATP_HV and V_PHV_INT nodes follow each other closely. If supply parasitic cap is higher (Lsup) then it can lead to device abnormal behavior like pulser output is not swinging as expected. Even overall parasitic inductance Lsup of 1nH can give ~2V swing at V_PHV_INT node and can affect device functionality.
- To avoid this issue, it is recommended to follow the layout guidelines as per given in the datasheet. In layout guidelines the float cap is placed as near to device supply to reduce Lsup inductance.



