It's a Buck; It's a Boost, No! It's a Switcher! (part two)

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As mentioned in the Introduction, it is important to also note the internal construction of the switcher IC. Since we are ignoring P-switches hereafter, our focus has in effect shifted entirely to N+ (Type A) and N- (Type B) LSD cells only, because we now know that C can be generated from A, and D from B.

Returning to Figure 3, Figure 4 and Figure 5, we see that the details of the control were not shown. In addition though the switch is shown outside the square block, it can be considered integrated into the IC. This is typical of National's Simple Switcher series. Let us now study typical integrated ICs first to see how they are internally configured.

Commonly, there are four basic Switcher IC types available (all use N-switches) as shown in Figure 8. On closer examination, we see that these fall into two basic categories, hereby designated Type 1 and Type 2. Note the bold trace shown in the figures is the connection trace between the switch and the control. And this is what makes the two types really different. Type 2 ICs are generally considered 'Flyback/Buck-Boost/Boost' ICs and Type 1 ICs are considered 'Buck ICs'. We will see that Type 1 ICs are generally the most versatile. Therefore we will discuss the various possibilities using a Type 1 IC first and later take up Type 2.

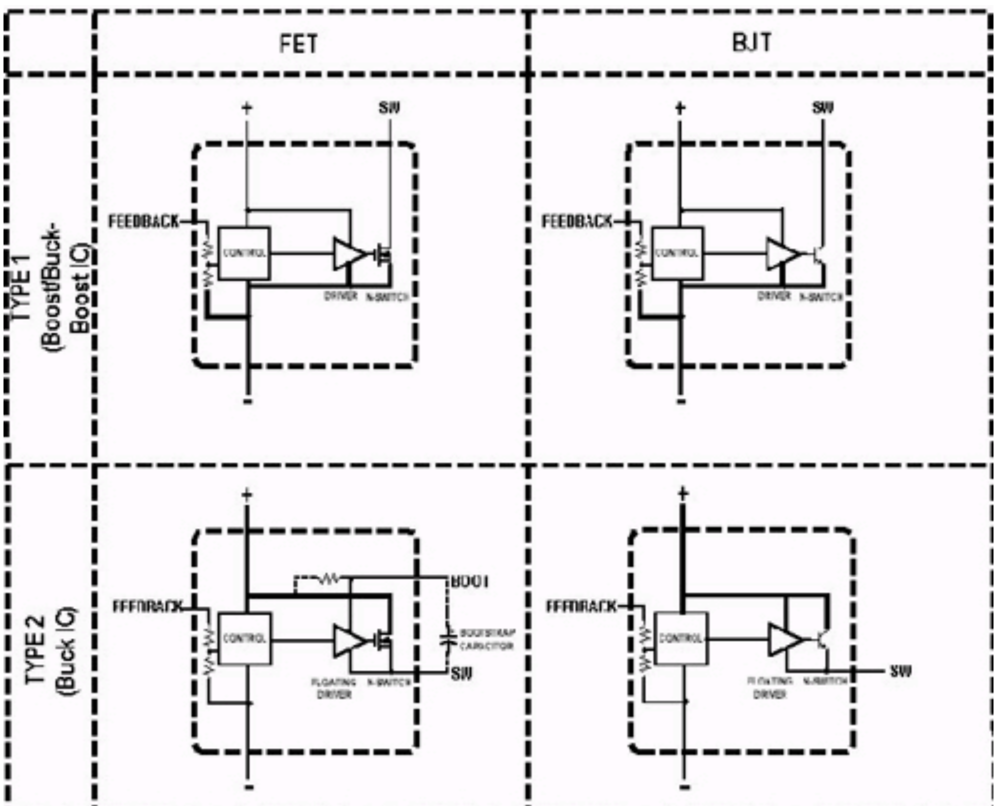


FIGURE 8

Before we go on let us briefly summarize some key observations from Figure 8.

* Type 1 connects the Source/Emitter (lower voltage switch pin) to the - pin of the control block.

* Type 2 connects the Drain/Collector (higher voltage switch pin) to the + pin of the control block.

* NPN switches are generally easier to drive since the Base has to be taken only slightly higher than the Emitter to turn the switch ON (note that even the small existing CE drop can be used for this purpose, as in Darlington/beta (gain)-multiplier drive arrangements).

* In Type 1 ICs, the Source/Emitter of the switch is connected to the 'GND pin' (lower rail) of the IC (the '-' pin). The slight positive bias voltage required to turn ON the switch can be easily derived by stepping down the voltage available at the '+' supply pin of the IC.

* Therefore a FET-based Type 2 is the hardest to drive. We must recognize that when the switch turns ON, the Source/Emitter pin becomes (almost) equal to the '+' supply pin. But to keep the FET ON, a voltage higher than the IC supply pin is required (typically 5-10 Volts higher depending on type of FET). This is not readily available as it is outside the range of the input supply rails. In fact there is no other easy way other than to bootstrap the driver stage, such that the driver floats on the switching node.

* Note that the actual 'SW' pin labeling in Figure 8 depends on the perceived application for the part, not necessarily on how it is actually used. It cannot always be assumed that the 'SW' pin is the switching node of the regulator power stage. In Figure 8 the SW pin is simply the uncommitted pin of the transistor, i.e. the one NOT directly connected to either the '+' or '-' pins (going to the supply rails). Under 'normal' expectations, it is expected to be the switching node (as it has the required degree of freedom to 'swing'). But in fact this may not be always true. As we will see later, this pin can be connected to a fixed rail, and in fact either the '+' or '-' pins may be forced to be the swinging/switching node! We had also seen earlier that the '-' pin (IC ground for negative ground schematics), may not be the system ground either. Therefore in all cases, the designer needs to take the labeling of the IC pins with a pinch of salt, never forgetting what they really are in terms of the internal construction of the IC.

* In all cases the feedback node is referred by the control to the lower ('-') rail of the IC. But in reality, how the output voltage of the converter is actually sensed and the voltage 'translated' so as to reference it correctly to the IC control, depends on the actual application the IC is being used for. This will be discussed later.

* Type 1 ICs usually have two voltage ratings: one for the control ('+' pins in Figure 8) and a higher rating for the switch (Drain/Collector), both measured with respect to the IC ground (the '-' pins in Figure 8).

* Type 2 ICs almost invariably do not permit the 'SW' pin to be taken more than 1V below IC ground. This limits some possible applications, particularly some 'clever' ideas using tapped inductors (which very few seem to need or want).

Now we will take up Type 1 and Type 2 ICs in more detail below.

Flyback/Buck-Boost/Boost ICs

These are generically referred to as Type 1 ICs in this article. We will now see why there is no essential difference between an IC intended primarily for a Boost application and one say for a Flyback/Buck-Boost application. We should first be aware of the basic topological difference between a Boost and a Buck-Boost power stage.

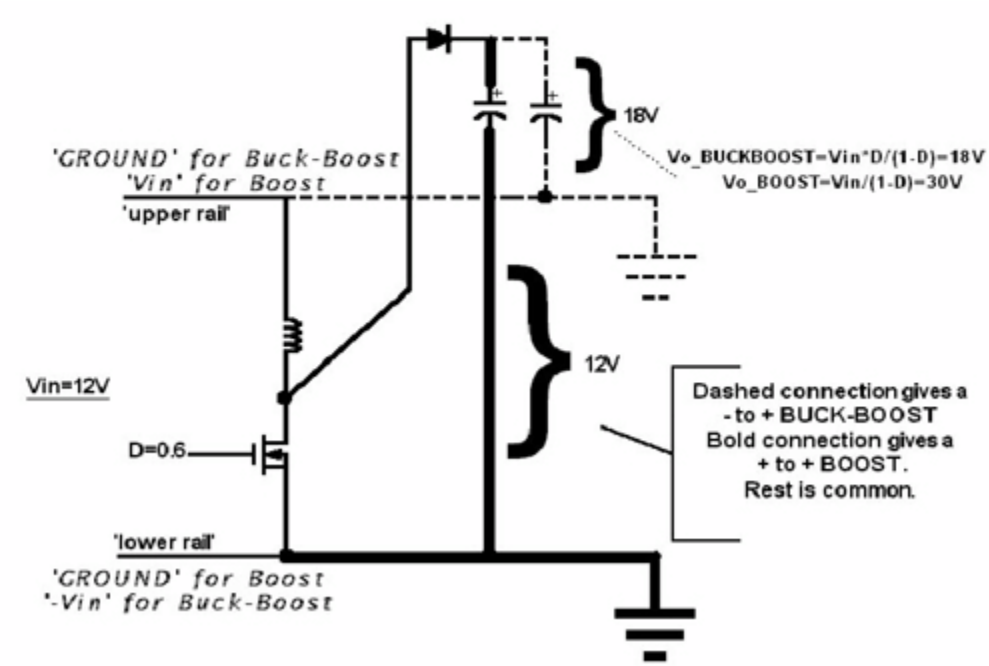


FIGURE 9

In Figure 9 we can see that the change from a 'positive to positive' Boost to a 'negative to positive' Buck-Boost is actually very simple: it involves just re-directing the connection of the negative terminal of the output capacitor from the 'lower rail' to the 'upper rail'. Therefore the two topologies are not all that different. In fact as far as the drive of the switch is concerned it sees absolutely no difference between these topologies, because basically only the designation (or labeling) of the rails has changed. The output voltage rail is exactly 30V above the IC ground (not system ground) in both cases (for the same duty cycle). So the IC doesn't know better.

The main difference is in the feedback. Since for a Boost, the IC control is typically always connected to the 'lower rail', a simple resistive divider across the output capacitor can be used to connect directly to the feedback pin of the IC control. But for the Buck-Boost, the output voltage is with respect to the system ground (the 'upper rail'), whereas the IC control is still referenced to the 'lower rail'. Therefore a more elaborate solution is required. This usually takes the form of a differential amplifier stage to sense the output voltage of the Buck-Boost and then to 'translate' it to the lower rail. But the requirements, specifications and ratings of such a differential stage are so diverse depending on the input/output levels that this extra stage is rarely (if ever) integrated into the switcher IC. This means that a 'true Buck-Boost integrated switcher' (with integrated feedback) may be near impossible to find. So, since the feedback implementation is generally external to the IC, there is no remaining architectural difference left between a 'Boost IC' or a Buck-Boost IC'. They are one and the same. It is no surprise that any switcher meant for a Flyback/Buck-Boost application can always successfully be used for a Boost application and vice versa.

In this article we will use the word 'Flyback' to refer exclusively to a Buck-Boost stage with inherent primary to secondary isolation. Obviously this requires a transformer. But we could also have a transformer-based Buck-Boost with no isolation present, because the primary and secondary windings are connected together for easier implementation of feedback. However, in both cases the feedback method involves using two resistors in a divider network positioned at the output, and no differential amplifier stage is required.

Coming back to the main focus of this article, we now see the other possible applications of a Flyback/Boost IC.

Flyback/Buck-Boost/Boost IC Applications

This is the IC shown as 'Type 1' in Figure 8. It can be used for all the applications presented below. For more details and a summary, view these figures along with the description and comments in the Table 2. This Table is also repeated as Table 3 in Part 2 of this article. Note that this table features only the transformer-less configurations, and also the Type 2 configurations are grayed-out in Part 1, as these will be discussed in Part 2. Note that for convenience, in all cases the main design equations are also provided within the figures themselves. They provide the required ratings of the SW pin (Vswmax), the IC/control pin (VICmax) (both measured with respect to the IC ground pin), and the maximum load possible (based on the set current limit of the switch 'ICLIM'). The maximum load current requires choosing inductance correctly. A current ripple ratio 'r' of 0.4 or less must be the target. Refer to AN-1197 and AN-1246 at http://power.national.com for more details.

Some of the configuration conditions/equations may depend on the minimum and/or maximum input voltages, Vinmin and Vinmax respectively. In addition, every controller is designed with a certain maximum possible duty cycle limit 'Dmax'. Clearly, if the input and output voltages demand more than 'Dmax' the circuit cannot work. Therefore the equation to check this possible limitation is also provided. The feedback scheme is also shown, and the equations to set the resistor values are also provided. 'Vfb' is the voltage on the feedback pin of the IC under regulation (for example it is the reference voltage to the internal error amplifier for an Adjustable output part). National's switcher ICs generally come either as 'Adjustable', requiring an external resistive divider to set output, or Fixed voltage parts, where the divider is internal to the IC.

In all the equations to follow, the switch and diode forward drops are generally assumed to be negligible. So a little additional guardbanding may be necessary to take these into account.

Now the crucial chain of logic behind hidden applications: the primary intended application for this IC is the positive to positive Boost. We can discover that this involves a 'N-' cell (Type B). Therefore we conclude that this IC is most 'comfortable' with any topology/configuration, provided it involves a (similar) Type B cell. This cell is a 'natural choice' for this IC. Note that we also start seeing the advantage in talking in terms of LSD cells rather than directly in terms of topologies/configurations. This common thread would have been missed in that case.

The only other possible cell choice using an N-switch is the Type A (N+) cell. Topologies/configurations requiring a Type A cell are therefore considered a 'forced' choice for a Type 1 IC. They can be implemented using a common underlying technique that involves floating the IC ground on the switching node and then doing a peak detect for implementing feedback. This will be described later.

Now we go through the figures one by one.

a) **Positive to Positive Boost**: Uses a **Type B** cell. The primary intended Application for a Type 1 IC. See Figure 10. Uses a simple resistive divider to implement feedback.

b) **Negative to Positive Buck-Boost**: Uses a **Type B** cell. Another intended Application for a Type 1 IC. See Figure 11. Note the 'cheap and dirty' differential output sense and voltage translation (actually a simple voltage-dependent current source) using a single PNP transistor. Note that 0.6V is assumed for the Vbe drop. Therefore the output regulation is not very accurate. Later more accurate differential op-amp techniques are presented, but they need an external supply rail to power them.

c) **Negative to Negative Buck**: Uses a **Type B** cell. See Figure 12. Note the 'cheap and dirty' output voltage sense technique as in Figure 11. Therefore the output regulation is not very accurate again. Differential op-amp techniques can be used instead for higher accuracy.

d) **Negative to Negative Boost**: Uses a **Type A** cell. A 'forced' application by definition. See Figure 13. Here the fact that the Drain/Collector is not connected to the input of the control section is exploited. The IC ground floats on the switching node (this can cause higher EMI). **Peak charge feedback technique is used**. Here a (near) copy of the output voltage is created by peak charging a small capacitor connected between the switching node (IC ground) and the output ground, via a diode. Note that because of the diode drops this is an inaccurate method. Some techniques to compensate for this error are available, but in general: The output regulation for any topology/configuration which uses a cell which is not the same as the cell for the IC's primary intended application is always inherently inaccurate. We will also later see that in Type 2 IC's such 'forced' applications are not even possible due to the due to the fact that the input to the switch (power stage) and the input to the IC (control section) are not separated out as in Type 1 ICs.

e) **Positive to Negative Buck-Boost**: Uses a **Type A** cell. A 'forced' application by definition. See Figure 14. Therefore again, inaccurate peak detect feedback technique must be used and this sub-circuit is again between the switching node and output ground. The IC floats on the switching node (this can cause higher EMI).

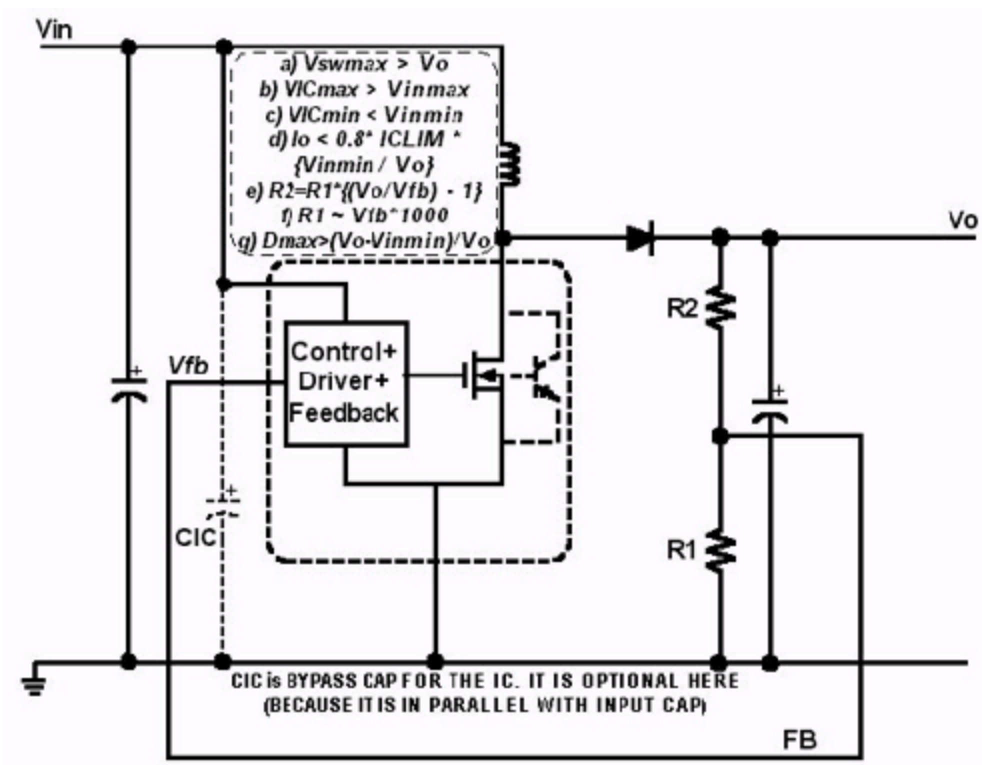
f) **Positive to Positive Buck**: Uses a **Type A** cell. A 'forced' application by definition. See Figure 15. Therefore again, inaccurate peak detect feedback technique must be used and this sub-circuit is now between the switching node and output rail. The IC floats on the switching node (this can cause higher EMI).

In addition to the inductor based topologies above, we could use transformers to 'correct' the polarity reversal of a buck-boost. This helps in implementing feedback too. With transformers, we could have primary to secondary isolation or no isolation. For completeness sake we present these variations too here.

g) **Positive to Positive Buck-Boost**: This involves a transformer with no isolation. See Figure 16.

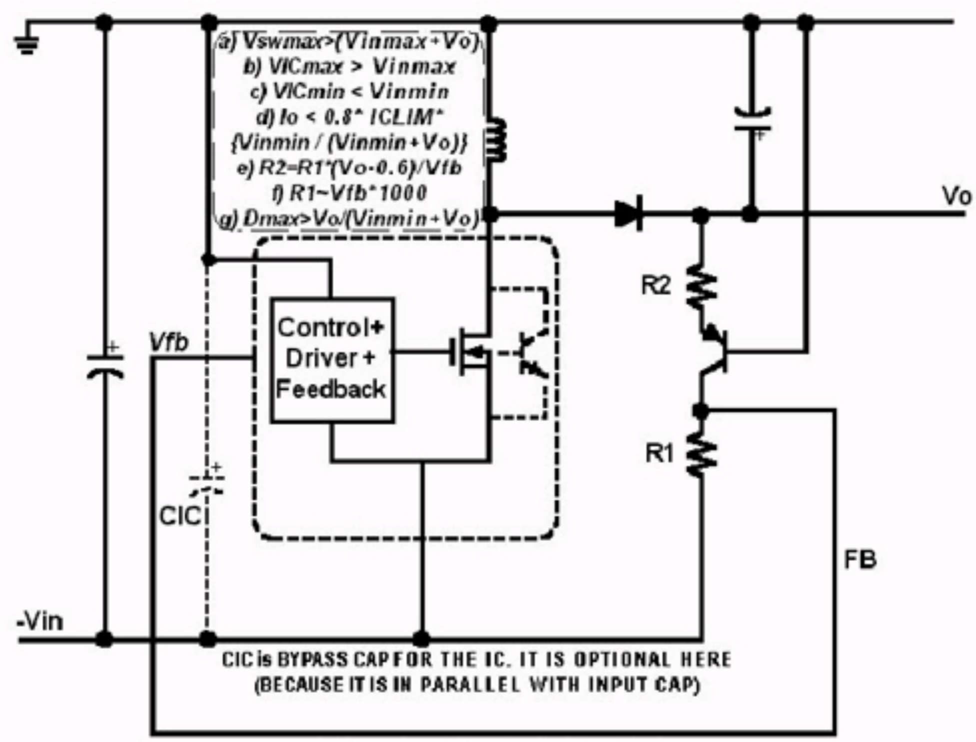
h) **Positive to Positive Flyback**: This involves a transformer with primary to secondary isolation. An external voltage reference is used with an opto-transistor to regulate. See Figure 17.

Figure 18 summarizes all the inductor-based possibilities. The P-switches are grayed out as it was indicated earlier how they can be derived by inverting N-switch configurations. The N-switch configurations with a 'natural' cell choice (Type B LSD cell) are shown with bold arrows and yellow highlighting. The non-bold arrows are possible forced choices involving peak detect feedback method and swinging IC ground, and all use Type A LSD cells.



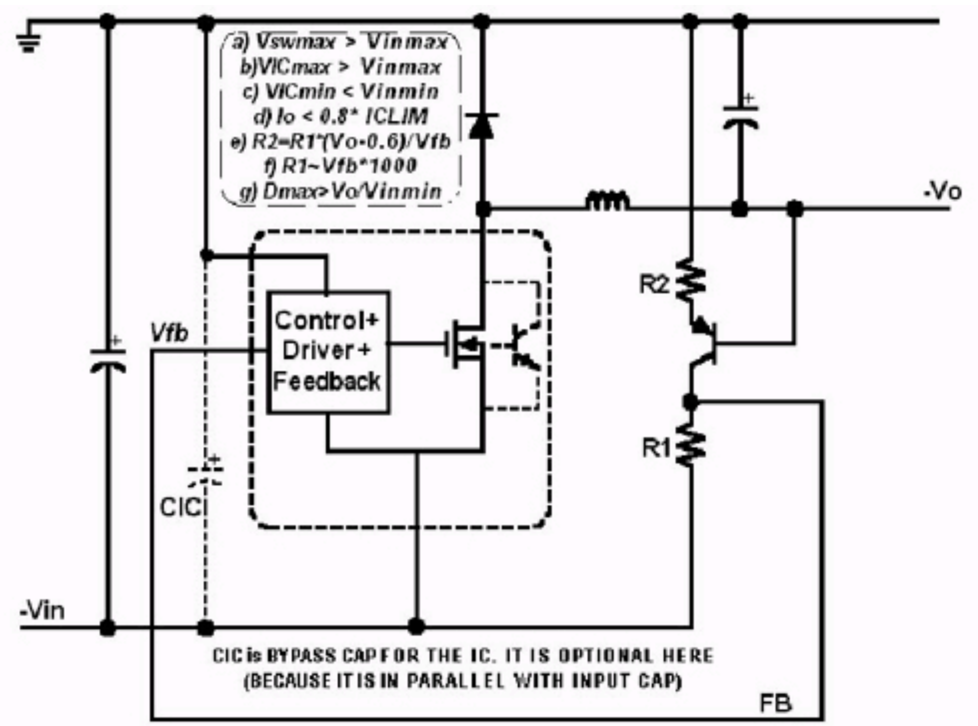
Positive to Positive Boost
using a Boost/Flyback (Type 1) IC

FIGURE 10



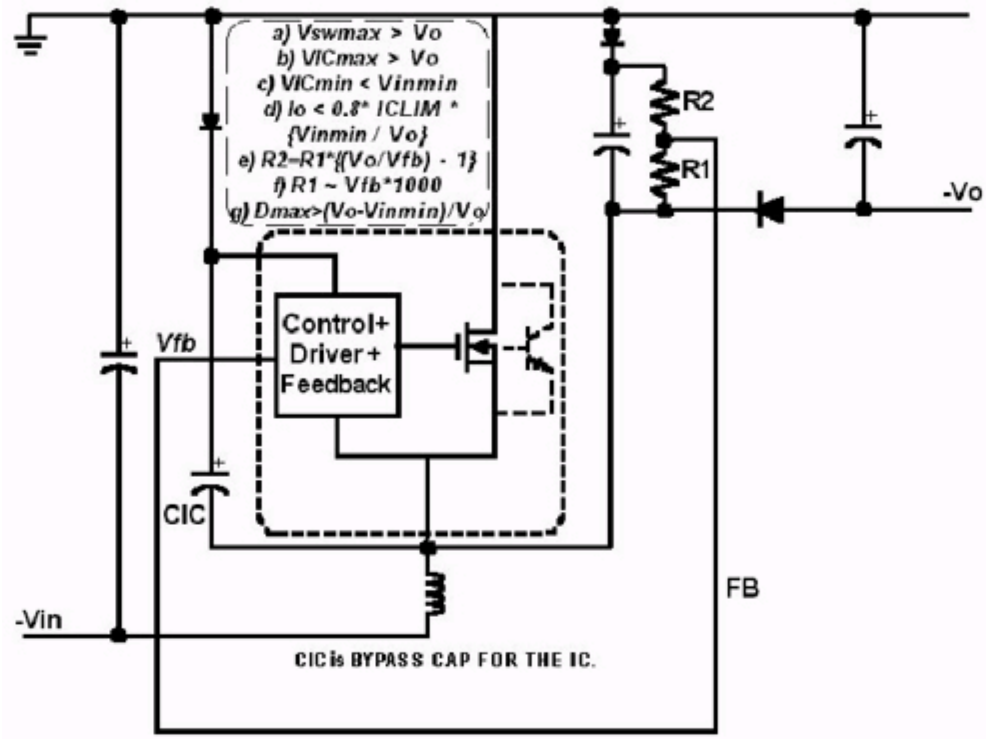
Negative to Positive Buck-Boost
using a Boost/Flyback (Type 1) IC

FIGURE 11



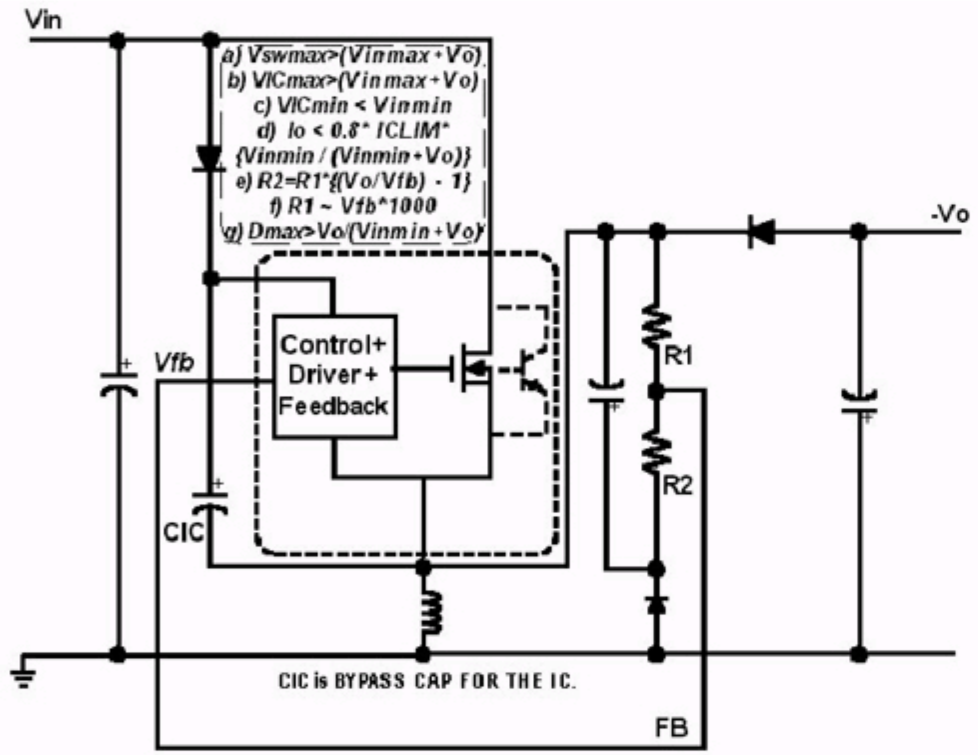
Negative to Negative Buck
using a Boost/Flyback (Type1) IC

FIGURE 12



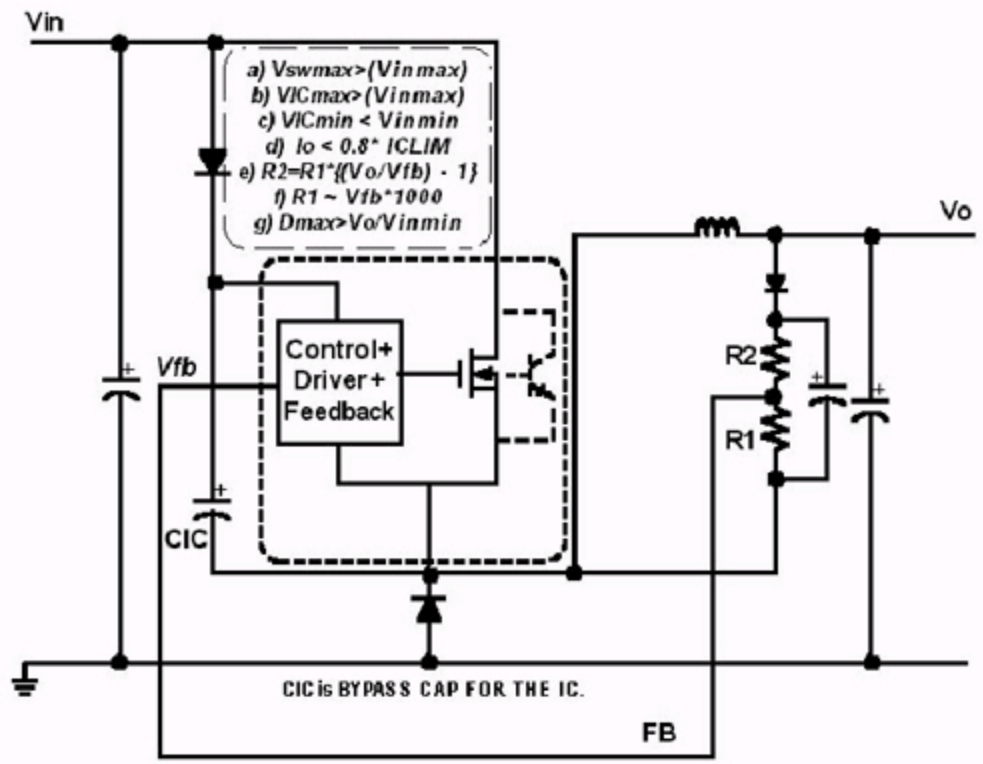
Negative to Negative Boost
using a Boost/Flyback (Type 1) IC

FIGURE 13



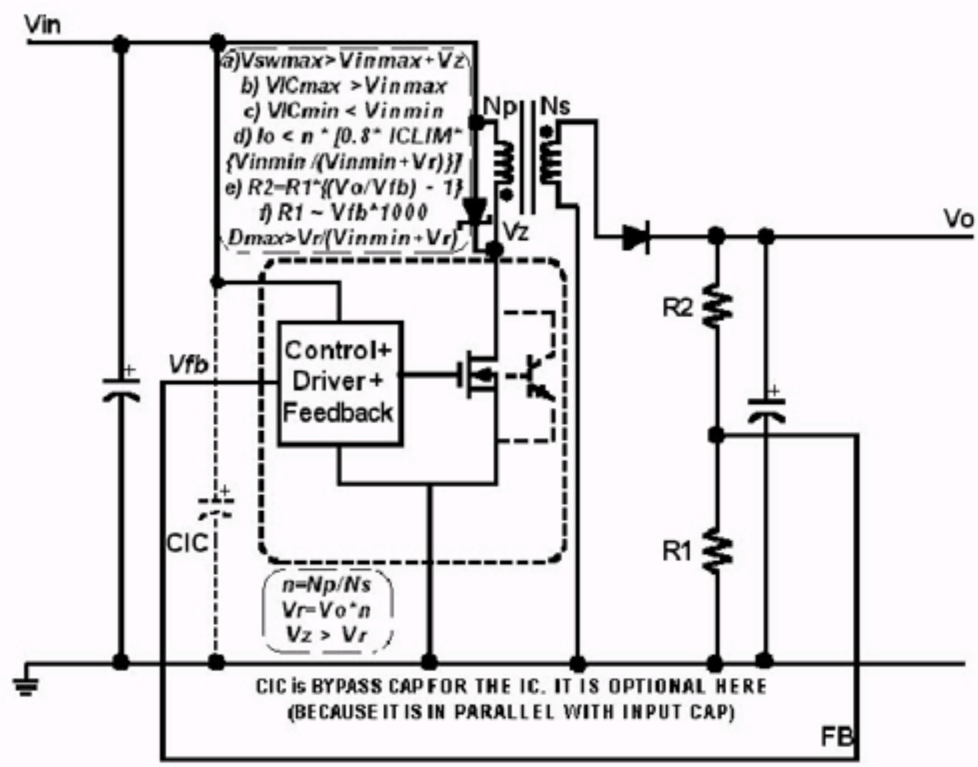
Positive to Negative Buck-Boost
using a Boost/Flyback (Type 1) IC

FIGURE 14



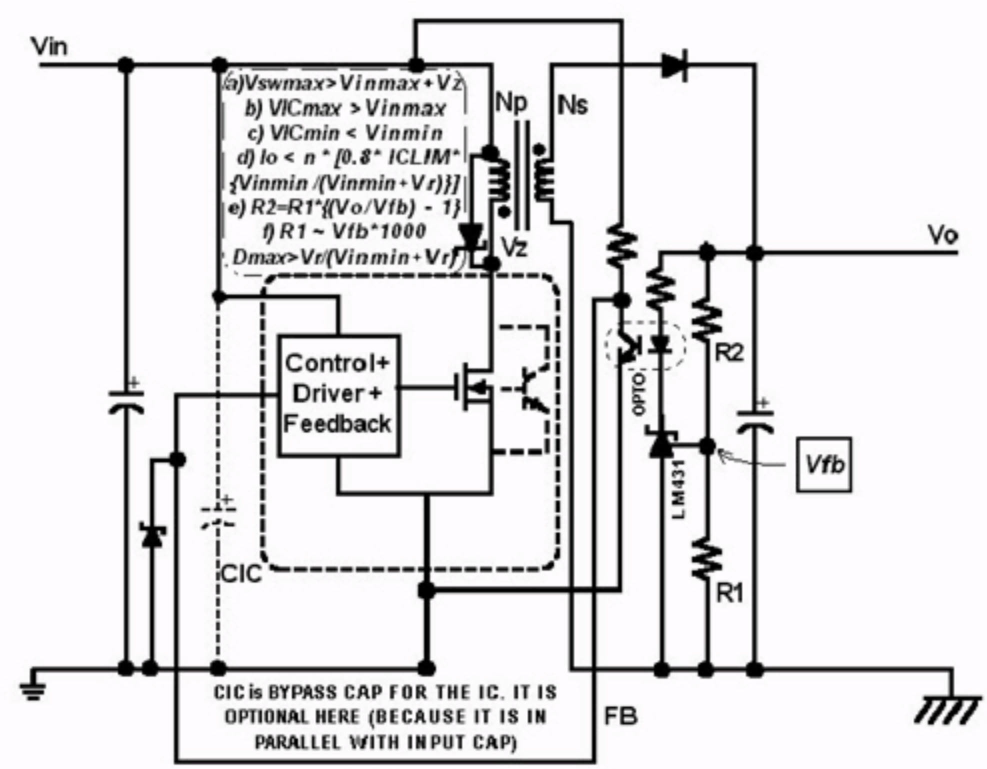
Positive to Positive Buck
using a Boost/Flyback (Type 1) IC

FIGURE 15



Positive to Positive Buck-Boost
using a Boost/Flyback (Type 1) IC

FIGURE 16



Positive to Positive Flyback
using a Boost/Flyback (Type 1) IC

FIGURE 17

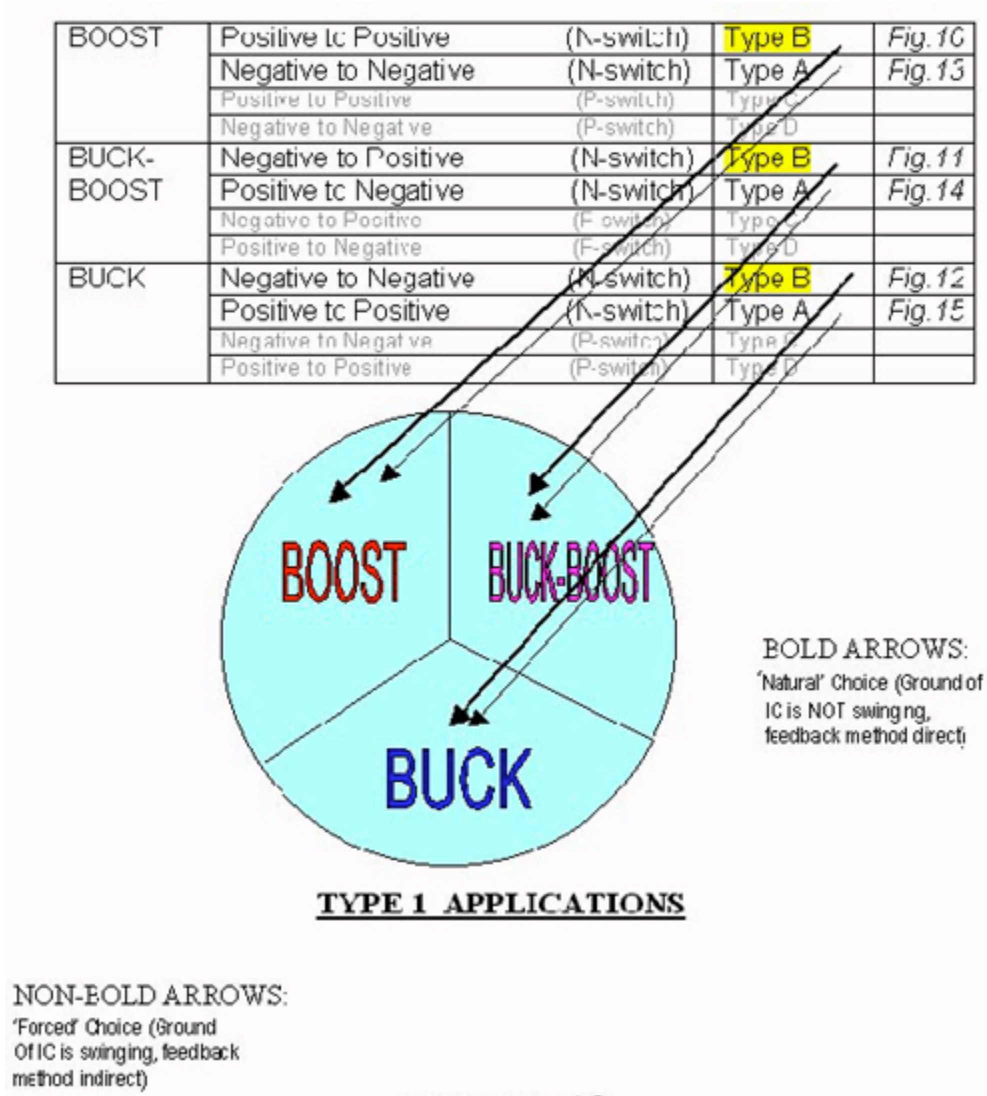


FIGURE 18

Table 2a: With Inductor

Topology	Configuration	IC*	Figure	Equation Set 1	Equation Set 2
BUCK	Positive to Positive	Type 1	Fig 15	$Vsw\ max \geq Vin\ max$ $VIC\ max \geq Vin\ max$ $VIC\ min \leq Vin\ min$	$Io \leq 0.8 \bullet ICLIM$ $R2 \approx R1 \bullet \left[\frac{Vo}{Vfb} - 1\right]$ $D\ max \geq \frac{Vo}{Vin\ min}$
		Type 2	Fig 19	$VIC\ max \geq Vin\ max$ $VIC\ min \leq Vin\ min$	$Io \leq 0.8 \bullet ICLIM$ $R2 = R1 \bullet \left[\frac{Vo}{Vfb} - 1\right]$ $D\ max \geq \frac{Vo}{Vin\ min}$
	Negative to Negative	Type 1	Fig 12 **	$Vsw\ max \geq Vin\ max$ $VIC\ max \geq Vin\ max$ $VIC\ min \leq Vin\ min$	$Io \leq 0.8 \bullet ICLIM$ $R2 \approx R1 \bullet \left[\frac{Vo - 0.6}{Vfb} - 1\right]$ $D\ max \geq \frac{Vo}{Vin\ min}$
		Type 2	X		
BOOST	Positive to Positive	Type 1	Fig 10	$Vsw\ max \geq Vo$ $VIC\ max \geq Vin\ max$ $VIC\ min \leq Vin\ min$	$Io \leq 0.8 \bullet ICLIM \bullet \frac{Vin\ min}{Vo}$ $R2 = R1 \bullet \left[\frac{Vo}{Vfb} - 1\right]$ $D\ max \geq \frac{Vo - Vin\ min}{Vo}$
		Type 2	X		
	Negative to Negative	Type 1	Fig 13	$Vsw\ max \geq Vo$ $VIC\ max \geq Vo$ $VIC\ min \leq Vin\ min$	$Io \leq 0.8 \bullet ICLIM \bullet \frac{Vin\ min}{Vo}$ $R2 \approx R1 \bullet \left[\frac{Vo}{Vfb} - 1\right]$ $D\ max \geq \frac{Vo - Vin\ min}{Vo}$
		Type 2	Fig 21	$VIC\ max \geq Vo$ $VIC\ min \leq Vin\ min$	$Io \leq 0.8 \bullet ICLIM \bullet \frac{Vin\ min}{Vo}$ $R2 = R1 \bullet \left[\frac{Vo}{Vfb} - 1\right]$ $D\ max \geq \frac{Vo - Vin\ min}{Vo}$

BUCK-BOOST	Positive to Negative	Type 1	Fig 14	$V_{sw\,max} \geq V_{in\,max} + V_o$ $V_{IC\,max} \geq V_{in\,max} + V_o$ $V_{IC\,min} \leq V_{in\,min}$	$I_o \leq 0.8 \bullet I_{CLIM} \bullet \frac{V_{in\,min}}{V_{in\,min} + V_o}$ $R2 = R1 \bullet \left[\frac{V_o}{V_{fb}} - 1\right]$ $D_{max} \geq \frac{V_o}{V_{in\,min} + V_o}$
		Type 2	Fig 20	$V_{IC\,max} \geq V_{in\,max} + V_o$ $V_{IC\,min} \leq V_{in\,min}$	$I_o \leq 0.8 \bullet I_{CLIM} \bullet \frac{V_{in\,min}}{V_{in\,min} + V_o}$ $R2 = R1 \bullet \left[\frac{V_o}{V_{fb}} - 1\right]$ $D_{max} \geq \frac{V_o}{V_{in\,min} + V_o}$
	Negative to Positive	Type 1	Fig 11 **	$V_{sw\,max} \geq V_{in\,max} + V_o$ $V_{IC\,max} \geq V_{in\,max}$ $V_{IC\,min} \leq V_{in\,min}$	$I_o \leq 0.8 \bullet I_{CLIM} \bullet \frac{V_{in\,min}}{V_{in\,min} + V_o}$ $R2 \approx R1 \bullet \left[\frac{V_o - 0.6}{V_{fb}} - 1\right]$ $D_{max} \geq \frac{V_o}{V_{in\,min} + V_o}$
		Type 2	X		

Table 2b: With Transformer

BUCK-BOOST	Positive to Positive	Type 1	Fig 16	$V_{sw\,max} \geq V_{in\,max} + V_z$ $V_{IC\,max} \geq V_{in\,max}$ $V_{IC\,min} \leq V_{in\,min}$ $n \equiv N_p / N_s$ $V_r \equiv V_o \bullet n$ $V_z > V_r$	$I_o \leq \left[0.8 \bullet I_{CLIM} \bullet \frac{V_{in\,min}}{V_{in\,min} + V_r}\right] \bullet n$ $R2 = R1 \bullet \left[\frac{V_o}{V_{fb}} - 1\right]$ $D_{max} \geq \frac{V_r}{V_{in\,min} + V_r}$
FLYBACK		Type 1	Fig 17***	$V_{sw\,max} \geq V_{in\,max} + V_z$ $V_{IC\,max} \geq V_{in\,max}$ $V_{IC\,min} \leq V_{in\,min}$ $n \equiv N_p / N_s$ $V_r \equiv V_o \bullet n$ $V_z > V_r$	$I_o \leq \left[0.8 \bullet I_{CLIM} \bullet \frac{V_{in\,min}}{V_{in\,min} + V_r}\right] \bullet n$ $R2 = R1 \bullet \left[\frac{V_o}{V_{fb}} - 1\right]$ $D_{max} \geq \frac{V_r}{V_{in\,min} + V_r}$

Note: By convention, R2 is always connected to the higher voltage rail of output and R1 to the lower.

*Type 1 IC is a 'Boost/Buck-Boost/Flyback IC'. Type 2 IC is a 'Buck IC'.

** For Figure 11 and 12, accurate differential amplifier sensing can be used: see Table 3 in the next Part of this article.

*** Vfb is NOT the voltage on feedback pin of IC in Figure 17. Also, set zener voltage Vz significantly higher than Vr (typically 20-30% higher) to minimize losses in zener and to maximize efficiency.

Conclusion of Part 2

In the next part we will cover applications using Type 2 (Buck) ICs. Improved techniques for implementing feedback using differential sensing will also be presented. Several worked examples will be provided using National's integrated switcher lineup. And finally some subtleties that must be kept in mind as we traverse topologies will also be presented.

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Previous issue - Part 1: It's A Switcher

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