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Implementing a CameraLink HS Interface Using the TLK3134

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ABSTRACT

This document is intended to aid designers in implementing a CameraLink HS interface using the TLK3134 SERDES. It discusses the reasons for choosing a discrete SERDES over an FPGA-integrated SERDES or custom ASIC, various considerations related to hardware development, how to configure the SERDES for a CameraLink HS application, and how to test and debug the high-speed serial interface.

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Introduction

CameraLink HS is a next generation machine vision interface that defines the connectivity between cameras, frame grabbers, and, in the future, intermediary devices. The interface defines the handling of video data, real-time triggers, and various command and control instructions.

Information sent using the CameraLink HS interface is divided into packets of various types: Trigger, GPIO, Ack/Nack, Video, Command, and Idle. For the M protocol variant, these packets consist of a sequence of data and control characters that are passed between the CameraLink HS IP Core and a physical layer device (PHY) using a nine-bit parallel interface. The interface uses one bit to indicate whether the word should be interpreted as data or control/status information, and the remaining eight bits to carry information.

To facilitate high-speed communication over physical media (such as CX4 copper cabling), physical layer devices are used to encode the nine-bit data bus, serialize it, transmit the high-speed data over some transmission medium, then deserialize and decode the received data at the far end of the link. CameraLink HS uses the 8b/10b encoding/decoding scheme to ensure DC balance of the serial data and to provide sufficient data transition density for proper recovery of embedded clock signals.

In implementing these physical layer functions, system designers are typically faced with a choice between custom IC (ASIC) development, using FPGA-integrated SERDES, or using a discrete SERDES solution. The discrete SERDES approach has several advantages:

- Using a discrete SERDES often provides substantial cost reductions when compared with custom ASIC development or use of a high-end FPGA.
- Full-featured FPGAs capable of supporting high-speed serial ports typically have large PCB footprints, and in many cases overall solution size can be reduced by using a discrete SERDES.
- Discrete SERDES are readily available “off the shelf,” and their performance has already been validated and characterized over their full specified operating range. This cuts down on the amount of additional development needed, resulting in reduced engineering costs and faster time-to-market.
- Discrete SERDES are often designed to operate over a wide range of clock frequencies, line rates, and parallel formats. This allows for more flexibility in design by supporting several operational modes using a single hardware platform.
- Adaptive receiver equalization, implemented in some discrete SERDES devices (such as the TLK3134), simplifies development by allowing the product to automatically adjust itself to accommodate various cable lengths.
- Many discrete SERDES devices feature improved ESD capability compared with FPGA solutions, enabling a more robust product.
- Integrated jitter cleaners in some discrete SERDES (such as the TLK3134) may result in a more robust clocking of data into an FPGA, or enable use of a less costly reference clock source.

- Features such as internal data loopback and recovered clock jitter cleaning allow for flexibility in system architectures. For example, parallel-side loopback enables data forwarding from a camera to a second frame grabber without the use of extra FPGA or ASIC pins.

This paper is intended to guide designers in implementing a CameraLink HS interface using the Texas Instruments TLK3134. The TLK3134 is a four-channel multi-rate transceiver that is capable of supporting all of the physical layer requirements of CameraLink HS. Additionally, the TLK3134 provides an extensive set of built-in self test features that allow for design validation and system margining. Although this paper focuses on the TLK3134, the guidelines presented can be applied to the single-channel (TLK3131) and dual-channel (TLK3132) variants as well.

Hardware Development

High-Speed Signals

The high-speed inputs (RDP/N) and outputs (TDP/N) of the TLK3134 use Current Mode Logic (CML) with integrated pull-up resistors. These signals can be DC-coupled or AC-coupled between devices, and no additional external components are necessary. For a CameraLink HS interface, AC-coupling is defined at both the transmitter and receiver devices. The TLK3134 transmitter supports adjustable differential swing levels and pre-emphasis, and the receiver features adaptive equalization. These features allow the device to be provisioned to operate over a wide variety of interconnect types and lengths.

It is important to follow all best practices of high-speed signal design. The signals should be routed over transmission lines with 100-Ω differential characteristic impedance. Intra-pair skew should be kept minimal, and impedance discontinuities should be avoided. Vias should be used as sparingly as possible, and when unavoidable should be used in such a way that via stubs are minimized.

Parallel Data Pins

The parallel HSTL inputs and outputs of the TLK3134 can be configured to operate in several different modes to suit a wide variety of applications. For a CameraLink HS M protocol interface, the device should be provisioned to operate in Nine Bit Interface mode. The mapping of a CameraLink HS parallel interface to the TLK3134 is as shown in Table 1:

Table 1. Parallel Pin Mapping

Channel Number	TX Data	TX Control Indicator	RX Data	RX Control Indicator	TX Input Clock	RX Output Clock
0	TXD_[7:0]	TXC_[0]	RXD_[7:0]	RXC_[0]	TXCLK_[0]	RXCLK[0]
1	TXD_[15:8]	TXC_[1]	RXD_[15:8]	RXC_[1]	TXCLK_[1]	RXCLK[1]
2	TXD_[23:16]	TXC_[2]	RXD_[23:16]	RXC_[2]	TXCLK_[2]	RXCLK[2]
3	TXD_[31:24]	TXC_[3]	RXD_[31:24]	RXC_[3]	TXCLK_[3]	RXCLK[3]

In interfacing the parallel inputs and outputs, it is important to ensure the following timing requirements are met between data and clocks:

Table 2. Parallel Input Timing Requirements

TXD data setup prior to TXCLK clock edge	480 ps (minimum)
TXD data hold after TXCLK clock edge	480 ps (minimum)
TXCLK clock duty cycle	40% to 60%
TXCLK clock frequency	30 MHz to 160 MHz

The timing characteristics of the TLK3134 parallel outputs are given in Table 3.

Table 3. Parallel Output Timing Characteristics

RXD data setup before RXCLK clock edge	1920 ps (minimum)
RXD data hold after RXCLK clock edge	1920 ps (minimum)
RXCLK clock duty cycle	40% to 60%
RXCLK clock frequency	30 MHz to 160 MHz

The HSTL input pins have selectable termination that can be configured as 150 Ω to VHSTL and ground, 200 Ω to VHSTL and ground, 300 Ω to VHSTL and ground, or high impedance. The high impedance option will consume the least power, and is a good default option to choose. If signal integrity is found to be an issue, then the lower-impedance termination options can be enabled.

Any unused parallel inputs should be grounded in the application.

Clocking Architecture

The TLK3134 requires a low-jitter reference clock to be supplied to the reference clock input (REFCLK). The device can tolerate frequency offsets of up to 200 ppm between the transmit and receive datapaths. In a CameraLink HS interface, this allows for the frame grabber and each camera to run with independent local clocks. Each local clock can have a +/- 100 ppm tolerance range, and is multiplied by the flexible PLL circuit in the TLK3134 to provide a 3.125 Gbps nominal data rate. The allowable reference clock frequencies and associated PLL multiplier values are shown below:

Table 4. Allowable Reference Clock Frequencies and Multiplier Values

REFCLK Frequency	Jitter Cleaner Multiplier	SERDES PLL Multiplier
312.5 MHz	OFF	5
156.25 MHz	OFF	10
78.125 MHz	OFF	20
312.5 MHz	0.25	20
312.5 MHz	0.5	10
156.25 MHz	0.5	20
156.25 MHz	1	10
78.125 MHz	1	20
78.125 MHz	2	10

In general, better jitter performance can be achieved by using a higher-frequency reference clock and a lower multiplier.

The TLK3134 has an internal narrow-band LC jitter cleaner that can optionally be used to reduce jitter on the reference clock input or the recovered clock output from Channel 0. The latter option can be used in custom data forwarding applications. Use of the internal jitter cleaner is not required for CameraLink HS as long as the reference clock input has less than 40 ps of total jitter. If use of the jitter cleaner is desired, consult the device datasheet for implementation details.

The parallel outputs of the TLK3134 will have a data rate that tracks the respective incoming serial line rate. Therefore, the receiving system must use the associated data strobe to clock the received data and K-code flag into the FPGA.

Control Pin Settings

The various control pins of the TLK3134 should be configured as follows:

- ST = ‘1’
- CODE = ‘0’
- PLOOP = ‘0’
- SLOOP = ‘0’
- SPEED[1:0] = “00” or “11”
- ENABLE = ‘1’
- PRBS_EN = ‘0.’

Device Configuration and CameraLink HS Discovery Process

Startup Procedure

To establish a high-speed link between a frame grabber and camera, the system must first go through a discovery process to bring up the link and determine which devices are connected. Note that at the time of this writing the CameraLink HS discovery process is not finalized. The following procedure may serve as an example until the standard is complete:

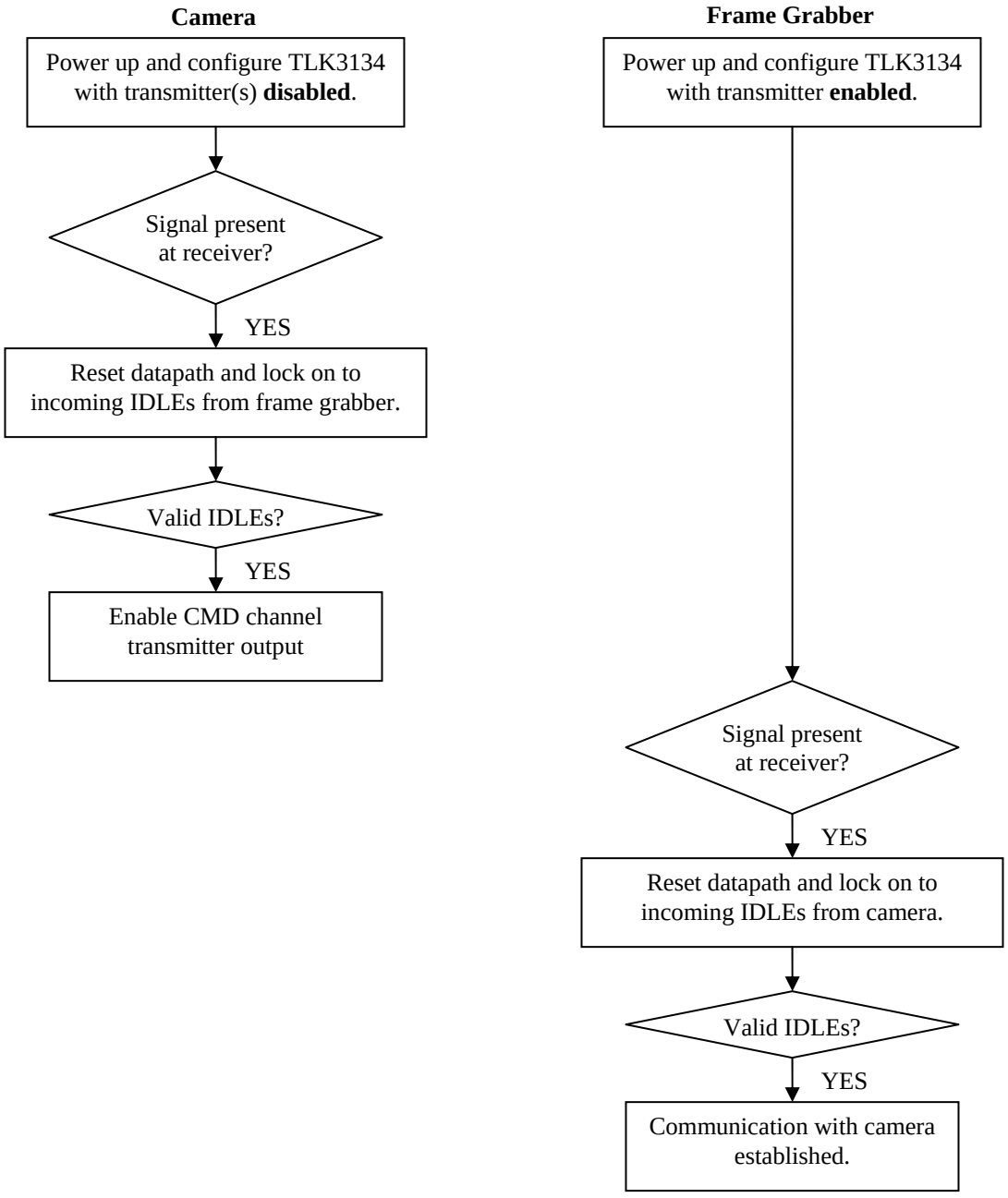

Figure 1. CameraLink HS Discovery Process.

Once the above flowchart is complete, a bidirectional command channel will have been established between the camera and frame grabber. At this point, the camera is ready to receive commands and normal link operation may begin.

TLK3134 Configuration

The TLK3134 register space is accessed through the Management Data Input/Output (MDIO) interface, a 2-wire serial control interface defined by the IEEE802.3 Ethernet standard. It consists of a bidirectional serial data line (called MDIO) and a clock line (called MDC) that is driven by a controller (such as an FPGA).

The TLK3134 supports two types of MDIO transactions – Clause 22 and Clause 45 – although not all registers are accessible through both methods. The registers needed for CameraLink HS can all be accessed via Clause 22. However, due to limitations of the 5-bit Clause 22 address field, MDIO operations to registers higher than 0x1F must use an indirect addressing method. In this method, the desired address is first written to location 0x1E. The register address stored in 0x1E can then be written or read by issuing write or read commands to register 0x1F.

Bits in the TLK3134 register space take on the following naming convention:

- Bits that are controlled directly through Clause 22 are named as x.y, where “x” is the decimal representation of the address, and “y” is the bit (or range of bits).
- Bits that are controlled indirectly through Clause 22 are named as 4/5.x.y. The “4/5” prefix indicates indirect addressing is needed, “x” represents the decimal value of the register in the extended register space (this is the address that needs to be written to 0x1E), and “y” represents the bit (or range of bits).

Each Clause 22 MDIO transaction will consist of the following steps:

- A preamble (32 consecutive “ones”)
- A start code (“01”)
- The operation code
  - For a read operation, the code is “10.”
  - For a write operation, the code is “01.”
- A 5-bit PHY address
  - This allows for multiple devices to share a common control bus.
  - For the TLK3134 in Clause 22 mode, the 3 MSBs of the PHY address are determined by the settings of the PRTAD[4:2] pins.
  - The 2 LSBs of the PHY address correspond to the channel being addressed. Note that only some registers are defined on a per-channel basis; others are defined globally for the device. For registers that take effect per-channel, the mapping between PHY address LSBs and TLK3134 channel number is:
    - “00” → Channel 0
    - “01” → Channel 1

- “10” → Channel 2
- “11” → Channel 3

- A 5-bit register address
- 2-bit turnaround
  - For a read command, the turnaround is when control of the bus is transferred from the controller to the device being addressed. It consists of one bit period in which neither device drives the MDIO line (and it is pulled high by an external resistor) followed by one bit period in which the device being read from drives the MDIO line low.
  - For a write command, the turnaround is still included but has no function. MDIO controller should just send the pattern “10.”
- 16 bits of data

The following sequence of register operations may be used to configure the device at startup:

- Issue a reset by asserting the RST_N pin low for at least 10 µs.
- If the device is used in a camera, the transmitter outputs can be disabled by writing 1’b0 to bits 4/5.36874.0, 4/5.36876.0, 4/5.36878.0, 4/5.36880.0 for Channels 0, 1, 2, and 3 respectively.
- Clock Configuration (assume differential reference clock input of 156.25 MHz, jitter cleaner bypassed)
  - Write 2’b01 to 4/5.37120.13:12 to select RX SERDES recovered clock as RXBYTECLK
  - Write 2’b10 to 16.10:9 to select RX SERDES recovered clock as RX_CLK output (per channel)
  - Write 7’h04 to 4/5.37121.6:0 to set HSTL_DIV2 to value of 4. This is needed to provide a clock frequency of approximately 40 MHz to the HSTL impedance compensation circuitry. Different divider values can be used depending on the clock source used.
  - If a higher or lower reference clock frequency is used, adjust the PLL multiplier settings in 4/5.36864.11:8 and 4/5.36864.3:0 accordingly.
- Mode Control (single data rate NBI mode, 312.5 MHz operation)
  - Write 1’b0 to 17.5 enable SDR mode (for channels 0 through 3, as appropriate)
  - Write 1’b0 to 17.1 for falling-edge aligned parallel input data (latched on rising edge), or write 1’b1 for rising-edge aligned input data (latched on falling edge) (for channels 0 through 3, as appropriate)
  - Write 1’b0 to 17.0 for falling-edge aligned parallel output data (latched on rising edge), or write 1’b1 for rising-edge aligned data (latched on falling edge) (for channels 0 through 3, as appropriate)
  - Write 1’b1 to 17.2 to enable 8B/10B encode decode functions (for channels 0 through 3, as appropriate)
- SERDES Transceiver Settings

- These transmit settings are appropriate for links between frame grabbers and cameras. They support interconnect lengths from one meter to the 15 meter maximum distance over CameraLink HS standard media:
  - Write 3'b111 to 4/5.36874.11:9 to set channel 0 TX swing setting amplitude to 1375 mVpp
  - Write 4'b1011 to 4/5.36874.7:4 to set channel 0 TX de-emphasis ratio to -6.44 dB
  - Write 1'b1 to 4/5.36874.8 to set channel 0 TX CM bit
  - Write 3'b111 to 4/5.36876.11:9 to set channel 1 TX swing setting amplitude to 1375 mVdfpp
  - Write 4'b1011 to 4/5.36876.7:4 to set channel 1 TX de-emphasis ratio to -6.44 dB
  - Write 1'b1 to 4/5.36876.8 to set channel 1 TX CM bit
  - Write 3'b111 to 4/5.36878.11:9 to set channel 2 TX swing setting amplitude to 1375 mVpp
  - Write 4'b1011 to 4/5.36878.7:4 to set channel 2 TX de-emphasis ratio to -6.44 dB
  - Write 1'b1 to 4/5.36878.8 to set channel 2 TX CM bit
  - Write 3'b111 to 4/5.36880.11:9 to set channel 3 TX swing setting amplitude to 1375 mVpp
  - Write 4'b1011 to 4/5.36880.7:4 to set channel 3 TX de-emphasis ratio to -6.44 dB
  - Write 1'b1 to 4/5.36880.8 to set channel 3 TX CM bit
- These transmit settings are appropriate for links between multiple frame grabbers. They support interconnect lengths of 10 meters or less:
  - Write 3'b100 to 4/5.36874.11:9 to set channel 0 TX swing setting amplitude to 750 mVpp
  - Write 4'b1000 to 4/5.36874.7:4 to set channel 0 TX de-emphasis ratio to -4.16 dB
  - Write 1'b1 to 4/5.36874.8 to set channel 0 TX CM bit
  - Write 3'b100 to 4/5.36876.11:9 to set channel 1 TX swing setting amplitude to 750 mVpp
  - Write 4'b1000 to 4/5.36876.7:4 to set channel 1 TX de-emphasis ratio to -4.16 dB
  - Write 1'b1 to 4/5.36876.8 to set channel 1 TX CM bit
  - Write 3'b100 to 4/5.36878.11:9 to set channel 2 TX swing setting amplitude to 750 mVpp
  - Write 4'b1000 to 4/5.36878.7:4 to set channel 2 TX de-emphasis ratio to -4.16 dB
  - Write 1'b1 to 4/5.36878.8 to set channel 2 TX CM bit
  - Write 3'b100 to 4/5.36880.11:9 to set channel 3 TX swing setting amplitude to 750 mVpp
  - Write 4'b1000 to 4/5.36880.7:4 to set channel 3 TX de-emphasis ratio to -4.16 dB

- Write 1’b1 to 4/5.36880.8 to set channel 3 TX CM bit

– These receive settings can be used in conjunction with the above transmit settings to achieve the CameraLink HS bit error rate requirements:
  - Write 4’b0001 to 4/5.36866.15:12 to turn on adaptive equalization
  - Write 4’b0001 to 4/5.36868.15:12 to turn on adaptive equalization
  - Write 4’b0001 to 4/5.36870.15:12 to turn on adaptive equalization
  - Write 4’b0001 to 4/5.36872.15:12 to turn on adaptive equalization
  - Write 2’b01 to 4/5.36866.3:2 since AC coupling is used
  - Write 2’b01 to 4/5.36868.3:2 since AC coupling is used
  - Write 2’b01 to 4/5.36870.3:2 since AC coupling is used
  - Write 2’b01 to 4/5.36872.3:2 since AC coupling is used
– TX DLL Offset settings:
  - Write 16'h0028 to 4/5.37888 TX0_DLL_CONTROL
  - Write 16'h0028 to 4/5.37889 TX1_DLL_CONTROL
  - Write 16'h0028 to 4/5.37890 TX2_DLL_CONTROL
  - Write 16'h0028 to 4/5.37891 TX3_DLL_CONTROL

- Poll Serdes PLL Status for Locked State
  – Read 4/5.36891.4,0 SERDES_PLL_STATUS – PLL_LOCK_TX/RX
  – Keep polling until both bits are high
- Issue data path reset and issue HSTL retrain
  – Write 1’b1 to 16.11 (for Channels 0 though 3, as appropriate)
  – Write 1'b0, 1'b1, followed by 1'b0 to 37636.14
  – Note that during a reset the transmitter output may not be valid.
- Clear Latched Registers
  – Read 1 PHY_STATUS_1 to clear (for Channels 0 though 3, as appropriate)
  – Read 28 PHY_CHANNEL_STATUS to clear (for Channels 0 though 3, as appropriate)
  – Read 4/5.36891 SERDES_PLL_STATUS to clear
- Monitor link status signals. In a frame grabber, these signals can be used to monitor each channel’s status and make sure there are no problems. In a camera, these signals can be used to gate the transmitter output.
  – Read Verify 1.2 PHY_STATUS_1 – Link Status (1’b1) (for Channels 0 though 3, as appropriate). When this bit is high, it means that the receiver has been able to align to the serial word boundary and valid codes are being received.

- If the device is used in a camera, wait for the above three signals to become valid and then enable the transmitter output by writing 1'b1 to bits 4/5.36874.0, 4/5.36876.0, 4/5.36878.0, 4/5.36880.0 for Channels 0, 1, 2, and 3 respectively (as appropriate).

System Evaluation and Test

The TLK3134 is capable of generating and verifying test patterns to aid system designers in evaluating their high speed link. These patterns can be sent over an interconnect and checked by the TLK3134 (or other capable receiver) at the far end for any errors. A detailed description of how to select and enable these test patterns and check for errors can be found in the device datasheet.

The test patterns supported are: PRBS (2^7 – 1 and 2^{23} – 1), CRPAT, CJPAT, and Mixed/High/Low Frequency. Each of these patterns will measure different aspects of a system's performance.

PRBS Pattern Testing

A PRBS pattern is a sequence that has similar properties to random data, but can be generated algorithmically. This makes it possible to verify whether or not the data is correct. The TLK3134 supports two PRBS patterns: PRBS 2^7 – 1 and PRBS 2^{23} – 1.

PRBS 2^7 – 1 data will repeat every 127 bits, and will have at most seven consecutive identical symbols (ones or zeros). This is more than the number found in 8b/10b-encoded data (which is limited to five consecutive identical symbols), and this decreased transition density makes clock recovery more difficult. In this sense, PRBS-based testing can be considered slightly more stringent than testing with encoded data patterns.

PRBS 2^{23} – 1 data will repeat every 8,388,607 bits. It will have much longer possible run lengths than CameraLink HS data, and may be unnecessarily stringent in evaluating the BER of a CameraLink HS system. This pattern is useful in evaluating the ability of a system to transmit and receive data streams with significant low-frequency components.

CRPAT and CJPAT Testing

CRPAT and CJPAT are both 8b/10b-encoded sequences, so their properties are the most similar to the data that will be passed over a CameraLink HS link. Note, however, that the data in these patterns is arranged in columns across all four channels, so it may not be valid if fewer channels are used.

CRPAT is designed to have frequency content that is distributed over a broad bandwidth and up to higher frequencies. Much of the frequency content in the CRPAT waveform will be higher than the bandwidth of the SERDES's clock recovery circuit, so it can be used to test the performance of the media independent of the performance of the receiver's clock recovery.

CJPAT has more substantial frequency content within the clock recovery circuit's bandwidth, and is useful in evaluating the full system (transmitter, receiver, and interconnect) performance. It is designed to stress the clock recovery circuit as well as the system's robustness against random and deterministic jitter.

Mixed/High/Low Frequency Testing

The High Frequency Test Pattern is made up of alternating ones and zeros, which represents the highest frequency content that can be output from the transmitter. It can be useful in evaluating the high-frequency loss over an interconnect. In jitter analysis, it is useful for measuring random jitter, since it is a clock pattern and as such will not exhibit data-dependent jitter.

The Low Frequency Test Pattern will create a clock pattern at a lower frequency by outputting several consecutive ones followed by several consecutive zeros. It can be useful in evaluating the ability of the link to transfer the lowest frequency content necessary for encoded data.

The Mixed Frequency Test Pattern consists of several consecutive ones or zeros followed by a few fast transitions. This type of pattern is strongly affected by intersymbol interference (ISI), so it can be a useful tool in determining whether ISI is a dominant cause of bit errors.

Debugging Using the TLK3134 Status Indicators

The TLK3134 provides several status indicators in its register map that can be used to identify and diagnose issues with the link. This section highlights some of the indicators that may be most useful to monitor in a CameraLink HS system. For a detailed description of all the available indicators, consult the device data sheet. Note that many of the status indicators can be addressed on a per-channel basis.

Link Status (Bit 1.2)

The Link Status bit gives a binary indication of whether the receive lane is up or down. A lane that is “up” has received comma characters and found stable byte delineation in the serial input data. Receiving misaligned commas or invalid code words can cause the link to become down. When the link is detected to be down, the other status bits should be polled to see if the cause can be determined.

TX_WIDE_FIFO_Overflow (Bit 20.15), TX_WIDE_FIFO_Underflow (Bit 20.14), and RX_CTC_Reset (Bit 18.15)

These bits indicate overflow or underflow conditions in the transmit- or receive-direction FIFOs. When FIFO collisions are detected, it means that there is some mismatch between the rate to which the FIFO is written and the rate at which it is read. If FIFO collisions are detected, the clocking architecture chosen and the quality of the reference clock should be examined.

Signal Detect (Bit 28.15)

This bit indicates whether or not a signal of sufficient amplitude is present at the serial input pins. It is latched low, so a “0” indicates that a valid signal was not present at some point between the current read and the previous read. Therefore, it can be polled twice to see if the invalid input condition was temporary or if it persists.

Encoder Invalid Code Word (Bit 28.13)

When high, this bit indicates and invalid input to the encoder. This indicates an issue with the parallel data. If this error is present, the parallel input data should be checked to make sure that it meets the signal level and timing requirements defined in the datasheet. The implementation of the nine-bit interface should be checked as well to make sure that it does not produce any invalid K-codes. Note that this bit is latched high.

Decoder Invalid Code Word (Bit 28.12)

When high, this bit indicates and invalid input to the decoder. This indicates an issue with the serial data. If these errors occur intermittently, the transmit and receive settings used with the link should be adjusted to see if a more robust operating point can be reached. If these errors can not be mitigated or if they occur with great frequency, there is likely some greater problem with the link. Decode errors are also signaled on the parallel outputs by the code 0xFE with the control bit set to "1." Note that this bit is latched high.

PLL_LOCK_RX (Bit 4/5.36891.4) and PLL_LOCK_TX (Bit 4/5.36891.0)

These bits indicate that the receive- or transmit-side PLLs have achieved lock to their reference clocks. A low level indicates that the PLLs have not achieved or have lost lock. Issues with PLL lock suggest an unstable or invalid reference clock.

INVPAIR (Bits 4/5.36866.8, 4/5.36868.8, 4/5.36870.8, 4/5.36872.8, 4/5.36874.8, 4/5.36876.8, 4/5.36878.8, 4/5.36880.8)

These bits allow for the polarity of each serial receive and transmit lane to be individually inverted. These are not status bits, but can be useful in debugging a miswired cable or PCB. Inverting the pair polarity is equivalent to swapping the "P" and "N" halves of the signal. Note that inverted 8b/10b data will often be detected as valid by the decoder (since it is still a valid 8b/10b code), but will appear as invalid data to higher protocol layers (such as a controller FPGA).

Conclusion

In implementing a CameraLink HS interface, using a discrete SERDES provides many advantages over an FPGA-integrated SERDES or custom ASIC. The TLK3134 SERDES device, along with the single- and dual-channel variants (TLK3131 and TLK3132), is able to meet the requirements of the CameraLink HS standard while providing additional capability, simplifying development, and lowering overall BOM cost. In addition, the TLK3134 offers a broad set of features that simplify camera and frame grabber development, system verification, and *in situ* debug.

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