

TI 参考设计: TIDA-01435

适用于微波回程连线的高带宽、零 IF 参考设计



说明

该参考设计描述了连接 TSW40RF82EVM 和 TRF370417EVM 的方法。TSW40RF82EVM 参考设计为连接 DAC38RF82 和高性能调制器 TRF370417EVM 提供了平台。TRF370417EVM 可在高达 6GHz 的频率下调制宽带信号。TRF370417 器件可替代适用的高频器件。只需进行极少的改动即可将数模转换器 (DAC) 与调制器对接。

资源

TIDA-01435	设计文件夹
DAC38RF82	产品文件夹
TRF370417EVM	产品文件夹
TSW40RF82EVM	产品文件夹

特性

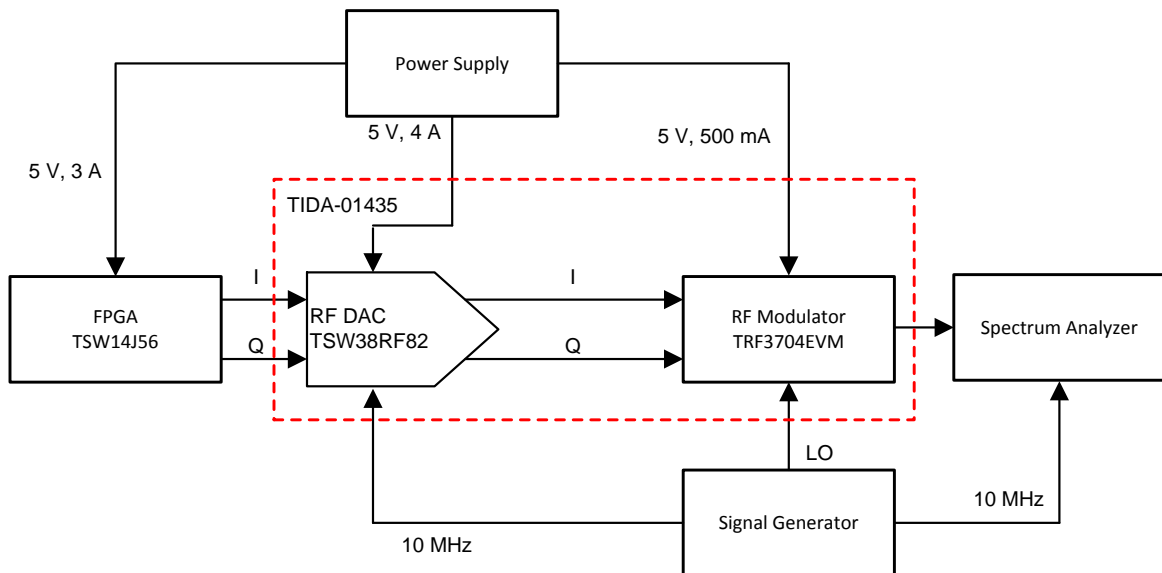
- 高带宽零中频 (零 IF) 发送器解决方案
- 射频采样速度高达 8 GSPS 的 DAC 解决方案
- TRF370417EVM 在高达 6GHz 的频率下进行宽带调制
- 调制器可互换以获得更高的射频频率
- 5GHz 频段内的调制误差比 (MER) 超过 40dB

应用

- [无线基础设施](#)
- [微波回程连线](#)



咨询我们的 E2E 专家



Copyright © 2017, Texas Instruments Incorporated



该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

The TSW40RF82EVM reference design demonstrates an RF transmitter solution that supports zero-IF microwave backhaul applications. This reference design includes the DAC38RF82 DAC, which interfaces with the TRF3704 modulator.

Quadrature amplitude modulation (QAM) is commonly used in microwave backhaul applications. Increasing the QAM level produces a higher throughput or capacity, but this method results in diminishing returns (see 表 1). The improvement in capacity is eventually outweighed by the deteriorating RF performance. Increasing the bandwidth instead of increasing the QAM level is a more efficient way to increase capacity. For example, increasing the level from 512 QAM to 1024 QAM results in a mere 11.11% increase in capacity at an additional cost of increased carrier-to-interference susceptibility; however, doubling the transmission bandwidth results in a 100% capacity increase, regardless of the QAM level, without the cost of increased sensitivity to interference.

表 1. Diminishing Efficiency With Increased QAM Level

QAM LEVEL	NUMBER OF BITS PER SYMBOL	EFFICIENCY OVER PREVIOUS QAM LEVEL
4 QAM	2	—
8 QAM	3	50.00%
16 QAM	4	33.33%
32 QAM	5	25.00%
64 QAM	6	20.00%
128 QAM	7	16.67%
256 QAM	8	14.29%
512 QAM	9	12.50%
1024 QAM	10	11.11%

The TIDA-01435 reference design allows the utilization of 5-GHz unlicensed bands. The benefits of utilizing 5-GHz bands include [1]:

1. Abundance of available channels – 21 non-overlapping 20-MHz channels (or 9 non-overlapping 40-MHz channels)
2. Less interference – Largely available and much less crowded, which translates into less RF interference
3. Improved performance – Improved spectrum efficiency and higher data rates due to lower interference levels and the availability of the channels

For applications operating at higher frequencies, substitute a higher frequency modulator for the TRF370417 device. This substitution may require an interface network that holds the respective common-mode voltages (V_{CM}) of the DAC and modulator to their nominal values. This type of network can be designed and implemented according to [High Bandwidth, High Frequency Transmitter Solution](#) [2].

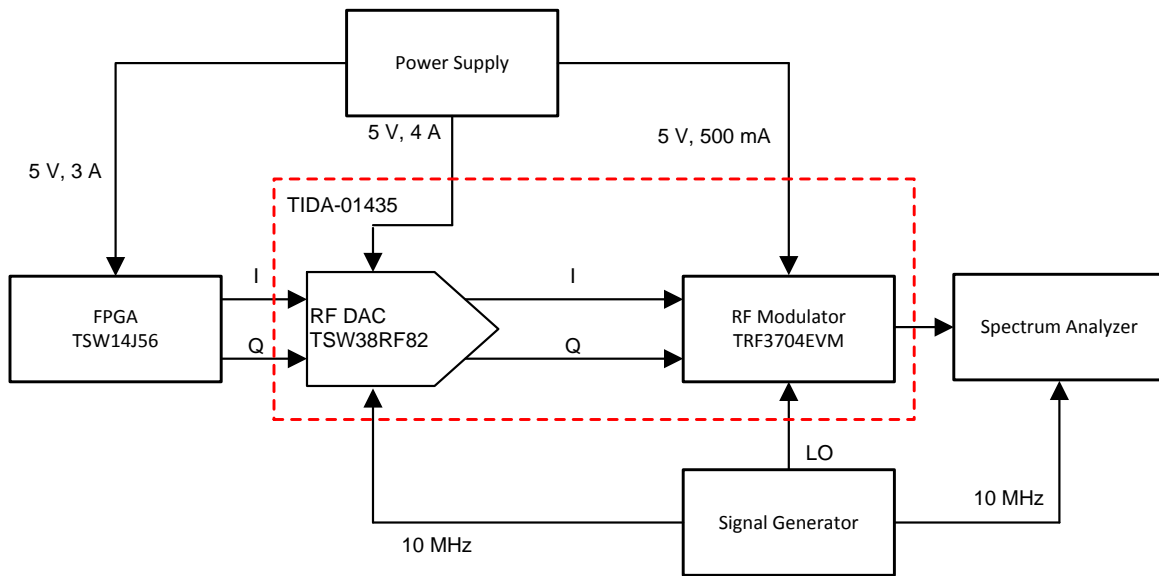
1.1 Key System Specifications

表 2. Key System Specifications

SPECIFICATIONS	TYPICAL	UNITS
Max frequency	6	GHz
Quadrature amplitude modulation (QAM)	64	Symbols
Bandwidth (BW)	80	MHz
Modulation error ratio (MER)	40	dB

2 System Overview

2.1 Block Diagram



Copyright © 2017, Texas Instruments Incorporated

图 1. TIDA-01435 Block Diagram

2.2 Highlighted Products

2.2.1 DAC38RF82

The DAC38RF82 is high performance RF Sampling Digital to Analog Converter (DAC). It is capable of sampling up to 9-GSPS. It is a dual channel device that supports a data rate up to 3.33-GSPS. This device is suited for using each channel as a very wide bandwidth quadrature input to an RF modulator.

2.2.2 TRF370417

The TRF370417 quadrature modulator operates up to 6-GHz. It supports wide bandwidths on the input baseband up to 1-GHz which yields up to 2-GHz RF signal bandwidth. The baseband ports operate at a common mode voltage of 1.7-V which matches the DAC38RF82 requirements.

2.2.3 TSW40RF82

The TSW40RF82 is a reference design that incorporates the DAC38RF82. The normal configuration of the reference design includes a transformer to convert the differential output to a single-ended output for interfacing with 50-ohm test equipment. The TSW40RF82 reference design also provides an option to access to the differential outputs directly. This access interfaces directly to the RF modulator.

3 Getting Started

3.1 Modifications for TSW40RF82EVM and TRF370417EVM Operation

3.1.1 Power Requirement

The TSW40RF82EVM requires a 5-V, 4-A supply, while the TRF370417EVM operates at a 5-V, 1-A supply. An additional external supply is applied at TP16 on the TSW40RF82EVM. This supply sets the common-mode voltage that is required by the DAC output and modulator input. The DAC gain is first set to the desired value and the external supply is then ramped up until the V_{CM} at the input of the modulator is equal to 1.7 V. If the DAC gain is changed, the external supply voltage must be adjusted accordingly. The DAC gain may overdrive the modulator if it is set at an extreme value. TI recommends a coarse DAC gain of 7 to 10 to drive the TRF370417EVM..

3.1.2 TSW40RF82EVM Modifications

- The RF shield near J3 must be removed to gain access to the interconnect components
- Resistors R380, R382, R383, R385, R388, and R390 must be populated with 0- Ω resistors
- Resistors R381, R384, R385, R386, R389, and R391 must be uninstalled
- 50- Ω resistors should be populated in place of L1, L2, L7, and L8

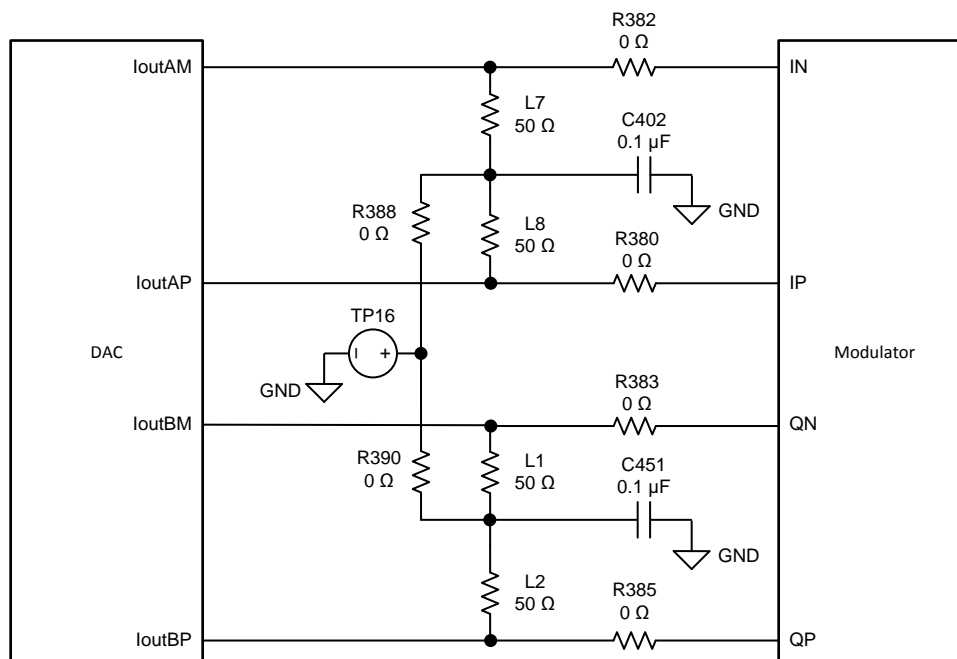


图 2. TSW40RF82EVM-to-TRF370417EVM Interface Schematic

4 DAC Configuration

The following restraints require consideration when interfacing the DAC with the modulator:

1. I and Q must be output in differential form because the modulator has two differential inputs.
2. The voltage-controlled oscillator (VCO) of the LMK04828 must be set to a valid frequency. This frequency sets the field-programmable gate array (FPGA) clock frequency and must be compatible with the input data rate, which is determined by the DAC sampling frequency and interpolation factor.
3. The sampling frequency must be within the range of valid frequencies of the DAC VCO.
4. The SerDes lane rate between the FPGA board and the DAC must not exceed the maximum JESD bit rate of 12.5 Gbps.

The DAC is set to dual DAC mode, real input, four lanes per DAC, and 4x interpolation operating at a JESD204B LMF configuration of 821. Setting the DAC to *real input*, despite actually outputting a complex baseband (BB) signal, isolates the DAC channels and preserves I and Q without adding them internally in the DAC.

The LMK04828 VCO is locked to 3072 GHz. This frequency is phase-locked to the on board 122.88-MHz voltage-controlled crystal oscillator (VCXO) through a 1/25 divider ratio. The numerator of the multiplier/divider ratio is set to one to ensure that the phase alignment occurs on every clock cycle of the crystal.

The DAC sampling clock is set to 8192 MHz and the interpolation is set to four, which, in turn, sets the data rate to 2048 MHz. This rate is divided down by a factor of 12 to produce the required FPGA clock of 256 MHz. The LMK04828 VCO must be divided down by an integer to produce the exact clock rate required by the FPGA.

The onboard VCXO can be interchanged with a different crystal or the divider ratio can be adjusted to obtain a different LMK04828 VCO frequency.

The following equations control the relevant frequencies for this design:

$$\text{Input Data Rate} = \left(\frac{f_s}{\text{Interpolation}} \right)$$

$$\text{SerDes Rate} = \left((\text{Input Data Rate}) \times (\text{Number of Channels}) \times \left(\frac{10}{8} \right) \times \left(\frac{1}{\text{Lanes}} \right) \times (\text{DAC}_{\text{RESOLUTION}}) \right)$$

$$\frac{\text{SerDes Rate}}{40} = f_{\text{FPGA}}$$

$$f_{\text{VCO_LMK04282}} = N_{\text{DIV}} \times f_{\text{FPGA}}$$

A data rate of 2048 MHz is used for this design. This data rate allows for an effective bandwidth of approximately 1 GHz ($f_s / 2$). The interpolation is set to four, which fixes the sampling frequency as follows in [公式 1](#):

$$2048 \times 4 = 8192 \text{ MHz} \quad (1)$$

Use [公式 2](#) to solve for the SerDes rate.

$$\left(\frac{8192}{4} \right) \times (2) \times \left(\frac{8}{10} \right) \times \left(\frac{1}{8} \right) \times (16) = 10240 \text{ MHz} \quad (2)$$

This rate is under the 12.5-GSPS limit and is a valid SerDes rate. Applying [公式 2](#) produces the FPGA frequency of the TSW14J56EVM in [公式 3](#):

$$\left(\frac{10240}{40} \right) = 256 \text{ MHz} \quad (3)$$

The quotient of the LMK04828 VCO frequency and the FPGA clock frequency must be an integer because the FPGA clock is synthesized from this VCO frequency through an integer divider. Any LMK04828 VCO frequency is valid as long as this requirement is satisfied and the selected frequency is confirmed to be within the specified locking range of the VCO. 公式 4 is then applied to obtain the LMK04828 VCO frequency:

$$256 \times 12 = 3072 \text{ MHz} \tag{4}$$

In summary, the frequency of the LMK04828 VCO and FPGA clock is determined and held constant. The system of equations is then solved to determine a valid sampling frequency that is within the range of the DAC phase-locked loop (PLL) and VCO. The previous configuration results in a SerDes lane rate of 10240 MHz, which is under the maximum lane rate of 12.5 GHz. 图 3 shows the design configuration.

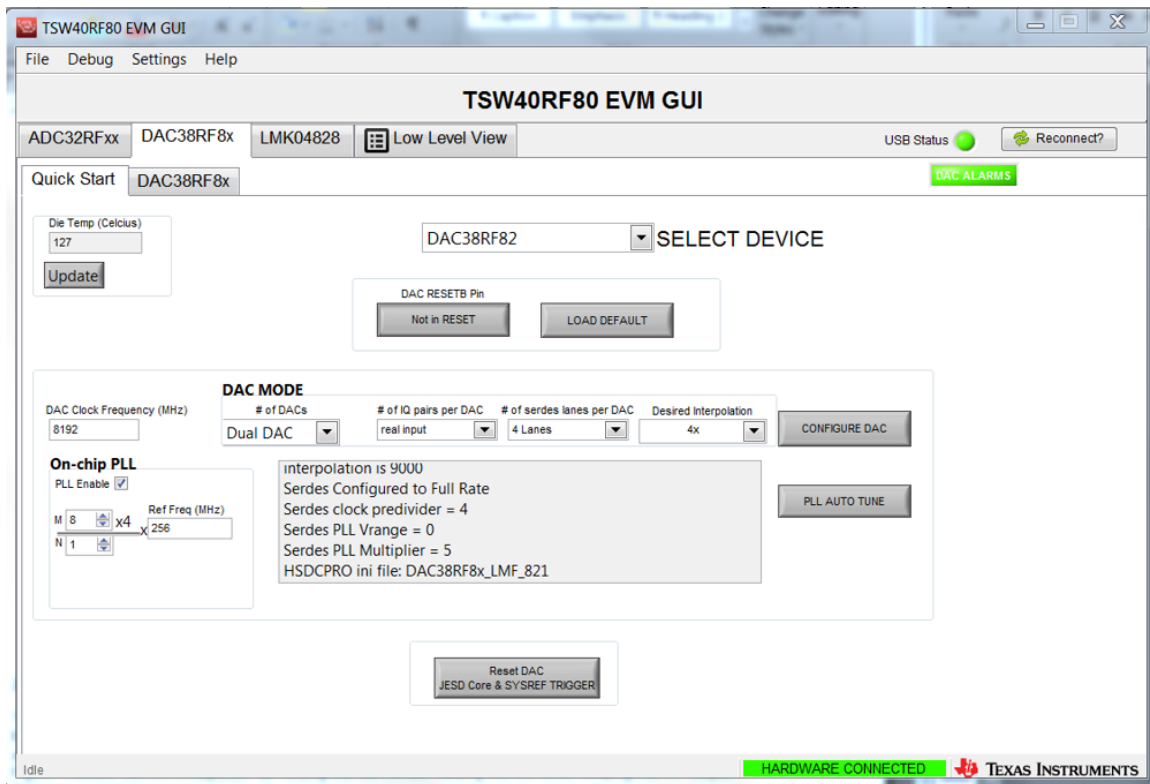


图 3. TSW40RF82EVM GUI DAC Configuration—Front Panel

5 Testing and Results

5.1 Measured Performance

The DAC38RF82 is a dual DAC that can sample at a rate of up to 9 GSPS. This DAC supports a maximum complex data rate of 3.33 GSPS. The device is also capable of synthesizing wideband signals up to 2.66-GHz bandwidth. The device is well suited for generating complex wide-bandwidth signals used in QAM schemes, such as the wideband signal shown in [图 4](#). The optional PLL/VCO simplifies the DAC clock generation by allowing use of a lower frequency to synthesize the high-frequency sampling clock.

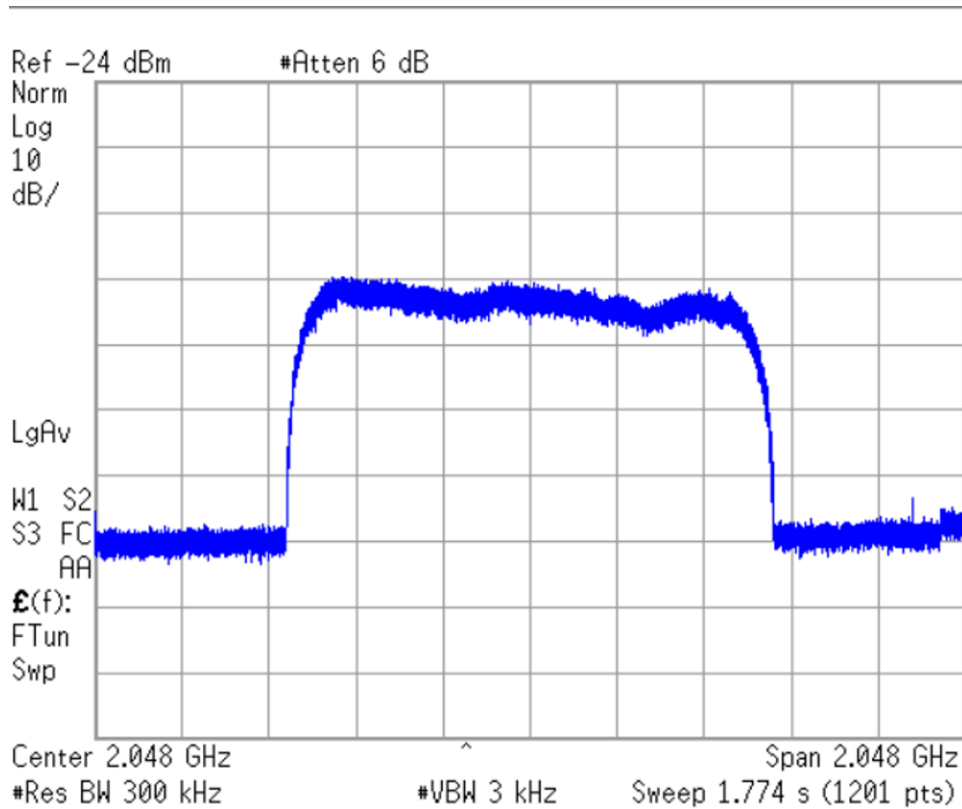


图 4. 1024-MHz Wide Signal Generated by RF DAC

5.1.1 OIP3 Response Over BB Frequency

The OIP3 performance over the BB frequency offset is measured with two tones separated by 10 MHz. The OIP3 over frequency is measured in two ways. The first measurement varies the LO across the frequency band while keeping the BB at a fixed 50-MHz offset. The second measurement keeps the LO constant at 5 GHz and varies the BB offset. 图 5 shows the OIP3 response.

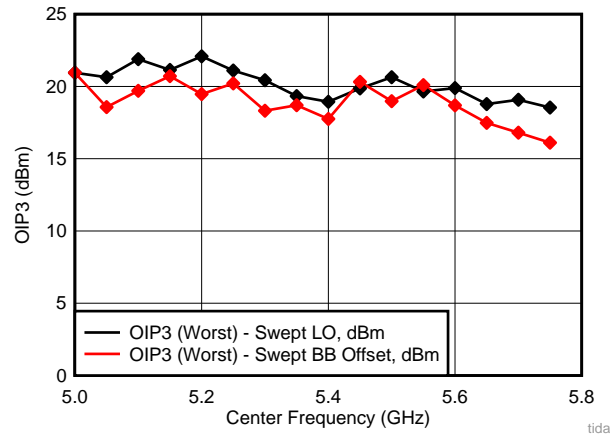


图 5. OIP3 Performance With Varying BB Frequency Offset and Varying LO

5.1.2 MER Response Over LO Frequency

Another key concern related to high-bandwidth modulated transmissions is modulation error ratio (MER). This metric indicates the quality of the received signal and is described in the following 公式 5:

$$\text{MER (dB)} = 10 \times \log_{10} \left[\frac{\text{Average Symbol Power}}{\text{Average Error Power}} \right] \quad (5)$$

For QAM transmissions, the higher the MER (dB), the closer the data points align to their ideal locations on the constellation diagram.

This test uses a 64-QAM signal with a bandwidth of 81.92 MHz generated by the DAC and then modulated by the TRF370417EVM. The product of the signal chip rate and interpolation must equal the DAC data rate. As the signal interpolation value must be an integer, and the data rate is already determined, the chip rate must be carefully selected such that it is a rational number. This careful selection reduces the demodulation error because the target demodulation chip rate matches the exact target demodulation chip rate on the receiver end. The signal bandwidth also represents the maximum allowed by the available demodulation equipment.

The first test is performed by offsetting the signal by 100 MHz from DC and sweeping it over the frequency. This test allows the examination of the MER without the sideband suppression limitation imposed by the modulator. The second test sweeps the signal with no offset from DC (Zero-IF). In this case, a number of things affect the MER, including the sideband suppression performance of the modulator, harmonics, and intermodulation products (especially second-order intermodulation products) of the signal itself. The third test is performed at Zero-IF as well; however, the VCM, LO power, and DAC gain are optimized at each data point to produce a more favorable MER. 图 6 shows how the equalization was applied.

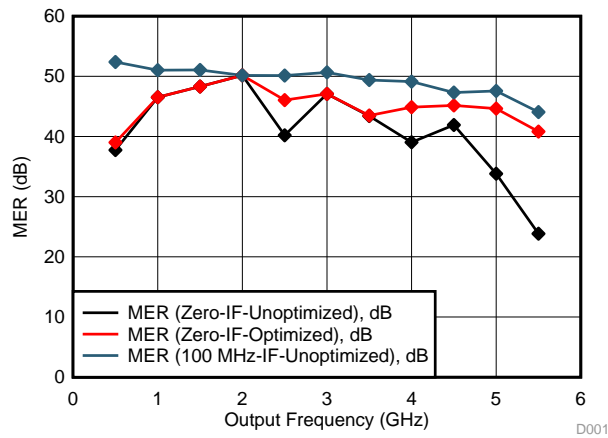


图 6. Equalized MER of 64-QAM Signal Over Output Frequency

5.2 Conclusion

The TSW40RF82EVM in conjunction with the TRF370417 device is a suitable platform to operate at output frequencies up to 6 GHz with BB signal bandwidths up to around 2 GHz. A simple network is required to interface the two devices because the DAC common-mode voltage is compatible with the TRF370417EVM common-mode voltage. The demand to increase capacity and improve performance in microwave backhaul applications is rising. Increasing the QAM level to satisfy this demand is neither a viable nor sustainable solution, however, increasing the BB signal bandwidth is a feasible solution.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at [TIDA-01435](#).

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01435](#).

7 Related Documentation

1. Ho, Quang-Dung; Tweed, Daneil; Le-Ngoc, Tho; *Long Term Evolution In Unlicensed Bands*, 1st Ed. Cham, Switzerland: Springer International Publishing, 2017.
2. Texas Instruments, [High Bandwidth, High Frequency Transmitter Solution](#), TSW38J84EVM Reference Design (TIDU579)

7.1 商标

All trademarks are the property of their respective owners.

8 Terminology

BB— Baseband

DAC— Digital-to-analog converter

FPGA— Field-programmable gate array

GUI— Graphical user interface

LMF— Limited mitigation factor

MER— Modulation error ratio

PLL— Phase-locked loop

QAM— Quadrature amplitude modulation

VCO— Voltage-controlled oscillator

VCXO— Voltage-controlled crystal oscillator

Zero-IF— Zero-intermediate frequency

9 About the Author

ABDALLAH OBIDAT is an Applications Engineer at Texas Instruments. He supports high-speed data converters, discrete RF devices, and integrated transceivers. Abdallah earned his bachelor of science in electrical engineering (BSEE) from the Georgia Institute of Technology.

修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (August 2017) to A Revision	Page
• Updated 图 5 : Y-axis changed from "MER (dB)" to "OIP3 (dBm)".....	8

有关 TI 设计信息和资源的重要通知

德州仪器 (TI) 公司提供的技术、应用或其他设计建议、服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用；如果您（个人，或如果是代表贵公司，则为贵公司）以任何方式下载、访问或使用了任何特定的 TI 资源，即表示贵方同意仅为该等目标，按照本通知的条款进行使用。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。

您理解并同意，在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，以及您的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。就您的应用声明，您具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。您同意，在使用或分发包含 TI 产品的任何应用前，您将彻底测试该等应用和该等应用所用 TI 产品的功能而设计。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

您只有在为开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与使用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对 TI 资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。

TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为您辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

您同意向 TI 及其代表全额赔偿因您不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

本通知适用于 TI 资源。另有其他条款适用于某些类型的材料、TI 产品和服务的使用和采购。这些条款包括但不限于适用于 TI 的半导体产品 (<http://www.ti.com/sc/docs/stdterms.htm>)、[评估模块](http://www.ti.com/sc/docs/sampterm.htm)和样品 (<http://www.ti.com/sc/docs/sampterm.htm>) 的标准条款。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2018 德州仪器半导体技术（上海）有限公司