TI Designs

Backup Power Reference Design for Smart Meters and Data Concentrators With GPRS

Description

The reference design describes a power management solution for data concentrators and smart meters that require both super capacitor and battery as backup power. The designed circuit implements uninterrupted power supply to drive GPRS module and other system loads by switching among the power grid, the super capacitor and the battery in setting sequence. The reference design also includes a simple, cost-effective linear charger circuit for the super capacitor and the battery.

Resources

PMP9802	Design Folder
TLV62130	Product Folder
TPS61089	Product Folder
TLV62084	Product Folder
ATL431	Product Folder

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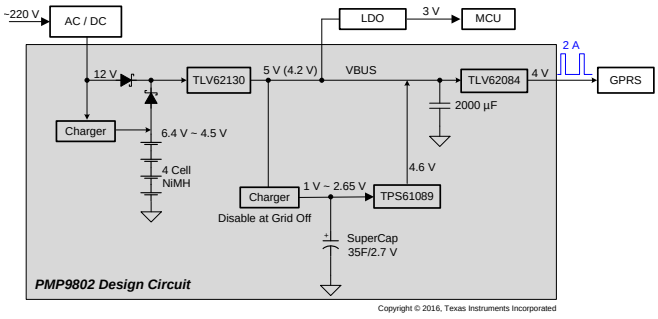
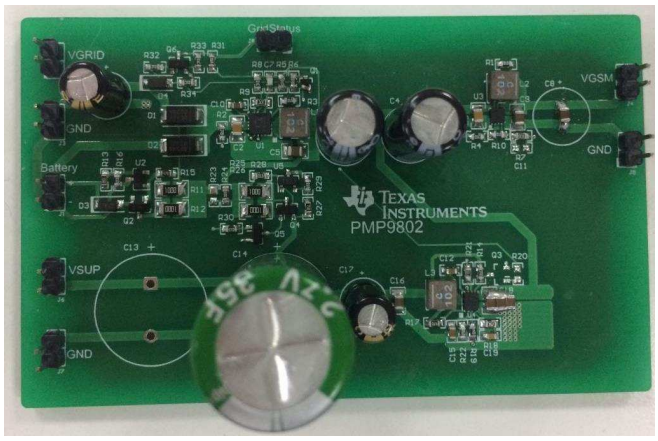
Features

- Capability to Drive the GPRS Module
- Super Capacitor and Battery for Backup Power
- Power Sequence Implementation for Power Grid and Backup Power
- Linear Charger Circuit for Super Capacitor and Battery
- 1-V to 2.65-V Operation Voltage of Super Capacitor

Applications

- Data Concentrator
- Smart Meter
- Super Capacitor Backup System





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1 System Overview

1.1 System Description

The data concentrator aggregates data from a number of meters and sends the data to the centralized utility servers through the GPRS or other telecom networks. Based on the requirement of the State Power Grid Corporation of China, the data concentrator must operate for a period of time using the internal backup energy of the super capacitor and battery after the power grid failure.

The reference design PMP9802 is a backup power-management solution for a GPRS module in the data concentrator. Figure 1 shows the block diagram. The design circuit has three operation modes which follow:

- When the 12-V input voltage from the power grid is normal, the 5-V VBUS voltage is supplied by the TLV62130. The battery and super capacitor are charged by the power grid through a linear charger circuit. The TPS61089 stops switching. The TLV62084 operates to support the GPRS.
- The power grid fails and the 12 V decreases below 5 V. The TPS61089 starts to switch and outputs 4.6 V using the energy from the super capacitor. The charger for the super capacitor turns off. The TLV62130 stops switching, so no current flows out of the battery. The TLV62084 keeps operating.
- The super capacitor is out of charge and its voltage drops below 1 V. The TPS61089 shuts down, so the VBUS voltage decreases. The TLV61230 operates again and maintains the VBUS at 4.2 V with the energy from the battery. The TLV62084 keeps operating.

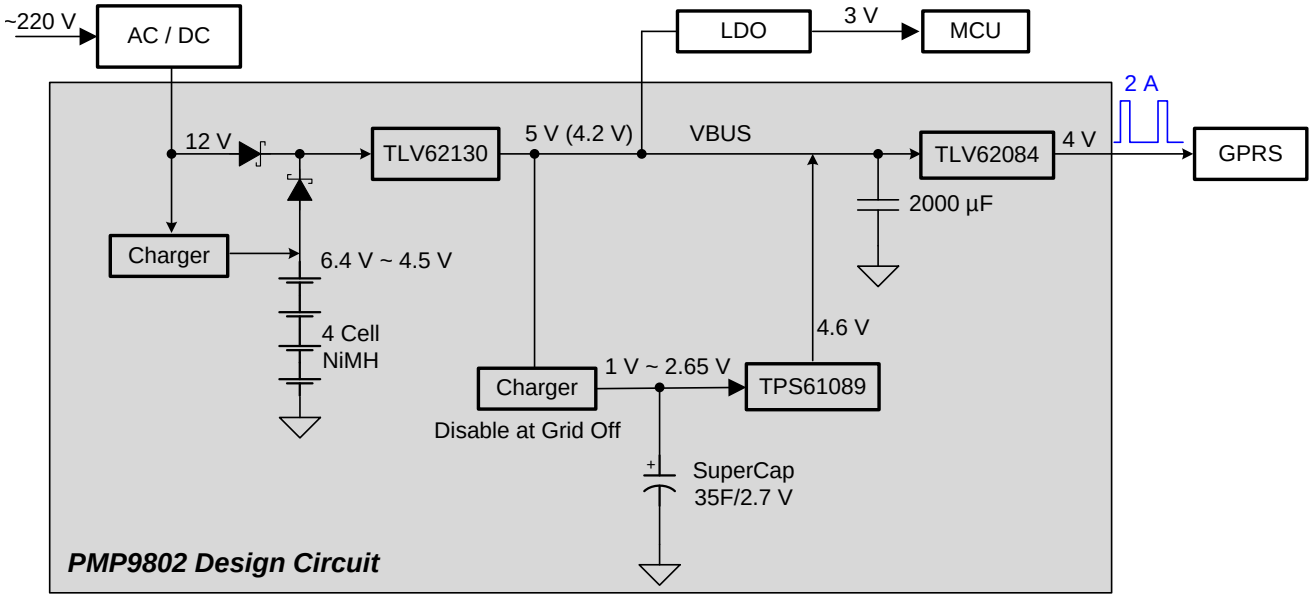

Figure 1. Block Diagram of Reference Design

The previous three operation modes transit smoothly to provide uninterrupted VBUS voltage for the GPRS module and the control circuit in the data concentrator.

1.2 Highlighted Products

1.2.1 TLV62130

The TLV62130 is a 3-V to 17-V input, 0.9-V to 5-V output, synchronous step-down DC-DC converter optimized for applications with high-power density. A high-switching frequency of typically 2.5 MHz allows the use of small inductors and provides a fast transient response as well as high-output voltage accuracy by use of DCS-Control™ topology. Other features of this device include the following:

- Up to 3-A output current
- Programmable soft start and tracking
- Seamless power-save mode transition
- 100% duty cycle mode
- Short-circuit protection

1.2.2 TPS61089

The TPS61089 is a 4.5-V to 12.6-V, fully integrated synchronous boost converter with a 19-mΩ main power switch and a 27-mΩ rectifier switch. The TPS61089 supports wide input voltage ranges from 2.7 V to 12 V. Furthermore, the power supply voltage can be down to zero if the VIN pin of the TPS61089 is powered by an external voltage higher than 2.7 V. Other features of this device follow:

- Programmable peak-current limit
- Adjustable switching frequency: 200 kHz to 2.2 MHz
- 4-ms built-in soft start time
- Cycle-by-cycle overcurrent protection

1.2.3 TLV62084

The TLV62084 is a small, low-cost synchronous buck converter with an input voltage range of 2.7 V to 5.5 V. The features of TLV62084 include the following:

- DCS-Control architecture for fast transient regulation
- 100% duty cycle for lowest dropout
- Power-save mode for light load efficiency
- Power good output

2 Operating Principle

The following content describes the operating principles of the key circuits in the schematic. The whole schematic of the reference design can be downloaded from the PMP9802 design folder.

2.1 Power Sequence Implementation

The VBUS is supported by the TLV62130 and TPS61089. The output of the two devices is directly connected to the VBUS. Both devices are synchronous DC-DC converters and support power-save mode (PSM) operation. When the voltage in their VOUT pin is higher than the setting voltage, the TLV62130 and TPS61089 stop switching. No reverse current is flowing into the converters. Using the principle of PSM, the operation sequence of the TLV62130 and TPS61089 can be implemented by setting a different target output voltage.

- When the power grid is on, the output voltage of the TLV62130 is set to 5 V. The target voltage of the TPS61089 is 4.6 V, so the TPS61089 powered by the super capacitor stops operating.
- When the power grid is off, the target output voltage of the TLV62130 is changed to 4.2 V by changing the feedback resistor divider. Because the setting output voltage of the TPS61089 is 4.6 V, the TPS61089 starts to operate and TLV62130 stops operating.
- When the super capacitor is out of charge and the grid is still off, the TLV62130 restarts and maintains the VBUS at 4.2 V.

2.2 Charger for Super Capacitor

Figure 2 shows the charger for the super capacitor. The maximum voltage of the super capacitor is limited to 2.65 V, because the voltage rating of the super capacitor is 2.7 V. The charge current is limited by resistors R25 and R26. The maximum power consumption of the two 100-Ω resistors is 0.25 W when VSUP is zero. Smaller resistance helps to reduce the super capacitor charging time, but results in larger power consumption. The charger circuit for the battery is almost the same.

Grid_ST in Figure 2 shows the status of the power grid. At the power grid off condition, Grid_ST is high logic and turns off the charger.

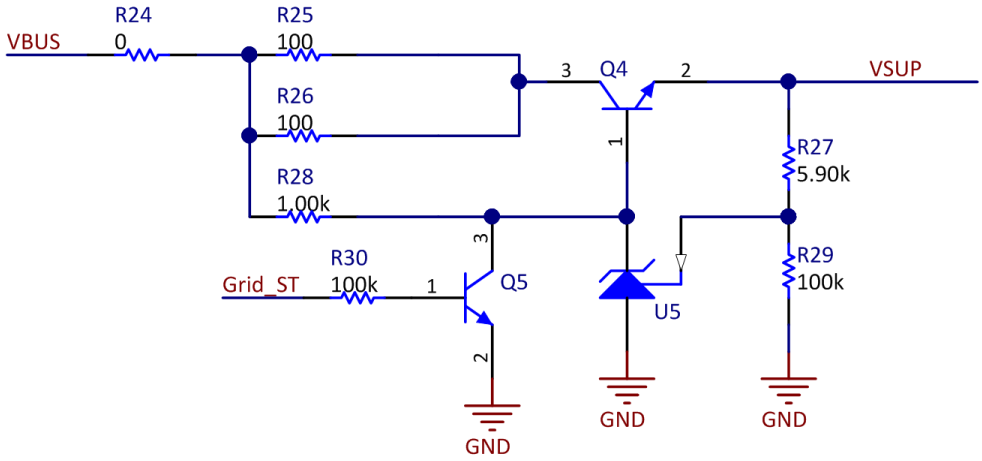

Figure 2. Charger for Super Capacitor

2.3 Boost Converter Solution

Figure 3 shows the schematic of the boost converter. The VIN pin of the TPS61089 is connected to VBUS, so the TPS61089 can operate with one cell super capacitor. The VBUS must be higher than 4.5 V when the TPS61089 is operating. The EN pin is connected to VSUP, so the boost converter shuts down when the voltage of the super capacitor is lower than the logic low voltage of the TPS61089.

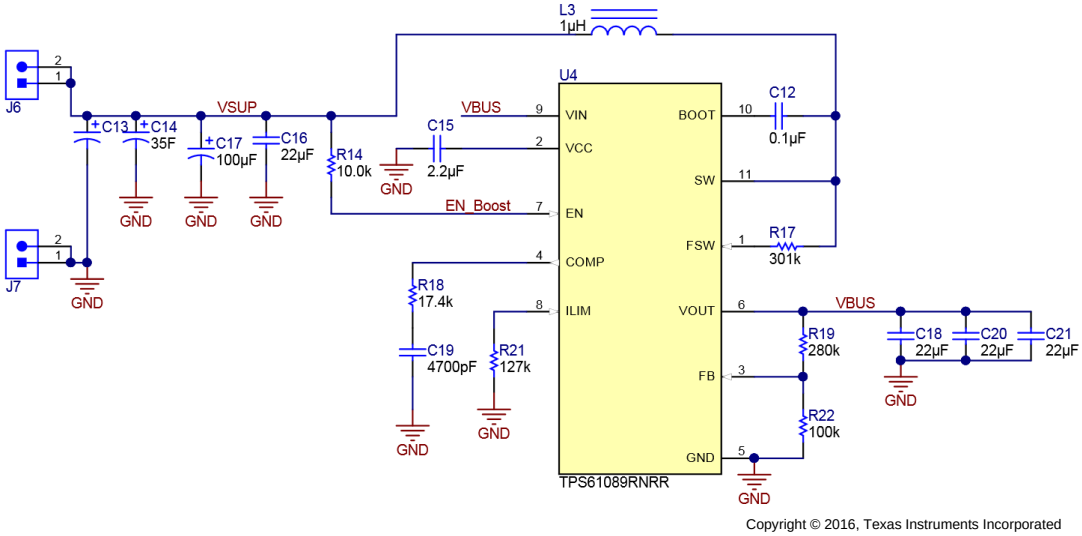

Figure 3. Schematic of Boost Converter Solution

2.4 Power Grid Status Indicator

Figure 4 shows the circuit of the power grid status indicator. When the power grid is on, VGRID is 12 V, so Grid_On is high logic and Grid_ST is low logic. When the power grid is off and VGRID voltage drops below 5.1 V, Grid_On is low logic and Grid_ST is high logic. Grid_On and Grid_ST can be used to control other circuits.

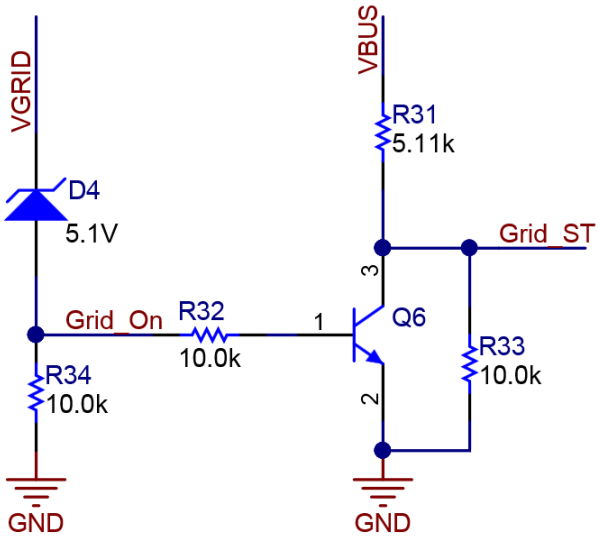

Figure 4. Power Grid Status Indicator

3 Test Results

Figure 5 shows the operating waveform when the grid voltage is normal. In the waveform, CH1 (V_{GPRS}) is the output voltage of the TLV62084 for the GPRS module; CH2 (V_{BUS}) is the BUS voltage; CH3 (V_{SUP}) is the super capacitor voltage; and CH4 (I_{OUT}) is the output current of the TLV62084, which is 2 A, 1/8 duty cycle, and 4.62-ms period current to simulate GPRS loading. Under the pulsed load condition, the V_{GRPS} and V_{BUS} keep stable.

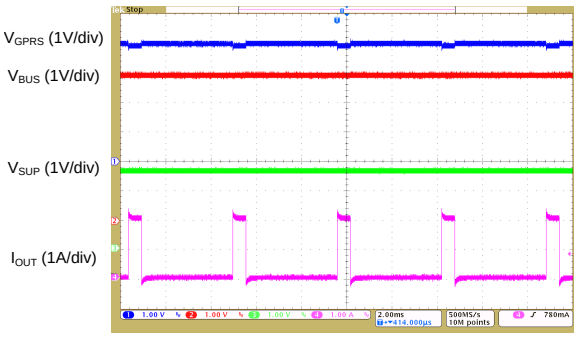

Figure 5. Operating Waveform When Grid is On

Figure 6 shows the transition waveform from the grid to the super capacitor. The V_{BUS} voltage maintains at 4.6 V by TPS61089 using the energy from the super capacitor when the V_{GRID} supplied by the power grid is off. The ripple at V_{BUS} is caused by the changing of the load current. The output voltage of the TLV62084 keeps stable at 4 V.

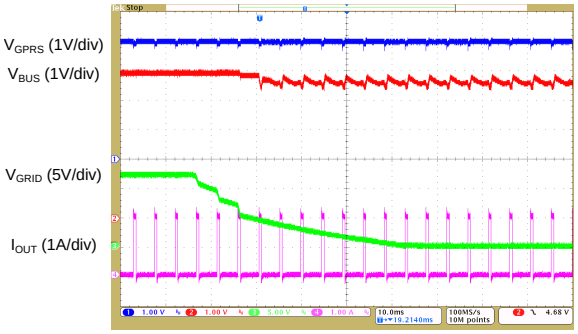

Figure 6. Transition Waveform When Grid Power is Off

When V_{GRID} resumes, the V_{BUS} is back to 5 V and the system load is powered by the V_{GRID}, as shown in Figure 7.

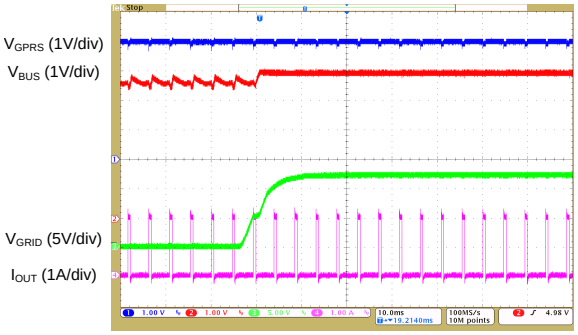

Figure 7. Transition Waveform When Grid Power is On

Figure 8 shows the transition waveform from the super capacitor to the battery. When the super capacitor is out of charge and its voltage drops below 1 V, the TPS61089 stops switching and the TLV62130 resumes operation, which maintains the V_{BUS} at approximately 4.2 V. The output voltage of the TLV62084 remains at 4 V for the GPRS module.

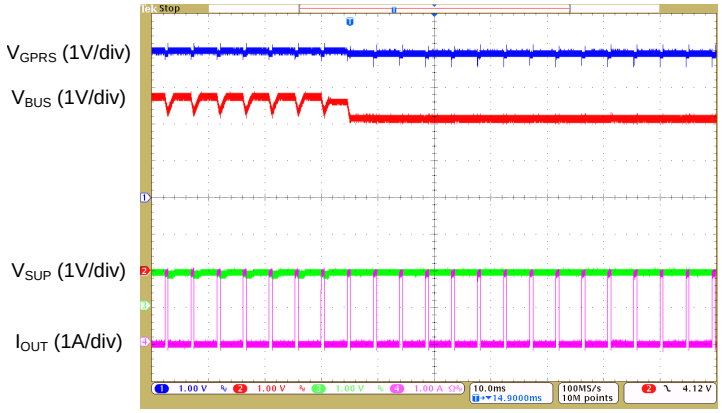

Figure 8. Transition Waveform from Super Capacitor to Battery

Without connecting the battery, the operating time of a 35F super capacitor is approximately 75 s at full load condition (2-A peak, 1/8th duty cycle, and 4.62-ms period), as shown Figure 9.

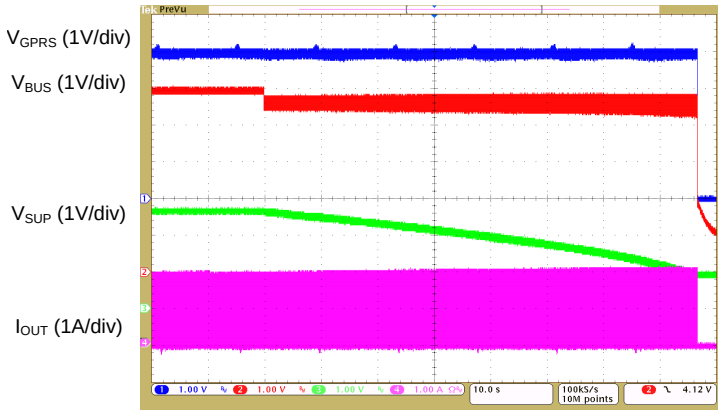

Figure 9. Operating Period of 35F Super Capacitor

4 Design Files

4.1 Schematics

To download the schematics, see the design files at PMP9802.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP9802.

4.3 Layout Prints

To download the layer plots, see the design files at PMP9802.

4.4 Altium Project

To download the Altium project files, see the design files at PMP9802.

4.5 Gerber Files

To download the Gerber files, see the design files at PMP9802.

5 Trademarks

DCS-Control is a trademark of Texas Instruments.

6 About the Author

JASPER LI is a Power Applications Engineer for the Texas Instruments Boost Converter Solution Group. In this role, he supports worldwide customers, writes application notes, and develops reference designs. Since 2013 his focus has been on ultra-low-power applications. Jasper received his master's degree in Power Electronics in 2013 at Zhejiang University in China.

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