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History:

The HPA470 / HPA602 EVMs were developed before we had a full understanding of the CPU / GPU Core current requirements and before the high speed NextFet switches were available. Based upon earlier available FETs and our understanding of the Core current requirements provisions for 2 hi side and 2 low side FETs per phase were made and the larger IHLP5050FD chokes were designed in.

Based upon the latest requirements of 48A peak electrical and 32A for thermal purposes and the availability of these new higher speed NextFets:

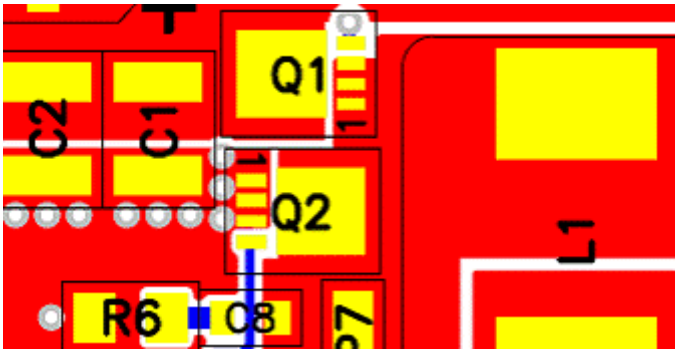
a) Only one hi side and low side MOSFET per phase is needed.
b) Smaller IHLP4040DZ chokes can be used.
c) The layout needs to be updated to accommodate the higher speed MOSFETs by having the input caps extremely closely coupled to the MOSFETs to reduce voltage overshoot and ringing noise. Also, a snubber needs to be added to reduce ~100Mhz ringing in noise sensitive applications.

A new layout PMP5783 is in the works to accommodate all the concerns listed in c) above. For now testing on the existing HPA-470 was done to demonstrate that the single set of FETs (per phase) and smaller chokes can meet the thermal requirements and all the electrical requirements. On the existing EVM I was able to demonstrate the elimination of ringing with the snubbers and the reduction of the peak Vds on the low side FETs by increasing R17 & R19 from zero to 5.6 ohms to slow turn on of high side MOSFETs. This came at a cost of increased losses as will be shown on Page 3. With the improved layout less snubbering and less slowing of gate drive will be needed allowing a higher efficiency.

See next page for best approach for layout which will be done in PMP5783.

For the choke the best part to use per the Vishay loss simulator is the IHLP4040DZ-01 0.56uHy choke. However, the closest part we had in our lab was IHLP4040DZ-11 0.47uHy choke. Based upon my simulations on Vishay's loss calculator the preferred part will save at 32A output an additional 350mW per phase or 700mW in all compared with the part I tested with. This will correspond to about a 2% increase in efficiency at the 32A load.

Proposed improved layout approach:



Q1 is the high side FET; Q2 is the low side FET; C1 and C2 are the input caps (ceramic size 1210); C8 and R6 is the snubber. Key is rotating Q1 and Q2 such that drain of high side FET and source of low side FET face same side where the input caps are to be placed. Snubber then should be placed as close to drain source of low side FET as feasible. Traces to gates are much less critical and can be on other layers and be signal trace (10 to 25 mils) width.

Output load line and conversion efficiency from the 12V input. Bias was always 5.00V and bias input power for gate drive is not included in calculations below. Based upon FETs used and 300kHz operation, 14mA will be needed off the 5V Bias for gate drive when switching at 300kHz.
Note: operation above 32A load (max thermal requirement) is with about 200 LFM airflow

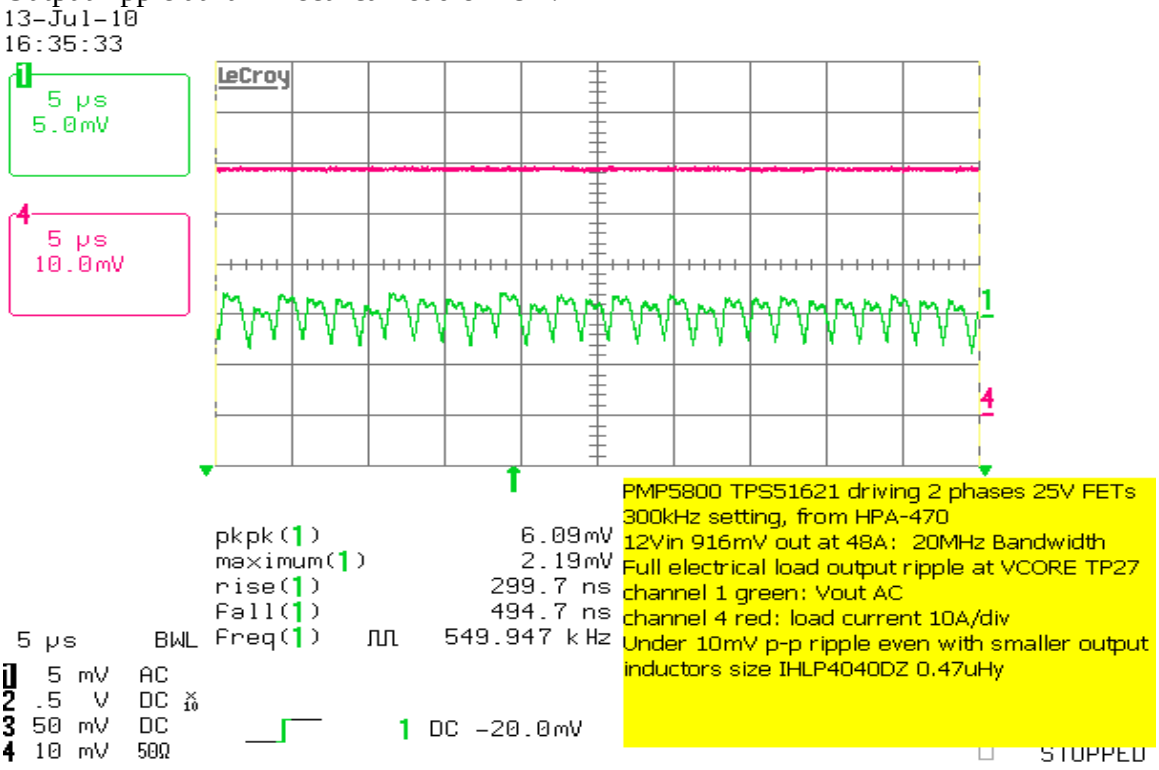
Regulation, losses and efficiency (from 12V excluding bias power):

Vin Volts	**Iin mA**	**Vout1 mVolts**	**Iout1 A**	**Efficiency %**	**Losses in mW**
Before	Snubber	Added	And	Gate	slowed
12.11	1	997	0	N/A	12
12.11	99	995	1.01	83.8	194
12.08	489	987	5.01	83.7	962
12.06	920	978	10.00	88.1	1315
12.03	1359	970	15.00	89.0	1799
12.10	1793	962	20.00	88.7	2455
12.07	2338	952	26.00	87.7	3468
12.03	2908	943	32.01	86.3	4798
12.04	4438	916	48.01	82.3	9456
After	Snubber	Added	And	Gate	slowed
12.12	1	997	0	N/A	12
12.11	100.5	995	1.01	82.6	212
12.08	482	988	5.01	85.0	873
12.06	927	978	10.00	87.5	1400
12.03	1367	970	15.00	88.5	1895
12.10	1804	962	20.00	88.1	2588
12.06	2356	953	26.00	87.2	3635
12.03	2931	944	32.01	85.7	5042
12.07	3671	929.5	40.01	83.9	7120
12.04	4470	916	48.01	81.7	9842

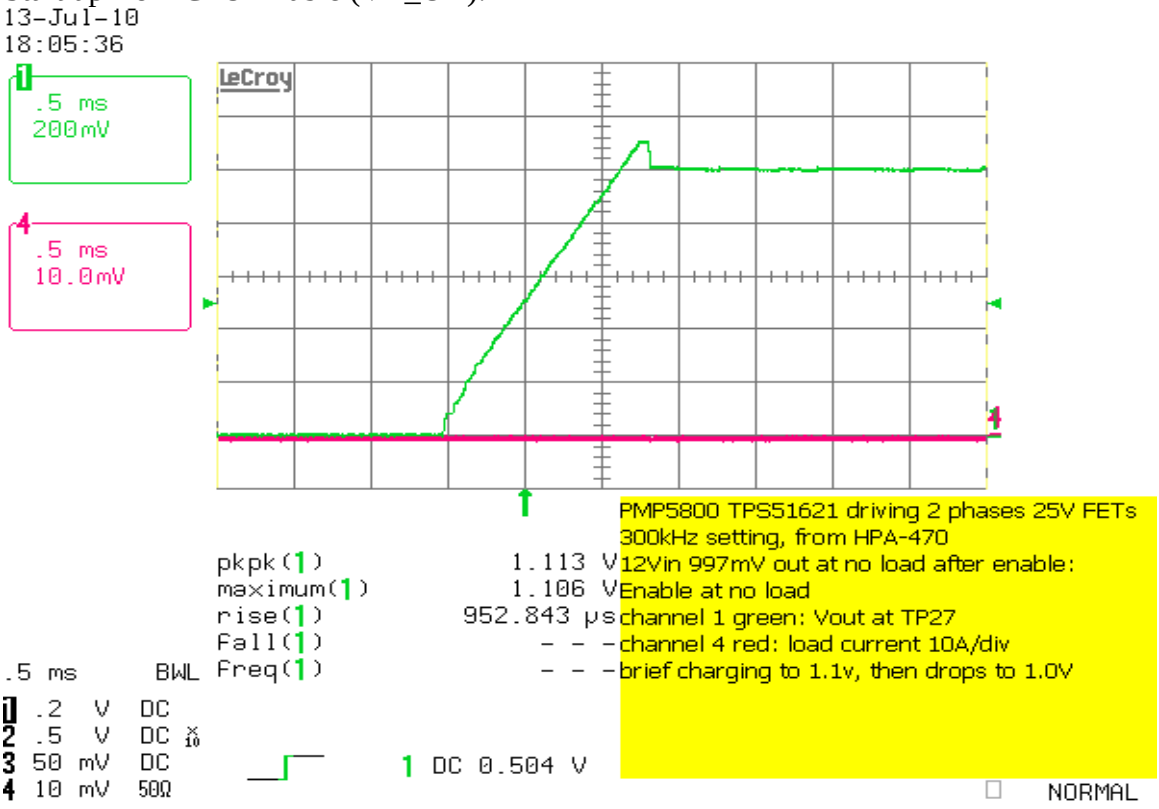
At Thermal max of 32A the added losses due to snubbers and gate slowing are 244mW.
At the 48A peak load the added losses due to snubbers and gate slowing are 386mW.

Load line is -1.7mV per A instead of target -1.9mV per A. This is probably due to actual resistance of choke being 11% less than value that was used to calculate load line.

Output ripple at full Electrical load of 48A:

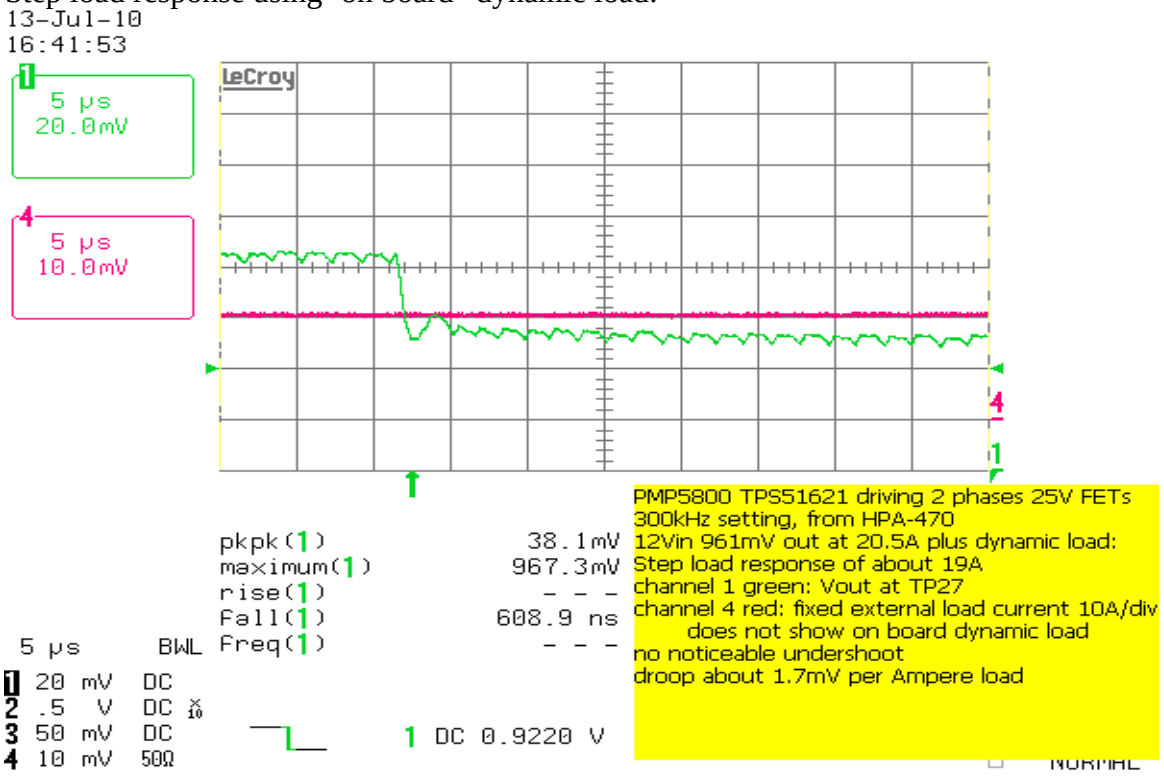


Start up from CPU Enable (VR_ON):

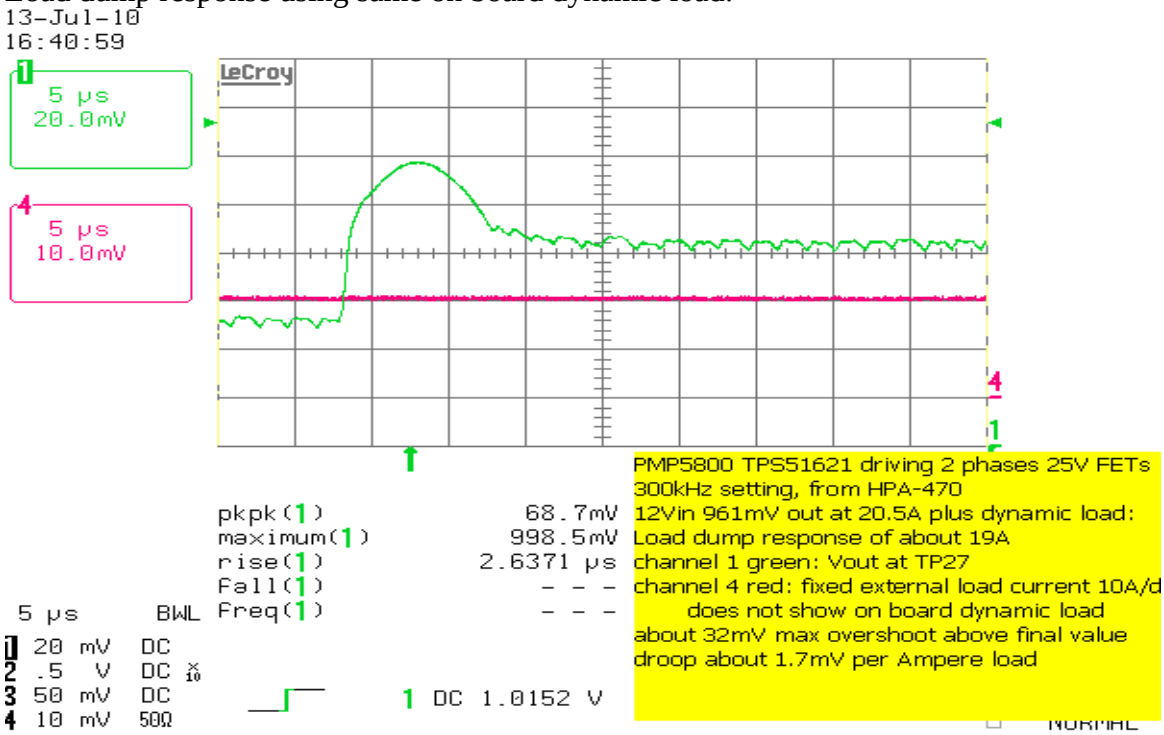


Qq

Step load response using ‘on board” dynamic load:



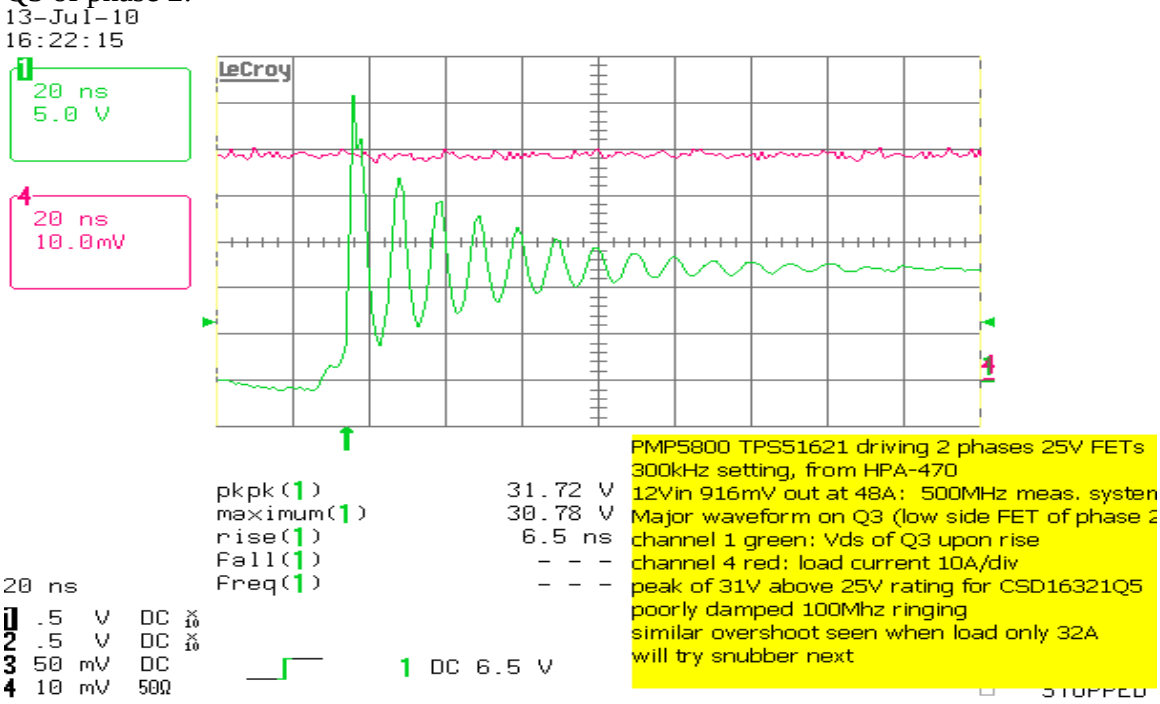
Load dump response using same on board dynamic load:



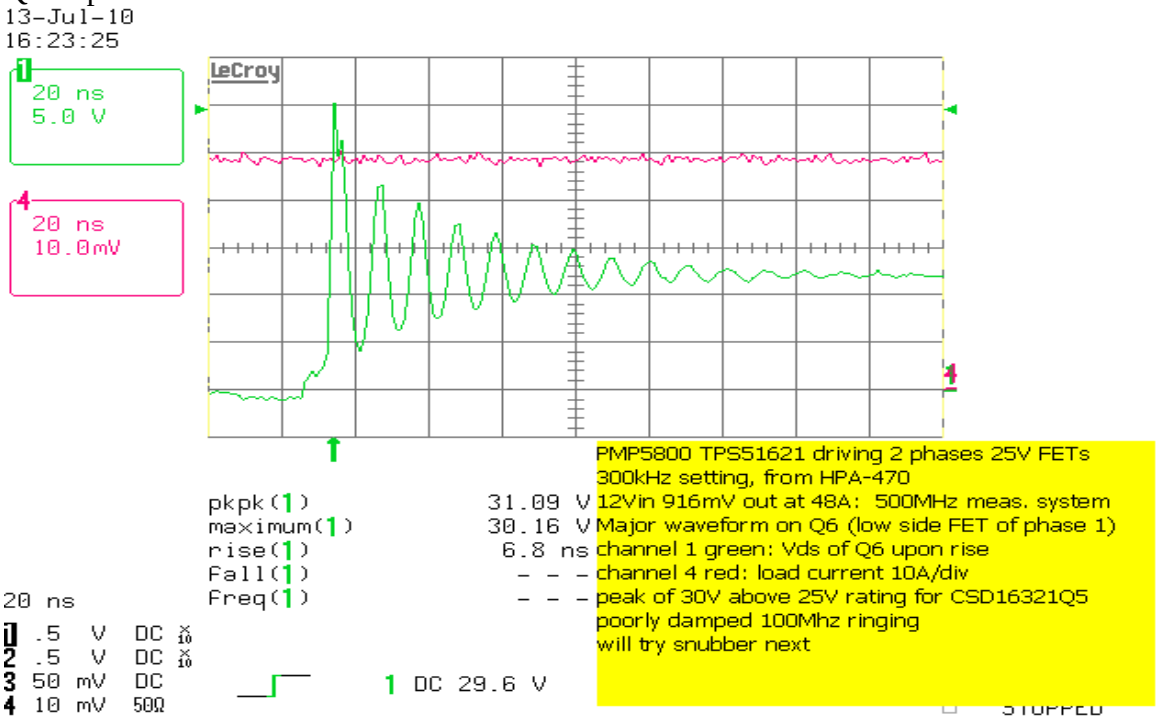
Qq

Major waveforms: Before snubber added or high side gate drive slowed:

Q3 of phase 2:

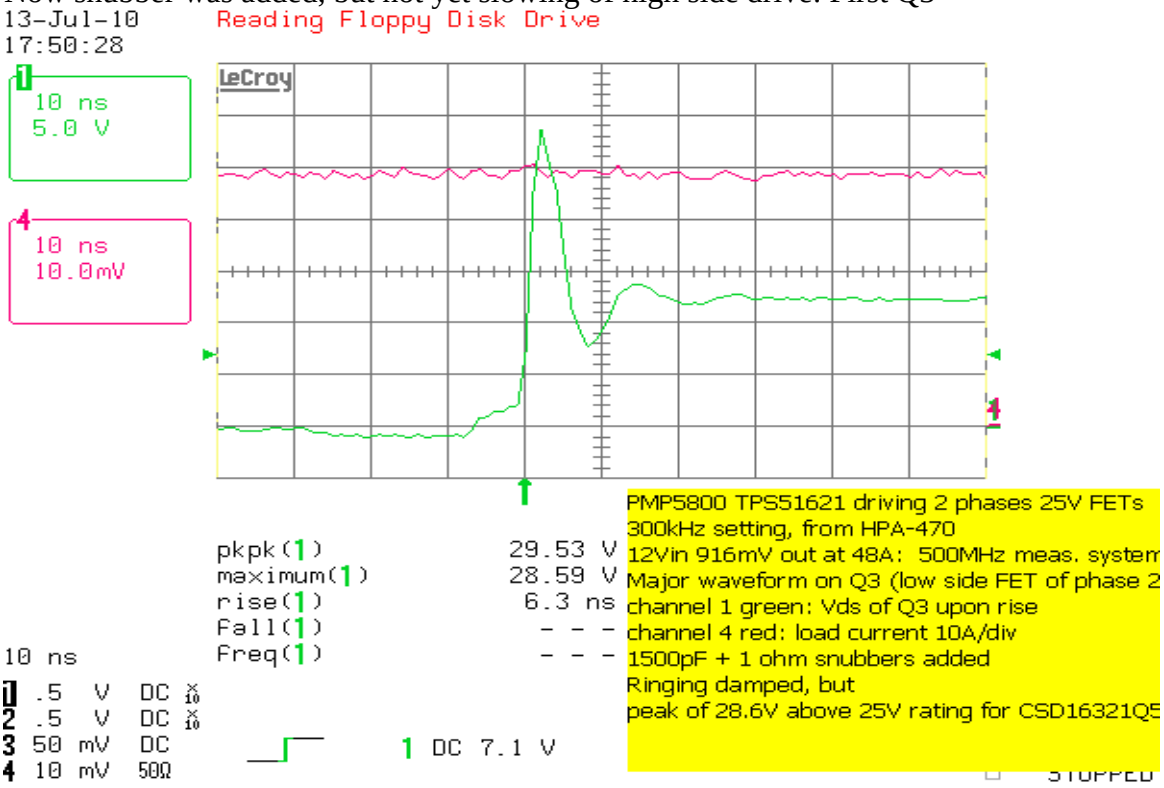


Q6 of phase 1:

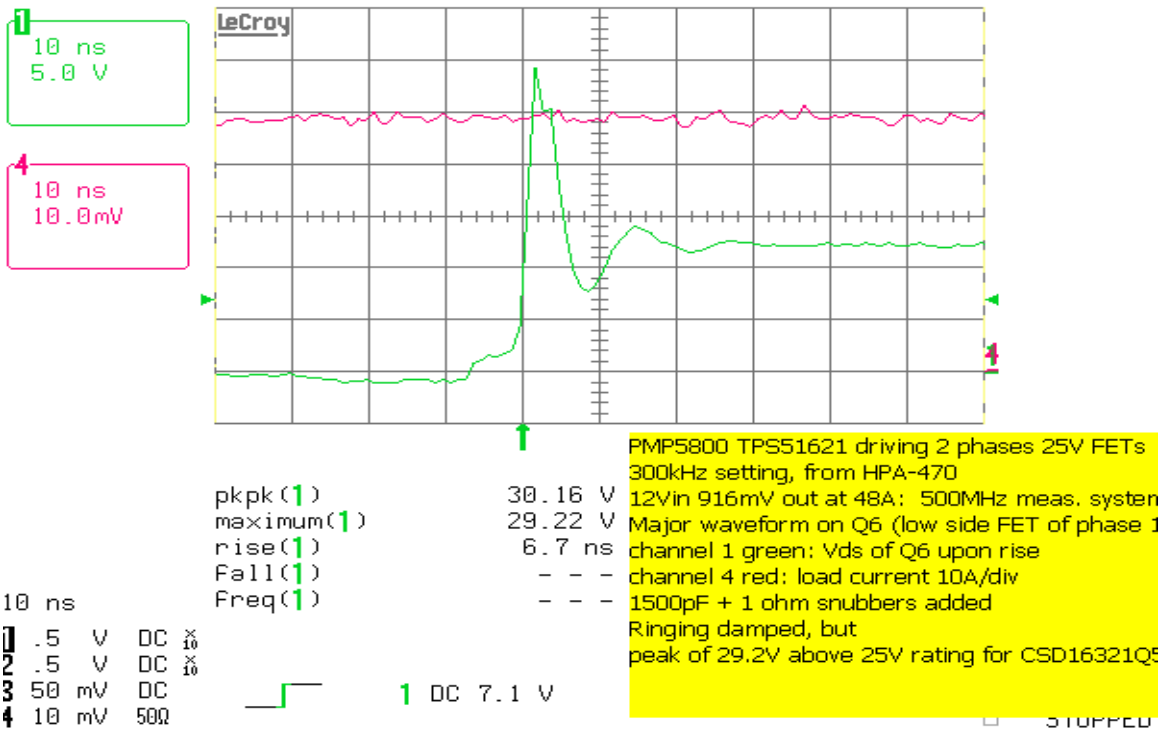


Such waveforms will have both System EMC Engineer and Reliability Engineer screaming !!!

Now snubber was added, but not yet slowing of high side drive: First Q3



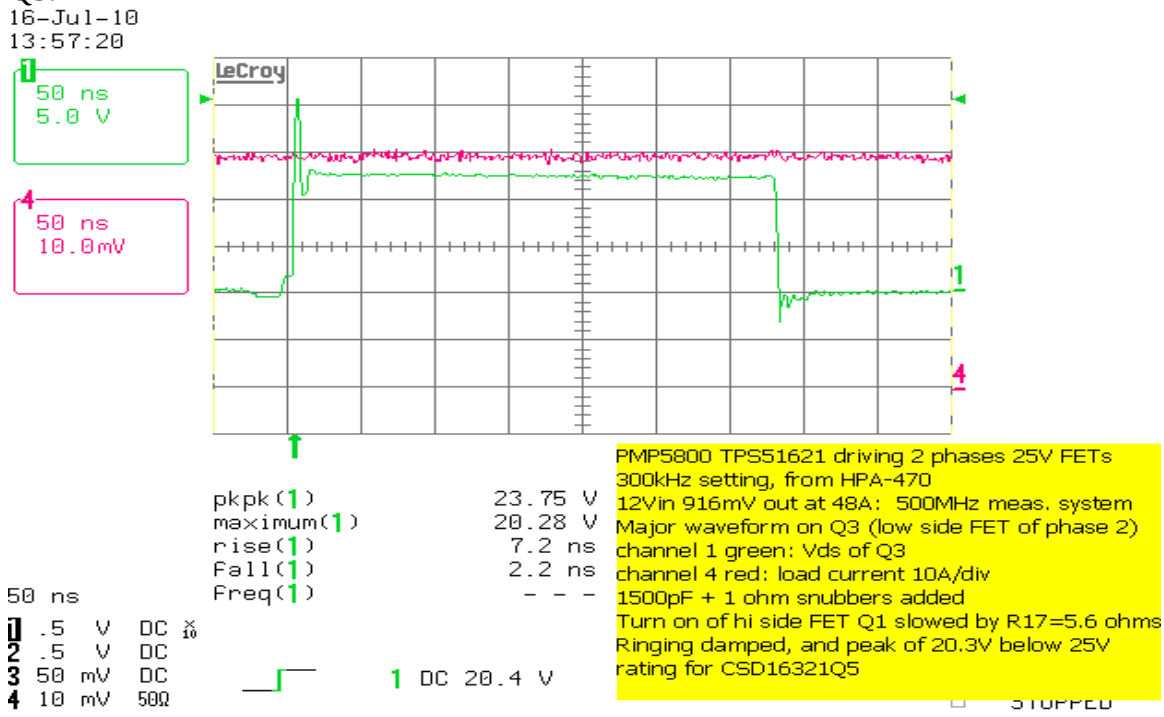
And Q6:



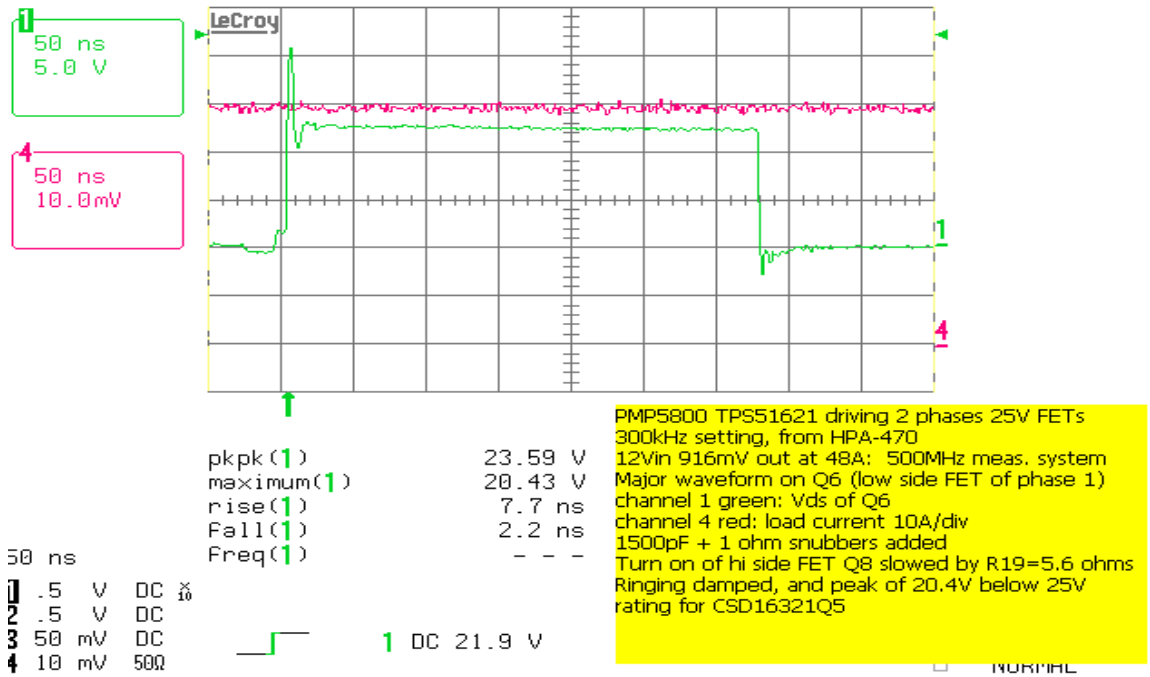
System EMC happy, but not Reliability!!!

Finally, the gate drive to the high side FETs were slowed with R17 and R19 increased to 5.6 ohms from zero. This change only slows turn on, not turn off of hi side FETs.

Q3:



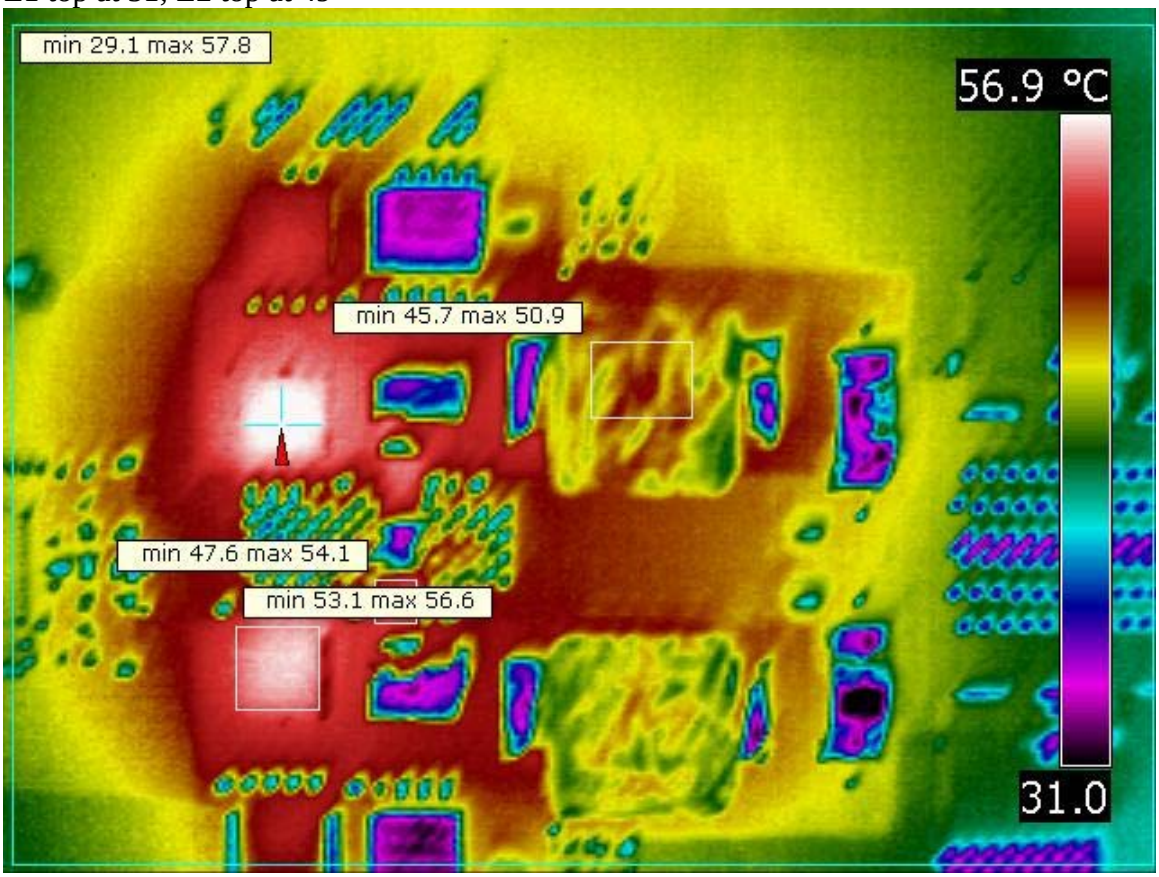
Q6:



Now both System EMC and Reliability happy!!!

Thermal results:
Note; Q3 & Q6 are the low side FETs and Q1 & Q8 are the high side FETs:
All thermal runs / images are after snubbers added and gate drives to high side FETs slowed with R17 & R19 changed from zero to 5.6 ohms:

PMP5800 snu slo gate 12.05Vin 2.936Ain 944mV 32.09A
Full Thermal load, no airflow 23-25 deg. C ambient
Q3 hottest at 58; Q6at57; Q1at54; Q8at52; snubbers at 55&54;
L1 top at 51; L2 top at 49



Thermal summaries for these two runs shown below at full 48A load with and without airflow. See the full Thermal Report in .pdf form for PMP5800 to see the actual images:

PMP5800 snu slo gate 12.03Vin 4.481Ain 916mV 48.09A
Full electrical load, ~200 LFM airflow ave. 23-25 deg. C ambient
Q3 hottest at 63; Q6at61; Q1at54; Q8at54; snubbers at 54&53;
L1 top at 52; L2 top at 49

PMP5800 snu slo gate 12.04Vin 4.545Ain 919mV 48.09A
Full electrical load, no airflow 10 minutes run 23-25 deg. C ambient
Q3 hottest at 88; Q6at86; Q1at78; Q8at76; snubbers at 79&78;
L1 top at 70; L2 top at 67

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