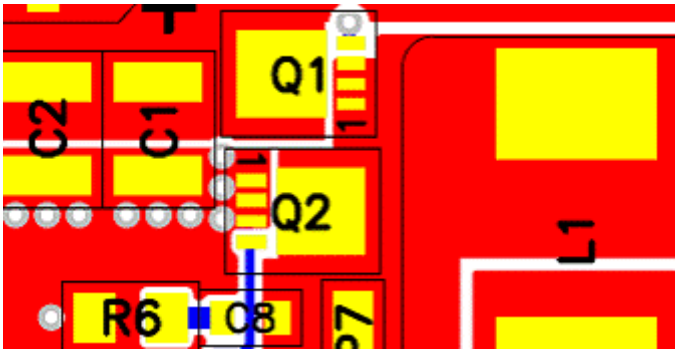
Table of Contents:

Proposed improved layout approach:



Q1 is the high side FET; Q2 is the low side FET; C1 and C2 are the input caps (ceramic size 1210); C8 and R6 is the snubber. Key is rotating Q1 and Q2 such that drain of high side FET and source of low side FET face same side where the input caps are to be placed. Snubber then should be placed as close to drain source of low side FET as feasible. Traces to gates are much less critical and can be on other layers and be signal trace (10 to 25 mils) width.

With improved layout, efficiency can be improved as less snubbering and less slowing of high side gate drive by R10 will be needed.

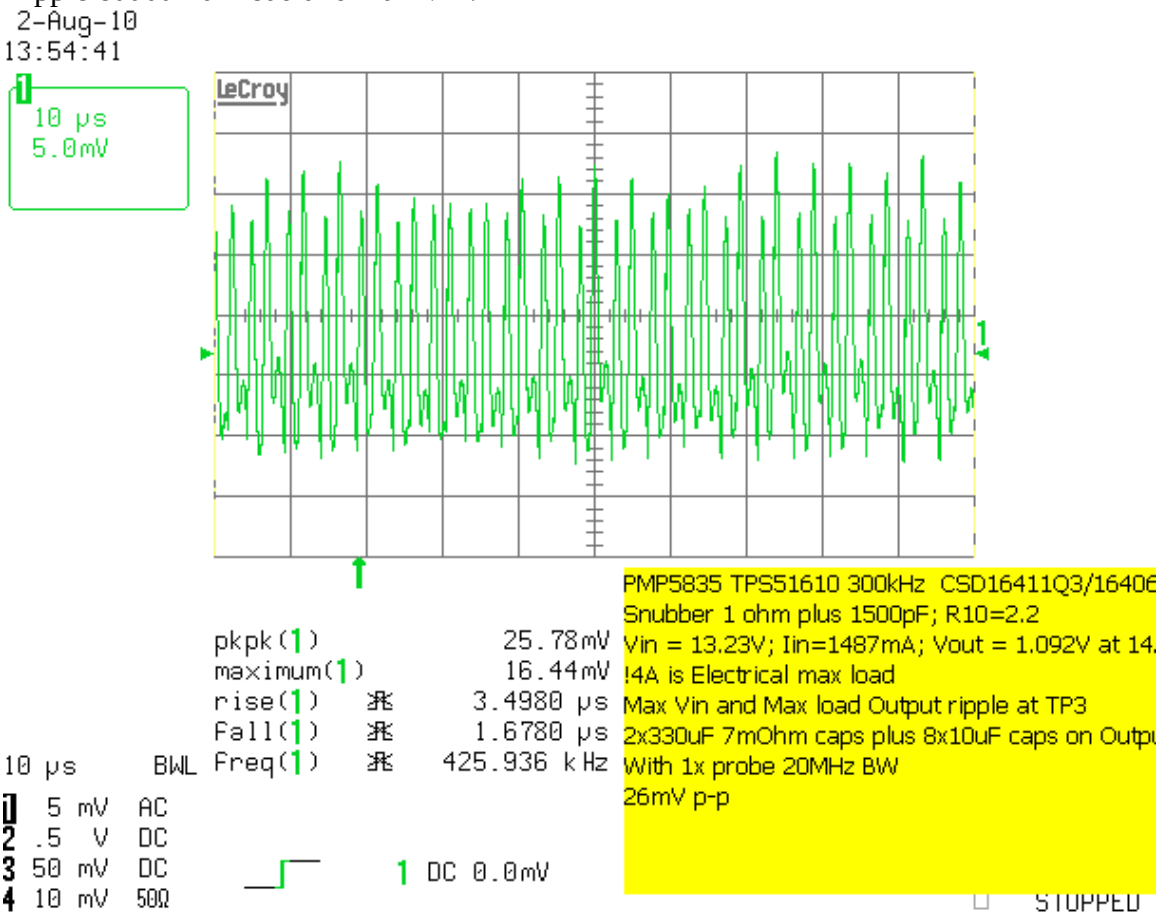
Output load line and conversion efficiency from the 12V input. Bias was always 5.007V and bias input power for gate drive is not included in calculations below. Based upon FETs used and 300kHz operation, 3mA will be needed off the 5V Bias for gate drive when switching at 300kHz.
Note: operation above 10A load (max thermal requirement) is with about 200 LFM airflow

Regulation, losses and efficiency (from 12V excluding bias power):

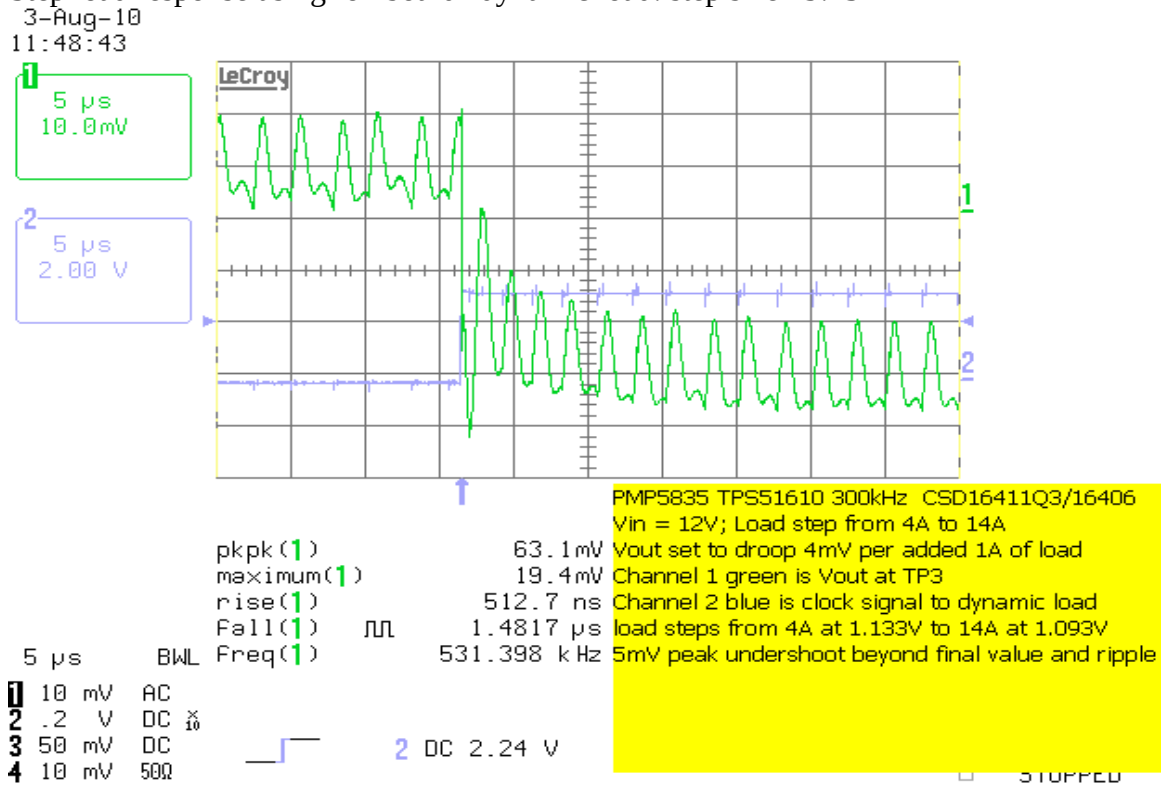
Vin Volts	Iin mA	Vout1 mVolts	Iout1 A	Efficiency %	Losses in mW
13.23	1487	1092	14.01	77.8	4374
13.21	1246	1100	12.01	80.3	3249
13.22	1021	1109	10.01	82.2	2397
13.20	804	1117	8.01	84.3	1666
13.21	595	1125	6.01	86.0	1099
13.20	396.5	1133	4.01	86.8	690
13.21	206.5	1141	2.01	84.1	434
13.20	108	1142	1.01	80.9	272
13.21	5	1141	0	N/A	66
12.02	1630	1092	14.01	78.1	4294
12.02	1364	1100	12.01	80.6	3184
12.03	1117	1108.5	10.01	82.6	2341
12.01	879	1117	8.01	84.8	1610
12.02	650.5	1125	6.01	86.5	1058
12.03	432.5	1132.5	4.01	87.3	662
12.00	225	1141	2.01	84.9	407
12.04	117.5	1142	1.01	81.5	261
12.00	6	1141	0	N/A	72
10.80	1806.5	1092	14.01	78.4	4211
10.80	1513	1100	12.01	80.8	3129
10.81	1239	1108.5	10.01	82.8	2298
10.80	974	1117	8.01	85.1	1572
10.79	720.5	1125	6.01	87.0	1013
10.80	479	1133	4.01	87.8	630
10.80	248	1141	2.01	85.6	385
10.81	130	1142	1.01	82.1	252
10.80	6	1141	0	N/A	65

Load line is -4mV per A for loads greater than 2A set by R6 at 2.61k.
Output voltage follows slope very well from 2A thru 14A. Below 2A it does not rise 8mV to 1149mV as per slope, but stays at the 2A output level. This may be due to reduction in duty cycle / frequency at these light loads to save power loss. At no load Vout is still well within the +/- 1.5% limits of target 1.150V.

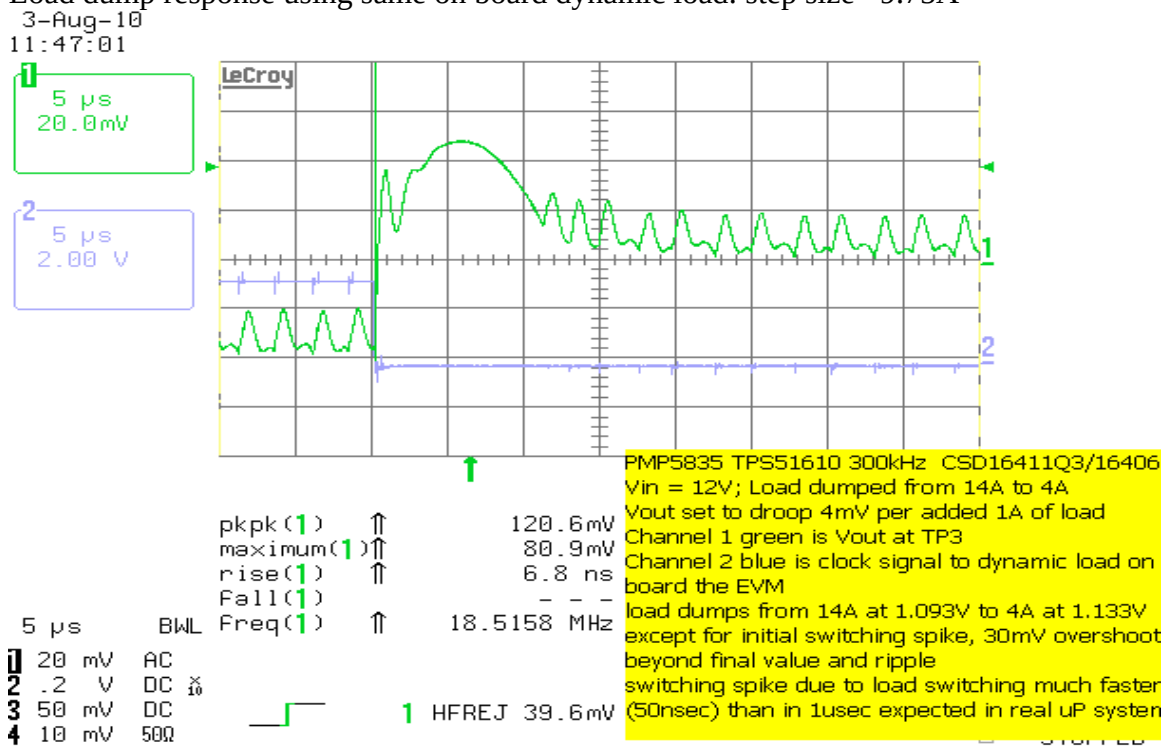
Ripple out at max load and max Vin:



Step load response using ‘on board” dynamic load: step size ~9.75A

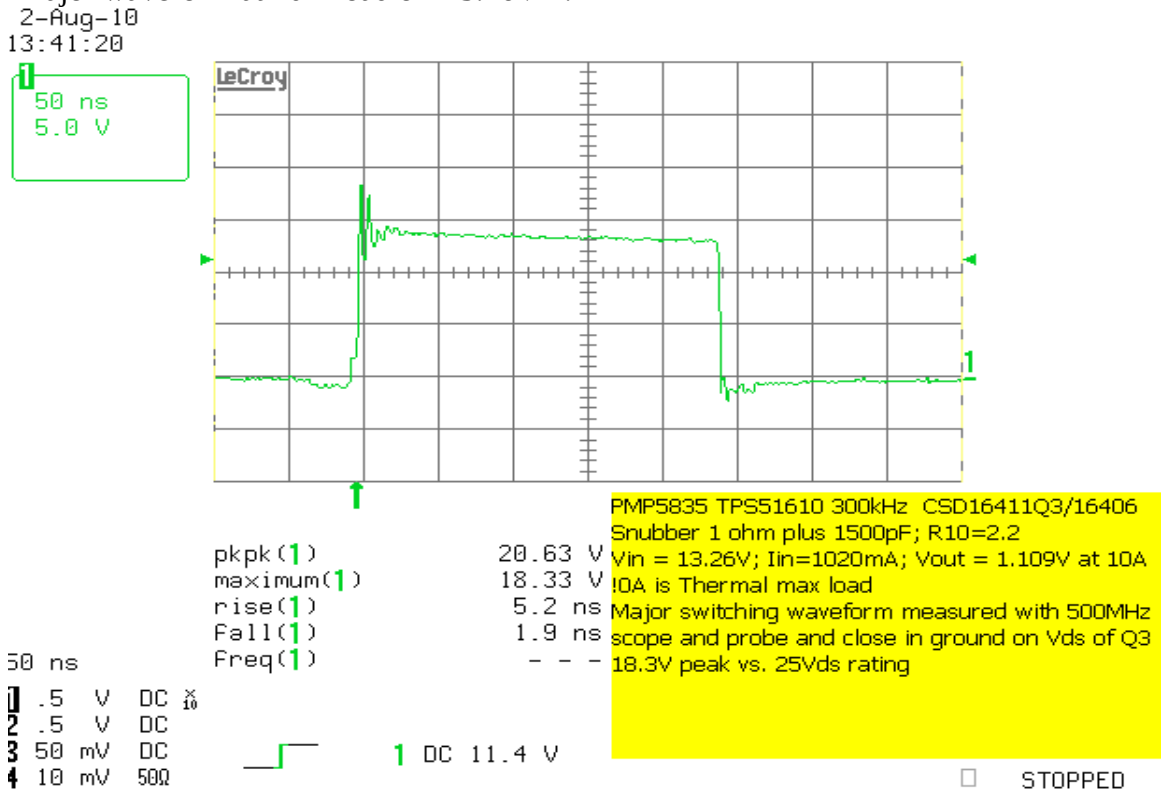


Load dump response using same on board dynamic load: step size ~9.75A

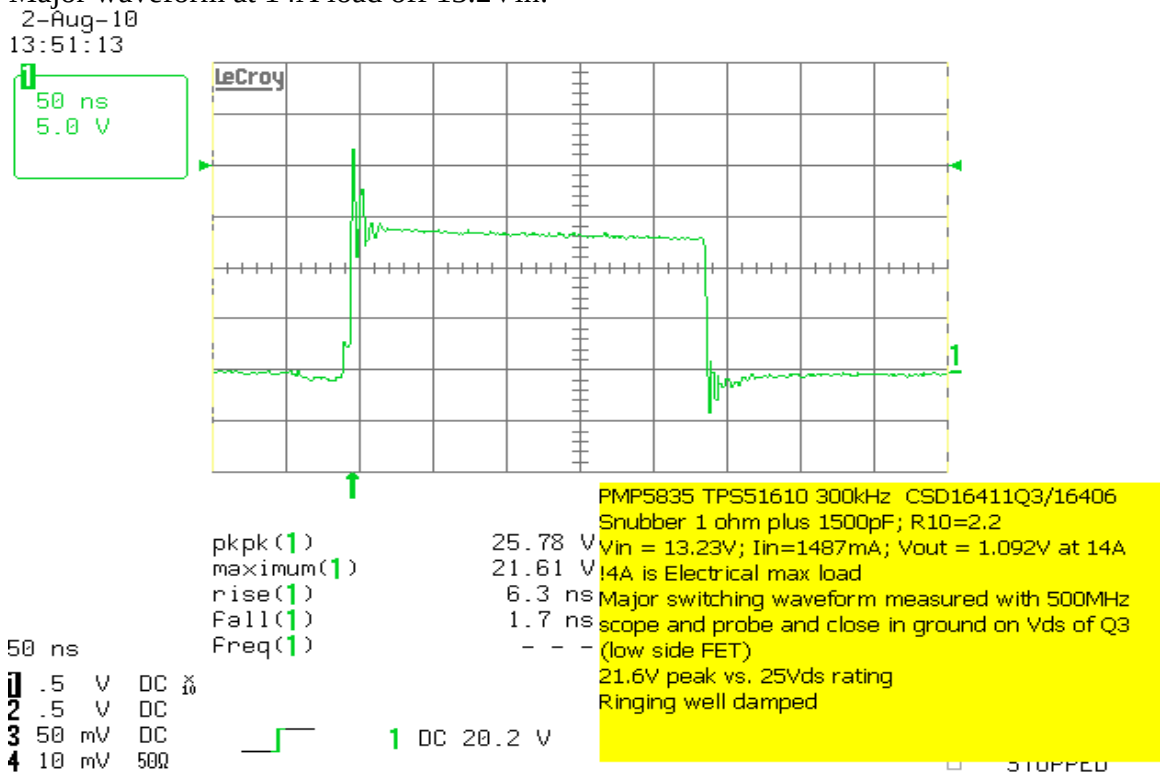


Qq

Major waveform at 10A load off 13.26Vin:

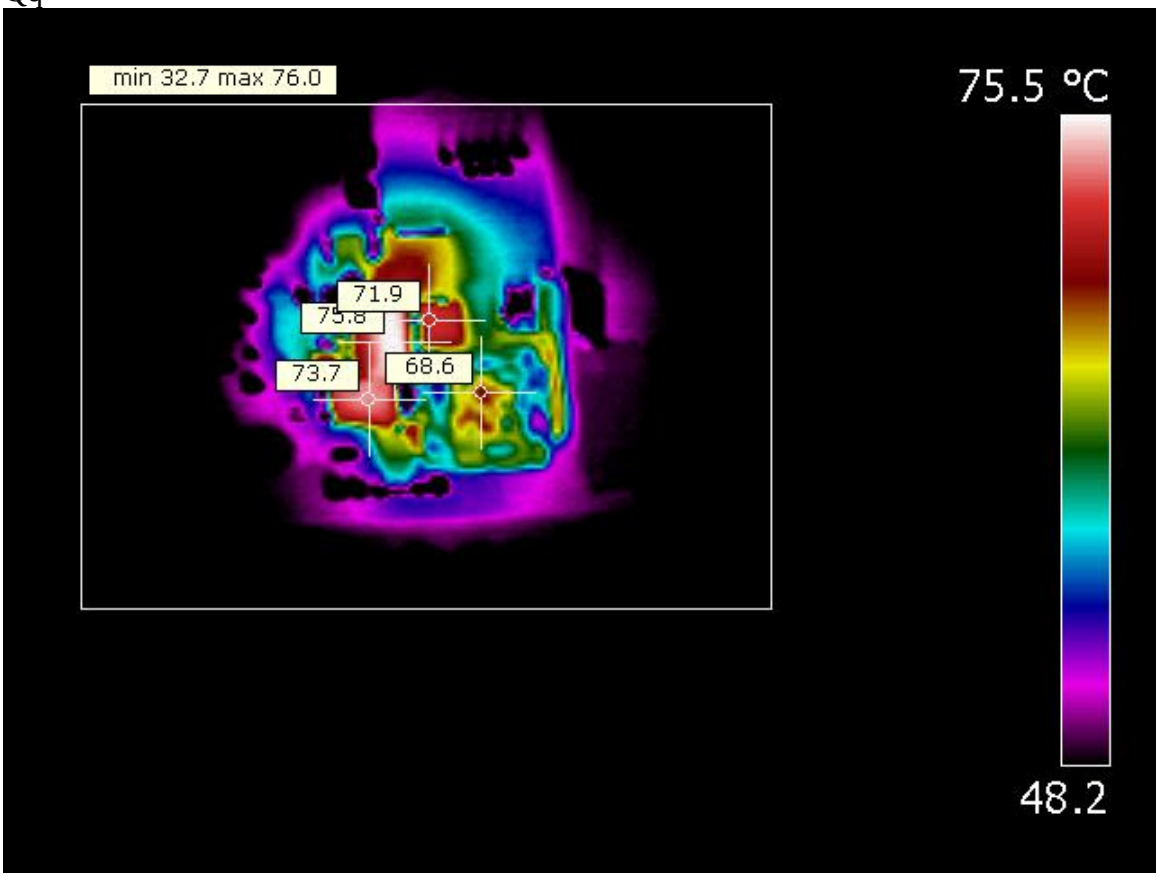


Major waveform at 14A load off 13.2Vin:



Qq

Thermal results:
Run for >10 minutes at 10A Thermal max off Vin max of 12V+10%: No forced air
Snubber added (1500pF size 805 plus 1 ohm size 2010 across Vds of lo side FET and R10 increased from zero to 2.2 ohm to slow down hi side turn on)
PMP5835 with snubber and R10=2.2; 13.26Vin, 5.007Vbias, 1020mA in 1.109Vout at 10.0A ambient 23-25 deg. C
Low side FET hottest at 76 deg C, hi side 72, choke 69, snubber resistor (1 ohm size 2010) 74
Qq



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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265