Test Report: PMP23209

Highly-Integrated, 12-V, 100-mA, Dual-Output, Isolated Bias Supply Reference Design

Description

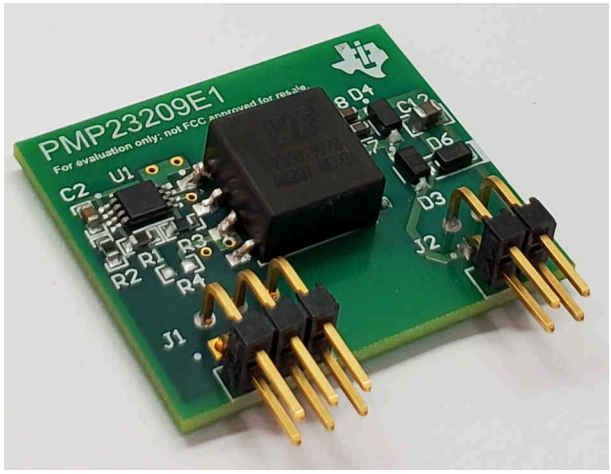
This reference design generates two isolated +12-V rails at 100 mA each from a 12-V_{DC} input voltage. The design is optimized for a small footprint by employing a primary resonant LLC topology with a single UCC25800 driver and a transformer with functional insulation.

Features

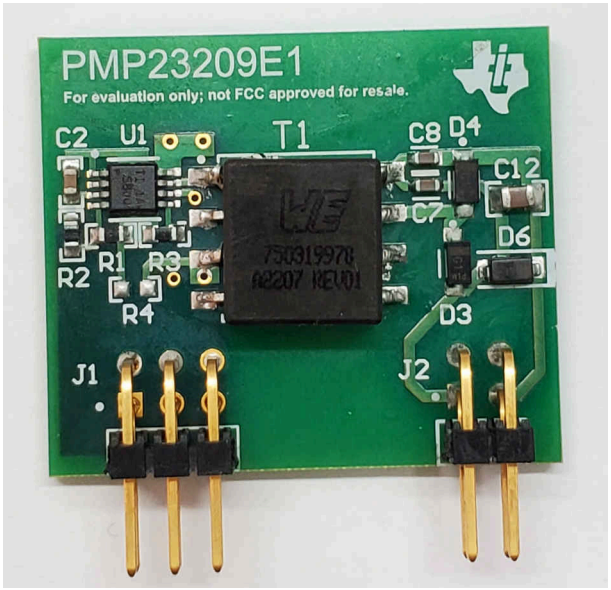
- Small size with simplified LLC design
- High efficiency: 85% at full load
- Dual output for high-side (HS) and low-side (LS) drivers
- Employs small and low-cost transformer

Applications

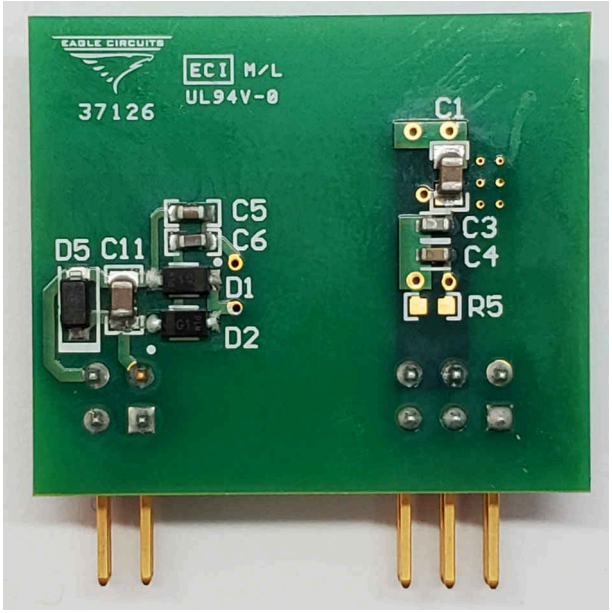
- GaN, IGBT and SiC gate transformer driver bias supply
- Automotive onboard charger (OBC)
- Automotive DC/DC converter
- Automotive traction inverter and motor control



Top of Board (Angled)



Top of Board



Bottom of Board

1 Design Information

1.1 Voltage and Current Specifications

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{IN}	12 V
V_{OUT} HS, V_{OUT} LS	12 V ±10%
I_{OUT} LS, I_{OUT} HS	100 mA

1.2 Dimensions

The dimensions of the board are 32 mm × 27 mm × 6.5 mm.

1.3 System Schematic

The following image illustrates the simplified schematic.

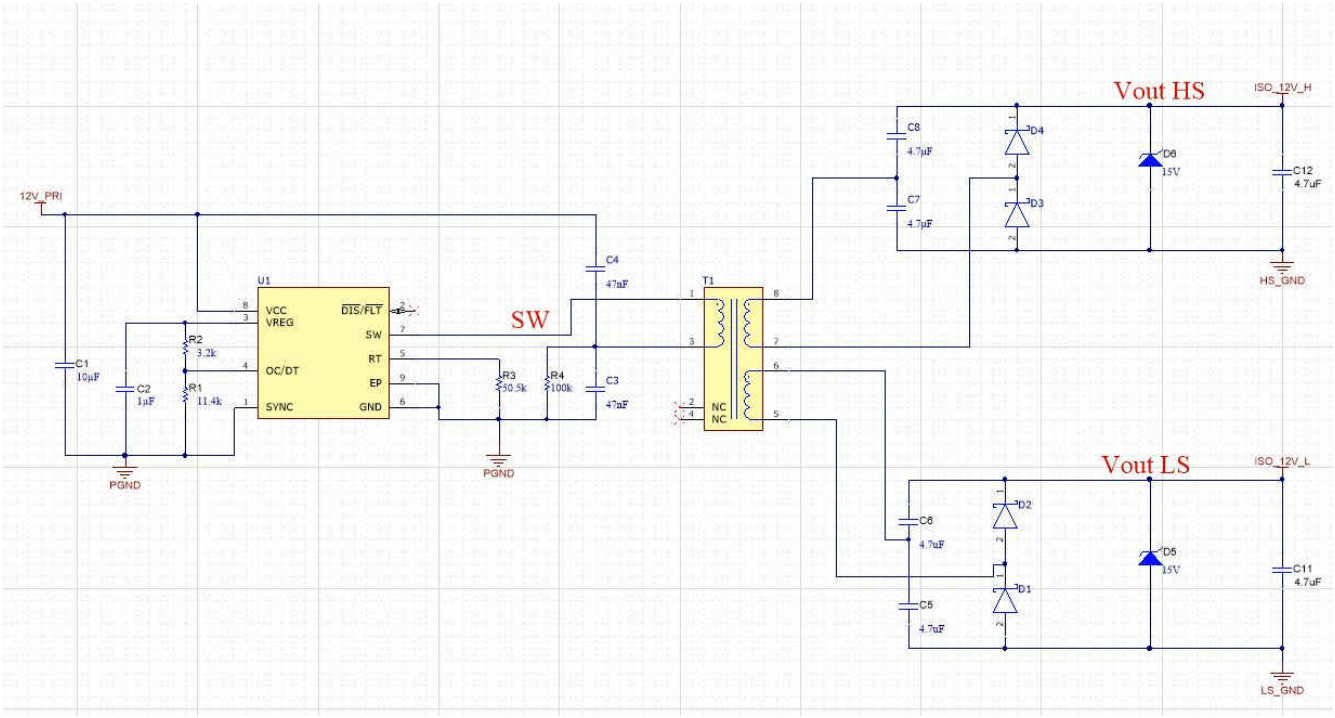


Figure 1-1. PMP23209 Schematic

2 Testing and Results

2.1 Output Voltage Regulation

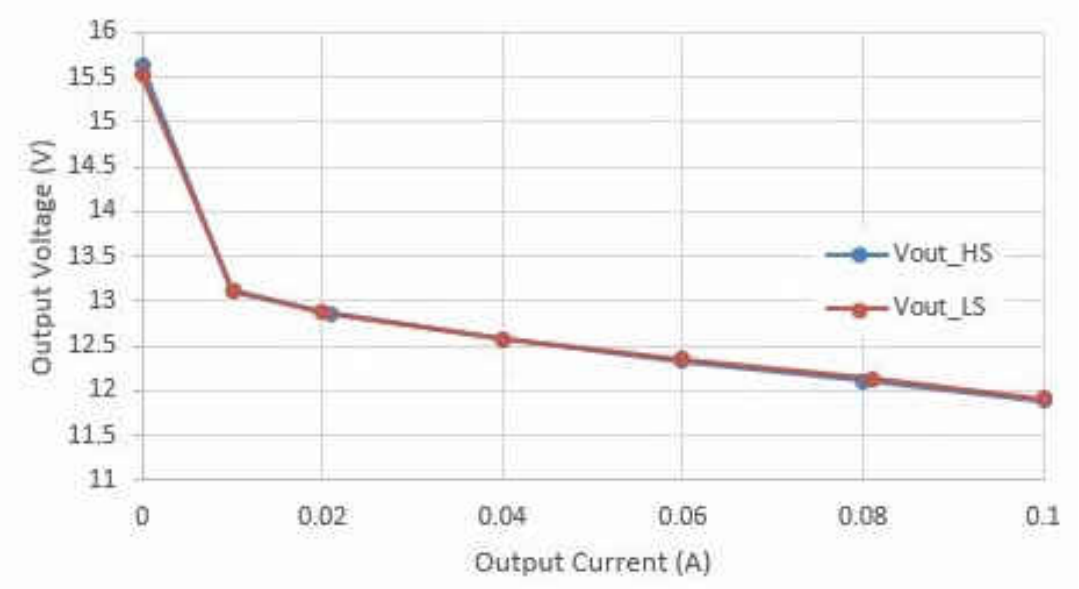


Figure 2-1. Open Loop Output Voltage vs Output Current

2.2 Efficiency Graphs

Efficiency and power loss are shown in the following figures.

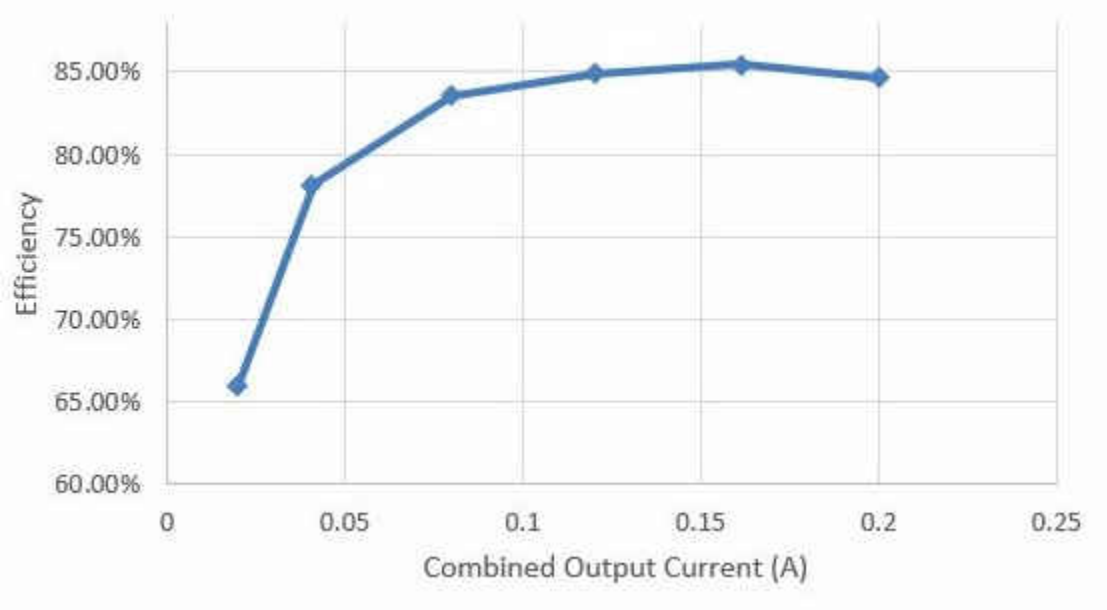


Figure 2-2. Efficiency – HS and LS Rail Current Split Evenly

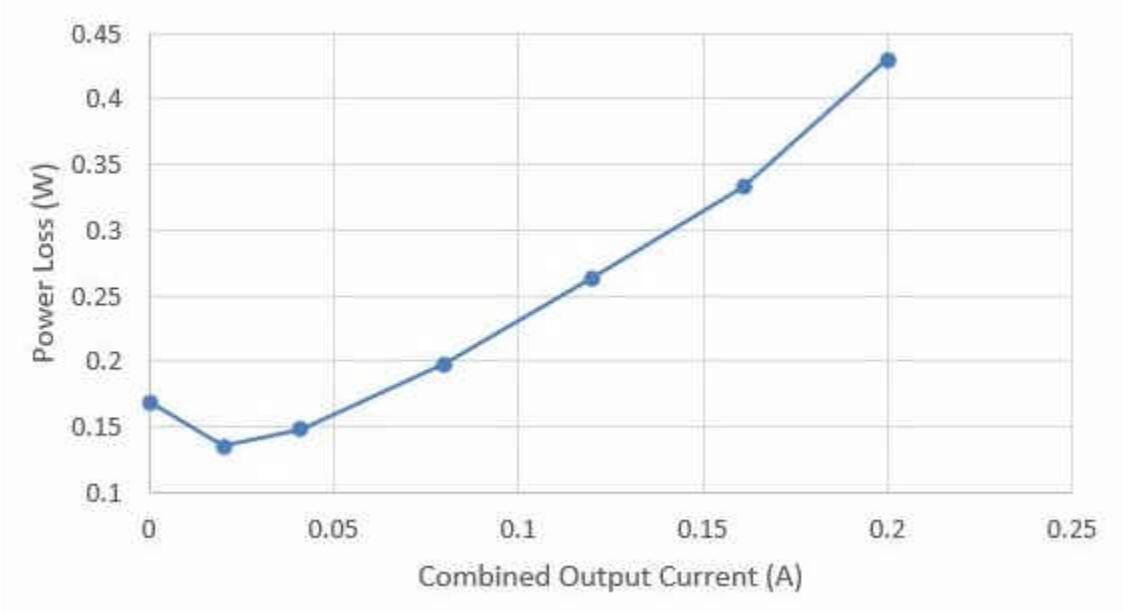


Figure 2-3. Power Loss – HS and LS Rail Current Split Evenly

2.3 Efficiency Data

Efficiency data is shown in the following table.

V_{IN} (V)	I_{IN} (A)	V_{OUT_HS} (V)	I_{OUT_HS} (A)	V_{OUT_LS} (V)	I_{OUT_LS} (A)	P_{IN} (W)	P_{OUT} (W)	P_{loss} (W)	Efficiency
12.06	0.014	15.64	0	15.52	0	0.16884	0	0.16884	0.00%
12.05	0.033	13.11	0.010	13.12	0.010	0.39765	0.2623	0.13535	65.96%
12.05	0.056	12.86	0.021	12.87	0.020	0.6748	0.52746	0.14734	78.17%
12.04	0.1	12.58	0.040	12.58	0.040	1.204	1.0064	0.1976	83.59%
12.03	0.145	12.33	0.060	12.35	0.060	1.74435	1.4808	0.26355	84.89%
12.02	0.19	12.11	0.080	12.13	0.081	2.2838	1.95133	0.33247	85.44%
12.01	0.234	11.89	0.100	11.91	0.100	2.81034	2.38	0.43034	84.69%

2.4 Thermal Images

All images were captured with the DUT at 25ºC ambient, after a 30-minute warm up. The output was loaded with 100 mA on both HS and LS rails.

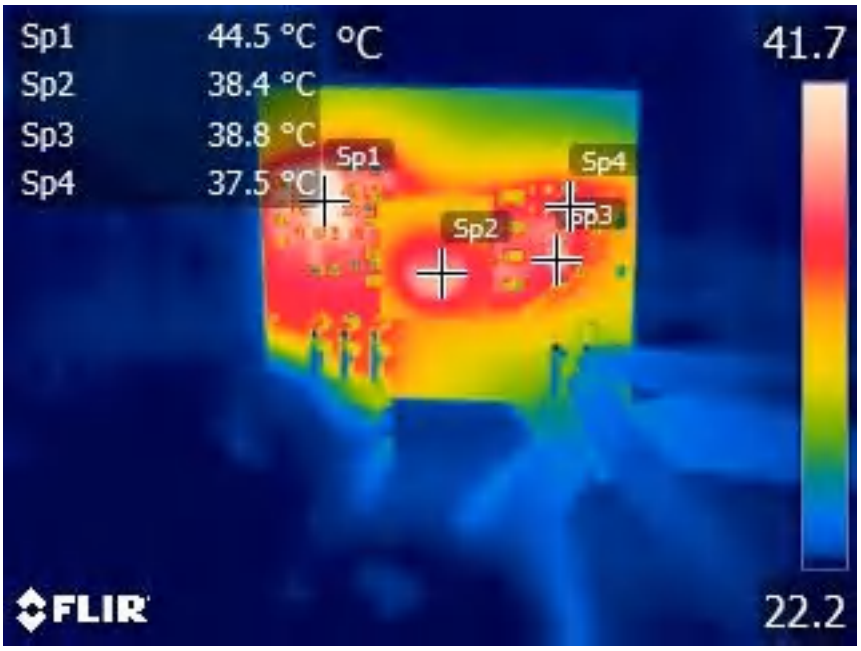


Figure 2-4. Front

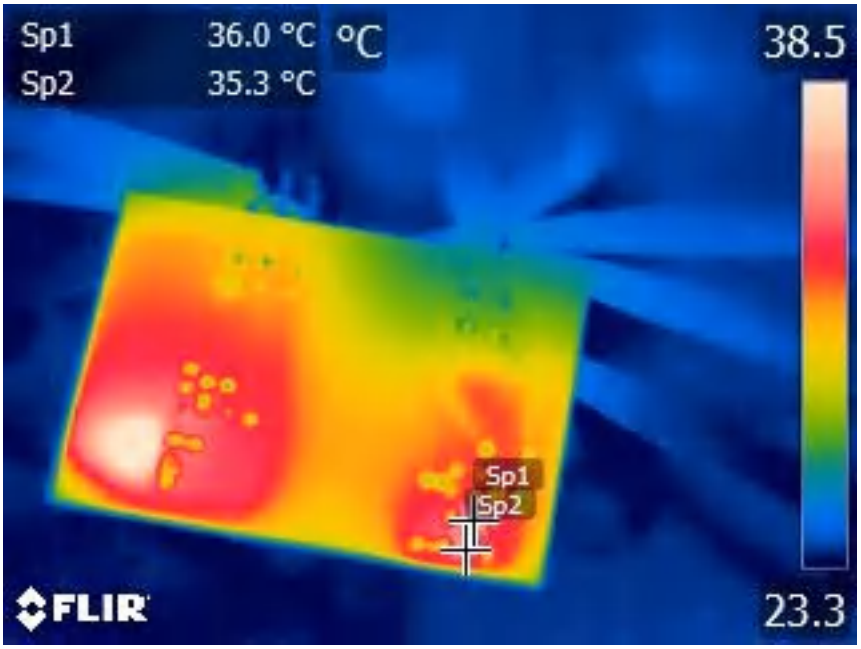


Figure 2-5. Back

3 Waveforms

3.1 Switching

The following waveform is the switch node at 12-V input, and 100 mA on both HS and LS rails.

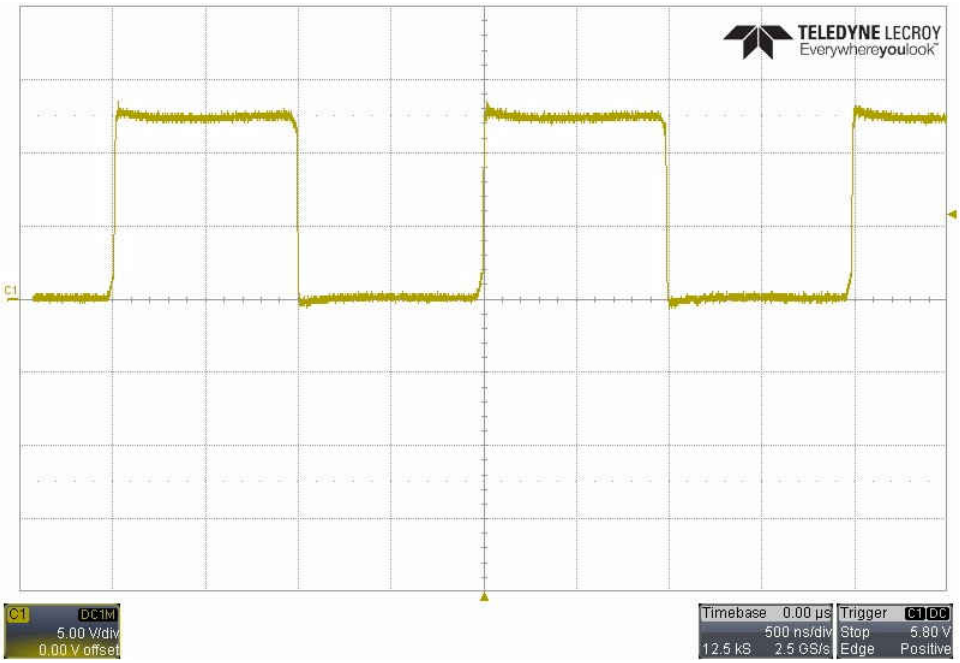


Figure 3-1. Switch Node: 12-V Input, 100 mA on Both HS and LS Rails

3.2 Output Voltage Ripple

Output voltage ripple waveforms are shown in the following figures.

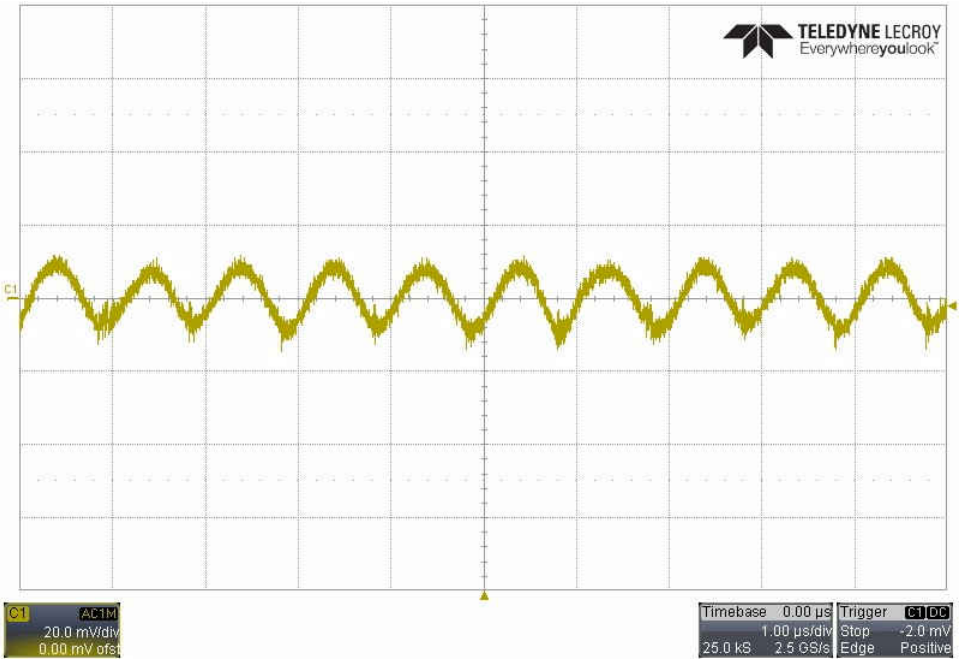


Figure 3-2. Output Voltage Ripple of HS Rail

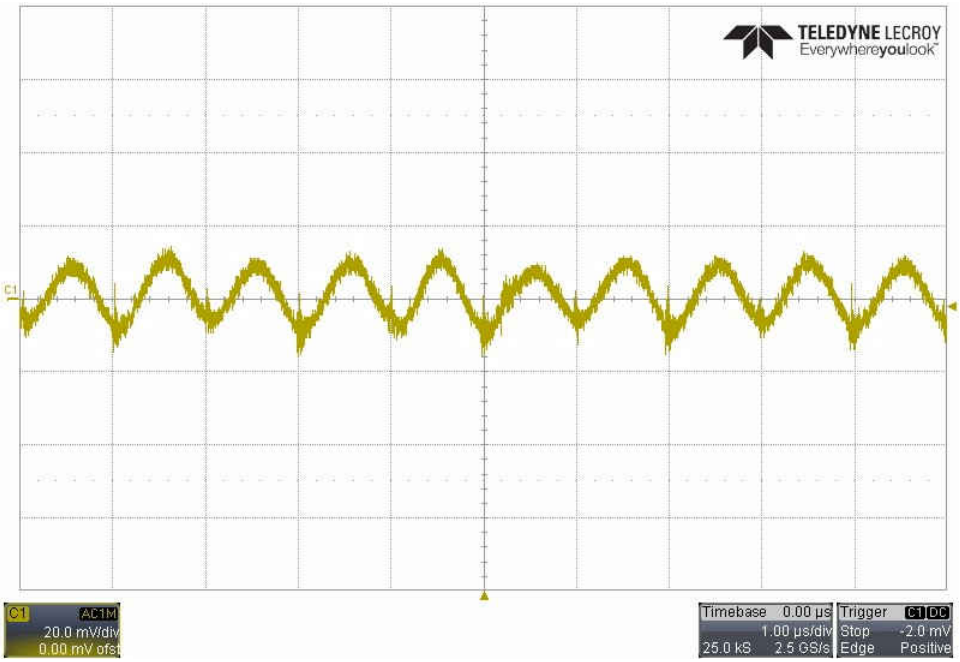


Figure 3-3. Output Voltage Ripple of LS Rail

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