

DRA71x Cost Effective Automotive Reference Design

User's Guide



Literature Number: SPRUII3

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1	Overview	5
1.1	Reference Design Feature List.....	5
1.2	CPU Board Component Identification.....	7
2	Hardware	9
2.1	Hardware Architecture.....	9
2.2	DRA71x Processor.....	9
2.3	Power Architecture.....	10
2.4	Reset Structure.....	10
2.5	Memory.....	11
2.6	Clocks.....	12
2.7	Boot Modes.....	12
2.8	JTAG/Emulator and Trace.....	13
2.9	UART Terminal.....	13
2.10	CAN Interfaces.....	13
2.11	Universal Serial Bus (USB).....	13
2.12	Wired Ethernet.....	13
2.13	Video Output.....	14
2.14	Video Input.....	14
2.15	Audio.....	14
2.16	WL1873.....	15
2.17	I2C Peripheral Map.....	16
2.18	GPIO List.....	16
2.19	Configuration EEPROM.....	17
3	Signal Multiplex Logic	18
3.1	MMC1 Selection (Mux A).....	18
4	Test Automation	19

List of Figures

1	DRA71x Reference Design Board (Front and Back)	5
2	CPU Board – Front	7
3	CPU Board – Back	8
4	CPU Board Block Diagram	9
5	Power Distribution Block Diagram	10
6	Reset Structure	11
7	Block Diagram of Audio System.....	15
8	Mux Diagram for SD Card/WiLink.....	18

List of Tables

1	Reset Signals Summary	11
2	SoC Boot Mode Switch Settings	12
3	Boot Mode Table	13
4	I2C Device Address Chart	16
5	SoC GPIO Map	16
6	EEPROM Configuration	17
7	PMIC Boot Pin Functions	18
8	Mux Settings	18
9	Automated Test Mapping.....	19
10	Power Measurement System	19

DRA71x Cost Effective Automotive Reference Design

This user guide (UG) is intended for software and hardware engineers (users) developing applications such as infotainment, reconfigurable digital cluster, or integrated digital cockpit. The guide describes the SoC hardware, firmware, and software functions supplied by Texas Instruments Inc. The term DRA71x and SoC are used in reference to the DRA71x application processor. The terms low-cost automotive reference design, LCARD, reference design, CPU board, board, board assembly, or CPU Bd are used in reference to the PCB board assembly that supports the DRA71x processor, along with peripheral and support components. The primary goal of this guide is to explain the reference design's functional blocks, signal routing, switch controls, system configurations, and signaling interfaces.

The version number of this manual has multiple digits: a single “ones” position digit followed by a two position decimal. A change to the “ones” digit designates a major document update, as may be required for significant reference design updates or features change over the course of development. A decimal place change is used for all other minor clarifications or text corrections, as needed.

Related Documentation from Texas Instruments:

- *DRA71x (SR2.0) SoC for Automotive Infotainment Technical Reference Manual* ([SPRUIC2](#))
- *DRA71x Infotainment Applications Processor Data Manual* ([SPRS960](#))

If you need assistance, contact your TI sales representative.

FCC Warning:

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy, and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user, at their own expense, will be required to take whatever measures may be required to correct this interference.

1 Overview

The DRA71x reference design is comprised of a CPU board system that includes a complete set of infotainment peripherals. The design (shown in [Figure 1](#)) is to be used for debug and development. This system has been designed to enable customers to evaluate the processor performance and flexibility in the following targeted markets:

- Entry-level IVI head unit
- Radio and audio coprocessor
- Audio amplifier

The reference design contains the DRA71x applications processor, a power solution, memory (DRAM (DDR3L), eMMC), and interface ports. The reference design provides additional complexities and support components to enhance SoC testing and software debugging capabilities that may not be needed in a final product.

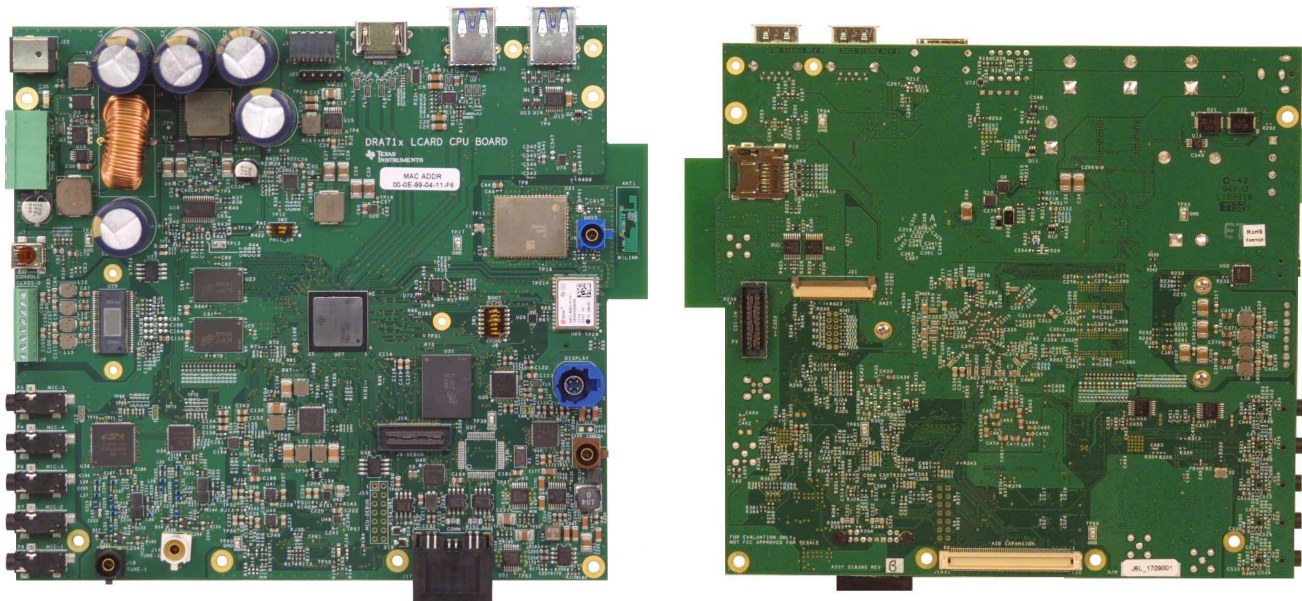


Figure 1. DRA71x Reference Design Board (Front and Back)

1.1 Reference Design Feature List

- Processor: DRA71x SoC (17-mm x 17-mm package, 0.65-mm pitch, 538-pin BGA (CBD))
- Power supply:
 - 12-V DC input
 - Optimized power management solution
 - Compliant with SoC power sequencing requirements
- PCB:
 - 6-layer PCB stack-up
 - Dimension (W x D) 150 mm x 150 mm
 - 100% PTH technology

WiLink is a trademark of Texas Instruments.
 ARM Cortex is a registered trademark of ARM.
 Bluetooth is a registered trademark of Bluetooth SIG, Inc..
 microSD is a trademark of SD-3C.

- Memory:
 - DRAM (DDR3L (2GB)): 16 Gbit (2 × (512M × 16))
 - EMMC flash: 32 Gbyte
 - I2C EEPROM, 512Kb
 - Optional SD card
- Boot mode selection DIP switch
- JTAG/emulator: 60-pin MIPI-60 JTAG/trace connector
- Supported interfaces and peripherals:
 - 2× USB ports (1× USB3.0, 1× USB2.0)
 - 5× Audio inputs (MIC1-MIC5)
 - 2× Video outputs (HDMI, FPD-Link III)
 - 2× Digital radio tuners
 - Camera sensor support through Coax
 - TI WL1873 for Bluetooth® and WLAN support
 - GPS support
 - CAN interface – 2-wire PHY on DCAN1
 - Automotive ethernet PHY

1.2 CPU Board Component Identification

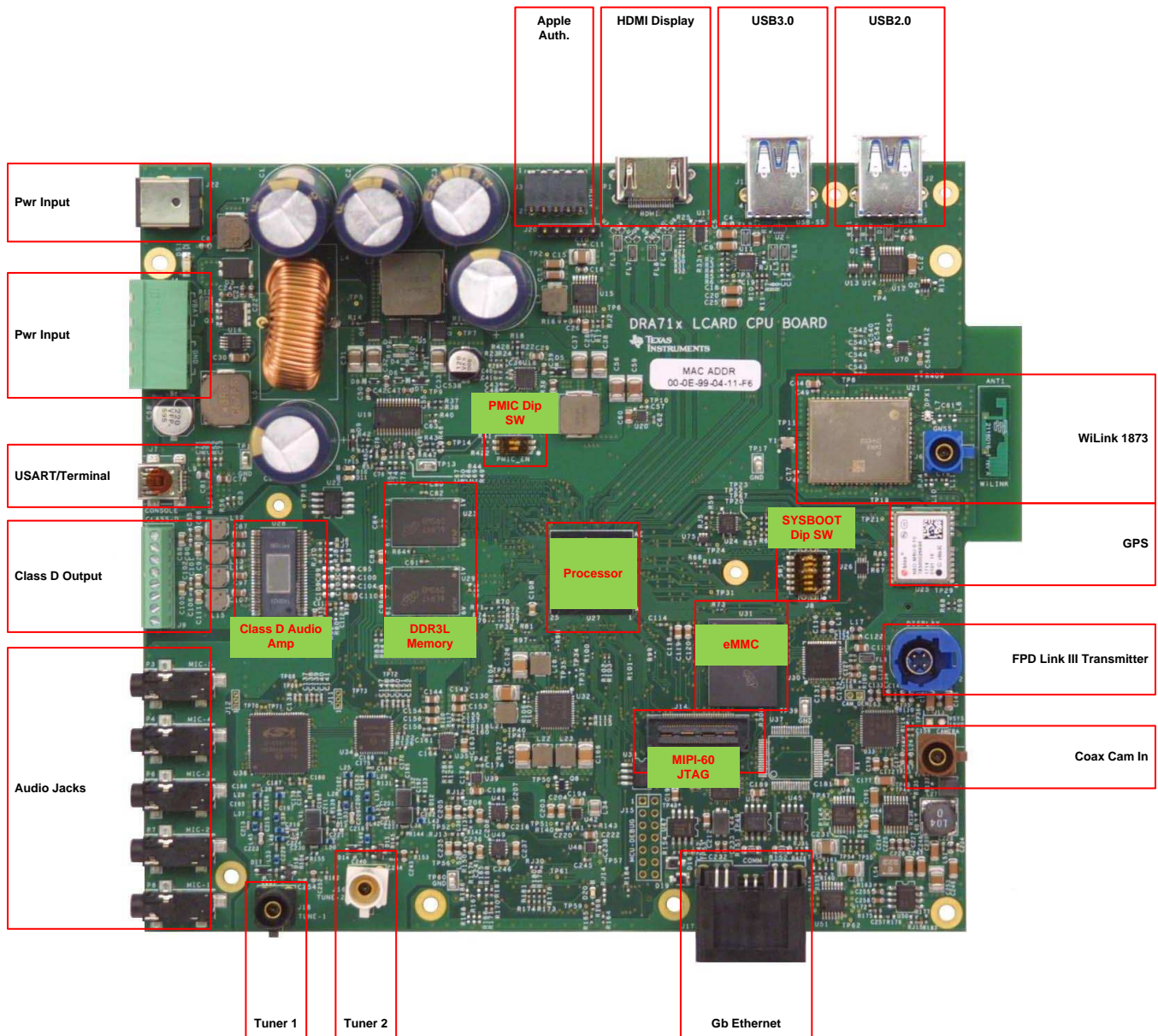


Figure 2. CPU Board – Front

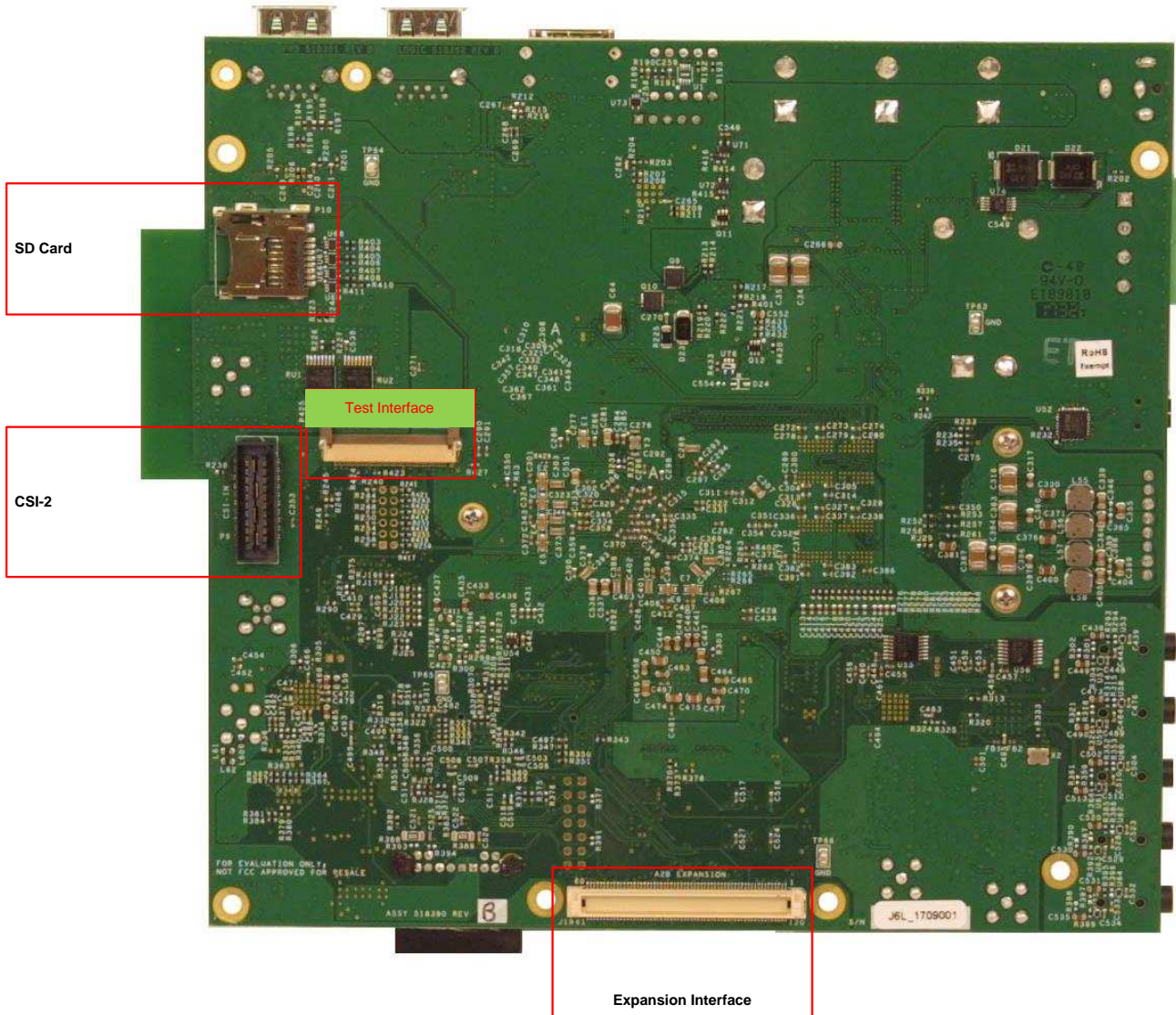
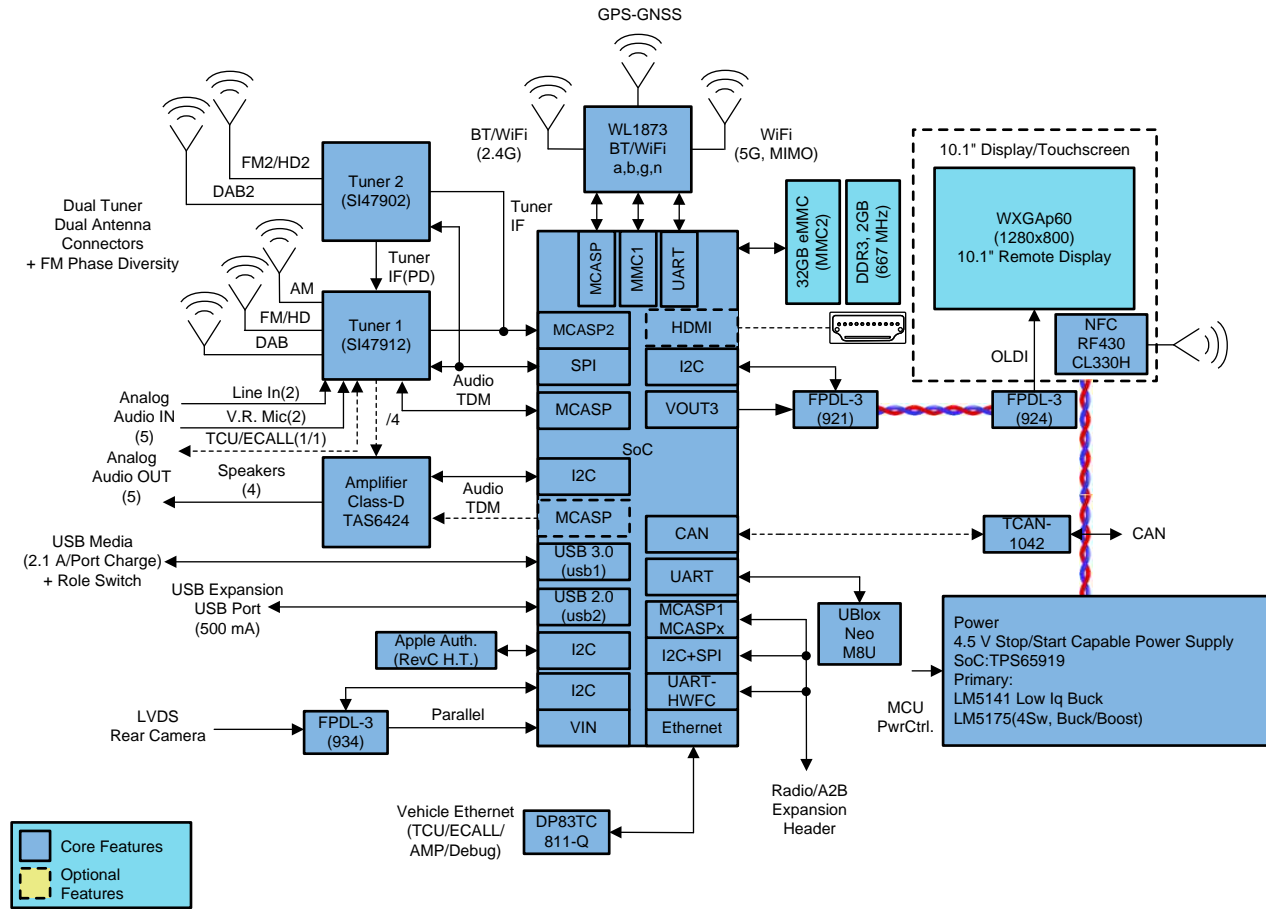


Figure 3. CPU Board – Back

2 Hardware

2.1 Hardware Architecture

The functional block diagram is shown in Figure 4.



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Figure 4. CPU Board Block Diagram

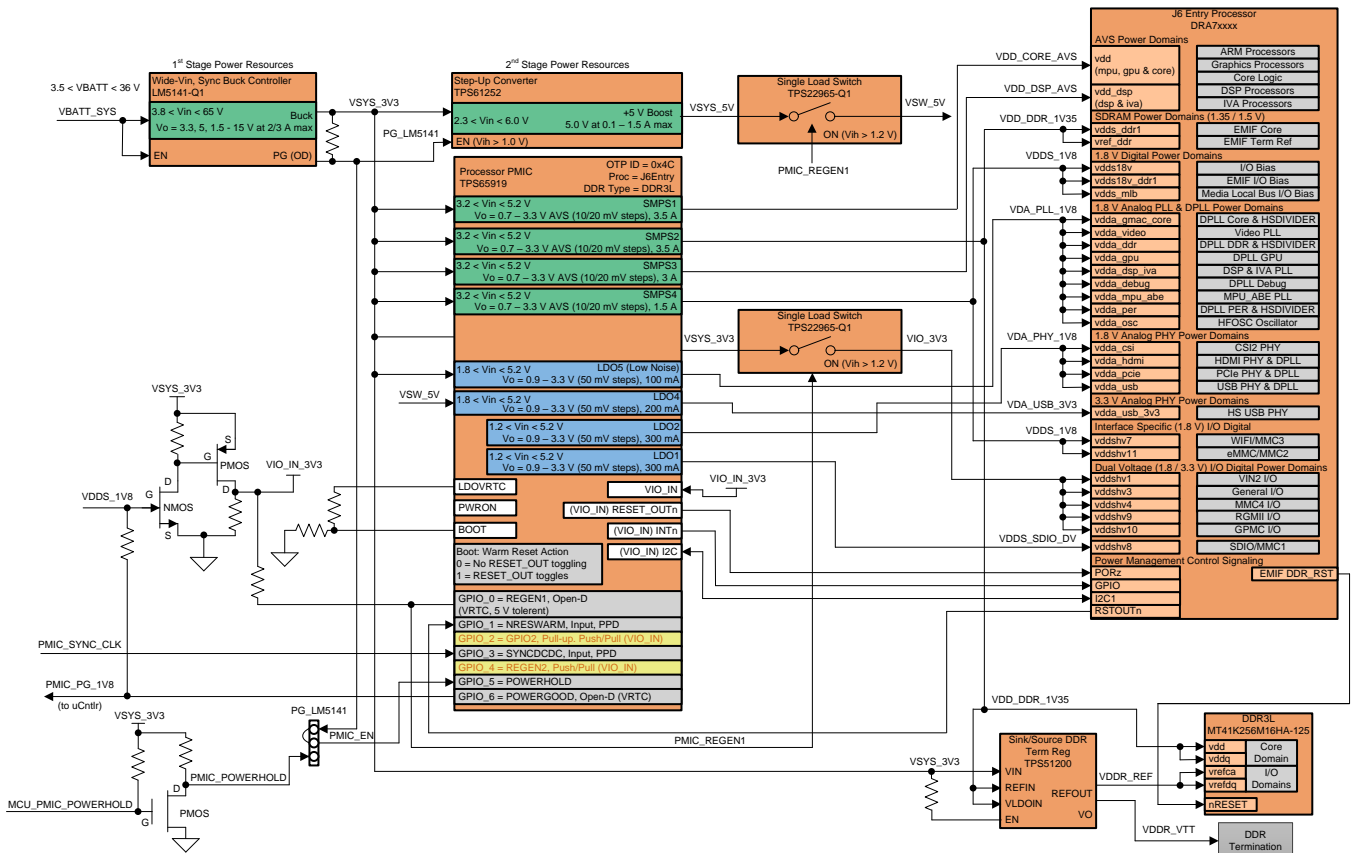
2.2 DRA71x Processor

The processor is highly-integrated, programmable SoC silicon solution. Device specifications and feature notes about SoC include:

- Video, image, and graphics processing support
 - Full-HD video (1920 × 1080p, 60 fps)
 - Multiple video input and video output
 - 2D and 3D graphics
- ARM Cortex®A-15 microprocessor subsystem
- C66x floating-point VLIW DSP
- DDR3/DDR3L memory interface (EMIF) module
- HDMI encoder
- SuperSpeed USB3.0 dual-role device

2.3 Power Architecture

The power architecture is optimized for this TI design. The input is designed for a 12-V power source, similar to a car battery, but can handle a range from 6 V to 36 V. The 12-V source is boosted to 16 V, and bucked down to 3.3 V. The 16 V is used for the media hub and display module. The 16 V is also bucked down to 10.5 V to be used for sensor ports and modules. The 3.3 V is the input to the TPS65919-Q1, which is optimized to provide a single PMIC power solution for the power rails of the SoC. Figure 5 shows the SoC portion of the power diagram.



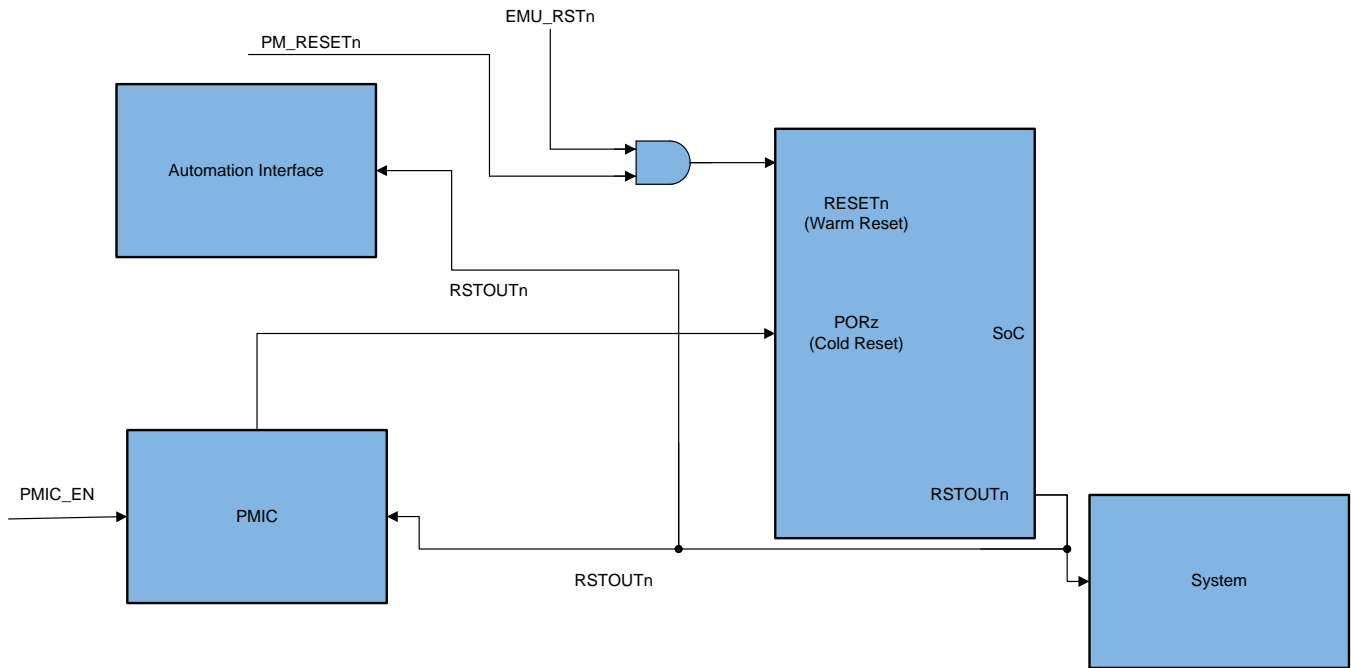
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Figure 5. Power Distribution Block Diagram

The power wires are included such that it connects to (J4) on the board. There is an optional barrel connector (J22), which can be used in place of J4 for powering the system. The maximum input voltage to the system is 36 V. Exceeding this value can damage the components.

2.4 Reset Structure

The reset structure is supported through the automation interface or through the PMIC, and shown in Figure 6. The power-on reset timing is controlled primarily from the system power IC (TPS65919). Warm reset is sourced from the LCPD automation system and the MIPI-60 JTAG/trace connector. Refer to Section 5 to see the pin mapping.



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Figure 6. Reset Structure

Table 1 summarizes the reset signals.

Table 1. Reset Signals Summary

Reset Type	Reset Signal Sources	Comments
Power-on reset (PORz)	PMIC_RESET_OUT	Power-on reset from PMIC
Warm reset	PM_RESETE _n	Reset from LDCP
	EMU_RST _n	Reset from emulator
PMIC power-on reset	PMIC GPIO5	PMIC reset input (PMIC_EN)
Processor reset out	RSTOUT _n	Reset output from processor to system, PMIC (warm reset input)

2.5 Memory

2.5.1 SDRAM Memory

The design includes 2 GBytes of DDR3L memory, and can operate at clock speeds up to 667 MHz (DDR3-1333). The memory is populated with two 1-GByte surface-mount memory chips. On the schematic, they are U23 and U29.

SDRAM device used: Micron MT41K512M16HA-125 AIT:A

The DDR3L power is generated from the SoC power solution, and set to 1.35 V. It uses fly-by topology with VTT termination. VTT supply is generated using a sink/source termination regulator (TPS51200).

2.5.2 eMMC Flash Memory

As a primary non-volatile storage device, the design includes 32 GBytes of eMMC flash memory. The memory device is EMMC v4.51-compliant, and connects to the MMC2 port of the SoC. The design can support rates up to HS-200.

EMMC device used: Micron MTFC8GLWDM-3M AIT Z

Booting from the EMMC flash memory is supported on the design. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (J8 or SW1).

2.5.3 microSD Card Cage

For non-volatile storage expansion, the design includes a microSD™ card cage. The cage is connected to the MMC1 port of the SoC. There is an active mux on MMC1 to support the SD card or the WiLink™ 1873 module, but both cannot be supported simultaneously. To support higher speed cards that operate at lower voltages, the I/O supply is changed from 3v3 to 1v8 by communication to PMIC. The default LDO1 out is 3v3.

2.6 Clocks

The SoC has a primary clock input. The device clock (OSC0) is source with a 19.2-MHz clock. The auxiliary clock inputs are grounded.

In addition to the SoC clock inputs, the design includes other clock sources. A 25-MHz clock is provided to ethernet PHY, 36.8 MHz provided for the radio tuner, and 8 MHz provided for the optional external MCU.

2.7 Boot Modes

The SoC supports a variety of different boot modes, which are determined by the 16-bit system boot setting present on the shared specific I/O balls during the power-on sequence (see the TRM for details). Boot mode selection is accomplished by the setting of DIP switches SW1, as shown [Table 2](#), prior to cycling power. Sysboot0-sysboot5 can be triggered, sysboot6-sysboot15 are hard-set on the design.

These SoC resources can be redeployed to support alternate interfaces after boot-up, by both the SoC pin EVM mux settings.

Table 2. SoC Boot Mode Switch Settings

SoC Interface (Internal System Boot Input)	CPU Bd Net	DIP Switch Ref Des. Position # Connections	Factory Settings
GPMC_AD0 (sysboot0)	VOUT3B_D0	SW1.P1	OFF
GPMC_AD1 (sysboot1)	VOUT3B_D1	SW1.P2	OFF
GPMC_AD2 (sysboot2)	VOUT3B_D2	SW1.P3	OFF
GPMC_AD3 (sysboot3)	VOUT3B_D3	SW1.P4	OFF
GPMC_AD4 (sysboot4)	VOUT3B_D4	SW1.P5	OFF
GPMC_AD5 (sysboot5)	VOUT3B_D5	SW1.P6	OFF
GPMC_AD6 (sysboot6)	VOUT3B_D6	N/A	OFF
GPMC_AD7 (sysboot7)	VOUT3B_D7	N/A	OFF
GPMC_AD8 (sysboot8)	VOUT3B_D8	N/A	ON
GPMC_AD9 (sysboot9)	VOUT3B_D9	N/A	ON
GPMC_AD10 (sysboot10)	VOUT3B_D10	N/A	OFF
GPMC_AD11 (sysboot11)	VOUT3B_D11	N/A	OFF
GPMC_AD12 (sysboot12)	VOUT3B_D12	N/A	OFF
GPMC_AD13 (sysboot13)	VOUT3B_D13	N/A	OFF
GPMC_AD14 (sysboot14)	VOUT3B_D14	N/A	OFF
GPMC_AD15 (sysboot15)	VOUT3B_D15	N/A	OFF

The default switch configuration boots from eMMC flash. The supported bootmodes are listed in [Table 3](#). The bootmodes in the table are listed in the 'ON' or 'OFF' state for all six switches on the component.

Table 3. Boot Mode Table

Boot Mode	sw1	sw2	sw3	sw4	sw5	sw6
eMMC(Default)	off	off	off	off	off	off
USB	off	off	off	on	off	on
UART	on	on	off	on	off	on
eMMC(USB)	off	off	off	on	on	off
eMMC(BOOT PART)	on	on	off	off	off	off
SD	off	off	off	on	off	off

2.8 JTAG/Emulator and Trace

The JTAG emulation interface is supported through the MIPI 60-pin interfaces. The EVM kit includes an adapter for supporting other JTAG interfaces, including TI's 20-pin cJTAG interface. Reset (warm reset) through the emulator is supported.

Debug and trace is also supported through the MIPI-60 connector. The EVM supports up to 20 trace bits. At the SoC level, the trace pins are shared with VIN2A, which also supports the deserializer output from the camera.

2.9 UART Terminal

The design supports a USB to UART connection for the user terminal. A FT232 device is used to transport the UART information over USB to a host PC. The EVM is designed to use the SoC UART3 as the primary terminal connection, and is connected to port A of the USART transceiver. The USB-side of the FT232 device is powered from the USB port, and the connection stays active regardless of power state of the EVM.

USART device used: FTD Chip FT232RQ

A USB cable (mini-B to type A) is used to connect the EVM to a PC, and is included as part of the EVM kit.

2.10 CAN Interfaces

The EVM supports access to two CAN interfaces through a Molex connector (J17). One CAN interface is supported through the optional external MCU, and the other one is supported through the SoC.

CAN device used: Texas Instruments TCAN1042HGVQ1

2.11 Universal Serial Bus (USB)

Two independent USB ports are supported on the EVM. USB3.0 super-speed bus (USB1) is supported using port USB1 to a Type-A connector. This interface supports rates up to 5 Gbps. USB2.0 high-speed interface is supported using port USB2 to a Type-A connector. It can support rates up to 480 Mbps. VBUS can be supplied to peripheral when in host mode, by enabling the VBUS switch (controlled through the SoC). However, the design cannot be powered from VBUS when operating in device mode.

2.12 Wired Ethernet

The DP83TC811-Q1 is a single-port automotive ethernet PHY-compliant to IEEE802.3bw. It provides all physical layer functions required to transmit and receive data over single twisted pair cables. Additionally, the DP83TC811 provides flexibility to connect to a MAC through a standard MII, RMII, RGMII, or SGMII. On the design, ethernet is connected through a Molex 34826-0124 automotive connector.

2.13 Video Output

The design supports two different options for supporting video output – HDMI, and FPD Link-III. Each can be supported independently, or used simultaneously.

2.13.1 HDMI Display

The SoC includes a dedicated HDMI display interface, which is supported on a type-A HDMI connector. The interface supports 1080p with 24b color. A communication channel (DDC/CEC) is supported to the HDMI connector for communication with the HDMI panel. A monitor detect indication is also provided. The DDC/CEC interface and monitor detect signals (HPD) are translated through the transceiver, and can be controlled using I/O from the expander.

DDC transceiver used: Texas Instruments TPD12S016

2.13.2 FPD-Link III Output/Panel

The EVM includes a FPD-Link III parallel to serial interface on VOUT3. It supports up to 24 bits of data, and can operate at pixel rates up to 85 MHz. The interrupt is supported to enable back-channel communication, typically needed if supporting a touch screen. The transceiver is configured using I2C (port 4, 0x18).

Serializer device used: Texas Instruments DS90UB921Q1

Connector used: Automotive HSD connector, right-angle plug for PCB, Rosenberger D4S20D-40ML5-Z.

2.14 Video Input

2.14.1 FPD-Link III Imaging

Parallel video input is supported through connections from external sensors and transceivers. The SoC port VIN2A is routed to a FPD-Link III deserializer, which is fed from the coax connector (P5). This approach provides flexibility for customers to select from a variety of available modules, while also supporting connections of custom solutions. The attached module can be configured using I2C (port 4).

Connector used: Fakra Connector Nut Brown – 59S10H-40ML5-F

Deserializer used: DS90UB934-Q1

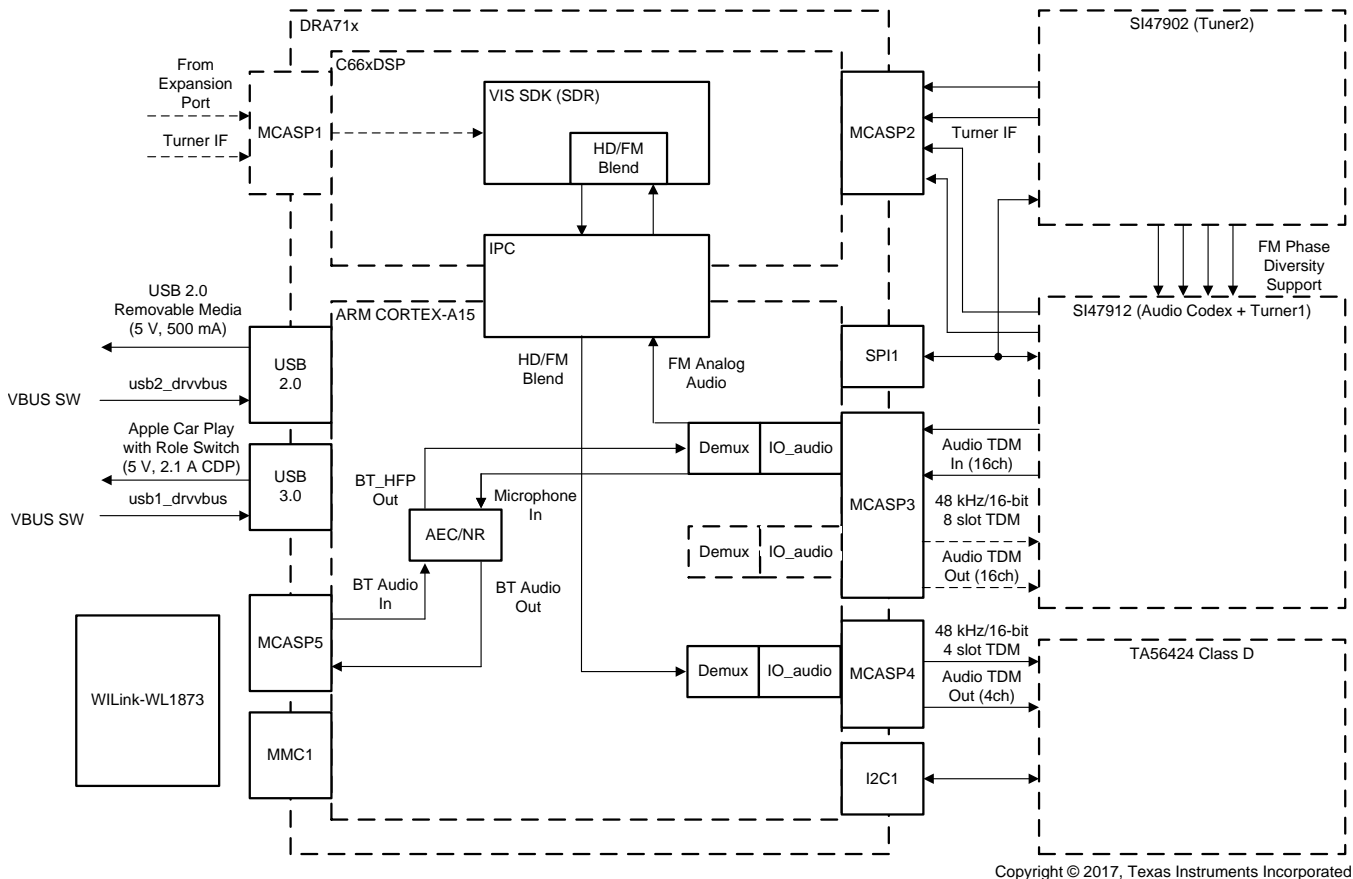
2.14.2 Serial Imaging

Serial video input is supported through connections from external sensors and transceivers. The SoC port CSI2-0 is routed to the connector (P9) interface designed to mate with external peripherals. This approach provides flexibility for customers to select from a variety of available modules. Both interfaces support additional signals for control and configuration of the attached modules. These interfaces (I2C port 1) are translated to 1.8-V I/O (with resistor option to leave at 3.3-V I/O).

Connector used: Samtec QSH-020-01-L-D-DP-A

2.15 Audio

The design includes the TAS6424-Q1 Digital Class D audio amplifier to provide quality audio output. The amplifier is designed to provide four channels with 4- Ω output capability with up to 75-W output power. The outputs have been broken out on the design to connect speakers to resemble a stereo load. The amplifier is located on the schematic at U28. The audio input is processed inside the SoC and pushed out digitally to the amplifier. The input can either be from the radio tuners (J16, J18) or the MIC IN ports (P3-P8). There are two radio tuners in the design; see [Figure 7](#). One tuner is a tuner only, and the other tuner has a built-in CODEC. These tuners can be used consecutively to provide FM phase support. The tuners are a SiLabs module, SI47912 and SI47902, capable of tuning to AM/FM/HD radio. [Figure 7](#) shows the flow from when the radio signal is received to its route to the SoC, where it is processed and then pushed out to the amplifier and speaker load. This design has a few options for which tuner and amplifier can be used, so the signal paths can vary depending on component choice.



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Figure 7. Block Diagram of Audio System

2.16 WL1873

U21 on the schematic is the Bluetooth/Wi-Fi/GPS module. The module is a Murata LBEN6ZZZHC built off of TI's WiLink8 WL1873 chipset that supports Standard Bluetooth, BLE, 2G, and 5G WLAN and GPS. The module offers an audio solution for Airplay receiver, full audio stack streaming, and more, in regards to audio streaming in infotainment. The WL1873 offers high throughput and extended range, along with Wi-Fi and Bluetooth coexistence in a power-optimized solution. The module uses a dual-band PCB antenna that can tune to 2.4 GHz and 5 GHz by using a diplexer. This solution saves space and money on the design by using only one antenna to tune to different bands. The WL1873 provides entry-level Global Positioning System (GPS) capabilities. The GPS feature on the WL1873 module supports 2 of the 4 GPS satellite constellations, thus making it a cost effective solution for entry-level navigation.

To support the feature, the PMIC must be changed to 1.8 V; then set the mux using the information from [Table 8](#). If the WiLink module is going to be used, the SD card feature will not be supported, as they cannot be used simultaneously.

2.17 I2C Peripheral Map

Table 4 shows the list of I2C interface available on the design, with a list of devices connected to each I2C interface and its corresponding device address.

Table 4. I2C Device Address Chart

CPU Board	Part No	I2C1	I2C2	I2C4	Device Addr (7b)
EEPROM	24WC256	X			0x50
Class D audio amp	TAS64240-Q1	X			0x6A
FPD-Link panel	DS90UB921-Q1			X	0x0C
FPD-Link imager	DS90UB934-Q1			X	0x30
PMIC	TPS65919-Q1	X			0x4C
Apple authentication	Apple I2C chip (no pop)	X			n/a
HDMI EEDID	TPD12S016RKTR		X		0x50
WiLink					

2.18 GPIO List

Table 5 shows the SoC GPIO list.

Table 5. SoC GPIO Map

Feature	Peripheral Device	EVM Bd Net	Function	SoC GPIO
Connectivity on module	WiLink1873	BT_EN	BT_EN	GPIO1_24
Connectivity on module	WiLink1873	IRQ_GNSS	IRQ_GNSS	GPIO6_30
Connectivity on module	WiLink1873	GNSS_TIME_STAMP	GNSS_TIME_STAMP	GPIO6_28
Connectivity on module	WiLink1873	WLAN_IRQ	WLAN_IRQ	GPIO6_29
Connectivity on module	WiLink1873	WL_EN	WL_EN	GPIO1_25
Gig ethernet	Ethernet PHY(s)	ENET_INTSn	ENET_IRQ	GPIO2_22
FPD-Link panel	FPD-Link Txmt	VOUT3_INTB	FPDTX_IRQ	GPIO1_0
Power mgmt	TPS65919	H_PMIC_INTn	PMIC_IRQ	GPIO1_3
SD card	Micro-SD	MMC1_SDCD	CARD_DETECT	GPIO6_27
Test	Automated test	GPIO5_17	USER_DEFINED	GPIO5_0

NOTE: Functional signals of pin mux are not considered for Table 5; refer to the schematic for further details.

2.19 Configuration EEPROM

The CPU board contains two EEPROM memory devices (U22, U38) for storing and retrieving configuration information. The EEPROM provides 256Kb (or 32KBytes) of storage space, and is accessible through I2C. (Device location information is located in [Table 4](#).) The configuration ID information is programmed by the factory at time of manufacturing, and should not be altered. Below is the configuration data format within the EEPROM.

EEPROM device used: Catalyst Semiconductor CAT24C256WI-G

I2C bus/addr: I2C1,0x50

Data format of the EEPROM is provided in [Table 6](#).

Table 6. EEPROM Configuration

EEPROM Field	Byte Location	Value (Rev B CPU Board example)	Description
ID.HEADER	[3:0]	0xAA5533EE	Fixed value at start of header ID
ID.BOARD_NAME	[19:4]	"DRA71x_LCARD" (ascii)	For J6Entry reference low EVM – fixed value of 'DRA71x_LCARD'
ID.VERSION_MAJOR	[21:20]	0x2	A=0x1 B=0x2 C=0x3
ID.VERSION_MINOR	[23:22]	0x0	0x0 for major revision 0x1-0x15 for others
ID.CONFIG_OPTION	[27:24]	0x0E	Bit 6: 1 – EMIF2 ECC supported; 0 – No Bit 5: 1 – EMIF2 supported; 0 – No Bit 4: 1 – EMIF1 ECC supported; 0 – No Bit 3: 1 – EMIF1 supported; 0 – No Bit 2: 1 – Extended memory EEPROM cfg support; 0 – No ⁽¹⁾ Bit 1: 1 – MAC addr in EEPROM (default) Bit 0: 0 - QSPI (default), 1 - NOR
EMIF1_SIZE_BYTES	[31:28]	0x8000 0000	Memory size for EMIF1 in bytes (unsigned long)**
EMIF2_SIZE_BYTES	[35:32]	0x0000 0000	Memory size for EMIF2 in bytes (unsigned long)**
RESERVED	[55:36]	0x0	Reserved**
MAC_ADDR	0x7F00	00.0E.99.zz.yy.xx	Optional MAC address

⁽¹⁾ If bit 2 set to 0, all EEPROM data beyond is set to 0 (not defined or used). If set to 1, the mapping is per the table.

For reference, a C-style coded structure is provided:

```
Struct EEPROM_ID_T
{
    Unsigned long header;          4
    Char board_name[16];          16
    Unsigned short version_major;  2
    Unsigned short version_minor;  2
    Unsigned long config_option;   4
    Unsigned long emif1_size_bytes; 4
    Unsigned long emif2_size_bytes; 4
    Char reserved[28];            20
} eeprom_id;
```

3 Signal Multiplex Logic

3.1 MMC1 Selection (Mux A)

An active multiplexer is used on MMC1 to select between using the SD card slot or the WiLink module. Both features cannot be used simultaneously. When using these features, ensure that the PMIC LDO1_OUT is set to the right output voltage, or there is a risk of damaging parts. The default upon powering ON is using the SD card for booting. WiLink should be held in reset when using this feature. The default for the LDO1_OUT is 3.3 V. If the WiLink feature is to be used, the voltage must be set to 1.8-V output on LDO1_OUT. To change the output voltage of LDO1_OUT, PIN 16, PMIC must be updated to set LDO1 to 1.8 V. [Table 7](#) lists the proper functions.

Table 7. PMIC Boot Pin Functions

PIN #	Value	Function
16(BOOT)	Low	LDO1_OUT = 1.8 V
	High	LDO1_OUT = Bypass (assumes 3.3 V on LDO12_IN) (default)

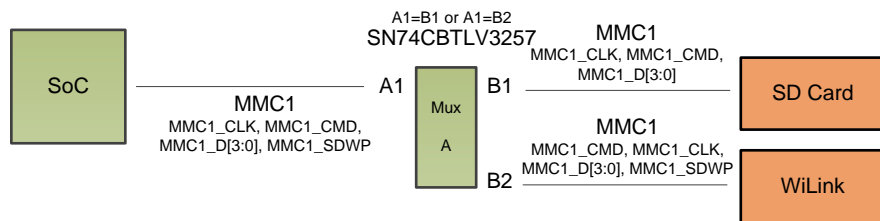
The default setting of the mux is to route MMC1 to the SD card by using the Select bit of the mux. The Select bit, by default, is pulled low by the pull-down resistor, but can be overridden by driving Ball N2 on the SoC HIGH. [Table 8](#) lists the control bit values and the appropriate mux settings.

Table 8. Mux Settings

MUX	Control Bit	Value	Mux Setting
A (RU1, RU2)	N2(GPIO5_26)	0	Route to SD card (MMC1) (default)
		1	Route to WiLink (MMC1)

Mux A: Selects between the SD card and WiLink support.

NOTE: MMC1 is routed to both features; however, both cannot be used simultaneously. Ensure the LDO voltage is set to the right voltage as mentioned earlier.



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Figure 8. Mux Diagram for SD Card/WiLink

4 Test Automation

The design has support for automated testing. J21 is the connector for the testing system. When using the automated testing, all the boot switches from SW1 must be set to OFF so that the automation can override the defaults. [Table 9](#) lists the functions of the pins in the connector. The connector is a FH12A-40S-0.5SH(55). The cable that fits in the connector is Parlex-050R40-76B, .5mm 3".

Table 9. Automated Test Mapping

PIN Number	Net Name	Function	PIN Map
1,2,3	VIO_3V3	Power	VDDSHV1/3/4/9/10
7,16,25,34, 40,41,42	GND	Ground	GND
8	VOOUT3B_D0	SYSBOOT0	GPMC_AD0
9	VOOUT3B_D1	SYSBOOT1	GPMC_AD1
10	VOOUT3B_D2	SYSBOOT2	GPMC_AD2
11	VOOUT3B_D3	SYSBOOT3	GPMC_AD3
12	VOOUT3B_D4	SYSBOOT4	GPMC_AD4
13	VOOUT3B_D5	SYSBOOT5	GPMC_AD5
26	PM_BRD_PWR_OFF	Power board off	To PMIC_EN
28	PM_RESETh	Reset into SoC	RESETh
29	H_RSTOUTH	Reset out from SoC	RSTOUTH
32	H_GPIOS_17	General Purpose I/O	RMII_MHZ_50_CLK
36	PM1_SCL	I2C SCL	N/A
38	PM1_SDA	I2C SDA	N/A

The automation header has a provision to monitor the system power. The measurement system is implemented using the TI INA226 I2C current/shunt power monitors. The INA226 device monitors both power supply voltage and shunt current measurements. Information is connected from the INA226 devices using a dedicated I2C bus. The INA226 can be controlled through an off-board module used for the automated testing.

[Table 10](#) shows the mapping of the INA226.

Table 10. Power Measurement System

I2C Addr	Power Net	Shunt/Resistor	Description
0x40	VBAT_PM	10m-Ω	VBAT input

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