OMAP5910 Dual-Core Processor Multichannel Buffered Serial Port (McBSP) Reference Guide

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Preface

Read This First

About This Manual

This document describes the three configurable McBSPs found on the OMAP5910 device.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

The following documents describe the OMAP5910 device and related peripherals. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

OMAP5910 Dual-Core Processor MPU Subsystem Reference Guide (literature number SPRU671)

OMAP5910 Dual-Core Processor DSP Subsystem Reference Guide (literature number SPRU672)

OMAP5910 Dual-Core Processor Memory Interface Traffic Controller Reference Guide (literature number SPRU673)

OMAP5910 Dual-Core Processor System DMA Controller Reference Guide (literature number SPRU674)

OMAP5910 Dual-Core Processor LCD Controller Reference Guide (literature number SPRU675)

OMAP5910 Dual-Core Processor Universal Asynchronous Receiver/Transmitter (UART) Devices Reference Guide (literature number SPRU676)

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OMAP5910 Dual-Core Processor Clock Generation and System Reset Management Reference Guide (literature number SPRU678)

OMAP5910 Dual-Core Processor General-Purpose Input/Output (GPIO) Reference Guide (literature number SPRU679)

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OMAP5910 Dual-Core Processor Inter-Integrated Circuit (I2C) Controller Reference Guide (literature number SPRU681)

OMAP5910 Dual-Core Processor Timer Reference Guide (literature number SPRU682)

OMAP5910 Dual-Core Processor Inter-Processor Communication Reference Guide (literature number SPRU683)

OMAP5910 Dual-Core Processor Camera Interface Reference Guide (literature number SPRU684)

OMAP5905 Dual-Core Processor Multichannel Serial Interface (MCSI) Reference Guide (literature number SPRU685)

OMAP5910 Dual-Core Processor Micro-Wire Interface Reference Guide (literature number SPRU686)

OMAP5910 Dual-Core Processor Real-Time Clock (RTC) Reference Guide (literature number SPRU687)

OMAP5910 Dual-Core Processor HDQ/1-Wire Interface Reference Guide (literature number SPRU688)

OMAP5910 Dual-Core Processor PWL, PWT, and LED Peripheral Reference Guide (literature number SPRU689)

OMAP5910 Dual-Core Processor Multichannel Buffered Serial Port (McBSP) Reference Guide (literature number SPRU708)

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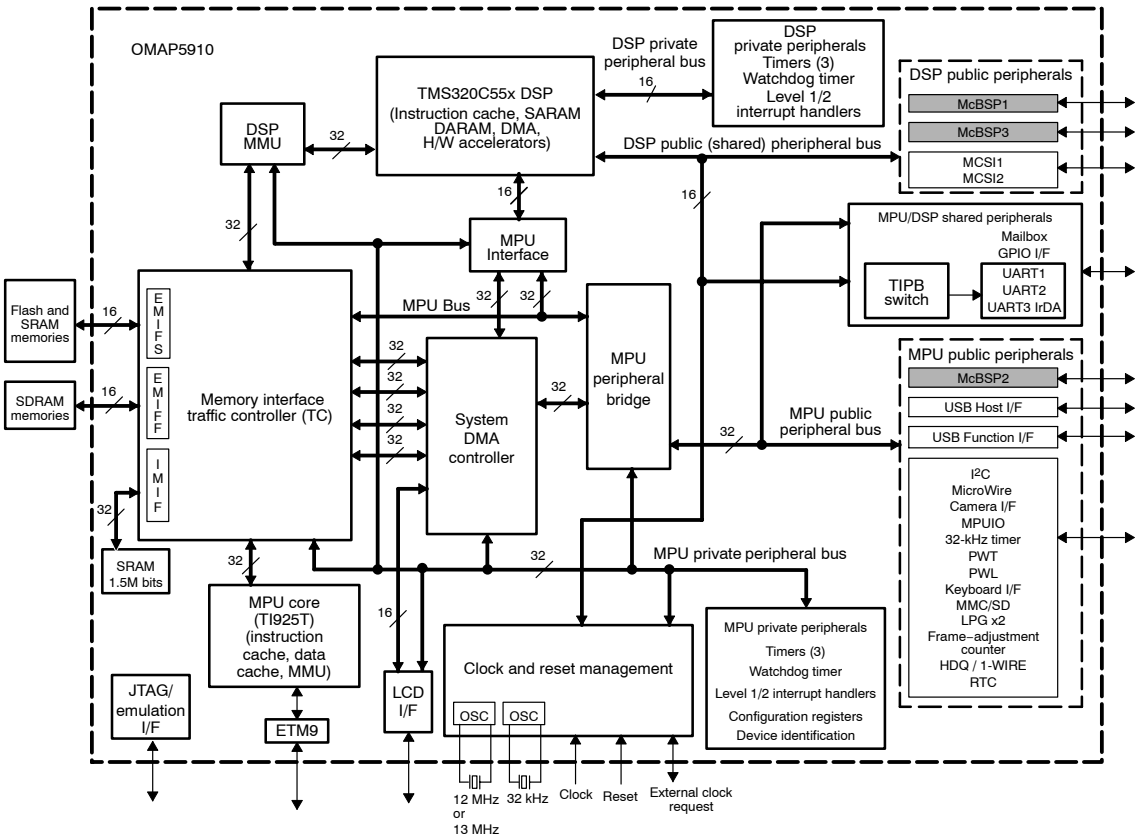
Multichannel Buffered Serial Port (McBSP)

1 Introduction

Multichannel buffered serial ports (McBSPs) are configurable, high-speed, full-duplex serial ports that allow direct interface to external communication devices. The OMAP5910 device has three McBSPs; McBSP1 and McBSP3 are on the DSP public peripheral bus, and McBSP2 is on the MPU public peripheral bus.

Figure 1 shows the OMAP5910 device with the McBSPs highlighted.

Figure 1. Highlight of McBSPs



2 McBSP Features

The key features of the McBSPs include:

- Full-duplex communication
- DMA support for both RX and TX transfers
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receives and transmits
- External shift clock generation or an internal programmable frequency shift clock
- Multichannel transmits and receives of up to 128 channels
- A wide selection of data sizes, including 8-, 12-, 16-, 20-, 24-, or 32-bits
- μ-Law and A-Law companding
- Data transfers with the LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Supports bit rates up to 25M bits/second
- RX and TX interrupts as well as RX data overrun interrupt

For a detailed description of the functionality of all three McBSPs, see SPRU592, *TMS320VC5501/5502/5509/5510 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide*. The operation of the OMAP5910 McBSPs is consistent with the description in SPRU592, with the following exceptions and clarifications:

- Only the DXENA = 0 setting is supported.
- The transmit output (DX) pins do not go to high impedance when the transmitter is not actively sending data. In other words, the OMAP5910 device always actively drives the DX pins.
- The CLKS input is only available on McBSP1.
- The receiver can only operate in the slave mode on McBSP1 and McBSP3.

3 McBSP1

This section provides information specific to the McBSP1 of the OMAP5910 device.

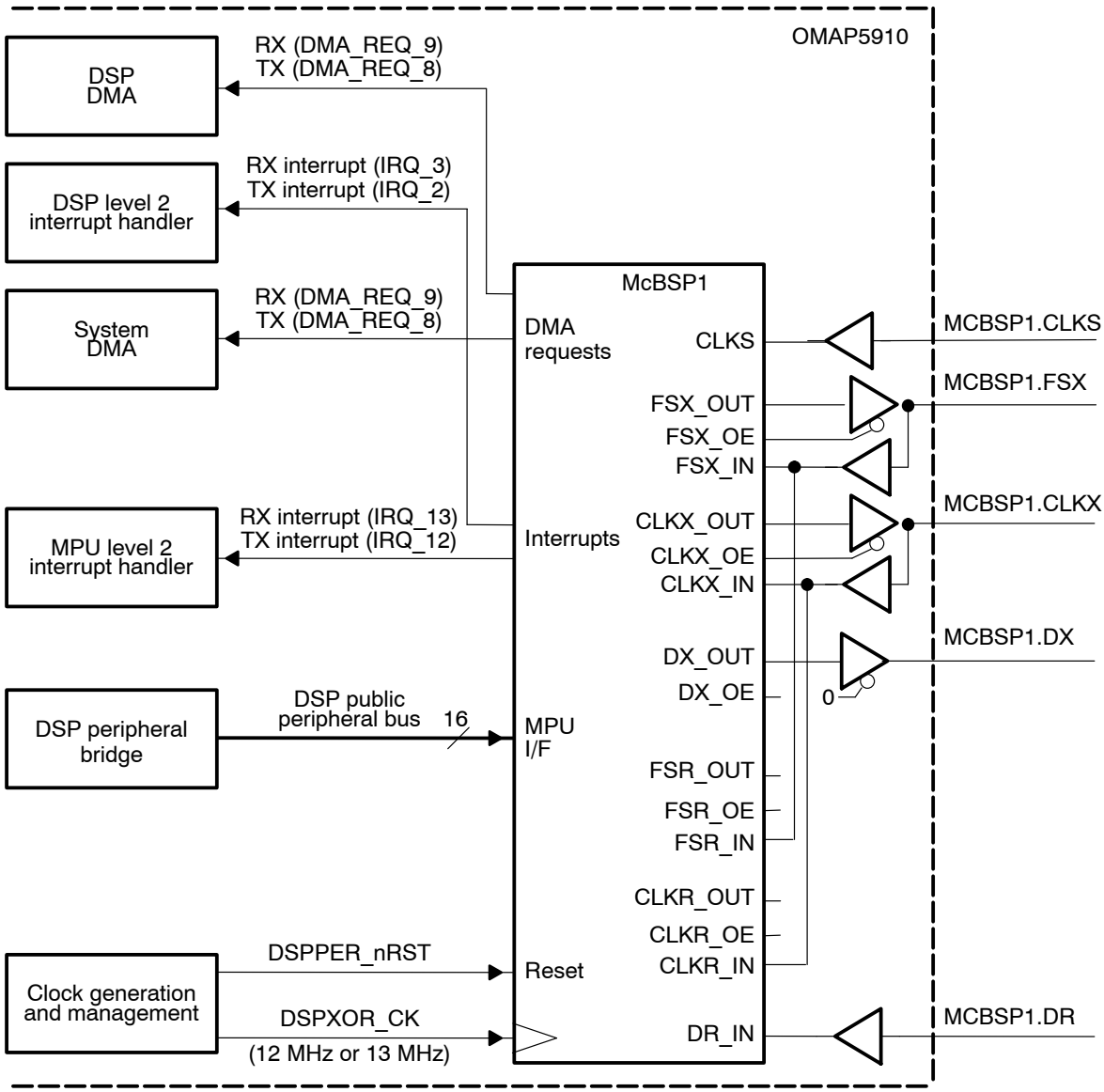
3.1 McBSP1 Pin Descriptions

Table 1 identifies the McBSP1 I/O pins.

Table 1. McBSP1 Pin Descriptions

Pin	I/O Direction	Description
MCBSP1.CLKS	In	Clock input
MCBSP1.DR	In	Data input
MCBSP1.DX	Out	Data output
MCBSP1.CLKX	In/out	Bit clock
MCBSP1.FSX	In/out	Frame synchronization

Figure 2. McBSP1-Interface Diagram



Note: The AUXON feature can be used to disable the functional clock to the McBSP1 module by setting MOD_CONF_CTRL_0[18] (CONF_MOD_MCBSP1_AUXON) to 1.

The McBSP1 is: half duplex master/slave for transmission, and half-duplexslave for reception. Table 2 lists the McBSP1 signals that are available at the OMAP5910 level

Table 2. Available McBSP1 Signals

Generic McBSP Signal Name	Description	McBSP1 Signal Name
FSX2	Transmission frame (bidirectional)	McBSP1.FSX
CLKX	Transmission clock (bidirectional)	McBSP1.CLKX
DX	Transmit data (output only)	McBSP1.DX
FSR	Receive frame (input only)	Not available (internal feedback from CLKX)
DR	Receive data	McBSP1.DR
CLKS	Clock input	McBSP1.CLKS

3.2 McBSP1 Interrupt Mapping

Table 3 identifies the McBSP1 interrupts. McBSP1 generates level 2 interrupts for both the DSP and the MPU.

Table 3. McBSP1 Interrupt Mapping

Incoming Interrupts	Level 2 DSP Interrupt	Level 2 MPU Interrupt
McBSP1 TX interrupt	IRQ_02	IRQ_12
McBSP1 RX interrupt	IRQ_03	IRQ_13

3.3 McBSP1 DMA Request Mapping

Table 4 identifies McBSP1 DMA request lines.

Table 4. DMA Request Mapping—McBSP1

DMA Request Source	DMA Request Line—DSP	System DMA Request Line—MPU
McBSP1 TX	DMA_REQ_08	DMA_REQ_08
McBSP1 RX	DMA_REQ_09	DMA_REQ_09

The McBSP1 registers are shown in Table 5.

Table 5. McBSP1 Registers

DSP Word Address	MPU Byte Address (VIA MPUI)	Register Name	Description	Access Width	Access Type	Reset Value
0x00 8C00h	E101:1800	MCBSP1_DRR2	McBSP1 data receive register 2	16	RW	0000h
0x00 8C01h	E101:1802	MCBSP1_DRR1	McBSP1 data receive register 1	16	RW	0000h
0x00 8C02h	E101:1804	MCBSP1_DXR2	McBSP1 data transmit register 2	16	RW	0000h
0x00 8C03h	E101:1806	MCBSP1_DXR1	McBSP1 data transmit register 1	16	RW	0000h
0x00 8C04h	E101:1808	MCBSP1_SPCR2	McBSP1 serial port control register 2	16	RW	0000h
0x00 8C05h	E101:180A	MCBSP1_SPCR1	McBSP1 serial port control register 1	16	RW	0000h
0x00 8C06h	E101:180C	MCBSP1_RCR2	McBSP1 receive control register 2	16	RW	0000h
0x00 8C07h	E101:180E	MCBSP1_RCR1	McBSP1 receive control register 1	16	RW	0000h
0x00 8C08h	E101:1810	MCBSP1_XCR2	McBSP1 transmit control register 2	16	RW	0000h
0x00 8C09h	E101:1812	MCBSP1_XCR1	McBSP1 transmit control register 1	16	RW	0000h
0x00 8C0Ah	E101:1814	MCBSP1_SRGR2	McBSP1 sample rate generator register 2	16	RW	2000h
0x00 8C0Bh	E101:1816	MCBSP1_SRGR1	McBSP1 sample rate generator register 1	16	RW	0001h
0x00 8C0Ch	E101:1818	MCBSP1_MCR2	McBSP1 multichannel control register 2	16	RW	0000h
0x00 8C0Dh	E101:181A	MCBSP1_MCR1	McBSP1 multichannel control register 1	16	RW	0000h
0x00 8C0Eh	E101:181C	MCBSP1_RCERA	McBSP1 receive channel enable register partition A	16	RW	0000h

Table 5. McBSP1 Registers (Continued)

DSP Word Address	MPU Byte Address (VIA MPUI)	Register Name	Description	Access Width	Access Type	Reset Value
0x00 8C0Fh	E101:181E	MCBSP1_RCERB	McBSP1 receive channel enable register partition B	16	RW	0000h
0x00 8C10h	E101:1820	MCBSP1_XCERA	McBSP1 transmit channel enable register partition A	16	RW	0000h
0x00 8C11h	E101:1822	MCBSP1_XCERB	McBSP1 transmit channel enable register partition B	16	RW	0000h
0x00 8C12h	E101:1824	MCBSP1_PCR0	McBSP1 pin control register 0	16	RW	0000h
0x00 8C13h	E101:1826	MCBSP1_RCERC	McBSP1 receive channel enable register partition C	16	RW	0000h
0x00 8C14h	E101:1828	MCBSP1_RCERD	McBSP1 receive channel enable register partition D	16	RW	0000h
0x00 8C15h	E101:182A	MCBSP1_XCERC	McBSP1 transmit channel enable register partition C	16	RW	0000h
0x00 8C16h	E101:182C	MCBSP1_XCERD	McBSP1 transmit channel enable register partition D	16	RW	0000h
0x00 8C17h	E101:182E	MCBSP1_RCERE	McBSP1 receive channel enable register partition E	16	RW	0000h
0x00 8C18h	E101:1830	MCBSP1_RCERF	McBSP1 receive channel enable register partition F	16	RW	0000h
0x00 8C19h	E101:1832	MCBSP1_XCERE	McBSP1 transmit channel enable register partition E	16	RW	0000h
0x00 8C1Ah	E101:1834	MCBSP1_XCERF	McBSP1 transmit channel enable register partition F	16	RW	0000h
0x00 8C1Bh	E101:1836	MCBSP1_RCERG	McBSP1 receive channel enable register partition G	16	RW	0000h
0x00 8C1Ch	E101:1838	MCBSP1_RCERH	McBSP1 receive channel enable register partition H	16	RW	0000h
0x00 8C1Dh	E101:183A	MCBSP1_XCERG	McBSP1 transmit channel enable register partition G	16	RW	0000h

Table 5. McBSP1 Registers (Continued)

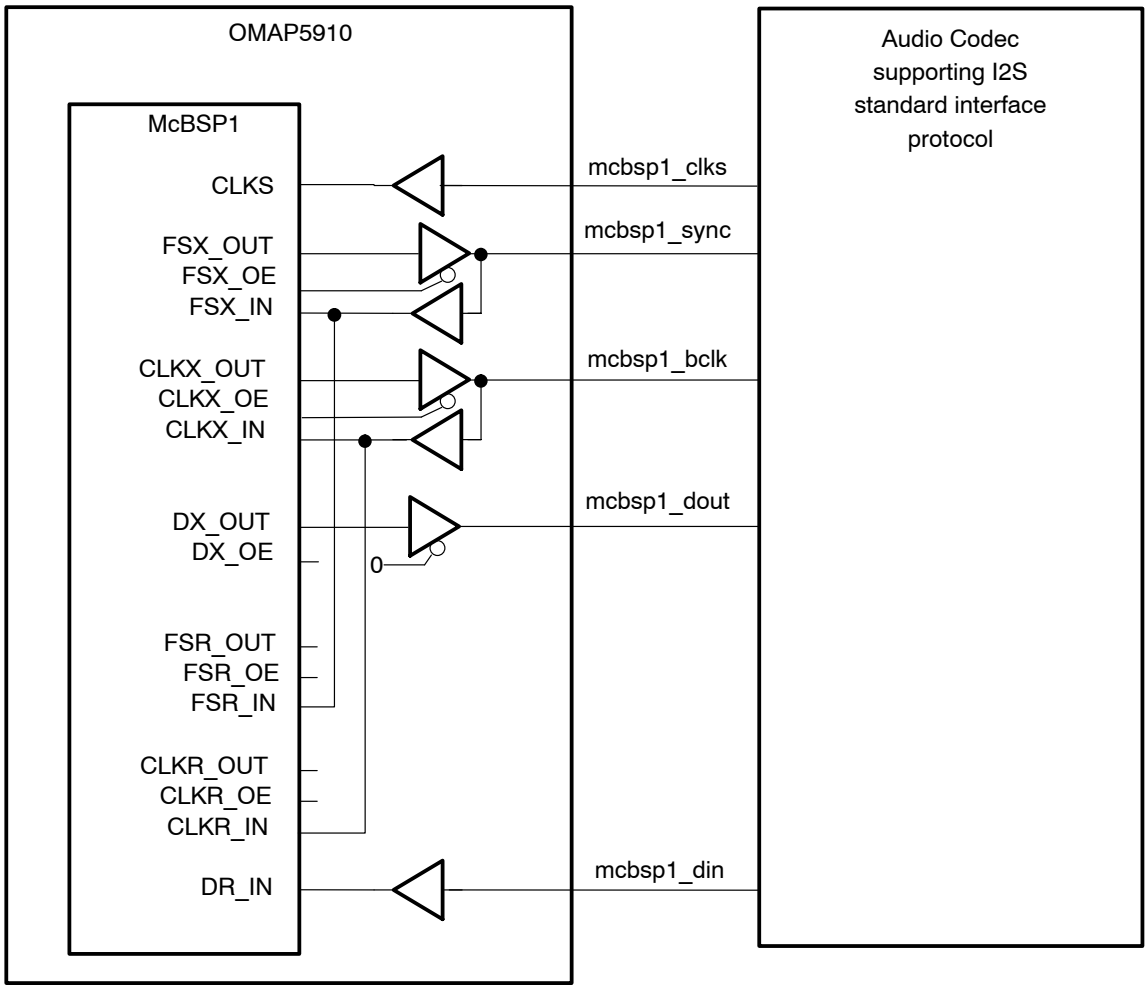
DSP Word Address	MPU Byte Address (VIA MPUI)	Register Name	Description	Access Width	Access Type	Reset Value
0x00 8C1Eh	E101:183C	MCBSP1_XCERH	McBSP1 transmit channel enable register partition H	16	RW	0000h

3.4 McBSP1 Application Example: I2S Interface

This application uses McBSP1 as an I2S audio codec interface (see Figure 3). The OMAP5910 is intended to be either the master or slave device; that is, it either receives or provides the frame synchronization and bit clock.

Section 3.4.1 through Section 3.4.9 explain how to set up the McBSP registers for I2S slave mode with 16-bit transfers using DMA support.

Figure 3. I2S Audio Codec Interface



3.4.1 Serial-Port-Control-Register Configuration

DSP_Write(0x0000) => SPCR1; set up the SPCR1 as the initial configuration.

DSP_Write(0x0000) => SPCR2; set up the SPCR2 as the initial configuration.

3.4.2 Pin-Control-Register Configuration

DSP_Write(0x0000) => PCR; set up the PCR as shown in Table 6.

Table 6. Pin-Control-Register-Configuration (DSP_Write(0x0000) => PCR)

Bits	Config Value	Description
15-14	00b	Reserved
13	0b	Set the serial port mode for the DX, FSX and CLKX pins
12	0b	Set the serial port mode for the DR, FSR and CLKR pins
11	0b	TX frame-synchronization signal is derived by the external source
10	0b	RX frame-synchronization signal is derived by the external source
9	0b	CLKX set input pin and derived by the external source
8	0b	CLKR set input pin and derived by the external source
7	0b	Sample rate generator input clock mode bit
6	0b	CLKS pin status (only valid for McBSP1 on OMAP5910)
5	0b	DX pin status
4	0b	DR pin status
3	0b	Set the FSX polarity as active high
2	0b	Set the FSR polarity as active high
1	0b	Set the CLKX polarity as data driven on a rising edge
0	0b	Set the CLKR polarity as data sampled on a falling edge

3.4.3 Receive-Control-Register Configuration

DSP_Write(0x00a0) => RCR1; set up the RCR1 as shown in Table 7.

Table 7. Receive-Control-Register-1 Configuration (DSP_Write(0x00a0) => RCR1)

Bit	Config Value	Description
15	0b	Reserved
14-8	000 0000b	Set the receive frame length as one word per frame
7-5	101b	Set the receive word length as 32 bits per frame
4-0	0 0000b	Reserved

DSP_Write(0x80a1) => RCR2; set up the RCR2 as shown in Table 8.

Table 8. Receive-Control-Register-2 Configuration (DSP_Write(0x80a1) => RCR2)

Bit	Config Value	Description
15	1b	Set to dual-phase frame
14-8	000 0000b	Set the receive frame length as one word per frame
7-5	101b	Set the receive word length as 32 bits per frame
4-3	00b	Don’t care for single-phase frame
2	0b	Setting the FSR to not ignore after the first receive frame synchronization pulse resets the transfer.
1-0	01b	Set the data delay as 1 bit

3.4.4 Transmit-Control-Register Configuration

DSP_Write(0x00a0) => XCR1; set up the XCR1 as shown in Table 9.

Table 9. Transmit-Control-Register-1 Configuration (DSP_Write(0x00a0) => XCR1)

Bit	Config Value	Description
15	0b	Reserved
14-8	000 0000b	Set the transmit frame length as one word per frame
7-5	101b	Set the receive word length as 32 bits per frame
4-0	0 0000b	Reserved

DSP_Write(0x80a1) => XCR2; set up the XCR2 as shown in Table 10.

Table 10. Transmit-Control-Register-2 Configuration (DSP_Write(0x80a1) => XCR2)

Bit	Config Value	Description
15	1b	Set to dual-phase frame
14-8	000 0000b	Don't care for single-phase frame
7-5	101b	Set the receive word length as 32 bits per frame
4:3	00b	Set to no companding data and transfer starting with the MSB first
2	0b	Setting the FSX to not ignore after the first transmit frame synchronization pulse resets the transfer.
1:0	01b	Set the data delay as 1 bit

3.4.5 Sample-Rate-Generator Configuration (SRGR[1,2])

It is not necessary to configure the sample-rate generator because the external clocks and frames are provided appropriately for the CLKX and FSX.

3.4.6 DMA Configuration

It is necessary to configure the REVT and XEVT bit for the DMA receive and transmit synchronized event.

3.4.7 Interrupt Flag Configuration and Clear (ILR, MIR)

1) DSP_Write => ILR; set the ILR appropriately for the interrupt handling priority.

2) DSP_Write (MIR or (0x0000 0000c)) => MIR; disables the McBSP1 TX and RX interrupt.

Note:

Enable the appropriate DMA channel interrupts.

3.4.8 Enable McBSP1 Transmit and Receive (SPCR[1,2])

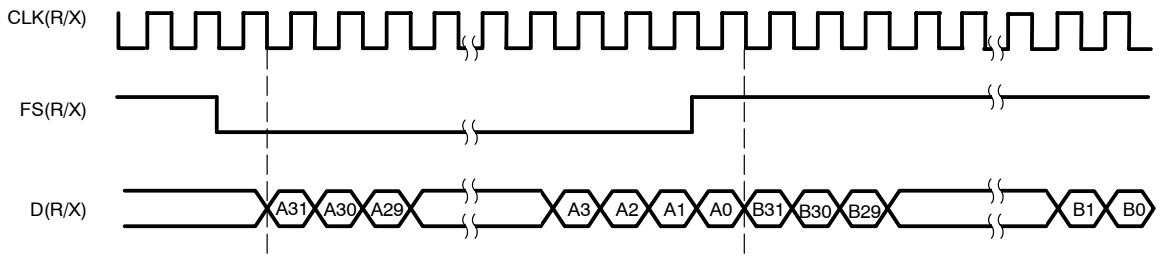
1) DSP_write (SPCR1 or (0x0001)) => SPCR1; enables the receive port

2) DSP_write (SPCR2 or (0x0001)) => SPCR2; enables the transmit port

3.4.9 Data Transfer (DMA channel)

The DMA channel transfers the received data to the appropriate data buffer and transfers the newly transmitted data to the appropriate TX buffer. The interrupt flag on the ITR is cleared when the interrupt handle is taken.

Figure 4. Waveform Example



4 McBSP3

This section provides information specific to McBSP3 on the OMAP5910 device.

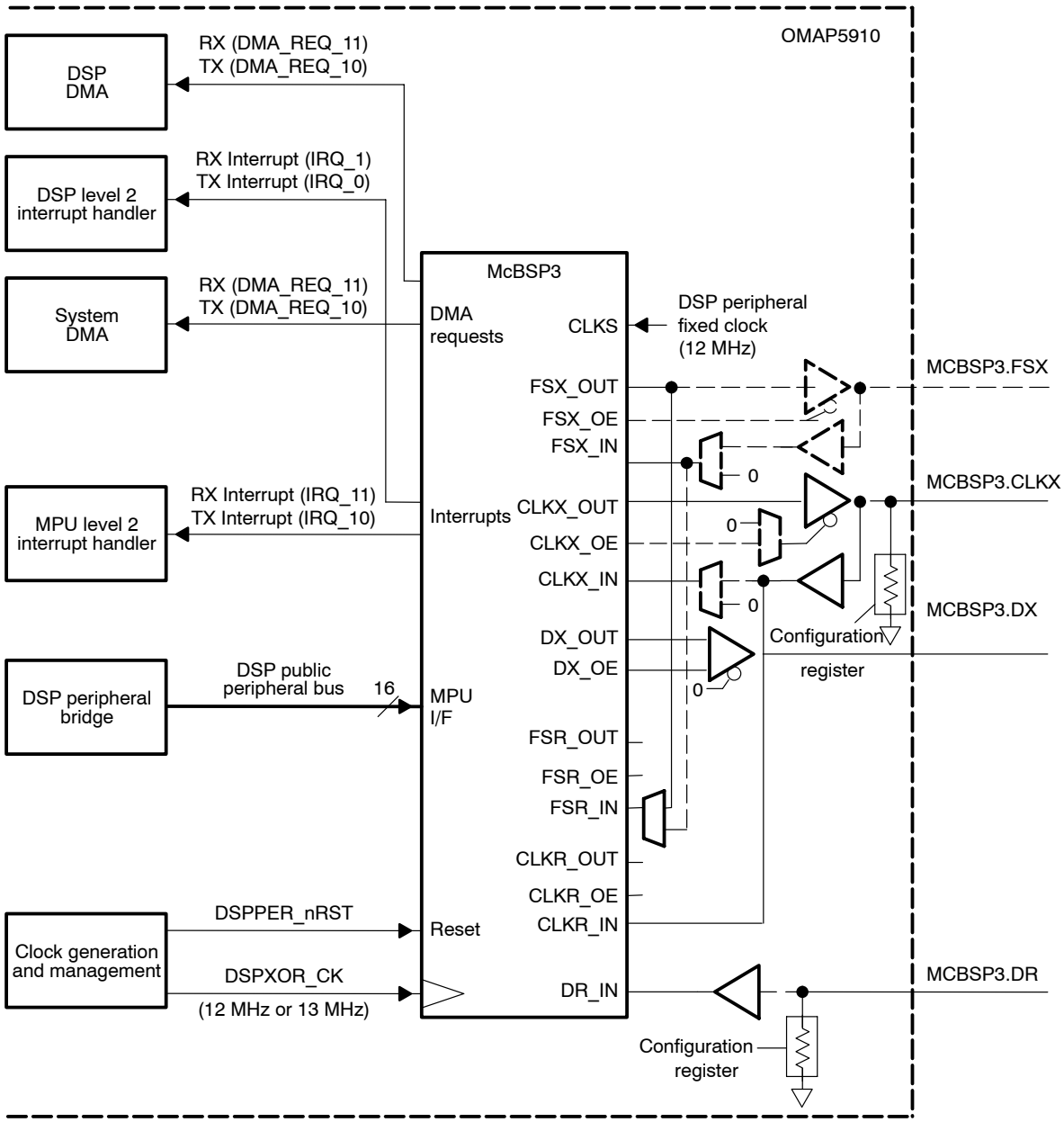
4.1 McBSP3 Pin Descriptions

Table 11 identifies the McBSP3 I/O pins.

Table 11. McBSP3 Pin Descriptions

Pin	I/O Direction	Description
MCBSP3.DR	In	Data input
MCBSP3.DX	Out	Data output
MCBSP3.CLKX	In/out	Bit clock
MCBSP3.FSX	In/out	Frame synchronization

Figure 5. McBSP3 Interface Diagram



Note: The AUXON feature can be used to gate the functional clock to the McBSP3 module by setting the MOD_CONF_CTRL_0[20] (CONF_MOD_MCBSP3_AUXON) to 1.

There are two modes for the McBSP3, which are selected by the bit 28, MOD_MCBSP3_MODE_R, of the MOD_CONF_CTRL_0 register:

- MOD_MCBSP3_MODE_R = 0 (default). In this case, the McBSP3 is: half duplex master for transmission, and half-duplex slave for reception. The paths shown as dashed lines in Figure 5 are not available in this mode. Table 12 lists the McBSP3 signals available in this mode at the OMAP5910 pins.

Table 12. McBSP3 Signals Available at Pins in R = 0 Mode

Generic McBSP Signal Name	Description	McBSP3 Pin Name
FSX	Transmission frame (output only)	Not available
CLKX	Transmission clock (output only)	McBSP3.CLKX
DX	Transmit data (output only)	McBSP3.DX
FSR	Receive frame (input only)	Not available (internal feedback from the FSX)
CLKR	Receive clock (input only)	Not available (internal feedback from the FSX)
DR	Receive data	McBSP3.DR

- MOD_MCBSP3_MODE_R = 1. In this case, the McBSP3 is: half duplex master/slave for transmission, and half-duplex slave for reception. This mode utilizes the paths shown as dashed lines in Figure 5. Table 13 lists the McBSP3 signals available in this mode at the OMAP5910 pins.

Table 13. McBSP3 Signals Available at Pins in R = 1 Mode

Generic McBSP Signal Name	Description	McBSP3 Pin Name
FSX	Transmission frame (bidirectional)	McBSP3.FSX (multiplexed on another pad)
CLKX	Transmission clock (bidirectional)	McBSP3.CLKX
DX	Transmit data (output only)	McBSP3.DX
FSR	Receive frame (input only)	Not available (internal feedback from the FSX)
CLKR	Receive clock (input only)	Not available (internal feedback from the CLXX)
DR	Receive data	McBSP3.DR

4.2 McBSP3 Interrupt Mapping

Table 14 identifies the McBSP3 interrupts. McBSP3 generates level 2 interrupts for both the DSP and the MPU.

Table 14. McBSP3 Interrupt Mapping

Incoming Interrupts	Level 2 DSP Interrupt	Level 2 MPU Interrupt
McBSP3 TX interrupt	IRQ_00	IRQ_10
McBSP3 RX interrupt	IRQ_01	IRQ_11

4.3 McBSP3 DMA Request Mapping

Table 15 identifies McBSP3 DMA request lines.

Table 15. DMA Request Mapping—McBSP3

DMA Request Source	DMA Request Line—DSP	System DMA Request Line—MPU
McBSP3 TX	DMA_REQ_10	DMA_REQ_10
McBSP3 RX	DMA_REQ_11	DMA_REQ_11

The McBSP3 registers are shown in Table 16.

Table 16. McBSP3 Registers

DSP Word Address	MPU Byte Address (VIA MPUI)	Register Name	Description	Access Width	Access Type	Reset Value
0x00 B800h	E101:7000	MCBSP3_DRR2	McBSP3 data receive register 2	16	RW	0000h
0x00 B801h	E101:7002	MCBSP3_DRR1	McBSP3 data receive register 1	16	RW	0000h
0x00 B802h	E101:7004	MCBSP3_DXR2	McBSP3 data transmit register 2	16	RW	0000h

Table 16. McBSP3 Registers (Continued)

DSP Word Address	MPU Byte Address (VIA MPUI)	Register Name	Description	Access Width	Access Type	Reset Value
0x00 B803h	E101:7006	MCBSP3_DXR1	McBSP3 data transmit register 1	16	RW	0000h
0x00 B804h	E101:7008	MCBSP3_SPCR2	McBSP3 serial port control register 2	16	RW	0000h
0x00 B805h	E101:700A	MCBSP3_SPCR1	McBSP3 serial port control register 1	16	RW	0000h
0x00 B806h	E101:700C	MCBSP3_RCR2	McBSP3 receive control register 2	16	RW	0000h
0x00 B807h	E101:700E	MCBSP3_RCR1	McBSP3 receive control register 1	16	RW	0000h
0x00 B808h	E101:7010	MCBSP3_XCR2	McBSP3 transmit control register 2	16	RW	0000h
0x00 B809h	E101:7012	MCBSP3_XCR1	McBSP3 transmit control register 1	16	RW	0000h
0x00 B80Ah	E101:7014	MCBSP3_SRGR2	McBSP3 sample rate generator register 2	16	RW	2000h
0x00 B80Bh	E101:7016	MCBSP3_SRGR1	McBSP3 sample rate generator register 1	16	RW	0001h
0x00 B80Ch	E101:7018	MCBSP3_MCR2	McBSP3 multichannel control register 2	16	RW	0000h
0x00 B80Dh	E101:701A	MCBSP3_MCR1	McBSP3 multichannel control register 1	16	RW	0000h
0x00 B80Eh	E101:701C	MCBSP3_RCERA	McBSP3 receive channel enable register partition A		RW	0000h
0x00 B80Fh	E101:701E	MCBSP3_RCERB	McBSP3 receive channel enable register partition B	16	RW	0000h
0x00 B810h	E101:7020	MCBSP3_XCERA	McBSP3 transmit channel enable register partition A	16	RW	0000h

Table 16. McBSP3 Registers (Continued)

DSP Word Address	MPU Byte Address (VIA MPUI)	Register Name	Description	Access Width	Access Type	Reset Value
0x00 B811h	E101:7022	MCBSP3_XCERB	McBSP3 transmit channel enable register partition B	16	RW	0000h
0x00 B812h	E101:7024	MCBSP3_PCR0	McBSP3 pin control register 0	16	RW	0000h
0x00 B813h	E101:7026	MCBSP3_RCERC	McBSP3 receive channel enable register partition C	16	RW	0000h
0x00 B814h	E101:7028	MCBSP3_RCERD	McBSP3 receive channel enable register partition D	16	RW	0000h
0x00 B815h	E101:702A	MCBSP3_XCERC	McBSP3 transmit channel enable register partition C	16	RW	0000h
0x00 B816h	E101:702C	MCBSP3_XCERD	McBSP3 transmit channel enable register partition D	16	RW	0000h
0x00 B817h	E101:702E	MCBSP3_RCERE	McBSP3 receive channel enable register partition E	16	RW	0000h
0x00 B818h	E101:7030	MCBSP3_RCERF	McBSP3 receive channel enable register partition F	16	RW	0000h
0x00 B819h	E101:7032	MCBSP3_XCERE	McBSP3 transmit channel enable register partition E	16	RW	0000h
0x00 B81Ah	E101:7034	MCBSP3_XCERF	McBSP3 transmit channel enable register partition F	16	RW	0000h
0x00 B81Bh	E101:7036	MCBSP3_RCERG	McBSP3 receive channel enable register partition G	16	RW	0000h
0x00 B81Ch	E101:7038	MCBSP3_RCERH	McBSP3 receive channel enable register partition H	16	RW	0000h

Table 16. McBSP3 Registers (Continued)

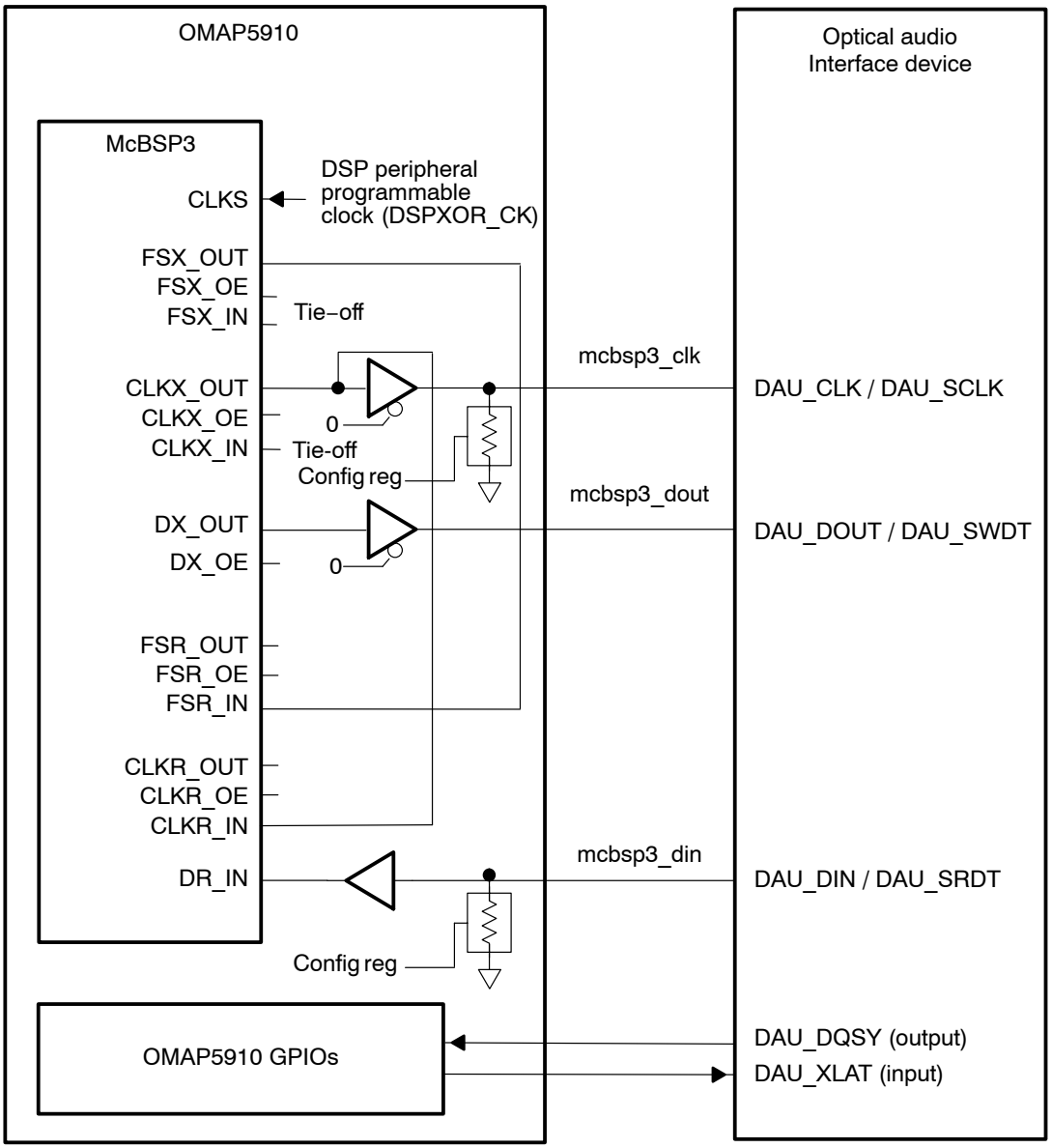
DSP Word Address	MPU Byte Address (VIA MPUI)	Register Name	Description	Access Width	Access Type	Reset Value
0x00 B81Dh	E101:703A	MCBSP3_XCERG	McBSP3 transmit channel enable register partition G	16	RW	0000h
0x00 B81Eh	E101:703C	MCBSP3_XCERH	McBSP3 transmit channel enable register partition H	16	RW	0000h

4.4 McBSP3 Application Example: Optical Interface

With the use of two GPIOs, the McBSP3 is configured to connect to an external optical audio interface (see Figure 6) device such as the Sanyo LC89051V.

Section 4.4.1 through Section 4.4.12 explain the McBSP register setup for an optical interface with an 8-bit transfer per frame in the SPI master mode and GPIO mode.

Figure 6. Optical Audio Interface



4.4.1 Serial-Port-Control-Register Configuration

DSP_Write(0x1000) => SPCR; set up the SPCR1 as shown in Table 17.

Table 17. Serial-Port-Control-Register Configuration (DSP_Write(0x1000) => SPCR)

Bits	Config Value	Description
15	0b	Disable the digital loopback mode
14-13	00b	Right-justify and zero-fill the MSBs in the DRR
12-11	10b	Enables the clock stop mode
10-8	000b	Reserved
7	0b	Turn off the DX enabler
6	0b	Reserved
5-4	00b	Set the RINT to be driven by the RRDY mode
3	0b	No synchronization error
2	0b	RBR is not in the overrun condition
1	0b	Receiver is not ready
0	0b	Disables the serial port receiver and places in reset state

DSP_Write(0x0000) => SPCR2; set up the SPCR2 as initial configuration.

4.4.2 Pin-Control-Register Configuration

DSP_Write(0x0a0b) => PCR; set up the PCR per below configuration.

Table 18. Pin-Control-Register Configuration (DSP_Write(0x0a0b) => PCR)

Bits	Config Value	Description
15-4	00b	Reserved
13	0b	Set the serial port mode for the DX, FSX and CLKX pins
12	0b	Set the serial port mode for the DR, FSR and CLKR pins
11	1b	TX frame-synchronization signal is driven by the internal generator
10	0b	RX frame-synchronization signal is derived by the external source
9	1b	McBSP is set as the master and generates a clock by the internal source
8	0b	CLKR sets the input pin and is derived by an external source

Table 18. Pin-Control-Register Configuration (DSP_Write(0x0a0b) => PCR) (Continued)

Bits	Config Value	Description
7	0b	Sample rate generator input clock mode bit
6	0b	CLKS pin status (no meaning in OMAP5910)
5	0b	DX pin status
4	0b	DR pin status
3	1b	Set the FSX polarity as active low
2	0b	Set the FSR polarity as active high
1	1b	Set the CLKX polarity as data driven on a falling edge
0	1b	Set the CLKR polarity as data sampled on a rising edge

4.4.3 Receive-Control-Register Configuration

The values of RWDLEN1, 2 and XWDLEN1, 2 must be set to the same value in the SPI mode.

DSP_Write(0x0000) => RCR1; set up the RCR1 per below configuration.

Table 19. Receive-Control-Register-1 Configuration (DSP_Write(0x0000) => RCR1)

Bits	Config Value	Description
15	0b	Reserved
14-8	000 0000b	Set the receive frame length as one word per frame
7-5	000b	Set the receive word length as 8 bits per frame
4-0	0 0000b	Reserved

DSP_Write(0x0000) => RCR2; set up the RCR2 as in the following configuration.

Table 20. Receive-Control-Register-2 Configuration (DSP_Write(0x0000) => RCR2)

Bits	Config Value	Description
15	0b	Set single-phase frame
14-8	000 0000b	Don’t care for single phase frame
7-5	000b	Don’t care for a single phase frame

Table 20. Receive-Control-Register-2 Configuration (DSP_Write(0x0000) => RCR2) (Continued)

Bits	Config Value	Description
4-3	00b	Set to no companding data and transfer starting with the MSB first
2	0b	Setting the FSR to not ignore after the first receive frame synchronization pulse resets the transfer
1-0	00b	Set the data delay as 0 bit

4.4.4 Transmit-Control-Register Configuration

The values of RWDLEN1, 2 and XWDLEN1, 2 must be set to the same value in the SPI mode.

DSP_Write(0x0000) => XCR1; set up the XCR1 as in the following configuration.

Table 21. Transmit-Control-Register-1 Configuration (DSP_Write(0x0000) => XCR1)

Bits	Config Value	Description
15	0b	Reserved
14-8	000 0000b	Set the transmit frame length as one word per frame
7-5	000b	Set the transmit word length as 8 bits per frame
4-0	0 0000b	Reserved

DSP_Write(0x0000) => XCR2; set up XCR2 per below configuration.

Table 22. Transmit-Control-Register-2 Configuration (DSP_Write(0x0000) => XCR2)

Bits	Config Value	Description
15	0b	Set single-phase frame
14-8	000 0000b	Don’t care for a single phase frame
7-5	000b	Don’t care for a single phase frame
4-3	00b	Set to no companding data and transfer starting with the MSB first
2	0b	Setting the FSX to not ignore after the first transmit frame synchronization pulse resets the transfer
1-0	00b	Set the data delay as 0 bit

4.4.5 Sample-Rate-Generator Configuration (SRGR[1,2])

DSP_Write (0x00FF) => SRGR1; set up the SRGR1 as shown in Table 23.

Table 23. Sample-Rate-Generator-1 Configuration (SRGR[1,2]) (DSP_Write (0x00FF) => SRGR1)

Bits	Config Value	Description
15-8	0000 0000b	These bits are ignored by the FSGM=0 (SRGR2[12:12])
7-0	1111 1111b	Set the sample rate generator clock divider

DSP_Write (0x2000) => SRGR2; set up the SRGR2 as shown in Table 24.

Table 24. Sample-Rate-Generator-2 Configuration (SRGR[1,2]) (DSP_Write (0x2000) => SRGR2)

Bits	Config Value	Description
15	0b	Set the sample rate generator clock synchronization
14	0b	Set the clock polarity
13	1b	Sample rate generator clock derived from the DSP clock
12	0b	Set frame-synchronization
11-0	0000 0000 0000b	These bits are ignored by the FSGM=0 (SRGR2[12:12])

Wait for two CLKSRG clock cycles.

4.4.6 Start-Sample-Rate Generator (SPCR2)

DSP_Write (SPCR2 or (0x0040)) => SPCR2; bring the sample rate generator out of reset.

Note:

Wait for two sample rate clock cycles for McBSP stability.

4.4.7 Interrupt Flag Configuration and Clear (ILR, ITR, MIR) on Level 2 Handler

1) DSP_Write => ILR; set ILR appropriately for the interrupt handling priority.
2) DSP_Write (ITR and (0xFFFF FFF3))=> ITR; clear the remaining TX and RX interrupts.
3) DSP_Write (MIR and (0xFFFF FFF3)) => MIR; enabled McBSP3 TX and RX interrupt.

4.4.8 Interrupt Flag Configuration MASK Release on Level 2 Handler

DSP_Write (IER0 or (0x0000 0008)) => IER0; enable INT3 (level 2 interrupt FIQ)

4.4.9 Enable McBSP3 Transmit and Receive (SPCR[1,2])

1) DSP_write (SPCR1 or (0x0001)) => SPCR1; enabled receive port
2) DSP_write (SPCR2 or (0x0001)) => SPCR2; enabled transmit port

Note:

Wait for two sample rate clock cycles for McBSP stability.

4.4.10 Transmit and Receive Data Loading (TX_INT and RX_INT Handling in Interrupt Service Routine)

For data transmit:

1) DSP_Write => DXR; transmit the data loading to the DXR
2) DSP_Read <= DRR; wait for the data read after the RINT

For two data words received:

1) DSP_Write => DXR; dummy write 0xFFFF for data received after the TINT
2) DSP_Read <= DRR; first data read after the RINT
3) DSP_Write => DXR; dummy write 0xFFFF for data received after the TINT
4) DSP_Read <= DRR; second data read after the RINT

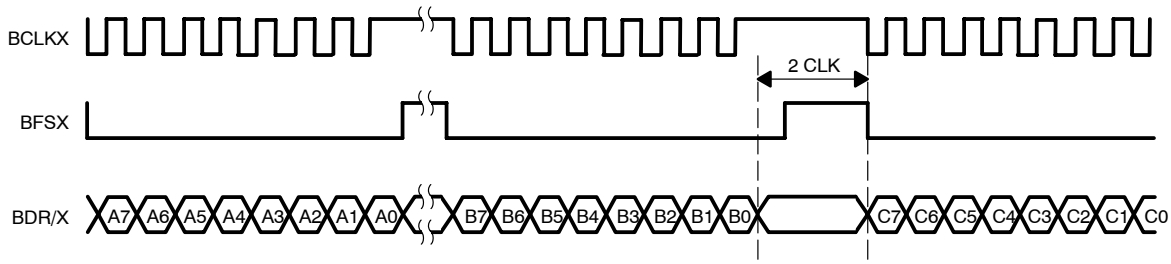
4.4.11 Register Setup for GPIO Mode

1) DSP_Write (SPCR1 and (0xFFFE)) => SPCR1; disabled receive port
2) DSP_Write (PCR or (0x1000)) => PCR; DR pin set as a general-purpose input (GPI)

4.4.12 Read From GPI

DSP_Read <= PCR; read the DR_STAT bit

Figure 7. Waveform Example



Section 4.4.13 through Section 4.4.18.3 explain the McBSP register setup for the TX master and RX slave with 8-bit data transfer using system DMA support.

4.4.13 Serial-Port-Control-Register Configuration

DSP_Write(0x1000) => SPCR1; set up the SPCR1 as shown in Table 25.

Table 25. Serial-Port-Control-Register Configuration (DSP_Write(0x1000) => SPCR1)

Bits	Config Value	Description
15	0b	Disables the digital loopback mode
14-13	00b	Right-justify and zero-fill the MSBs in the DRR
12-11	10b	Enables the clock stop mode
10-8	000b	Reserved
7	0b	Turns off the DX enabler
6	0b	Reserved
5-4	00b	Set the RINT driven by the RRDY mode
3	0b	No synchronization error
2	0b	RBR is not in overrun condition.
1	0b	Receiver is not ready.
0	0b	Disables the serial port receiver and in reset state

DSP_Write(0x0000) => SPCR2; set up the SPCR2 as the initial configuration.

4.4.14 Pin-Control-Register Configuration

DSP_Write(0x0a0b) => PCR; set up the PCR as shown in Table 26.

Table 26. Pin-Control-Register Configuration (DSP_Write(0x0a0b) => PCR)

Bits	Config Value	Description
15-14	00b	Reserved
13	0b	Set the serial port mode for the DX, FSX and CLKX pins
12	0b	Set the serial port mode for the DR, FSR and CLKR pins

Table 26. Pin-Control-Register Configuration (DSP_Write(0x0a0b) => PCR) (Continued)

Bits	Config Value	Description
11	1b	TX frame-synchronization signal driven by the internal generator
10	0b	RX frame-synchronization signal derived by the external source
9	1b	McBSP is set as the master and generate clock by the internal source
8	0b	CLKR set as the input pin and derived by the external source
7	0b	Sample rate generator input clock mode bit
6	0b	CLKS pin status (no meaning in the OMAP5910 for McBSP3)
5	0b	DX pin status
4	0b	DR pin status
3	1b	Set the FSX polarity as active high
2	0b	Set the FSR polarity as active high
1	1b	Set the CLKX polarity as data driven on a falling edge
0	1b	Set the CLKR polarity as data sampled on a rising edge

4.4.15 Receive-Control-Register Configuration

The values of RWDLEN1, 2 and XWDLEN1, 2 must be set to the same value in the SPI mode.

DSP_Write(0x0000) => RCR1; set up the RCR1 as shown in Table 27.

Table 27. Receive-Control-Register-1 Configuration (DSP_Write(0x0000) => RCR1)

Bits	Config Value	Description
15	0b	Reserved
14-8	000 0000b	Set the receive frame length as one word per frame
7-5	000b	Set the receive word length as 8 bits per frame
4-0	0 0000b	Reserved

DSP_Write(0x0000) => RCR2; set up the RCR2 as shown in Table 28.

Table 28. Receive-Control-Register-2 Configuration (DSP_Write(0x0000) => RCR2)

Bits	Config Value	Description
15	0b	Set single-phase frame
14-8	000 0000b	Set the receive frame length as one word per frame
7-5	000b	Set the receive word length as 8 bits per frame
4-3	00b	Set to no companding data and transfer starting with the MSB first
2	0b	Setting the FSR to ignore after the first receive frame synchronization pulse resets the transfer
1-0	00b	Set the data delay as 0 bit

4.4.16 Transmit-Control-Register Configuration

The values of RWDLEN1, 2 and XWDLEN1, 2 must be set to the same value in the SPI mode.

DSP_Write(0x0000) => XCR1; set up the XCR1 as shown in Table 29.

Table 29. Transmit-Control-Register-1 Configuration (DSP_Write(0x0000) => XCR1)

Bits	Config Value	Description
15	0b	Reserved
14-8	000 0000b	Set the transmit frame length as one word per frame
7-5	000b	Set the transmit word length as 8 bits per frame
4-0	0 0000b	Reserved

DSP_Write(0x0000) => XCR2; set up the XCR2 as shown in Table 30.

Table 30. Transmit-Control-Register-2 Configuration (DSP_Write(0x0000) => XCR2)

Bits	Config Value	Description
15	0b	Set single-phase frame
14-8	000 0000b	Set the transmit frame length as one word per frame
7-5	000b	Set the transmit word length as 8 bits per frame
4-3	00b	Set to no companding data and transfer starting with the MSB first
2	0b	Setting the FSX to not ignore after the first transmit frame synchronization pulse resets the transfer
1-0	00b	Set the data delay as 0 bit

4.4.17 Sample Rate-Generator Configuration (SRGR[1,2])

1) Configure the sample rate generator appropriately for the CLKX and FSX. For details, see SPRU592A, *TMS320VC5501/5502/5509/5510 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide*.
2) Wait for two CLKSRG clock cycles.
3) ARM_Write (SPCR2 or (0x0000 0040))=>SPCR2;CLKG enable
4) Wait for two CLKG clock cycles.

4.4.18 System DMA Configuration

Configure the REVT and XEVT bits for the system DMA receive and transmit synchronized event. For details, see *OMAP5910 Dual-Core Processor System DMA Controller Reference Guide* (literature number SPRU674).

4.4.18.1 Interrupt Flag Configuration and Clear (ILR, MIR)

1) ARM_Write => ILR; set the ILR appropriately for the interrupt handling priority.
2) ARM_Write (MIR or (0x0000 0C00)) => MIR; disables the McBSP3 TX and RX interrupt

Note:

Enable the appropriate system DMA channel interrupts.

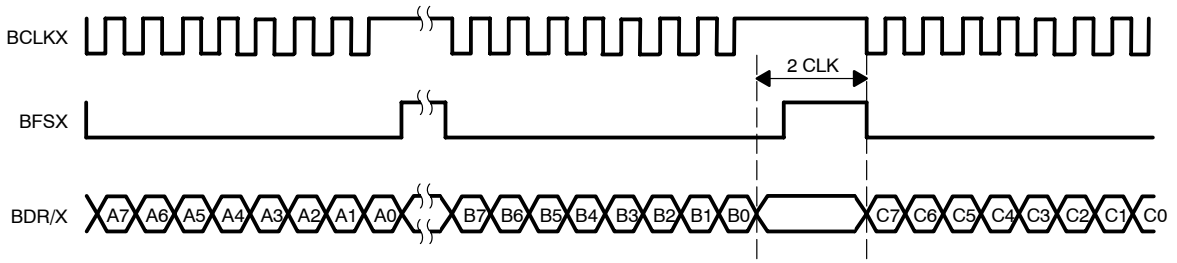
4.4.18.2 Enable McBSP3 Transmit and Receive (SPCR[1,2])

1) ARM_write (SPCR1 or (0x0001)) => SPCR1; enables the receive port
2) ARM_write (SPCR2 or (0x0001)) => SPCR2; enables the transmit port

4.4.18.3 Data Transfer (System DMA Channel)

The system DMA channel transfers the received data to the appropriate data buffer and transfers the newly transmitted data to the appropriate TX buffer. The interrupt flag on the ITR must be cleared when taking the interrupt handle.

Figure 8. Waveform Example



5 McBSP2

This section provides information specific to the McBSP2 of the OMAP5910 device. The McBSP2 is configured on the OMAP5910's MPU public peripheral bus.

5.1 McBSP2 Pin Descriptions

Table 31 describes the McBSP2 pins. Table 32 lists the McBSP2 registers. Figure 9 shows the McBSP2 interface.

Table 31. McBSP2 Pin Descriptions

Pin	I/O Direction	Description
MCBSP2.CLKR	In/out	Receive clock
MCBSP2.CLKX	In/out	Transmit clock
MCBSP2.DR	In	Data input
MCBSP2.DX	Out	Data output
MCBSP2.FSR	In/out	Receive frame synchronization
MCBSP2.FSX	In/out	Transmit frame synchronization

The McBSP2 registers are shown in Table 32.

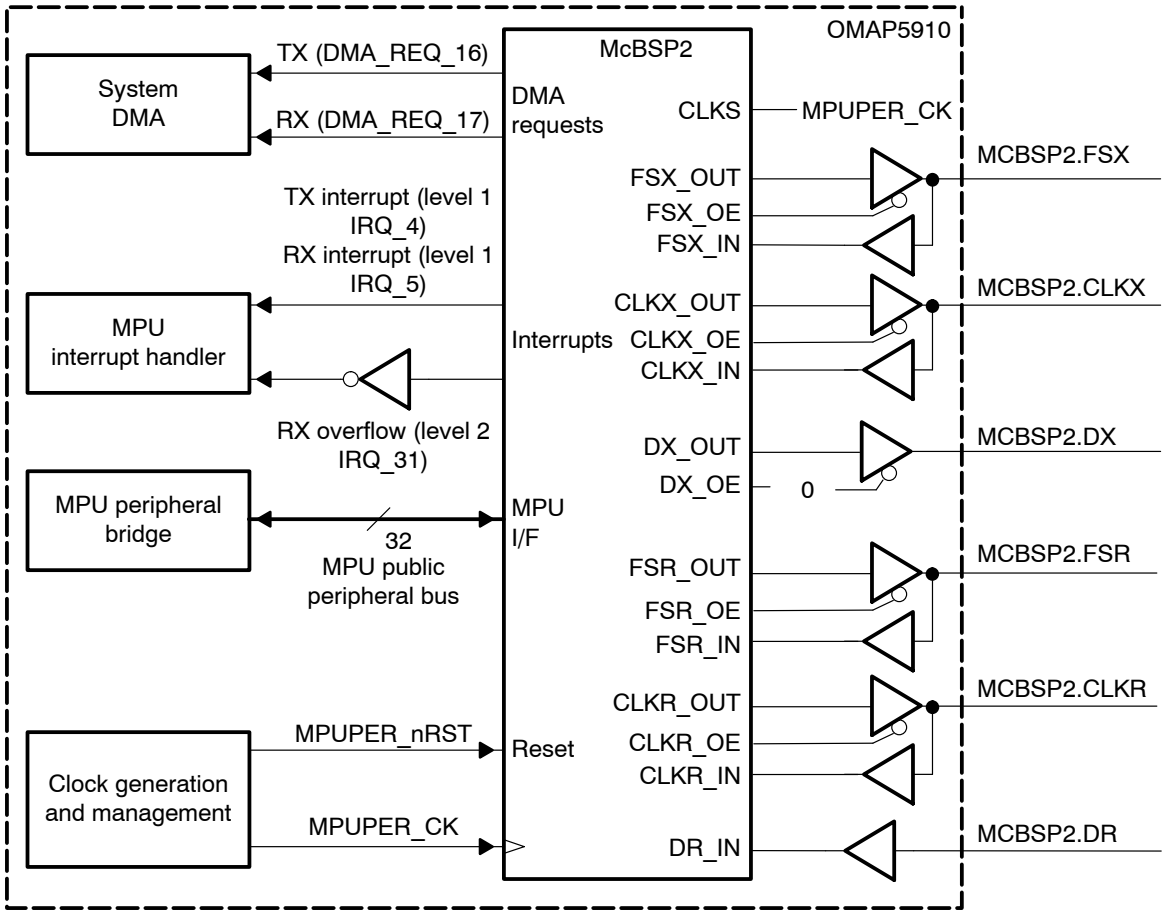
Table 32. McBSP2 Registers

Byte Address	Register Name	Description	Access Width	Access Type	Reset Value
FFFB:1000	MCBSP2_DRR2	McBSP2 Data receive register 2	16	RW	0000h
FFFB:1002	MCBSP2_DRR1	McBSP2 Data receive register 1	16	RW	0000h
FFFB:1004	MCBSP2_DXR2	McBSP2 Data transmit register 2	16	RW	0000h
FFFB:1006	MCBSP2_DXR1	McBSP2 Data transmit register 1	16	RW	0000h
FFFB:1008	MCBSP2_SPCR2	McBSP2 Serial port control register 2	16	RW	0000h
FFFB:100A	MCBSP2_SPCR1	McBSP2 Serial port control register 1	16	RW	0000h
FFFB:100C	MCBSP2_RCR2	McBSP2 Receive control register 2	16	RW	0000h
FFFB:100E	MCBSP2_RCR1	McBSP2 Receive control register 1	16	RW	0000h
FFFB:1010	MCBSP2_XCR2	McBSP2 Transmit control register 2	16	RW	0000h
FFFB:1012	MCBSP2_XCR1	McBSP2 Transmit control register 1	16	RW	0000h
FFFB:1014	MCBSP2_SRGR2	McBSP2 Sample rate generator register 2	16	RW	2000h
FFFB:1016	MCBSP2_SRGR1	McBSP2 Sample rate generator register 1	16	RW	0001h
FFFB:1018	MCBSP2_MCR2	McBSP2 Multichannel control register 2	16	RW	0000h
FFFB:101A	MCBSP2_MCR1	McBSP2 Multichannel control register 1	16	RW	0000h
FFFB:101C	MCBSP2_RCERA	McBSP2 Receive channel enable register partition A	16	RW	0000h
FFFB:101E	MCBSP2_RCERB	McBSP2 Receive channel enable register partition B	16	RW	0000h
FFFB:1020	MCBSP2_XCERA	McBSP2 Transmit channel enable register partition A	16	RW	0000h
FFFB:1022	MCBSP2_XCERB	McBSP2 Transmit channel enable register partition B	16	RW	0000h
FFFB:1024	MCBSP2_PCR0	McBSP2 Pin control register 0	16	RW	0000h

Table 32. McBSP2 Registers (Continued)

Byte Address	Register Name	Description	Access Width	Access Type	Reset Value
FFFB:1026	MCBSP2_RCERC	McBSP2 Receive channel enable register partition C	16	RW	0000h
FFFB:1028	MCBSP2_RCERD	McBSP2 Receive channel enable register partition D	16	RW	0000h
FFFB:102A	MCBSP2_XCERC	McBSP2 Transmit channel enable register partition C	16	RW	0000h
FFFB:102C	MCBSP2_XCERD	McBSP2 Transmit channel enable register partition D	16	RW	0000h
FFFB:102E	MCBSP2_RCERE	McBSP2 Receive channel enable register partition E	16	RW	0000h
FFFB:1030	MCBSP2_RCERF	McBSP2 Receive channel enable register partition F	16	RW	0000h
FFFB:1032	MCBSP2_XCERE	McBSP2 Transmit channel enable register partition E	16	RW	0000h
FFFB:1034	MCBSP2_XCERF	McBSP2 Transmit channel enable register partition F	16	RW	0000h
FFFB:1036	MCBSP2_RCERG	McBSP2 Receive channel enable register partition G	16	RW	0000h
FFFB:1038	MCBSP2_RCERH	McBSP2 Receive channel enable register partition H	16	RW	0000h
FFFB:103A	MCBSP2_XCERG	McBSP2 Transmit channel enable register partition G	16	RW	0000h
FFFB:103C	MCBSP2_XCERH	McBSP2 Transmit channel enable register partition H	16	RW	0000h

Figure 9. McBSP2 Interface Diagram

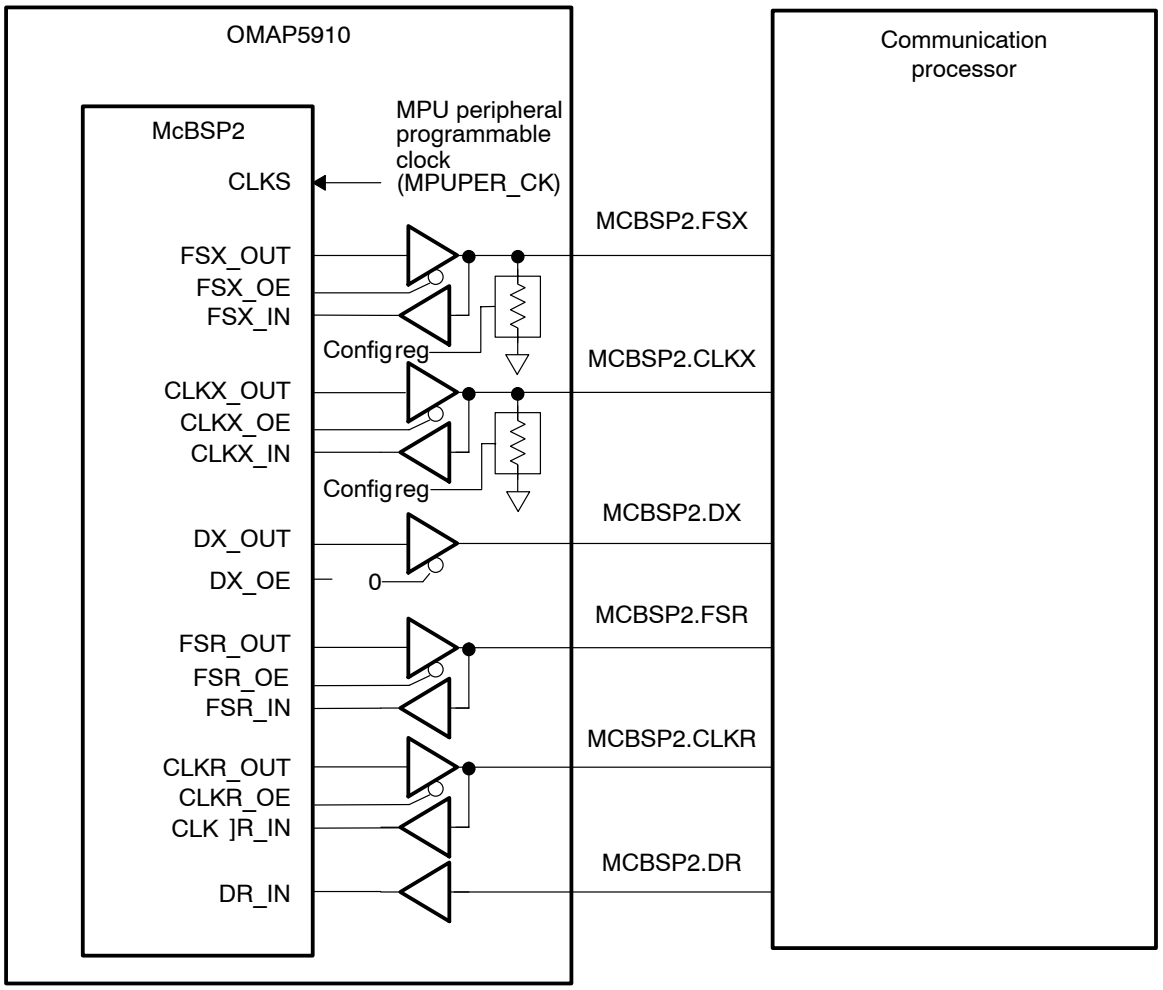


Note: The AUXON feature can be used to gate the functional clock to the McBSP2 module by setting the MOD_CONF_CTRL_0[19] (CONF_MOD_MCBSP2_AUXON) to 1.

5.2 McBSP2 Application Example: Communication Interface

Figure 10 illustrates the use of the McBSP2 as a communication processor data interface that is the master of the TX and slave for the RX communications. The actual implementation is generic: the FSX, CLKX, FSR, and CLKR are bidirectional. The direction of these signals is configured by registers in the McBSP module.

Figure 10. Communication Processor Data Interface



Section 5.2.1 through Section 5.2.9 explain how to set up the McBSP registers for the TX master and the RX slave mode with 16-bit transfers using MPU interrupts.

5.2.1 Serial-Port-Control-Register Configuration

ARM_Write(0x0000) => SPCR1; set up the SPCR1 as the initial configuration.

ARM_Write(0x0000) => SPCR2; set up the SPCR2 as the initial configuration.

5.2.2 Pin-Control-Register Configuration

ARM_Write(0x0a00) => PCR; set up PCR as shown in Table 33.

Table 33. Pin-Control-Register Configuration

Bits	Configuration Value	Description
15-14	00b	Reserved
13	0b	Set the serial port mode for the DX, FSX and CLKX pins
12	0b	Set the serial port mode for the DR, FSR and CLKR pins
11	1b	TX frame-synchronization signal driven by the internal generator
10	0b	RX frame-synchronization signal derived by the external source
9	1b	CLKX set output pin and driven by the internal generator
8	0b	CLKR set input pin and derived by the external source
7	0b	Sample rate generator input clock mode bit
6	0b	CLKS pin status (no meaning in the OMAP5910 device for McBSP2)
5	0b	DX pin status
4	0b	DR pin status
3	0b	Set the FSX polarity as active high
2	0b	Set the FSR polarity as active high
1	0b	Set the CLKX polarity as data driven on a rising edge
0	0b	Set the CLKR polarity as data sampled on a falling edge

5.2.3 Receive-Control-Register Configuration

ARM_Write(0x0040) => RCR1; set up the RCR1 as shown in Table 34.

Table 34. Receive-Control-Register-1 Configuration

Bits	Configuration Value	Description
15	0b	Reserved
14-8	000 0000b	Set the receive frame length as one word per frame
7-5	010b	Set the receive word length as 16 bit per frame
4-0	0 0000b	Reserved

ARM_Write(0x0001) = > RCR2; set up the RCR2 as shown in Table 35.

Table 35. Receive-Control-Register-2 Configuration

Bits	Configuration Value	Description
15	0b	Set single-phase frame
14-8	000 0000b	Don't care for a single-phase frame
7-5	000b	Don't care for a single-phase frame
4-3	00b	Set to no companding data and transfer starting with the MSB first
2	0b	Setting the FSR to not ignore after the first receive frame synchronization pulse resets the transfer
1-0	01b	Set the data delay as 1 bit

5.2.4 Transmit-Control-Register Configuration

ARM_Write(0x0040) => XCR1; set up the XCR1 as shown in Table 36.

Table 36. Transmit Control Register 1 Configuration

Bits	Configuration Value	Description
15	0b	Reserved
14-8	000 0000b	Set the transmit frame length as one word per frame
7-5	010b	Set the transmit word length as 16 bits per frame
4-0	0 0000b	Reserved

ARM_Write(0x0001) => XCR2; set up the XCR2 as shown in Table 37.

Table 37. Transmit-Control-Register-2 Configuration

Bits	Configuration Value	Description
15	0b	Set single-phase frame
14-8	000 0000b	Don't care for a single-phase frame
7-5	000b	Don't care for a single-phase frame
4-3	00b	Set to no companding data and transfer starting with the MSB first
2	0b	Setting the FSX to not ignore after the first transmit frame synchronization pulse resets the transfer
1-0	01b	Set the data delay as 1 bit

5.2.5 Sample-Rate-Generator Configuration (SRGR[1,2])

1) Configure the sample rate generator appropriately for the CLKX and FSX. For details, see SPRU592A, *TMS320VC5501/5502/5509/5510 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide*.
2) Wait for two CLKSRG clocks.
3) ARM_Write (SPCR2 or (0x0000 0040)) → SPCR2;CLKG enable
4) Wait for two CLKG clock cycles.

5.2.6 Interrupt-Flag Configuration and Clear (ILR, ITR, MIR)

1) ARM_Write → ILR; set the ILR appropriately for the interrupt handling priority.
2) ARM_Write (ITR and (0xFFFF FFCF)) → ITR; clear the remaining TX and RX interrupts.
3) ARM_Write (MIR and (0xFFFF FFCF)) → MIR; enables the McBSP2 TX and RX interrupts

5.2.7 Enable McBSP2 Transmit and Receive (SPCR[1,2])

1) ARM_write (SPCR1 or (0x0001)) → SPCR1; enables the receive port
2) ARM_write (SPCR2 or (0x0001)) → SPCR2; enables the transmit port

5.2.8 Transmit Data Loading (TX_INT Handling in Interrupt Service Routine (ISR))

ARM_Write → DXR

Note:

The interrupt flag on the ITR must be cleared by the ISR when taking the interrupt handle.

5.2.9 Receive Data Loading (RX_INT Handling in Interrupt Service Routine (ISR))

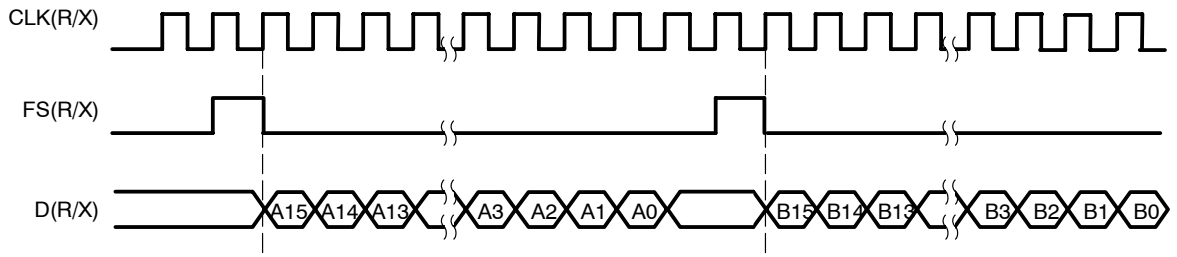
ARM_Read ← DRR

Note:

The interrupt flag on the ITRmust be cleared by the ISR, when taking the interrupt handle.

Waveform Example

Figure 11. Waveform Example



Section 5.2.10 through Section 5.2.18 explain how to set up the McBSP registers for the TX master and RX slave mode with 16-bit transfers using system DMA support.

5.2.10 Serial-Port-Control-Register Configuration

ARM_Write(0x0000) => SPCR1; set up the SPCR1 as the initial configuration.

ARM_Write(0x0000) => SPCR2; set up the SPCR2 as the initial configuration.

5.2.11 Pin-Control-Register Configuration

ARM_Write(0x0a00) => PCR; set up the PCR as shown in Table 38.

Table 38. Pin Control Register Configuration

Bits	Configuration Value	Description
15-14	00b	Reserved
13	0b	Set the serial port mode for the DX, FSX and CLKX pins
12	0b	Set the serial port mode for the DR, FSR and CLKR pins
11	1b	TX frame-synchronization signal driven by the internal generator
10	0b	RX frame-synchronization signal derived by the external source
9	1b	CLKX sets the output pin and driven by the internal generator
8	0b	CLKR sets the input pin and derived by the external source
7	0b	Sample rate generator input clock mode bit
6	0b	CLKS pin status (no meaning in OMAP5910 for McBSP2)
5	0b	DX pin status
4	0b	DR pin status

Table 38. Pin Control Register Configuration (Continued)

Bits	Configuration Value	Description
3	0b	Set the FSX polarity as active high
2	0b	Set the FSR polarity as active high
1	0b	Set the CLKX polarity as data driven on a rising edge
0	0b	Set the CLKR polarity as data sampled on a falling edge

5.2.12 Receive-Control-Register Configuration

ARM_Write(0x0040) => RCR1; set up the RCR1 as shown in Table 39.

Table 39. Receive-Control-Register-1 Configuration

Bits	Configuration Value	Description
15	0b	Reserved
14-8	000 0000b	Set the receive frame length as one word per frame
7-5	010b	Set the receive word length as 16 bits per frame
4-0	0 0000b	Reserved

ARM_Write(0x0001) => RCR2; set up the RCR2 as shown in Table 40.

Table 40. Receive-Control-Register-2 Configuration

Bits	Configuration Value	Description
15	0b	Set single-phase frame
14-8	000 0000b	Set the receive frame length as one word per frame
7-5	000b	Don’t care for single-phase frame
4-3	00b	Don’t care for single-phase frame
2	0b	Setting the FSR to not ignore after the first receive frame synchronization pulse resets the transfer
1-0	01b	Set the data delay as 1 bit

5.2.13 Transmit-Control-Register Configuration

ARM_Write(0x0040) => XCR1; set up the XCR1 as shown in Table 41.

Table 41. Transmit-Control-Register-1 Configuration

Bits	Configuration Value	Description
15	0b	Reserved
14-8	000 0000b	Set the transmit frame length as one word per frame
7-5	010b	Set the transmit word length as 16 bits per frame
4-0	0 0000b	Reserved

ARM_Write(0x0001) => XCR2; set up XCR2 per below configuration.

Table 42. Transmit-Control-Register-2 Configuration

Bits	Configuration Value	Description
15	0b	Set single-phase frame
14-8	000 0000b	Don't care for single-phase frame
7-5	000b	Don't care for single-phase frame
4-3	00b	Set to no companding data and transfer starting with the MSB first
2	0b	Setting the FSX to not ignore after the first transmit frame synchronization pulse resets the transfer
1-0	01b	Set the data delay as 1 bit

5.2.14 Sample-Rate-Generator Configuration (SRGR[1,2])

1) Configure the sample rate generator appropriately for the CLKX and FSX. For details, see SPRU592A, *TMS320VC5501/5502/5509/5510 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide*.

2) Wait for two CLKSRG clock cycles.

3) ARM_Write (SPCR2 or (0x0000 0040))=>SPCR2;CLKG enable.

4) Wait for two CLKG clock cycles.

5.2.15 System DMA Configuration

Configure the REVT and XEVT bit for the system DMA receive and transmit synchronized event (request). For details, see *OMAP5910 Dual-Core Processor System DMA Controller Reference Guide* (literature number SPRU674).

5.2.16 Interrupt Flag Configuration and Clear (ILR, MIR)

1) ARM_Write => ILR; set the ILR appropriately for the interrupt handling priority.
2) ARM_Write (MIR or (0x0000 0030)) => MIR ; disables the McBSP2 TX and RX interrupt

Note:

Enable the appropriate system DMA channel interrupts.

5.2.17 Enable McBSP2 Transmit and Receive (SPCR[1,2])

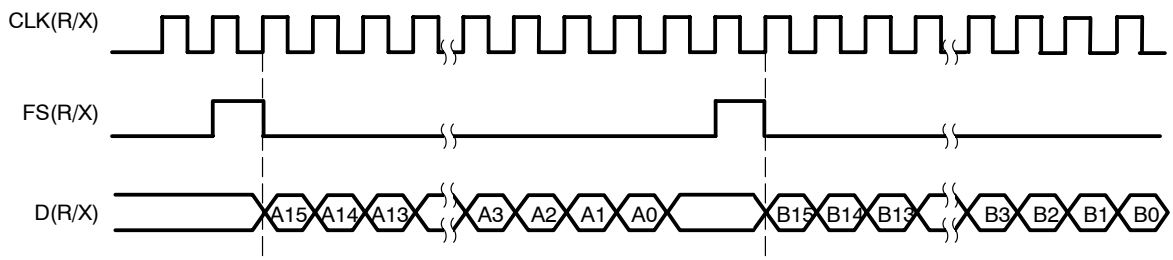
1) ARM_write SPCR1 or (0x0001) => SPCR1; enables the receive port.
2) ARM_write SPCR2 or (0x0001) => SPCR2; enables the transmit port.

5.2.18 Data Transfer (System DMA Channel)

The system DMA channel transfers the received data to the appropriate data buffer and transfers the newly transmitted data to the appropriate TX buffer. The interrupt flag on the ITR is cleared, when taking the interrupt handle.

Waveform Example

Figure 12. Waveform Example



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