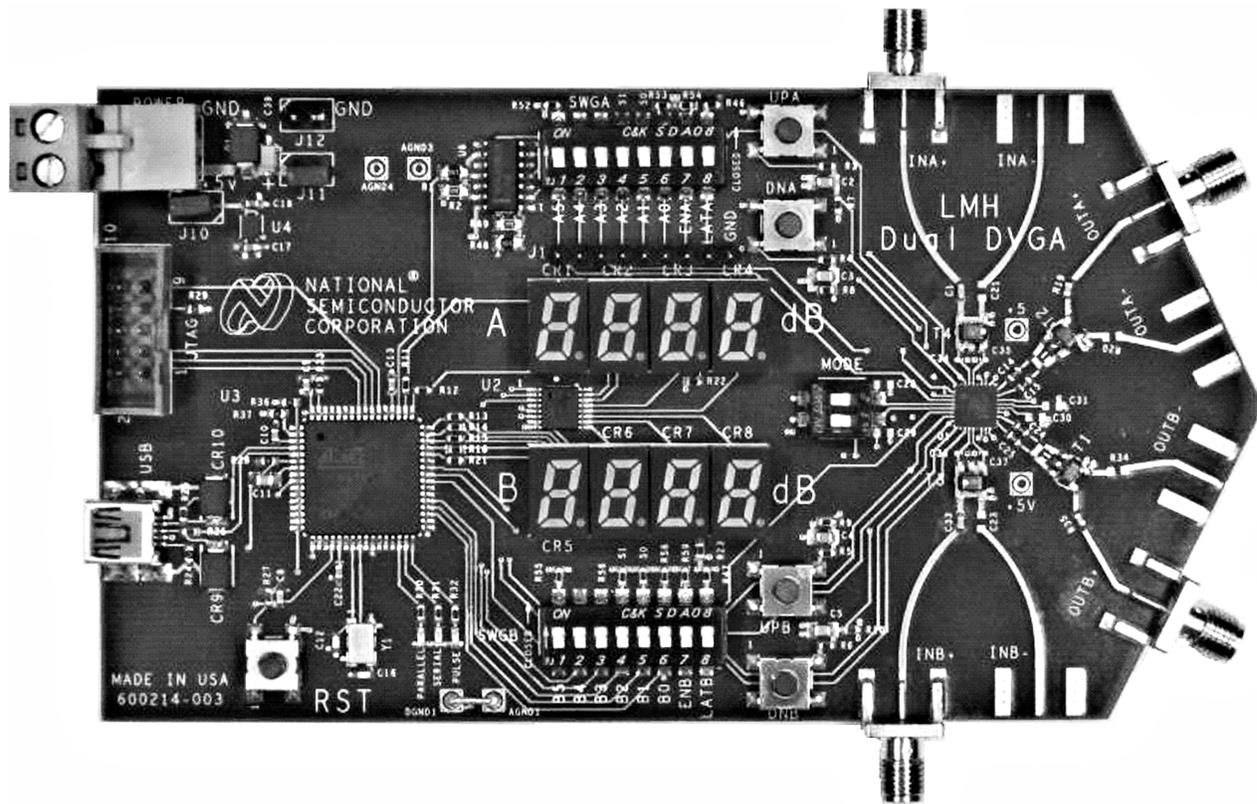


## AN–1942 LMH6517 Evaluation Board

### 1 General Description

The LMH6517EVAL evaluation board is designed to aid in the characterization of high speed LMH6517 digital controlled variable gain amplifier (DVGA).

Use the evaluation board as a guide for high frequency layout and as a tool to aid in device testing and characterization.



**Figure 1. LMH6517EVAL Evaluation Board**

### 2 Basic Operation

The LMH6517 DVGA has differential input and differential output. To aid evaluation with 50  $\Omega$  single ended test equipment the LMH6517EVAL evaluation board provides for input and output transformers. As shipped, the board has both input and output transformers loaded. The signal path uses the IN+ and OUT+ marked connectors. The IN– and OUT– signal paths are grounded.

The evaluation board uses edge mounted SMA connectors. When using the differential inputs a termination resistor can be placed on the pads used by the transformer primary coils. For DC coupled operation capacitors C1 and C21 can be replaced by 0  $\Omega$  resistors.

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The LMH6517EVAL evaluation board is designed to be used with transformers or baluns. If baluns (no DC blocking) are used, then make sure that the DC operating levels are within the amplifier's operating voltage range. There are pads for DC blocking capacitors on both the input and output signal traces. The input and output pins of the LMH6517 will self bias to approximately mid supply (2.5 V).

Transformers T1– T4 can provide both impedance matching as well as single ended to differential conversion. The board is shipped with 2:1 turns ratio transformers that will match 50  $\Omega$  equipment with the 200  $\Omega$  input impedance of the LMH6517 DVGA. Do not connect the transformer secondary winding directly to ground. The LMH6517 has a self-biased input common mode voltage of approximately 2.5 V. The amplifier will bias up to the optimal input common mode point. If differential operation is desired, the copper on the grounded input must be cut.

On the output side of the board are transformers T1 and T2. The capacitors C14, C15, C24 and C25 isolate the output common mode voltage from the output transformer primary windings and are not required if the transformer provides DC blocking. Resistors R19, R20, R34 and R35 are matching resistors. If not needed, than 0  $\Omega$  resistors can be loaded in these positions. The output impedance of the LMH6517 amplifier is very low (<2  $\Omega$  at 50 MHz), so almost any load can be matched by loading appropriate valued resistors. The LMH6517 evaluation board comes built with 1:1 balun transformers and 10  $\Omega$  series output resistors. A 4.7 pF load capacitor is placed between the resistors and the transformer. The 10  $\Omega$  resistors and 4.7 pF capacitor form a snubber circuit that reduces high frequency peaking and enhances stability. The combination of the snubber circuit and the 1:1 balun gives very good power gain and very good OIP3 performance. Other load conditions can be achieved by changing out the components on the evaluation board. Not all load conditions will require a snubber circuit, but it should be included in the final circuit design unless sufficient testing has shown it to be unnecessary.

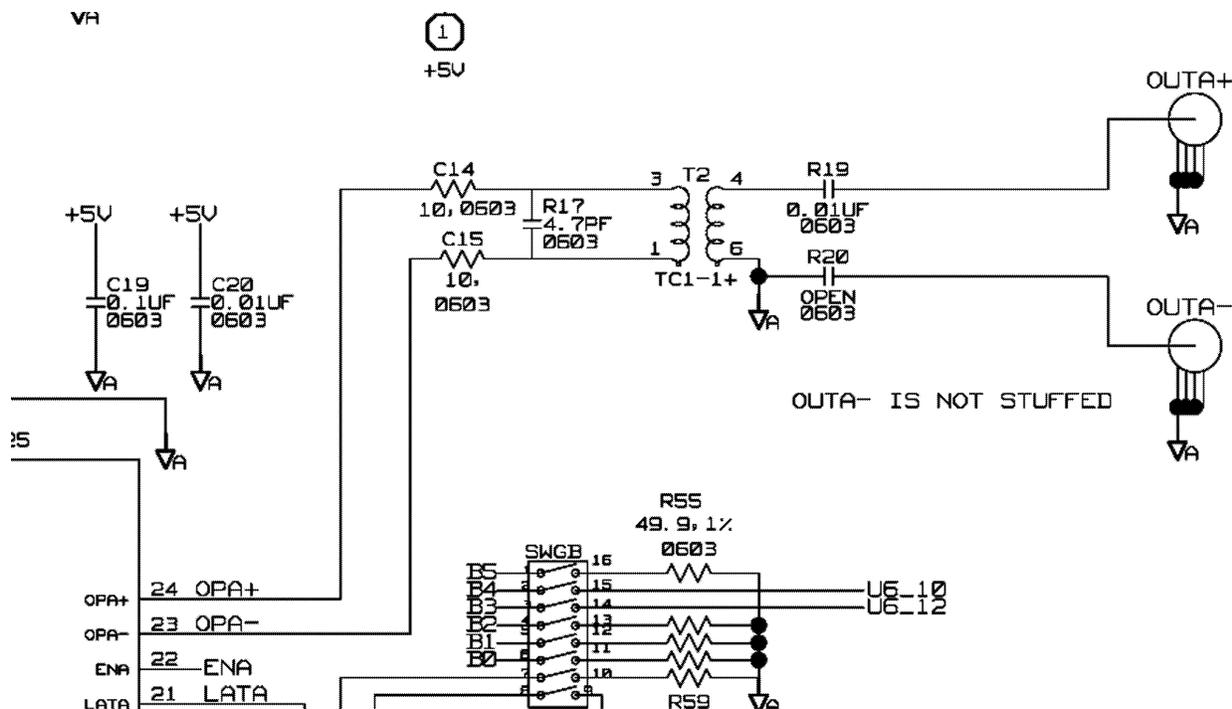


Figure 2. Output Schematic

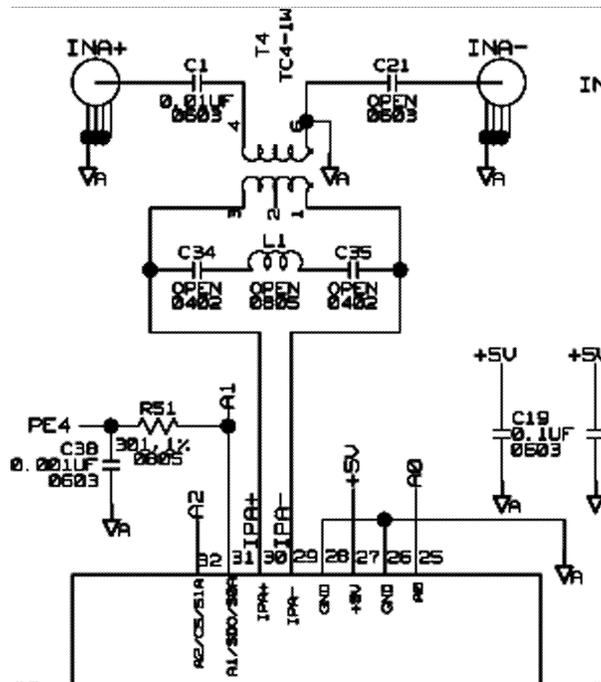


Figure 3. Input Schematic

The board was designed to be very flexible for many different configurations. Zoomed in portions of the input and output schematics are shown above in Figure 2 and Figure 3. The evaluation board, as shipped, has been optimized for ease of use with single ended 50  $\Omega$  test equipment. This configuration may not emulate the most common application circuits. The signal path schematic is shown in Figure 8 and the full schematic in .PDF format is included on the software CD included with the LMH6517EVAL evaluation board kit.

### 3 Using With Different Sources or Loads

The LMH6517EVAL board supports differential operation on both inputs and outputs. However, they will require additional components and some board rework. For driving the evaluation board from a differential source, symmetrical signal paths are provided. Both input and output paths support fully differential test equipment.

To drive the LMH6517 evaluation board from a differential source, the transformers T3 and T4 must be removed. The diagrams in Figure 6 and Figure 7 show the required connections for differential inputs. DC coupled operation is possible using differential signals. Make sure that the test equipment can provide the  $2.5 \pm 1$  V offset voltage on the input and output.

For differential output signals, remove transformers T1 and T2. Wire jumpers or 0  $\Omega$  resistors must be added to complete the signal path across the transformer pads similar to the changes required for differential inputs.

### 4 Other Board Configurations

For other applications or experiments there are many options for changing the output circuit to simulate different circuit conditions. One option is to use a 2:1 transformer to simulate high impedance loads. In this case one would use 100  $\Omega$  resistors for R19, R20, R34 and R35. This would present a load of 200  $\Omega$  to the amplifier output. Many common filter circuits have 200  $\Omega$  input impedance. Other combinations can also be used to simulate different load conditions.

## 5 Additional Design Tools

The RD-179: High-IF sub-sampling receiver subsystem board (SP16160CH1RB) is also available. This reference design includes the ADC16DV160 ADC, the LMH6517 DVGA, and the LMK04031B precision clock conditioner. Power regulation, filters and controlled impedance board layout are all provided in this reference design. For further details, visit the Texas Instruments website located at: [www.ti.com](http://www.ti.com).

## 6 Gain Control

For ease of use, a micro-controller and banks of LED displays give gain settings and status information. The 7 segment LED displays show the gain for each channel in units of dB. The LMH6517 DVGA has three control modes including, parallel mode, serial (SPI compatible) mode and pulse mode. Parallel and pulse modes are fully supported on the board. Serial mode control requires the use of a PC and the software provided in the evaluation board kit. To set the board in parallel mode, dip-switch SW 1, which is labeled MODE, must be set such that the top switch is in the OFF position and the bottom switch is in the OFF position (the top of the board is the Channel A portion). To move the MODE switches to the OFF position, slide them toward the output SMA connectors.

In parallel mode, the switch banks adjacent to the 7 segment displays are used to set the gain of the DVGA. When using the DIP switches to change gain in parallel mode ensure that the switch labeled LATA or LATB is in the ON position. With the latch switch in the ON state the device is in transparent mode and any change in the dip switches is immediately reflected in the device gain. Moving the latch pin switch to the OFF position holds the last gain setting and ignores changes in the gain control switches. When the latch switch is in the OFF position the dip switches that control the gain can be configured as desired and then implemented by momentarily switching the LATA or LATB switch. For detailed instructions on the pin functions, see the *LMH6517 Low Power, Low Noise, IF and Baseband, Dual 16 bit ADC Driver With Digitally Controlled Gain Data Sheet* ([SNOSB19](#)).

The easiest gain control mode is parallel mode. In this mode, the dip switch banks SWGA and SWGB are used to set the gain of the DVGA. The gain bits are binary weighted with the LSB representing a 0.5dB gain step and the MSB representing a 16dB step. The steps increase the gain when the switch is in the ON position. For example, switching B5 from OFF to ON will increase the gain by 16dB. Between the gain control bits and the latch switch is an enable (ENA or ENB) switch. Setting this switch to the OFF position enables the respective DVGA channel.

The DVGA is also very easy to control in pulse mode. For system implementations, pulse mode requires fewer digital control lines than parallel mode at the expense of gain control speed. To use pulse mode, the mode switches should be set such that MODE 1 is in the ON position and MODE2 is in the OFF position. Gain changes are accomplished by using the UP and DN buttons. There are separate buttons for the A channel and the B channel. Gain will be indicated on the LED displays.

The push button switches located between the DVGA and the parallel dip switch banks are for use in pulse mode. The UPA and UPB buttons increment the gain up one step while the DNA and DNB buttons decrement the gain by one step. The gain step sizes are set by the DIP switches labeled GB1 and GB2 on the parallel control DIP switches. Each channel can have a different gain step size.

Serial mode is the most complex control mode and is considerably slower than parallel mode, but it is very flexible and requires fewer digital control lines. Serial mode requires a PC, USB cable and the serial mode control software, in addition to the LMH6517EVAL board. The software and USB cable are included in the evaluation board kit; the software is Windows® compatible. The first step for using the board in serial mode is to place the MODE switches in the proper configuration. The MODE1 switch will be in the OFF position and the MODE2 switch will be in the ON position. If no computer is connected to the evaluation board the LED indicators will flash. Directions for installing the USB control software and evaluation board drivers are included on the CD shipped with the evaluation board.

Near the power connector are a number of 0.1" 2-pin headers. The jack labeled J10 is normally loaded with a shorting jumper, it provides power to the micro controller and LED display banks. Removing the shorting jumper on this jack will disable those components (and leave only the LMH6517 powered on). With the micro controller disabled the LMH6517 can be controlled by an external logic analyzer or microcontroller. The header labeled J1 provides off board access to the LMH6517 digital control pins. The J1 pins and functions are described in [Table 1](#).

A 0.1" header strip is located near SWGA (J1). This strip can be used to connect a micro-controller or logic analyzer to the serial control pins, the pulse control pins and the channel A parallel control pins. This header jack pins function as shown in [Table 1](#). For the full description of these pin functions, see the device-specific data sheet. Note that the SWGA dip switches will impact the on-board impedance for the J1 header pins. The SWGA dip switches should be set to the OPEN position. There is no on-board termination for the J1 header pins and they will appear as high impedance to the logic analyzer. Make sure that this does not result in logic signals that are beyond the absolute maximum rating for the LMH6517.

**Table 1. Header Jack Pin Assignments (J1)**

Header Pin	LMH6517 Pin No	Parallel Function	Serial Function	Pulse Function
J1-1	3	Address bit 5	N/A	N/A
J1-2	2	Address bit 4	CLK	Up A
J1-3	1	Address bit 3	Serial Data In	Down A
J1-4	32	Address bit 2	Chip Select	Step Size MSB
J1-5	31	Address bit 1	Serial Data Out	Step Size LSB
J1-6	25	Address bit 0	N/A	N/A
J1-7	22	Enable A	Enable A	Enable A
J1-8	21	Latch A	N/A	N/A
J1-9	N/A	Ground	Ground	Ground

The jack labeled J11 is also normally loaded with a shorting jumper and it provides power to the DVGA. By removing the short on this jack and replacing it with an ammeter the current drawn by the DVGA can be measured. The jack labeled J12 is a ground connector and is normally left empty. The connector labeled JTAG is for programming the micro-controller. Under normal operation it should not be required. The jack labeled USB accepts a standard USB peripheral cable and is used for PC control of the gain states of the DVGA.

Near the micro-controller is a reset button that initializes the microcontroller software. If the software is not operating correctly first try the reset button. The next step would be a complete power cycle of the board.

The LMH6517EVAL board supports all three digital control modes offered on the LMH6517DVGA. Most system designs should implement only one control mode and will, therefore, require substantially fewer components. For details on each digital control mode, see the *LMH6517 Low Power, Low Noise, IF and Baseband, Dual 16 bit ADC Driver With Digitally Controlled Gain Data Sheet* ([SNOSB19](#)). The RD-179 reference design uses parallel mode.

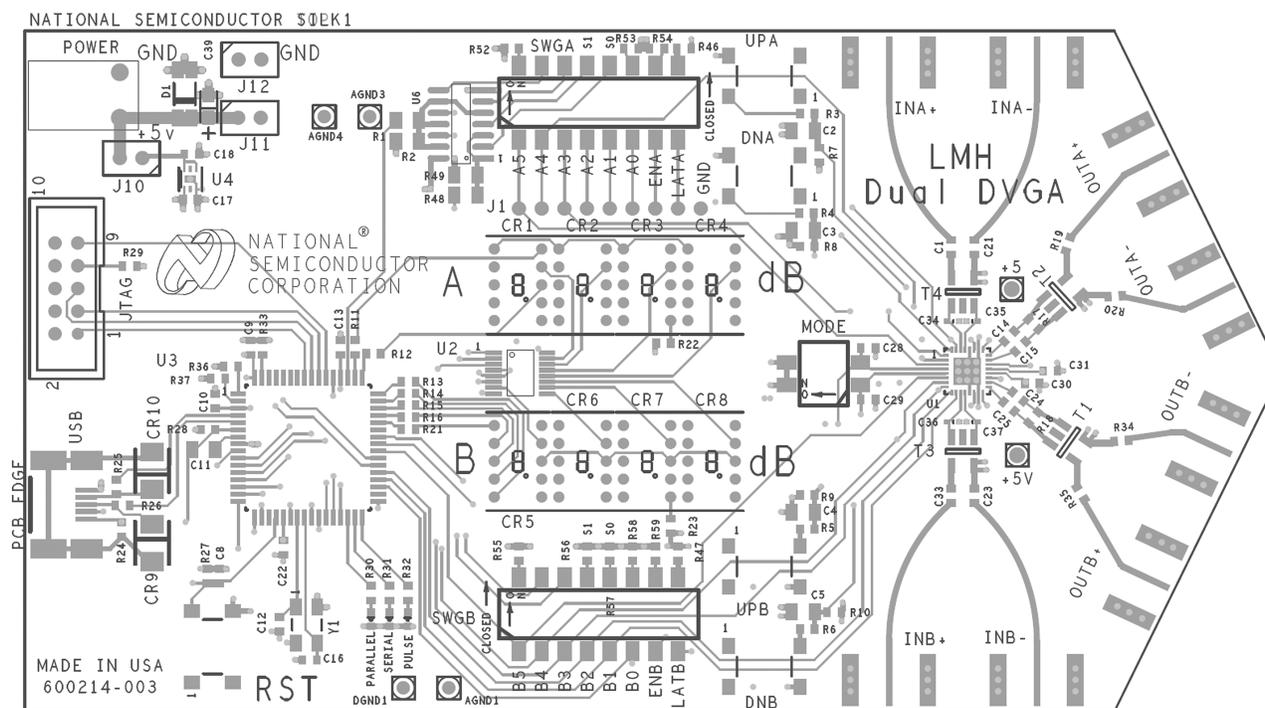


Figure 4. Evaluation Board Top Layer

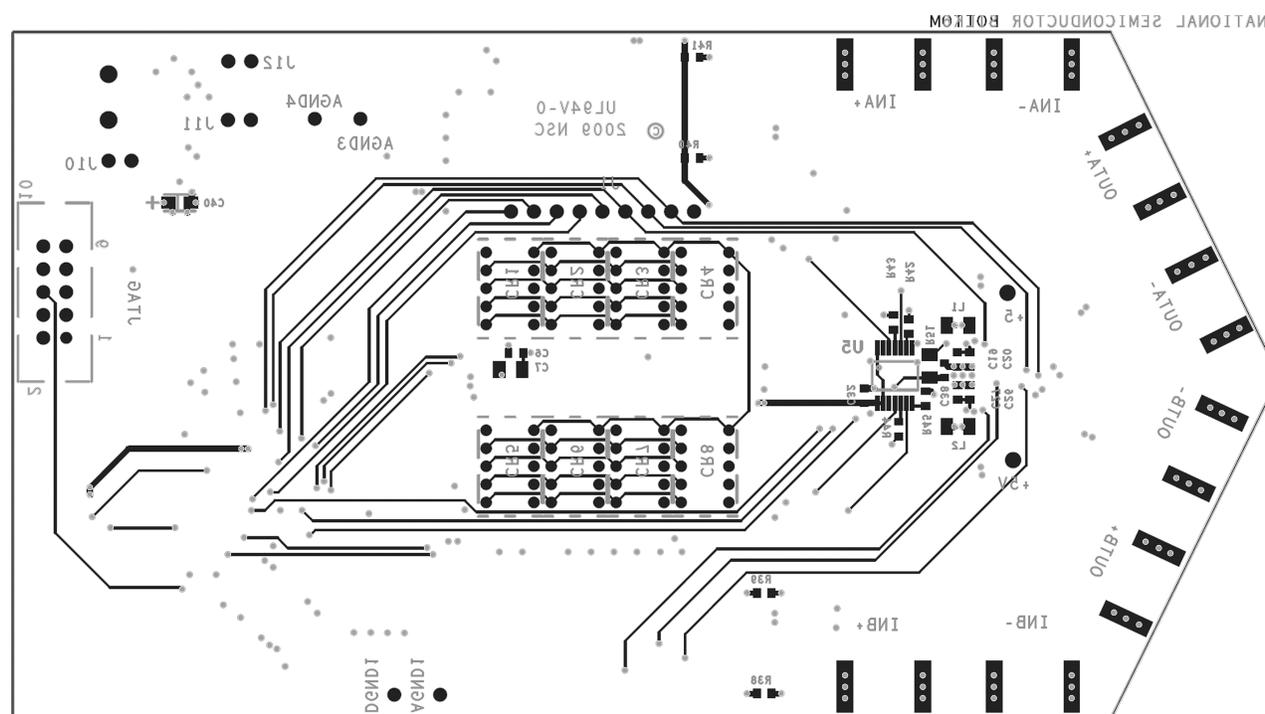


Figure 5. Evaluation Board Bottom Layer

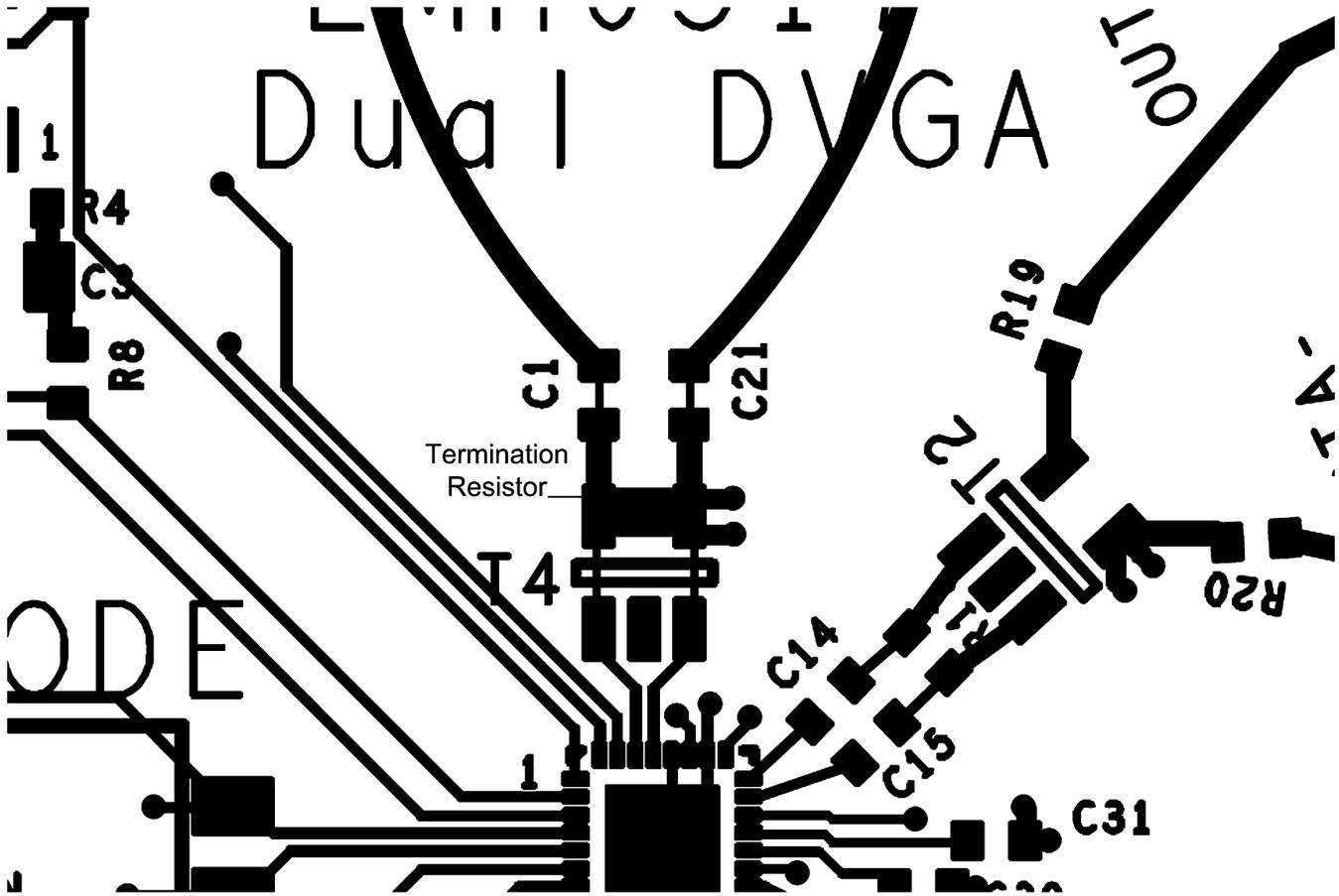


Figure 6. Connections for Differential Input.

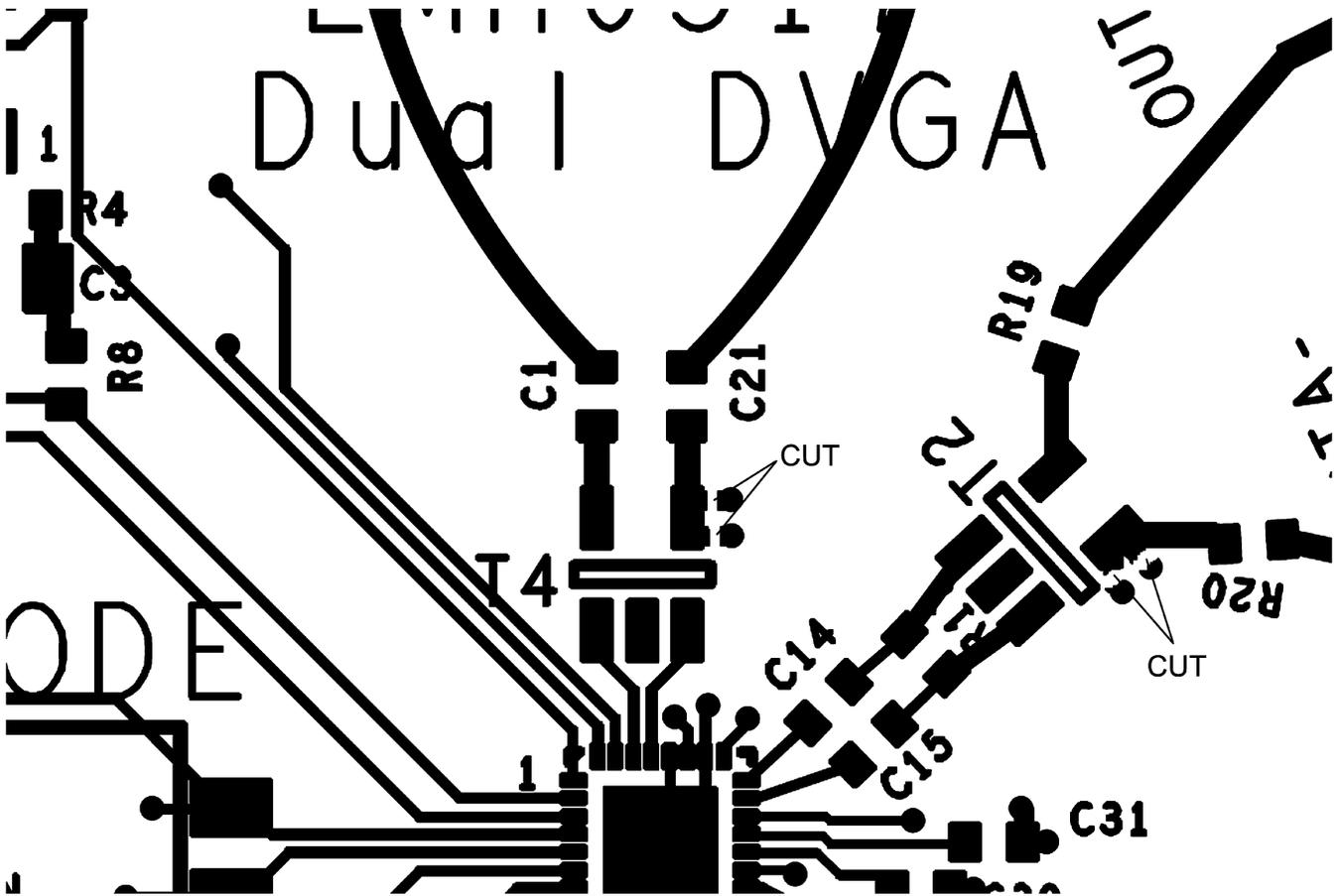
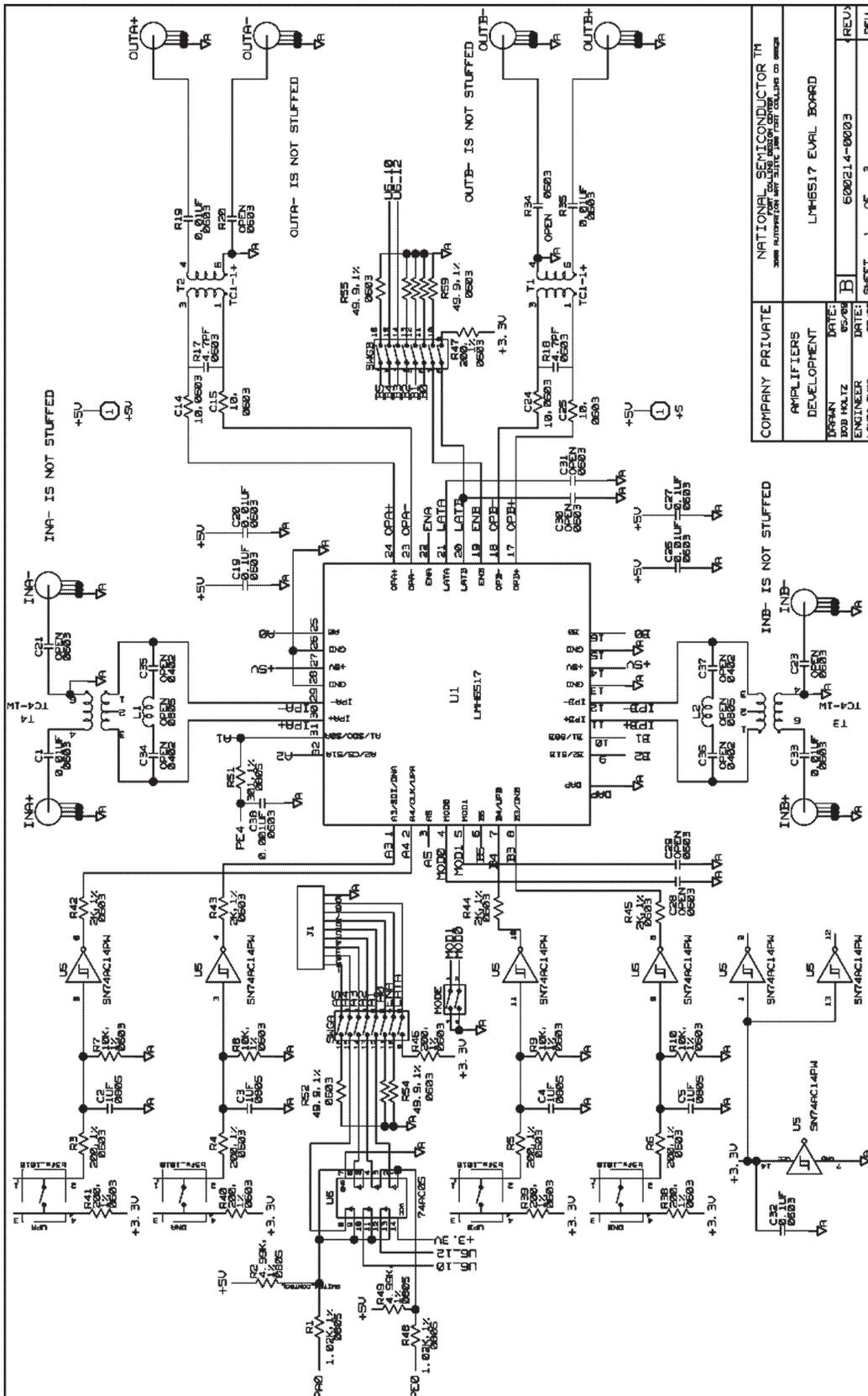


Figure 7. Trace Cuts for Differential Input and Output



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Figure 8. Signal Path Schematic

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