TPS25751 Technical Reference Manual

Technical Reference Manual

Literature Number: SLVUCR8
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Read This First

About This Manual

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers may be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

Related Documents

- USB Power Delivery Specification Revision 3.1 www.usb.org/developers/docs
- USB Type-C Cable and Connector Specification Revision 2.0. www.usb.org/developers/docs

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Chapter 1

Introduction

1.1 Introduction

1.1.1 Purpose and Scope

This document describes the Host Interface for the TPS25751S and TPS25751D Type-C Port Switch / Power Delivery (PD) Controller devices.

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1.2 PD Controller Host Interface Description

1.2.1 Overview

The PD Controller provides one I2C target. The I2Ct target is meant to be connected to an Embedded Controller (EC).

The Host Interface defines how the registers are accessed from I2C target port and target addresses. Target Address #1 is selected by the customer using the ADCIN1 and ADCIN2 pins on the PD controller. See also Table 5-1 for more details about the target addresses.

The Host Interface provides general status information to the controller of these I2C interfaces about the PD Controller, ability to control the PD Controller, status of USB Type-C® Port and communications to/from a connected device (Port Partner) and/or cable plug through USB PD messages. All Host Interface communication that uses the Unique I2C address is referred to as Unique Address Interface.

The PD Controller supports a register-based Unique Address Interface. Chapter 3 lists the Unique Address Interface registers and provides detailed Unique Address Interface register descriptions.

The key to the protocol diagrams is in the SMBus Specification, version 2.0 and is repeated here in part in Figure 1-1.

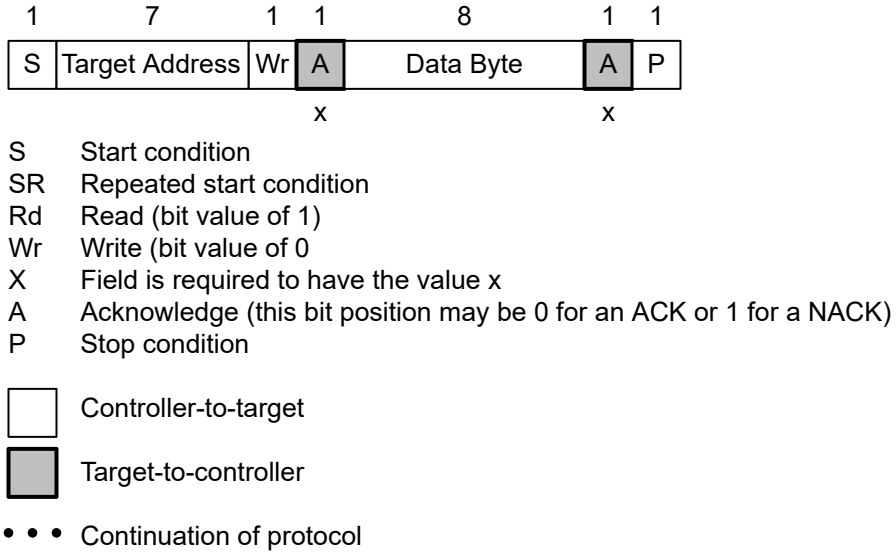

Figure 1-1. I2C Read/Write Protocol Key

1.2.2 Register and Field Notation

In this document the register names use an ALL CAPS notation, and the field names use a CamelBack notation. For example *TX_SOURCE_CAPS* refers to register 0x32, and *TX_SOURCE_CAPS.numValidPDOs* refers to a specific field in Byte 1 of that register.

Some registers have the same definition, but there are multiple instantiations at different register addresses. The following lists these registers.

- *INT_EVENTx ~ INT_EVENT1* (0x14)
- *INT_MASKx ~ INT_MASK1* (0x16)
- *INT_CLEARx ~ INT_CLEAR1* (0x18)
- *CMDx ~ CMD1* (0x08)
- *DATAx ~ DATA1* (0x09)

In this document, the "x" indicates that it is referring to an instantiations of that register.

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1.3 Unique Address Interface

1.3.1 Unique Address Interface Protocol

The Unique Address Interface allows for complex interactions between an I2C controller and a single PD Controller. The I2C target unique address is used to receive or respond to Host Interface protocol commands. Figure 1-2 and Figure 1-3 show the write and read protocols, respectively. The Byte Count used during a register write can be longer than the number of bytes actually written, in other words the controller can issue the stop bit without writing N bytes. Similarly, during a register read, the controller can issue the stop bit before reading all N bytes.

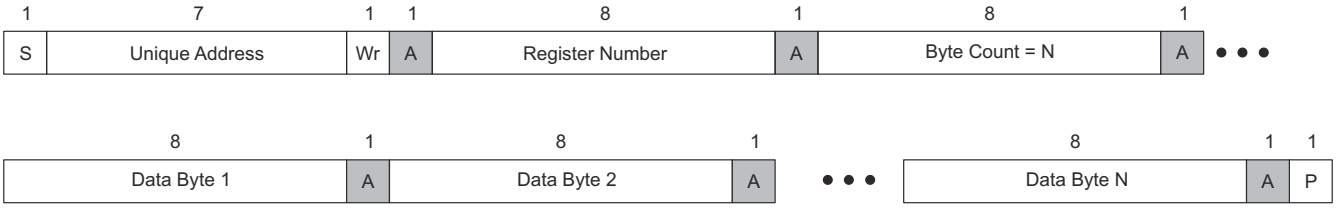

Figure 1-2. I2C Unique Address Write Register Protocol

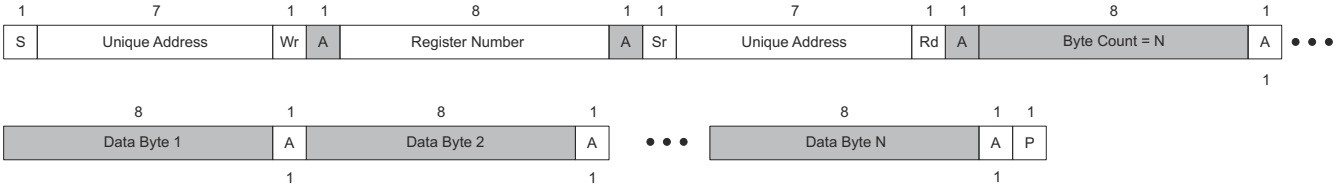

Figure 1-3. I2C Unique Address Read Register Protocol

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Chapter 2

PD Controller Policy Modes

2.1 Overview

The PD Controller implements modes for "SRC Policy" (handing out Source contracts), modes for "SNK Policy" (issuing Requests for Sink contracts), and modes for "AM Policy" (Alternate Mode negotiation).

2.2 Source Policy Mode

The PD Controller uses the *TX_SOURCE_CAPS* register (0x32) to know what PDO(s) to advertise. The PD Controller will automatically respond to Request messages as appropriate, and each port acts independently. The host can dynamically change the *TX_SOURCE_CAPS* register, then issue the 'SSrC' 4CC Task and the PD controller will advertise the new PDOs.

2.3 Sink Policy Mode

The PD Controller will always prepare its own Request message based on the settings in the *AUTO_NEGOTIATE_SINK* register (0x37) and the *TX_SINK_CAPS* register (0x33). The PD Controller will send its prepared Request message as soon as it is ready. The host can change the *AUTO_NEGOTIATE_SINK* register and/or the *TX_SINK_CAPS* register, then issue the 'GSrC' or 'ANeg' 4CC Task and the PD controller will re-negotiate the PD contract based on the updated values.

2.4 Alternate Modes and Alternate Mode Policy

Power Delivery enables alternative modes of operation by providing the mechanisms to discover, enter, and exit Alternate Modes. The PD Specification defines mechanisms to discover, enter and exit Modes defined either by a standard or by a particular vendor. These Modes can be supported either by the Port Partner or by a cable connecting the two Port Partners.

The PD controller will automatically send the Discover Identity message to both the Cable Plug and the Port Partner in compliance wtih USB PD rules. The responses are available in the *RX Identity SOP* register (0x48) and the *RX_IDENTITY_SOPp* register (0x49). The PD controller will also automatically send a Discover SVIDs message and store the response in the *DISCOVERED_SVIDS* register (0x21). The host must wait until *INT_EVENTx.DiscoverModesComplete* is asserted to read the information that was gathered. The host can configure other automatic behavior (even automatic mode entry) using the *USER_VID_CONFIG* register (0x4A), *DP_SID_CONFIG* register (0x51), and *INTEL_VID_CONFIG* register (0x52).

When allowed by the USB PD specification, the PD controller will respond to SVDM commands as appropriate. The *TX_IDENTITY* register (0x47) is used to formulate the response when a Discover Identity SVDM is received. When an SVDM is received it is stored in the *RX_ATTENTION_VDM* register (0x4E) or *RX_OTHER_VDM* register (0x4F), and either *INT_EVENTx.AttentionReceived* or *INT_EVENTx.VDMReceived* will get assserted.

The host can use the 4CC Tasks listed in Chapter 4 to implement other VDM behaviors.

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Chapter 3

TPS25751 Registers

Table 3-1 lists the memory-mapped registers for the TPS25751 registers. All register offset addresses not listed in Table 3-1 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. TPS25751 Registers

Offset	Acronym	Register Name	Section
3h	Mode	Mode	Section 3.1
8h	Command Register for I2C1	Command Register for I2C1	Section 3.2
9h	Data Register for CMD1	Data Register for CMD1	Section 3.3
14h	Interrupt Event for I2C1	Interrupt Event for I2C1	Section 3.4
16h	Interrupt Mask for I2C1	Interrupt Mask for I2C1	Section 3.5
18h	Interrupt Clear for I2C1	Interrupt Clear for I2C1	Section 3.6
1Ah	Status	Status	Section 3.7
26h	Power Path Status	Power Path Status	Section 3.8
29h	Port Control	Port Control	Section 3.9
2Dh	Boot Flags	Boot Flags	Section 3.10
30h	Received Source Capabilities	Received Source Capabilities	Section 3.11
31h	Received Sink Capabilities	Received Sink Capabilities	Section 3.12
32h	Transmit Source Capabilities	Transmit Source Capabilities	Section 3.13
33h	Transmit Sink Capabilities	Transmit Sink Capabilities	Section 3.14
34h	Active PDO Contract	Active PDO Contract	Section 3.15
35h	Active RDO Contract	Active RDO Contract	Section 3.16
37h	Autonegotiate Sink	Autonegotiate Sink	Section 3.17
3Ch	SPM Client Control	SPM Client Control	Section 3.18
3Fh	Power Status	Power Status	Section 3.19
40h	PD Status	PD Status	Section 3.20
69h	Type C State	Type C State	Section 3.21
70h	Sleep Control Register	Sleep Control Register	Section 3.22
72h	GPIO Status	GPIO Status	Section 3.23
98h	Moisture Detection Config	Moisture Detection Config	Section 3.24

Complex bit access types are encoded to fit into small table cells. Table 3-2 shows the codes that are used for access types in this section.

Table 3-2. TPS25751 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		

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Table 3-2. TPS25751 Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

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3.1 Mode Register (Offset = 3h) [Reset = 00000000h]

Mode is shown in Table 3-3.

Return to the Summary Table.

Indicates the operational state of the port. The PD controller has limited functionality in some modes.

Table 3-3. Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Mode	R	0h	The mode described in 4 ASCII characters.

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3.2 Command Register for I2C1 (Offset = 8h) [Reset = 00000000h]

Command Register for I2C1 is shown in Table 3-4.

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Command register for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".

Table 3-4. Command Register for I2C1 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Command	R/W	0h	Command register for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".

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3.3 Data Register for CMD1 (Offset = 9h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Data Register for CMD1 is shown in Table 3-5.

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Data register for the primary command interface (CMD1).

Table 3-5. Data Register for CMD1 Field Descriptions

Bit	Field	Type	Reset	Description
511-0	Data	R/W	0h	Data register for the primary command interface (CMD1).

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3.4 Interrupt Event for I2C1 Register (Offset = 14h) [Reset = 00000000000000002000008h]

Interrupt Event for I2C1 is shown in Table 3-6.

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Interrupt event bit field for I2C_EC_IRQ. If any bit in this register is 1, then the I2C_EC_IRQ pin is pulled low. Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-6. Interrupt Event for I2C1 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R	0h	Reserved
82	I2C Controller NACked	R	0h	A transaction on the I2C Controller was NACKed.
81	Ready for Patch	R	0h	Device ready for a patch bundle from the host.
80	Patch Loaded	R	0h	Patch was loaded to the device.
79	RESERVED	R	0h	Reserved
78	RESERVED	R	0h	Reserved
77	RESERVED	R	0h	Reserved
76	RESERVED	R	0h	Reserved
75-74	RESERVED	R	0h	Reserved
73	RESERVED	R	0h	Reserved
72	RESERVED	R	0h	Reserved
71	RESERVED	R	0h	Reserved
70	RESERVED	R	0h	Reserved
69-67	RESERVED	R	0h	Reserved
66	RESERVED	R	0h	Reserved
65	TX Memory Buffer Empty	R	0h	Transmit memory buffer empty.
64	RESERVED	R	0h	Reserved
63	RESERVED	R	0h	Reserved
62	RESERVED	R	0h	Reserved
61	RESERVED	R	0h	Reserved
61	RESERVED	R	0h	Reserved
60	Moisture Detection	R	0h	Moisture Detection
60	RESERVED	R	0h	Reserved
62-59	RESERVED	R	0h	Reserved
59	RESERVED	R	0h	Reserved
58	RESERVED	R	0h	Reserved
57	RESERVED	R	0h	Reserved
56	RESERVED	R	0h	Reserved
55	RESERVED	R	0h	Reserved
54	RESERVED	R	0h	Reserved
53	RESERVED	R	0h	Reserved
52	RESERVED	R	0h	Reserved
51	RESERVED	R	0h	Reserved
50	RESERVED	R	0h	Reserved
49	RESERVED	R	0h	Reserved
48	RESERVED	R	0h	Reserved
47	RESERVED	R	0h	Reserved
46	Unable to Source Error	R	0h	The Source was unable to increase the voltage to the negotiated voltage of the contract.

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Table 3-6. Interrupt Event for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
45	RESERVED	R	0h	Reserved
44	RESERVED	R	0h	Reserved
43	Plug Early Notification	R	0h	A connection has been detected but not debounced.
42	Sink Transition Completed	R	0h	This event only occurs when in source mode (PD_STATUS.PresentPDRole = 1b). It occurs tSrcTransition (ms) after sending an Accept message to a Request message, just before sending the PS_RDY message.
41-40	RESERVED	R	0h	Reserved
39	Message Data Error	R	0h	An erroneous message was received.
38	Protocol Error	R	0h	An unexpected message was received from the partner device.
37	RESERVED	R	0h	Reserved
36	Missing Get Capabilities Message Error	R	0h	The partner device did not respond to the Get_Sink_Cap or Get_Source_Cap message that was sent.
35	Power Event Occurred Error	R	0h	An OVP, or ILIM event occurred on VBUS. Or a TSD event occurred.
34	Can Provide Voltage or Current Later Error	R	0h	The USB PD Source can provide acceptable voltage and current, but not at the present time. A "wait" message was sent or received.
33	Cannot Provide Voltage or Current Error	R	0h	The USB PD Source cannot provide an acceptable voltage and/or current. A Reject message was sent to the Sink or a Capability Mismatch was received from the Sink.
32	Device Incompatible Error	R	0h	When set to 1, a USB PD device with an incompatible specification version was connected. Or the partner device is not USB PD capable.
31	RESERVED	R	0h	Reserved
30	CMD1 Complete	R	0h	Set whenever a non-zero value in CMD1 register is set to zero or ! CMD.
29-28	RESERVED	R	0h	Reserved
27	PD Status Updated	R	0h	Set whenever contents of PD_STATUS register (0x40) change.
26	Status Updated	R	0h	Set whenever contents of STATUS register (0x1A) change.
25	RESERVED	R	0h	Reserved
24	Power Status Updated	R	0h	Set whenever contents of POWER_STATUS register (0x3F) change.
23	Power Path Switch Changed	R	0h	Set whenever contents of POWER_PATH_STATUS register (0x26) changes.
22	RESERVED	R	0h	Reserved
21	USB Host No Longer Present	R	0h	Set when STATUS.UsbHostPresent transitions to anything other than 11b.
20	USB Host Present	R	0h	Set when STATUS.UsbHostPresent transitions to 11b.
19	RESERVED	R	0h	Reserved
18	Data Swap Requested	R	0h	A DR swap was requested by the Port Partner.
17	Power Swap Requested	R	0h	A PR swap was requested by the Port Partner.
16	RESERVED	R	0h	Reserved
15	Sink Cap Message Received	R	0h	
14	Source Capabilities Message Received	R	0h	This is asserted when a Source Capabilities message is received from the Port Partner.
13	New Contract as Provider	R	0h	An RDO from the far-end device has been accepted and the PD Controller is a Source. This is asserted after the PS_RDY message has been sent. See ACTIVE_CONTRACT_PDO register (0x34) and ACTIVE_CONTRACT_RDO register (0x35) for details.

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Table 3-6. Interrupt Event for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	New Contract as Consumer	R	0h	Far-end source has accepted an RDO sent by the PD Controller as a Sink. See ACTIVE_CONTRACT_PDO register (0x34) and ACTIVE_CONTRACT_RDO register (0x35) for details.
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	Data Swap Complete	R	0h	A Data Role swap has completed. See STATUS register (0x1A) and PD_STATUS register (0x40) for port state.
4	Power Swap Complete	R	0h	A Power role swap has completed. See STATUS register (0x1A) and PD_STATUS register (0x40) for port state.
3	Plug Insert or Removal	R	1h	USB Plug Status has Changed. See Status register for more plug details.
2	RESERVED	R	0h	Reserved
1	PD Hardreset	R	0h	A PD Hard Reset has been performed. See PD_STATUS.HardResetDetails for more information.
0	RESERVED	R	0h	Reserved

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3.5 Interrupt Mask for I2C1 Register (Offset = 16h) [Reset = 0000000F000000CD33380Ah]

Interrupt Mask for I2C1 is shown in Table 3-7.

Return to the Summary Table.

Interrupt mask bit field for INT_EVENT1. A bit in INT_EVENT1 cannot be set if it is cleared in this register. Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-7. Interrupt Mask for I2C1 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	RESERVED	R/W	0h	
78	RESERVED	R/W	0h	
77	RESERVED	R/W	0h	
76	RESERVED	R/W	0h	
75	RESERVED	R/W	0h	
74	RESERVED	R/W	0h	
73	RESERVED	R/W	0h	Reserved
72	RESERVED	R/W	0h	
71	RESERVED	R/W	0h	
70	RESERVED	R/W	0h	
69	RESERVED	R/W	0h	
68	RESERVED	R/W	0h	
67	RESERVED	R/W	0h	
66	RESERVED	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	RESERVED	R/W	0h	
63	RESERVED	R/W	0h	
62	RESERVED	R/W	0h	
61	RESERVED	R/W	0h	Reserved
60	Moisture Detection	R/W	0h	Moisture Detection
59	RESERVED	R/W	0h	
58	RESERVED	R/W	0h	
57	RESERVED	R/W	0h	
56	RESERVED	R/W	0h	
55	RESERVED	R/W	0h	
54	RESERVED	R/W	0h	
53	RESERVED	R/W	0h	
52	RESERVED	R/W	0h	
51	RESERVED	R/W	0h	
50	RESERVED	R/W	0h	
49	RESERVED	R/W	0h	
48	RESERVED	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	
45	RESERVED	R/W	0h	Reserved

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Table 3-7. Interrupt Mask for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
44	RESERVED	R/W	0h	
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	RESERVED	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	Reserved
36	Missing Get Capabilities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	RESERVED	R/W	0h	
30	CMD1 Complete	R/W	1h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	1h	
26	Status Updated	R/W	1h	
25	RESERVED	R/W	0h	
24	Power Status Updated	R/W	1h	
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	1h	
20	USB Host Present	R/W	1h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	1h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	1h	
12	New Contract as Consumer	R/W	1h	
11	RESERVED	R/W	0h	
10	RESERVED	R/W	0h	
9	RESERVED	R/W	0h	
8-7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	
3	Plug Insert or Removal	R/W	1h	
2	RESERVED	R/W	0h	Reserved

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Table 3-7. Interrupt Mask for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PD Hardreset	R/W	1h	
0	RESERVED	R/W	0h	Reserved

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3.6 Interrupt Clear for I2C1 Register (Offset = 18h) [Reset = 00000000000000000000h]

Interrupt Clear for I2C1 is shown in Table 3-8.

Return to the Summary Table.

Interrupt clear bit field for INT_EVENT1. Bits set in this register are cleared from INT_EVENT1. Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-8. Interrupt Clear for I2C1 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	RESERVED	R/W	0h	
78	RESERVED	R/W	0h	
77	RESERVED	R/W	0h	
76	RESERVED	R/W	0h	
75	RESERVED	R/W	0h	
74	RESERVED	R/W	0h	
73	RESERVED	R/W	0h	Reserved
72	RESERVED	R/W	0h	
71	RESERVED	R/W	0h	
70	RESERVED	R/W	0h	
69	RESERVED	R/W	0h	
68	RESERVED	R/W	0h	
67	RESERVED	R/W	0h	
66	RESERVED	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	RESERVED	R/W	0h	
63	RESERVED	R/W	0h	
62	RESERVED	R/W	0h	
61	RESERVED	R/W	0h	Reserved
60	Moisture Detection	R/W	0h	Reserved.
59	RESERVED	R/W	0h	
58	RESERVED	R/W	0h	
57	RESERVED	R/W	0h	
56	RESERVED	R/W	0h	
56-55	RESERVED	R/W	0h	
57-55	RESERVED	R/W	0h	Reserved
55-54	RESERVED	R/W	0h	Reserved
56-54	RESERVED	R/W	0h	Reserved
53	RESERVED	R/W	0h	
52	RESERVED	R/W	0h	
51	RESERVED	R/W	0h	
50	RESERVED	R/W	0h	
49	RESERVED	R/W	0h	
48	RESERVED	R/W	0h	
47	RESERVED	R/W	0h	Reserved

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Table 3-8. Interrupt Clear for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
46	Unable to Source Error	R/W	0h	
45	RESERVED	R/W	0h	Reserved
44	RESERVED	R/W	0h	
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	RESERVED	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	Reserved
36	Missing Get Capabilities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	RESERVED	R/W	0h	
30	CMD1 Complete	R/W	0h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	0h	
26	Status Updated	R/W	0h	
25	RESERVED	R/W	0h	
24	Power Status Updated	R/W	0h	
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	0h	
20	USB Host Present	R/W	0h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	0h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	0h	
12	New Contract as Consumer	R/W	0h	
11	RESERVED	R/W	0h	
10	RESERVED	R/W	0h	
9	RESERVED	R/W	0h	
8-7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	

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Table 3-8. Interrupt Clear for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	Plug Insert or Removal	R/W	0h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	0h	
0	RESERVED	R/W	0h	Reserved

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3.7 Status Register (Offset = 1Ah) [Reset = 0000000000h]

Status is shown in Table 3-9.

Return to the Summary Table.

Status bit field for non-interrupt events.

Table 3-9. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-34	RESERVED	R	0h	Reserved
33-32	RESERVED	R	0h	Reserved
31	RESERVED	R	0h	Reserved
30	SOC Ack Timeout	R	0h	Indicates whether the attached SoC has responded timely. 0h = SoC has responded timely 1h = SoC has not responded timely
29-28	RESERVED	R	0h	Reserved
27	BIST	R	0h	Indicates if a BIST procedure is in progress. 0h = No BIST in progress 1h = BIST in progress
26	RESERVED	R	0h	Reserved
25-24	Acting as Legacy	R	0h	Indicates when PD Controller has gone into a mode where it is acting like a legacy (non PD) device. It can take approximately 10 seconds for the PD controller to determine that it is attached to a legacy source or sink. 0h = PD Controller is not in a legacy (non PD) mode 1h = PD Controller is acting like a legacy sink 2h = PD Controller is acting like a legacy source 3h = Acting as legacy sink due to dead-battery.
23-22	USB Host Present	R	0h	USB host attachment status. 0h = No host present 1h = Attached source is not data capable 2h = Attached source is not USB PD capable 3h = Host present
21-20	VBUS Status	R	0h	Indicates the present state of VBUS. 0h = At vSafe0V (less than 0.8V) 1h = At vSafe5V (4.75V to 5.5V) 2h = Within expected limits 3h = Not within any of the other specified ranges
19-7	RESERVED	R	0h	Reserved
6	Data Role	R	0h	PD controller data role. This is only valid once there is a connection. 0h = Upward-facing port (UFP) 1h = Downward-facing port (DFP)
5	Port Role	R	0h	Current state of PD Controller CCx terminations. This also indicates the PD Controller Power Role, once connected. This bit does not toggle during Unattached.* state transitions. 0h = PD Controller is in the Sink role 1h = PD Controller is Source (CCx pull-up active)
4	Plug Orientation	R	0h	Plug orientation indicator. Indicates port orientation when known (requires connection). 0h = Upside-up orientation (plug CC on CC1) 1h = Upside-down orientation (plug CC on CC2)
3-1	Connection State	R	0h	Details of a connected plug. 0h = No connection 1h = Port is disabled 2h = Audio connection (Ra/Ra) 3h = Debug connection (Rd/Rd) 4h = No connection Ra detected (Ra but no Rd) 5h = Reserved (may be used for Rp/Rp Debug connection) 6h = Connection present no Ra detected 7h = Connection present Ra detected

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Table 3-9. Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Plug Present	R	0h	Status of the plug 0h = No plug is connected 1h = A plug is connected

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3.8 Power Path Status Register (Offset = 26h) [Reset = 0000000000h]

Power Path Status is shown in Table 3-10.

Return to the Summary Table.

Power Path Status.

Table 3-10. Power Path Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-38	Power Source	R	0h	Indicates current PD Controller power source. NOTE: Since the Dead Battery flag forces PD Controller to be powered from VBUS, only 10b is valid when this flag is set. Any other setting indicates that the Dead Battery flag is not set. 0h = Reserved 1h = PD Controller is powered from VIN_3V3 2h = PD Controller is powered from VBUS 3h = Reserved
37-35	RESERVED	R	0h	Reserved
34	PPCable1 Overcurrent	R	0h	PP_CABLE1 overcurrent indicator. Asserted if an overcurrent condition exists on PP_CABLE1 (VCONN).
33-29	RESERVED	R	0h	Reserved
28	PP1 Overcurrent	R	0h	PP_5V1 overcurrent indicator. Asserted if an overcurrent conditions exists on PP1 switch (PP_5V1).
27-21	RESERVED	R	0h	Reserved
20-18	RESERVED	R	0h	Reserved
17-15	RESERVED	R	0h	Reserved
14-12	PP3 Switch	R	0h	Indicates current state of PP3 (PP_EXT1). 0h = PP3 switch disabled 1h = PP3 switch currently disabled due to fault 2h = PP3 switch enabled (system output) 3h = PP3 switch enabled (system input)
11-9	RESERVED	R	0h	Reserved
8-6	PP1 Switch	R	0h	Indicates current state of PP1 switch (PP_5V1). 0h = PP1 switch disabled 1h = PP1 switch currently disabled due to fault 2h = PP1 switch enabled (system output)
5-2	RESERVED	R	0h	Reserved
1-0	PPCable1 Switch	R	0h	Indicates current state of PP_CABLE1 switch. 0h = PP_CABLE1 switch disabled 1h = PP_CABLE1 switch currently disabled 2h = PP_CABLE1 switch CC1 enabled (system output) 3h = PP_CABLE1 switch CC2 enabled (system output)

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3.9 Port Control Register (Offset = 29h) [Reset = 03C15052h]

Port Control is shown in Table 3-11.

Return to the Summary Table.

Configuration bits affecting system policy. These bits may change during normal operation and are used for controlling the respective port. The PD Controller will not take immediate action upon writing. Changes made to this register will take effect the next time the appropriate policy is invoked. Initialized by Application Customization.

Table 3-11. Port Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Charger Detect Enable	R/W	0h	Configure the types of legacy chargers to detect. 0h = Do not detect any legacy chargers 1h = Detect BC 1.2 chargers 2h = Reserved do not use 3h = Detect BC 1.2 and proprietary legacy chargers
29	RESERVED	R/W	0h	Reserved
28-26	Charger Advertise Enable	R/W	0h	Configure the types of legacy chargers to emulate. 0h = Do not emulate any legacy charger 1h = BC 1.2 CDP only 2h = BC 1.2 DCP only 3h = Reserved 4h = Reserved 5h = DCP Auto 1 (2.7V and DCP) 6h = DCP Auto 2 (1.2V 2.7V and DCP) 7h = Reserved
25	RESERVED	R/W	0h	Reserved
24	Resistor 15k Present	R/W	1h	Configure D+ and D- termination. Assert this bit if there is a 15kOhm pull-down on D+ and D- (USB2.0 Host Phy pull-downs enabled). This should not be used for DCP or DCP Auto modes. 0h = System does NOT have 15 kOhm pull-down 1h = System has 15 kOhm pull-down
23	RESERVED	R/W	0h	Reserved
22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	0h	Reserved
20	RESERVED	R/W	0h	Reserved
19	RESERVED	R/W	0h	Reserved
18	RESERVED	R/W	0h	Reserved
17	RESERVED	R/W	0h	Reserved
16	RESERVED	R/W	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	Auto PPS Status Enable	R/W	0h	When this bit is enabled, the PD controller calculates the message field then automatically returns PPS_Status message when a Get_PPS_Status message is received. When this bit is cleared, register value in TX_PPS_SDB(0x7A) prior to clearing the bit is retained until the TX_PPS_SDB is overridden by an external controller.
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved

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Table 3-11. Port Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3-2	RESERVED	R/W	0h	Reserved
1-0	TypeC Current	R/W	2h	Type-C Current advertisement. This setting is ignored if a Source role is not enabled and active. This setting is also ignored during an explicit USB PD contract, where the Rp value is used for collision avoidance as required by the USB PD specification. Note that when PP5V is low, the FW will only use the default Type-C current regardless of the value in this field. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Reserved

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3.10 Boot Flags Register (Offset = 2Dh) [Reset = 0000000000h]

Boot Flags is shown in Table 3-12.

Return to the Summary Table.

Detailed status of boot process. This register provides details on PD Controller boot flags, Customer OTP configuration, and silicon revision

Table 3-12. Boot Flags Register Field Descriptions

Bit	Field	Type	Reset	Description
39-32	Revision ID	R	0h	Revision ID for the PD controller.
31-29	Patch Config Source	R	0h	Source of patch configuration. This field indicates the source of the configuration patch that has been successfully loaded. 0h = No configuration has been loaded 1h = Source-only default configuration 00b 2h = Source-only default configuration 01b 3h = Source-only default configuration 10b 4h = Reserved 5h = A configuration has been loaded from EEPROM 6h = A configuration has been loaded from I2C 7h = Reserved
28-27	RESERVED	R	0h	Reserved
26-25	RESERVED	R	0h	
24	RESERVED	R	0h	Reserved
23-20	RESERVED	R	0h	Reserved
19	System TSD	R	0h	System thermal shut-down indicator. This bit is asserted if the PD controller is rebooting after the system thermal sensor caused a reset.
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16-14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	Patch Download Error	R	0h	Asserted when a patch download error occurs.
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	I2C EEPROM Present	R	0h	EEPROM presence indicator. This bit is asserted when an EEPROM device was discovered on I2C3m during boot.
2	Dead Battery Flag	R	0h	Dead Battery flag indicator. This bit is asserted when the PD Controller booted in dead-battery mode.
1	RESERVED	R	0h	Reserved
0	Patch Header Error	R	0h	Asserted when a patch bundle header errors.

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3.11 Received Source Capabilities Register (Offset = 30h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Received Source Capabilities is shown in Table 3-13.

Return to the Summary Table.

Received Source Capabilties. This register stores latest Source Capabilities message received over BMC.

Table 3-13. Received Source Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-232	RESERVED	R	0h	Reserved
231-200	Source PDO 7	R	0h	Seventh Source Capabilities PDO received
199-168	Source PDO 6	R	0h	Sixth Source Capabilities PDO received
167-136	Source PDO 5	R	0h	Fifth Source Capabilities PDO received
135-104	Source PDO 4	R	0h	Fourth Source Capabilities PDO received
103-72	Source PDO 3	R	0h	Third Source Capabilities PDO received
71-40	Source PDO 2	R	0h	Second Source Capabilities PDO received
39-8	Source PDO 1	R	0h	First Source Capabilities PDO received
7-3	RESERVED	R	0h	Reserved
2-0	Number Valid PDOs	R	0h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

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3.12 Received Sink Capabilities Register (Offset = 31h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Received Sink Capabilities is shown in Table 3-14.

Return to the Summary Table.

Received Sink Capabilities. This register stores latest Sink Capabilities message received over BMC.

Table 3-14. Received Sink Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-232	RESERVED	R	0h	Reserved
231-200	Sink PDO 7	R	0h	Seventh Sink Capabilities PDO received
199-168	Sink PDO 6	R	0h	Sixth Sink Capabilities PDO received
167-136	Sink PDO 5	R	0h	Fifth Sink Capabilities PDO received
135-104	Sink PDO 4	R	0h	Fourth Sink Capabilities PDO received
103-72	Sink PDO 3	R	0h	Third Sink Capabilities PDO received
71-40	Sink PDO 2	R	0h	Second Sink Capabilities PDO received
39-8	Sink PDO 1	R	0h	First Sink Capabilities PDO received
7-3	RESERVED	R	0h	Reserved
2-0	Number Valid PDOs	R	0h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

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3.13 Transmit Source Capabilities Register (Offset = 32h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000058260C844C2AA801h]

Transmit Source Capabilities is shown in Table 3-15.

Return to the Summary Table.

Source Capabilities for sending. This register stores PDOs and settings for outgoing Source Capabilities PD messages. Initialized by Application Customization.

Table 3-15. Transmit Source Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
503-485	RESERVED	R/W	0h	Reserved
484	RESERVED	R/W	0h	Reserved
483	RESERVED	R/W	0h	Reserved
482	RESERVED	R/W	0h	Reserved
481	RESERVED	R/W	0h	Reserved
480	RESERVED	R/W	0h	Reserved
479	RESERVED	R/W	0h	Reserved
478	RESERVED	R/W	0h	Reserved
477	RESERVED	R/W	0h	Reserved
476	RESERVED	R/W	0h	Reserved
475	RESERVED	R/W	0h	Reserved
474	RESERVED	R/W	0h	Reserved
473	RESERVED	R/W	0h	Reserved
472	RESERVED	R/W	0h	Reserved
471-248	RESERVED	R/W	0h	Reserved
247-216	TX Source PDO 7	R/W	0h	Seventh Source Capabilities PDO contents.
215-184	TX Source PDO 6	R/W	0h	Sixth Source Capabilities PDO contents.
183-152	TX Source PDO 5	R/W	0h	Fifth Source Capabilities PDO contents.
151-120	TX Source PDO 4	R/W	0h	Fourth Source Capabilities PDO contents.
119-88	TX Source PDO 3	R/W	0h	Third Source Capabilities PDO contents.
87-56	TX Source PDO 2	R/W	58h	Second Source Capabilities PDO contents.
55-24	TX Source PDO 1	R/W	260C844Ch	First Source Capabilities PDO contents.
23-22	RESERVED	R/W	0h	Reserved
21-20	Power Path for PDO 7	R/W	2h	Configures which PP to use for PDO7. Same format as PowerPathForPDO2.
19-18	Power Path for PDO 6	R/W	2h	Configures which PP to use for PDO6. Same format as PowerPathForPDO2.
17-16	Power Path for PDO 5	R/W	2h	Configures which PP to use for PDO5. Same format as PowerPathForPDO2.
15-14	Power Path for PDO 4	R/W	2h	Configures which PP to use for PDO4. Same format as PowerPathForPDO2.
13-12	Power Path for PDO 3	R/W	2h	Configures which PP to use for PDO3. Same format as PowerPathForPDO2.
11-10	Power Path for PDO 2	R/W	2h	Configures which PP to use for PDO2. 0h = Reserved 1h = Reserved 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO

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Table 3-15. Transmit Source Capabilities Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	Power Path for PDO 1	R/W	0h	Configures which PP to use for PDO1. 0h = PP_5V1 is used for this PDO 1h = PP_5V2 is used for this PDO 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO
7-3	RESERVED	R/W	0h	Reserved
2-0	Number Valid PDOs	R/W	1h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

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3.14 Transmit Sink Capabilities Register (Offset = 33h) [Reset = 0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000091258360C839D04h]

Transmit Sink Capabilities is shown in Table 3-16.

Return to the Summary Table.

Sink Capabilities for sending. This register stores PDOs for outgoing Sink Capabilities USB PD messages. Initialized by Application Customization. The PD controller transmits the contents of this register as a Sink_Capabilities message after receiving a Get_Sink_Cap message unless its configuration or USB PD rules require a different response in the context. Writes to this register have no immediate effect. The PD controller updates and uses this register each time it needs to send a Sink Capabilities message.Each PDO in this TX_SINK_CAPS register follows the definition from the USB PD specification. For more details on the meaning of each field refer to the USB PD specification.

Table 3-16. Transmit Sink Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-232	RESERVED	R/W	0h	Reserved
231-200	TX Sink PDO 7	R/W	0h	Seventh Sink Capabilities PDO contents.
199-168	TX Sink PDO 6	R/W	0h	Sixth Sink Capabilities PDO contents.
167-136	TX Sink PDO 5	R/W	0h	Fifth Sink Capabilities PDO contents.
135-104	TX Sink PDO 4	R/W	0h	Fourth Sink Capabilities PDO contents.
103-72	TX Sink PDO 3	R/W	0h	Third Sink Capabilities PDO contents.
71-40	TX Sink PDO 2	R/W	00091258h	Second Sink Capabilities PDO contents.
39-8	TX Sink PDO 1	R/W	360C839Dh	First Sink Capabilities PDO contents.
7-3	RESERVED	R/W	0h	Reserved
2-0	Number Valid PDOs	R/W	4h	

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3.15 Active PDO Contract Register (Offset = 34h) [Reset = 000000000000h]

Active PDO Contract is shown in Table 3-17.

Return to the Summary Table.

Power data object for active contract. This register stores PDO data for the current explicit USB PD contract, or all zeroes if no contract.

Table 3-17. Active PDO Contract Register Field Descriptions

Bit	Field	Type	Reset	Description
47-42	RESERVED	R	0h	Reserved
41-32	First PDO Control Bits	R	0h	Contains bits 29:20 of the first PDO. It does not matter which PDO was selected, this field is always drawn from the first PDO.
31-0	Active PDO	R	0h	Power data object. This field contains the contents of the PDO Requested by PD Controller as Sink and Accepted by Source, once it is Accepted by Source.

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3.16 Active RDO Contract Register (Offset = 35h) [Reset = 00000000000000000000000h]

Active RDO Contract is shown in Table 3-18.

Return to the Summary Table.

Power data object for the active contract. This register stores the RDO of the current explicit USB PD contract, or all zeroes if no contract.

Table 3-18. Active RDO Contract Register Field Descriptions

Bit	Field	Type	Reset	Description
95-32	RESERVED	R	0h	Reserved
31-28	Object Position	R	0h	As defined by USB PD.
27	Give Back Flag	R	0h	As defined by USB PD.
26	Capability Missmatch	R	0h	As defined by USB PD.
25	USB Communication Capable	R	0h	As defined by USB PD.
24	No USB Suspend	R	0h	As defined by USB PD.
23	Unchunked Supported	R	0h	As defined by USB PD.
22-20	RESERVED	R	0h	Reserved
19-10	Operating Current	R	0h	As defined by USB PD.
9-0	Max Min Operation Current	R	0h	As defined by USB PD.

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3.17 Autonegotiate Sink Register (Offset = 37h) [Reset = 00000000000000000000000000000000000191904114503Eh]

Autonegotiate Sink is shown in Table 3-19.

Return to the Summary Table.

Configuration for sink power negotiations. This register defines the voltage range between which the system can function properly, allowing the PD Controller to negotiate its own contracts. Initialized by Application Customization.

Table 3-19. Autonegotiate Sink Register Field Descriptions

Bit	Field	Type	Reset	Description
191-116	RESERVED	R/W	0h	Reserved
115-105	PPS Output Voltage	R/W	0h	This is the desired output voltage in 20mV units. This is inserted as-is into the Request USB PD message. Note that some PD controllers are unable to turn on the gate-drivers if VBUS less than 3.8V, check the VBUS UVLO value in the data-sheet.
104-103	RESERVED	R/W	0h	Reserved
102-96	PPS Operating Current	R/W	0h	Operation current in Sink PPS mode. This is the desired operating current in 50 mA units. This is inserted as-is into the Request USB PD message.
95-70	RESERVED	R/W	0h	Reserved
69	RESERVED	R/W	0h	Reserved
68	PPS Required Full Voltage Range	R/W	0h	Select only a source with full voltage range. If this bit is asserted, a PPS supply type is not selected unless the APDO.MinVoltage ≤ TX_SINK_CAPS.MinPpsVoltage, APDO.MaxVoltage ≥ TX_SINK_CAPS.MaxPpsVoltage, and APDO.MaxCurrent ≥ TX_SINK_CAPS.MaxPpsCurrent. This bit has no effect unless PPSEnableSinkMode is asserted.
67	PPS Source Operating Mode	R/W	0h	Selection for CV or CC mode. If this bit is set to 1, then the PD controller assumes the system is in constant voltage mode and sets the VBUS disconnect threshold accordingly. If this bit is set to 0, then the PD controller will assume the system is in current limit mode and it will lower the VBUS disconnect threshold accordingly.
66-65	PPS Request Interval	R/W	0h	Sink PPS request interval. This field sets the frequency at which the PD controller will send a new request to the source even if the host has not made any change in the request. 0h = 8 seconds 1h = 4 seconds 2h = 2 seconds 3h = 1 second
64	PPS Enable Sink Mode	R/W	0h	Enable Sink PPS mode. If this bit is asserted, then the PD controller will attempt to negotiate a PPS sink contract. PPS contracts are prioritized over any other supply type.
63-62	RESERVED	R/W	0h	Reserved
61-52	RESERVED	R/W	0h	Reserved
51-42	RESERVED	R/W	0h	Reserved
41-32	RESERVED	R/W	0h	Reserved
31-22	RESERVED	R/W	0h	Reserved
21-12	RESERVED	R/W	0h	Reserved
11-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved

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Table 3-19. Autonegotiate Sink Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

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3.18 SPM Client Control Register (Offset = 3Ch) [Reset = 0036010001000Ah]

SPM Client Control is shown in Table 3-20.

Return to the Summary Table.

Source Policy Manager Client Control register used to allocate power to the port. All PDO voltages are exposed, current for each PDO is adjusted to stay within the allocated power.

Table 3-20. SPM Client Control Register Field Descriptions

Bit	Field	Type	Reset	Description
55-40	SPM Forced Safe State Power	R/W	36h	SPM Force Safe State Power is used to force the port a abolute minimum power. This is triggered by the GPIO DMC_FORCE_SAFE_STATE_EVENT (25 mW per LSB)
39-33	RESERVED	R/W	0h	Reserved
32	Port Disabled By SPM	R/W	1h	SPM Port Disable. Must be cleared to re-enable the port.
31-16	SPM Guaranteed Power	R/W	1h	Guaranteed Power for the port and is recommended to leave this constant and modify only the SPM Allocated Extra Power field. (25 mW per LSB)
15-0	SPM Allocated Extra Power	R/W	Ah	The total power allocated to the port is the SPM Allocated Extra Power + SPM Guaranteed Power. The SPM Allocated Extra Power is modified according to the power capabilities in the system. (25 mW per LSB)

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3.19 Power Status Register (Offset = 3Fh) [Reset = 0000h]

Power Status is shown in Table 3-21.

Return to the Summary Table.

Details about the power of the connection. This register reports status regarding the power of the connection.

Table 3-21. Power Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-8	Charger Advertise Status	R	0h	Charger Advertise Status 0h = Charger advertise disabled or not run 1h = Charger advertisement in process 2h = Charger advertisement complete 3h = Reserved
7-4	Charger Detect Status	R	0h	0h = Charger detection disabled or not run 1h = Charger detection in progress 2h = Charger detection complete none detected 3h = Charger detection complete SDP detected 4h = Charger detection complete BC 1.2 CDP detected 5h = Charger detection complete BC 1.2 DCP detected 6h = Charger detection complete Divider1 DCP detected 7h = Charger detection complete Divider2 DCP detected 8h = Charger detection complete Divider3 DCP detected 9h = Charger detection complete 1.2V DCP detected
3-2	TypeC Current	R	0h	This field is redundant with PD_STATUS.CCPullUp in register 0x40 when SourceSink is 1b. This field is redundant with PORT_CONTROL.TypeCCurrent in register 0x29 when SourceSink is 0b. In the future, this redundant field may be removed. This field is intended for Type-C Sink operation. If the port is connected as source, the field is updated upon initial connection only. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Explicit PD contract sets current
1	SourceSink	R	0h	Source / Sink indicator. This bit is equivalent to PresentPDRole in register 0x40. It is replicated in this register for convenience. In the future, this redundant bit may be removed. 0h = Connection requests power 1h = Connection provides power (PD Controller as sink)
0	Power Connection	R	0h	Asserted if there is a connection. This bit is asserted when PlugPresent is TRUE and ConnState is greater than 5h. So it is redundant with information from register 0x1A. It is replicated in this register for convenience. In the future this redundant bit may be removed. 0h = No connection 1h = Connection present

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3.20 PD Status Register (Offset = 40h) [Reset = 00000000h]

PD Status is shown in Table 3-22.

Return to the Summary Table.

Status of PD and Type-C state-machine. This register contains details regarding the status of PD messages and the Type-C state machine.

Table 3-22. PD Status Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	Data Reset Details	R	0h	Reason for Data Reset. 0h = Reset value: no data reset 0x1=Data Reset message received from port partner 2h = Requested by host: 'DRST'. 3h = Requested by host: DATA_CONTROL 0x4=Exit USB4 following DR_Swap 0x5=Reserved1 0x6=Reserved2 0x7=Reserved3
27-22	Error Recovery Details	R	0h	Reason for Error Recovery 0h = reset value: no error recovery 1h = System: over-temperature shut-down 2h = System: PP5V went low unexpectedly 3h = System: fault input GPIO was asserted 4h = System: Over-voltage detected on the Px_VBUS pin 0x5=Reserved 6h = System: ILIM on PP_5V 7h = System: ILIM on PP_CABLE 8h = System: OVP on CC detected 0x9=Back to Normal System Power State 10h = Protocol error: invalid DR_Swap 0x11=no Good_CRC during a PR_Swap sequence. 0x12=no Good_CRC during a FR_Swap sequence. 0x15=NoResponse timer timed out 0x16=PSSourceOffTimer timed out during PR_Swap 0x17=PSSourceOnTimer timed out during PR_Swap 0x18=PSSourceOnTimer timed out during FR_Swap 0x19=The Type-C source failed to change during FR_Swap 0x1a=SenderResponseTimer timed out during FR_Swap 0x1b=PSSourceOffTimer timed out during FR_Swap 1Ch = Policy Engine: Error reaching the Attached 20h = HI: PortConfig 21h = HI: Error with DATA_CONTROL 22h = HI: Swapping error during dead-battery 0x23=Host updated the GLOBAL_SYSTEM_CONFIG 24h = HI: Host issued the 4CC 'GAID' command 25h = HI: Host issued the 4CC 'Gaid' command 26h = HI: Host issued the 4CC 'DISC' command 0x27=Host issued a reset using the 'UCSI' 30h = Type-C: an error occurred in the Attached 31h = Type-C: VCONN failed to discharge 0x32=System Power State 0x33=Host Data Control USB disable 0x34=SPM Client Port disable changed 0x35=GPIO event TypeC disable 0x36=CC OVP 0x37=SBU_OVP 0x38=SBU_RX_OVP

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Table 3-22. PD Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	Hard Reset Details	R	0h	Reason for Hard Reset 0h = Reset value no hard reset 1h = Received from Port Partner 2h = Requested by host 3h = Invalid DR_Swap request during Active Mode 4h = DischargeFailed. 5h = NoResponseTimeOut. 6h = SendSoftReset. 7h = Sink_SelectCapability. 8h = Sink_TransitionSink. 9h = Sink_WaitForCapabilities. Ah = SoftReset. Bh = SourceOnTimeout. Ch = Source_CapabilityResponse. Dh = Source_SendCapabilities. Eh = SourcingFault. Fh = UnableToSource. 10h = FRS failure 11h = Unexpected message 12h = Failure to to complete the VCONN recovery sequence within 200ms after PP5V rising edge
15-13	RESERVED	R	0h	Reserved
12-8	Soft Reset Details	R	0h	Reason for Soft Reset 0h = Reset value no soft reset 1h = Soft reset received from Port Partner 2h = Reserved 3h = Reserved 4h = Received source capabilities message was invalid 5h = Message retries were exhausted 6h = Received an accept message unexpectedly 7h = Received a control message unexpectedly 8h = Received a GetSinkCap message unexpectedly 9h = Received a GetSourceCap message unexpectedly Ah = Received a GotoMin message unexpectedly Bh = Received a PS_RDY message unexpectedly Ch = Received a Ping message unexpectedly Dh = Received a Reject message unexpectedly Eh = Received a Request message unexpectedly Fh = Received a Sink Capabilities message unexpectedly 10h = Received Source Capabilities message unexpected 11h = Received a Swap message unexpectedly 12h = Received a Wait Capabilities message unexpectedly 13h = Received an unknown control message 14h = Received an unknown data message 15h = To initialize SOP' controller in plug 16h = To initialize SOP'' controller in plug 17h = Received an Extended message unexpectedly 18h = Received an unknown Extended message 19h = Received a data message unexpectedly 1Ah = Received a Not Supported message unexpectedly 1Bh = Received a Get_Status message unexpectedly
7	RESERVED	R	0h	Reserved
6	Present PD Role	R	0h	Present PD power role. The PD Controller is acting under this PD power role. 0h = Sink 1h = Source
5-4	Port Type	R	0h	Present Type-C power role. The PD Controller is acting under this Type-C power role. 0h = Sink/Source 1h = Sink 2h = Source 3h = Source/Sink

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Table 3-22. PD Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	CC Pullup	R	0h	CC Pull-up value. The pull-up value detected by PD Controller when in CC Pull-down mode. 0h = Not in CC pull-down mode / no CC pull-up detected 1h = USB Default current 2h = 1.5 A (SinkTxNG) 3h = 3.0 A (SinkTxOK)
1-0	RESERVED	R	0h	Reserved

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3.21 Type C State Register (Offset = 69h) [Reset = 00000000h]

Type C State is shown in Table 3-23.

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Contains current status of both CCn pins.

Table 3-23. Type C State Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TypeC Port State	R	0h	Present state of Type-C state-machine. 0h = Disabled 5h = ErrorRecovery 24h = Unattached.Accessory 2Bh = AttachWait.Accessory 45h = Try.SRC 4Eh = TryWait.SNK 4Fh = Try.SNK 50h = TryWait.SRC 60h = Attached.SRC 61h = Attached.SNK 62h = AudioAccessory 63h = DebugAccessory 64h = AttachWait.SRC 65h = AttachWait.SNK 66h = Unattached.SNK 67h = Unattached.SRC
23-16	CC2 Pin State	R	0h	State of CC2 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only) 3h = USB Default Advertisement detected (SInk only) 4h = 1.5A Advertisement detected (Sink Only) 5h = 3.0A Advertisement detected (Sink Only)
15-8	CC1 Pin State	R	0h	State of CC1 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only) 3h = USB Default Advertisement detected (SInk only) 4h = 1.5A Advertisement detected (Sink Only) 5h = 3.0A Advertisement detected (Sink Only)
7-0	CC Pin for PD	R	0h	CC pin used for PD communication. 0h = Not connected 1h = CC1 is used for USB PD communication 2h = CC2 is used for USB PD communication

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3.22 Sleep Control Register (Offset = 70h) [Reset = 01h]

Sleep Control Register is shown in Table 3-24.

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Sleep configurations.

Table 3-24. Sleep Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2-1	Sleep Time	R/W	0h	Minimum time the PD controller waits before entering sleep mode. 0h = Reserved 1h = 100 ms 2h = 1200 ms 3h = Reserved
0	Sleep Mode Allowed	R/W	1h	If this bit is asserted the PD controller will enter sleep modes after device is idle for Sleep Time.

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3.23 GPIO Status Register (Offset = 72h) [Reset = 0000000000000000h]

GPIO Status is shown in Table 3-25.

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Captures status and settings of all GPIO pins. Check the device-specific data sheet for the available GPIO because it may vary by device type.

Table 3-25. GPIO Status Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39	GPIO 7 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
38	GPIO 6 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
37	GPIO 5 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
36	GPIO 4 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
35	GPIO 3 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
34	GPIO 2 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
33	GPIO 1 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
32	GPIO 0 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
31-13	RESERVED	R	0h	Reserved
12	GPIO 12 Data	R	0h	Asserted if a logic high is detected on the GPIO.
11-8	RESERVED	R	0h	Reserved
7	GPIO 7 Data	R	0h	Asserted if a logic high is detected on the GPIO.
6	GPIO 6 Data	R	0h	Asserted if a logic high is detected on the GPIO.
5	GPIO 5 Data	R	0h	Asserted if a logic high is detected on the GPIO.
4	GPIO 4 Data	R	0h	Asserted if a logic high is detected on the GPIO.
3	GPIO 3 Data	R	0h	Asserted if a logic high is detected on the GPIO.
2	GPIO 2 Data	R	0h	Asserted if a logic high is detected on the GPIO.
1	GPIO 1 Data	R	0h	Asserted if a logic high is detected on the GPIO.
0	GPIO 0 Data	R	0h	Asserted if a logic high is detected on the GPIO.

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3.24 Moisture Detection Config Register (Offset = 98h) [Reset = 5500000000000D0h]

Moisture Detection Config is shown in Table 3-26.

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Moisture Detection Configuration

Table 3-26. Moisture Detection Config Register Field Descriptions

Bit	Field	Type	Reset	Description
56	Moisture Detection State	R/W	0h	Moisture Detection State
55-52	RESERVED	R/W	0h	Reserved
51-48	RESERVED	R/W	0h	Reserved
47-40	RESERVED	R/W	0h	Reserved
39-32	RESERVED	R/W	0h	Reserved
31-24	RESERVED	R/W	0h	Reserved
23-16	RESERVED	R/W	0h	Reserved
15-8	RESERVED	R/W	0h	Reserved
7-4	RESERVED	R/W	0h	Reserved
3-0	RESERVED	R/W	0h	Reserved

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Chapter 4

4CC Task Detailed Descriptions

4.1 Overview

This section describes the 4CC Tasks defined by the PD Controller Host Interface. The Tasks are categorized into various sub-groups in this section. All Tasks that return data using the DATAx registers will always ensure the proper output data is loaded into those registers before setting the CMDx register to 0 to indicate Task completion. DATAx is never modified by PD Controller after CMDx has been changed to 0, to ensure the Host can retrieve data from the previously-executed Task, and to ensure the Host can load these registers for a future Task without risk of overwriting. Note that other registers can continue to be updated after a Task completes, as Tasks can have additional side effects.

Many of the Tasks return a status code in the first byte of the DATAx register. The standard Task response byte is defined in Table 4-1. The remaining DATAx bytes can be used at each Task's discretion.

Table 4-1. Standard Task Response

Description	**Tasks are a special form of Tasks that return a status code in the first byte of the DATAX register.**			
Output DATAX	**Bit**	**Name**	**Description**	
	Byte 1: Task Return Code			
	7:4	Reserved	Reserved for standard Tasks. May be used by certain Tasks for Task-specific return codes. Successful return codes can use this byte provided TaskResult is 0x0.	
	3:0	TaskResult	Standard Task return codes.	
			0x0	Task completed successfully.
			0x1	Task timed-out or aborted by 'ABRT' Request.
			0x2	Reserved.
			0x3	Task rejected.
			0x4	Task rejected because the Rx Buffer was locked. This is for Tasks that can require the PD controller to use the Rx Buffer.
			0x5-0xF	Reserved for standard Tasks. May be used by certain Tasks for Task-specific error codes. Treated as an error when encountered.

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4.2 CPU Control Tasks

4.2.1 'Gaid' - Return to Normal Operation

Table 4-2. 'Gaid' - Return to Normal Operation

Description	The 'Gaid' Task causes a warm restart of the PD Controller processor.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete.
Side Effects	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
Additional Information	The PD controller is in the 'APP ' mode, then it immediately goes to the Error Recovery state then after delaying 1 second (typical) it does a warm restart.

4.2.2 'GAID' - Cold Reset Request

Table 4-3. 'GAID' - Cold Reset Request

Description	The 'GAID Task causes a cold restart of the PD Controller processor.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete. This Task forces the PD Controller to reboot its OTP bootloader.
Side Effects	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
Additional Information	The PD controller immediately goes to the Error Recovery state, then after delaying 1 second (typical) it does a cold restart.

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4.3 PD Message Tasks

4.3.1 'SWSk' - PD PR_Swap to Sink

Table 4-4. 'SWSk' - PD PR_Swap to Sink

Description	The 'SWSk' Task instructs PD Controller to attempt to become a Sink through PR_Swap at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SWSk' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the Source. The 'SWSk' Task shall be considered rejected if: • The Source indicated through Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The 'SWSk' Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The 'SWSk' Task shall be considered successful if: • PD Controller is already in the Sink power role. • The PR_Swap is Accepted and completes normally.
Side Effects	When the 'SWSk' Task completes successfully PD Controller will have transitioned to the Sink power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

4.3.2 'SWSr' - PD PR_Swap to Source

Table 4-5. 'SWSr' - PD PR_Swap to Source

Description	The 'SWSr' Task instructs PD Controller to attempt to become a Source through PR_Swap at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SWSr' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the Sink. The 'SWSr' Task shall be considered rejected if: • The Sink previously indicated through Sink or Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The 'SWSr' Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The 'SWSr' Task shall be considered successful if: • PD Controller is already in the Source power role. • The PR_Swap is Accepted and completes normally.
Side Effects	When the 'SWSr' Task completes successfully PD Controller will have transitioned to the Source power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

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4.3.3 'SWDF' - PD DR_Swap to DFP

Table 4-6. 'SWDF' - PD DR_Swap to DFP

Description	**The 'SWDF' Task instructs PD Controller to attempt to become a DFPthrough DR_Swap at the first opportunity while maintaining policy enginecompliance. If there are any active Alternate Modes as a UFP PD Controller willattempt to exit those Modes first before sending the DR_Swap.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SWDF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the DFP. The 'SWDF' Task shall be considered rejected if: • The UFP indicated through Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWDF' Task shall be considered successful if: • PD Controller is already in the DFP data role. • The DR_Swap is Accepted and completes normally.
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the DFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

4.3.4 'SWUF' - PD DR_Swap to UFP

Table 4-7. 'SWUF' - PD DR_Swap to UFP

Description	**The 'SWUF' Task instructs PD Controller to attempt to become a UFPthrough DR_Swap at the first opportunity while maintaining policy enginecompliance. If there are any active Alternate Modes as a DFP PD Controller willexit those Modes first before attempting the DR_Swap.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SWUF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the UFP. The 'SWUF' Task shall be considered rejected if: • The DFP indicated through Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWUF' Task shall be considered successful if: • PD Controller is already in the UFP data role. • The DR_Swap is Accepted and completes normally.
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the UFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

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4.3.5 'GSkC' - PD Get Sink Capabilities

Table 4-8. 'GSkC' - PD Get Sink Capabilities

Description	The 'GSkC' Task instructs PD Controller to issue a Get_Sink_Capmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'GSkC' Task completes either when the Sink Capabilities message is received or the Task otherwise fails. • The Port Partner is a Source and indicated it was not Dual-Role Power. • The Port Partner responds to the Get_Sink_Cap message with a Reject or Not_Supported message. The 'GSkC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'GSkC' Task shall be considered successful if: • The Get_Sink_Cap message is sent, GoodCRC'ed and a Sink Capabilities response is received and processed.
Side Effects	When the 'GSkC' Task completes successfully the *RX_SINK_CAPS* register (0x31) will have been updated.
Additional Information	None

4.3.6 'GSrC' - PD Get Source Capabilities

Table 4-9. 'GSrC' - PD Get Source Capabilities

Description	The 'GSrC' Task instructs PD Controller to issue a Get_Source_Capmessage to the Port Partner device at the first opportunity while maintainingpolicy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'GSrC' Task completes either when the Source Capabilities message is received or the Task otherwise fails. The 'GSrC' Task shall be considered rejected if: • The Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power. • The Port Partner responds to the Get_Source_Cap message with a Reject or Not_Supported message. The 'GSrC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'GSrC' Task shall be considered successful if: • The Get_Source_Cap message is sent, GoodCRC'ed and a Source Capabilities response is received and processed.
Side Effects	When the 'GSrC' Task completes successfully the *RX_SOURCE_CAPS* register (0x30) will have been updated.
Additional Information	None

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4.3.7 'SSrC' - PD Send Source Capabilities

Table 4-10. 'SSrC' - PD Send Source Capabilities

Description	**The 'SSrC' Task instructs the PD Controller to send a SourceCapabilities message at the first opportunity while maintaining policy enginecompliance.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SSrC' Task completes either when the Sink Capabilities message GoodCRC is received or the Task otherwise fails. The 'SSrC' Task shall be considered rejected if: • PD Controller is not in a Source role. The 'SSrC' Task shall be considered timed-out if: • The Source Capabilities message was sent but no GoodCRC was received. The 'SSrC' Task shall be considered successful if: • The Source Capabilities message was sent and a GoodCRC is received.
Side Effects	Other registers can change as a result of the contract negotiation that begins with the new Source Capabilities message.
Additional Information	None

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4.4 Patch Bundle Update Tasks

The following tasks are used for updating a Patch Bundle.

4.4.1 'PBMs' - Start Patch Burst Mode Download Sequence

Table 4-11. 'PBMs' - Start Patch Burst Download Sequence

Description	**The 'PBMs' Task starts the patch loading sequence. This Task initializes the firmware in preparation for a patch bundle load sequence and indicates what the patch bundle will contain.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	Byte 6: Burst Mode Timeout			
	7:6	Reserved		
	5:0	Timeout value	Timeout value for this task. A non-zero value must be used, it is recommended to always use 0x32 in this field (5 seconds) (LSB of 100ms).	
	Byte 5: I2C target for downloading patch.			
	7	Reserved		
	6:0	I2C Target Address	The following target addresses are not valid: • 0x00 • The I2Ct target address of any port selected using the ADCINx pins. Refer to data-sheet.	
	Bytes 0-3: Low Region Binary bundle size in of bytes: [Byte4, Byte3, Byte2, Byte1]			
	39:32	Byte4 of bundle size		
	31:24	Byte3 of bundle size		
	23:16	Byte2 of bundle size		
	15:8	Byte1 of bundle size		
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	PatchStartStatus	Status of the patch start.	
			0x00	Patch start success
			0x04	Invalid bundle size
			0x05	Invalid target address
			0x06	Invalid Timeout value
Task Completion	The 'PBMs' Task completes after output has a valid PatchStartStatus. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.			
Side Effects	When the 'PBMs' is successful, the second target address will be set to the input value.			
Additional Information	The host can only issue a 'PBMs' Task to the I2Ct port of the PD controller. If the host issues 'PMBs' a second time, then the PD controller ignores the DATAX input, restarts the burst-mode timer, and resets the pointer to the beginning of the patch space in RAM. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMs' Task.			

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4.4.2 'PBMc' - Patch Burst Mode Download Complete

Table 4-12. 'PBMc' - Patch Burst Download Complete

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**			
INPUT DATAX	None			
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	319:288	acCalculatedCRC	The CRC calculated in FW for the configuration data.	
	287:256	acTransferredCRC	The CRC transferred along with the configuration data	
	255:240	Reserved	reads as 0	
	239:224	acIndicatedDataSize	The indicated DataSize in the transferred configuration data.	
	223:216	acHeaderVersion	The indicated header version in the transferred configuration data.	
	215:208	acFailCode	An error code indicating why the app config data failed to apply, if it failed to apply	
			0x00	AC_FAIL_NONE: No failure
			0x01	AC_FAIL_WRONG_HEADER_VERSION: The header version is expected to be 1 and was not
			0x02	AC_FAIL_TOO_MUCH_DATA: The DataSize field indicates that you are trying to load more configuration data that there is allocated SRAM for
			0x03	AC_FAIL_CRC_CHECK_FAIL: The CRC comparison failed
	207:200	acState	The current internal state of the AppConfig state machine	
			0x00	AC_NODATA: No configuration data found yet, because we haven't started looking
			0x01	AC_LOADING_DEFAULT: Attempting to load configuration data from a factory default
			0x02	AC_LOADING_SRAM: Attempting to load configuration data from SRAM
			0x03	AC_LOADING_FLASH: Attempting to load configuration data from Flash
			0x04	AC_LOADING_I2C: Attempting to load configuration data from I2C
			0x05	AC_LOADING_DONE: Done loading configuration data, we found valid data
			0x06	AC_ERROR: A generic error state
			0x07	AC_DONE_SUCCESS: Completely done with the app customization process and the records were applied successfully.
			0x08	AC_DONE_FAIL: Completely done with the app customization process and the records were not applied
	199:192	configBundleGood	1 if the top-level state machine found a valid configuration bundle, otherwise 0.	
	191:160	rpRomVersionExpected	The romVersionExpected in the transferred bundle's patch header	
	159:144	rpBundleTotalSize	The bundleTotalSize in the transferred bundle's patch header	
	143:128	rpBundleFlags	The bundleFlags in the transferred bundle's patch header	
	127:96	rpPatchBodyCrc	The patchBodyCrc in the transferred bundle's patch header	
	95:64	rpPatchHeaderCrc	The patchHeaderCrc in the transferred bundle's patch header	

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Table 4-12. 'PBMc' - Patch Burst Download Complete (continued)

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**			
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	55:48	rpBundleSignature	The bundleSignature in the transferred bundle's patch header	
	47:40	rpState	The current internal state of the RomPatch state machine.	
			0x00	RP_NOPATCH: No patch has been loaded
			0x01	RP_LOADING: In the process of loading patch data
			0x02	RP_LOADINGDONE: All patch data has been received
			0x03	RP_RUNNING: A patch has been loaded and is running. Could also indicate that a NULL patch is active.
			0x04	RP_EARLYLOAD_SKIPPED: Indicates that the early boot process does not need to wait for a patch over I2C
			0x05	RP_UARTBOOTED: Checking for a patch in RAM
			0x06	RP_ERROR: A generic error state
	39:32	patchBundleGood	0x01 if the top-level state machine found a good ROM patch, otherwise 0x00.	
	31:24	AppConfigPatchCompleteStatus	0x00	
			0x40	Warning
			0x80	Failure
	23:16	DevicePatchCompleteStatus	A return code indicating whether the RomPatch state machine executed successfully. This value is always valid, and reflective of the internal state of the RomPatch mechanism, but must only be considered if the bundle transferred did in fact include patch data.	
			0x00	Success
			0x20	Not ready
			0x40	Not a patch
			0x41	Patch header checksum mismatch
			0x42	Patch not compatible with this version of ROM
			0x43	Patch code checksum mismatch
			0x44	Null patch received
			0x45	Error patch received
	15:8	cpReturn	Always returns success, there is no way for it to fail.	
	Byte 1: Return Code			
	7:4	rpReturnIndicator	The most significant nibble of the rpReturn value.	
			0x0	Success
			0x2	Informational
			0x4	Warning
			0x8	Error
	3:0	acReturnIndicator	The most significant nibble of the acReturn value.	
			0x0	Success
			0x2	Informational
			0x4	Warning
			0x8	Error
Task Completion	The 'PBMc' Task completes as output has a valid DevicePatchCompleteStatus and AppConfigPatchCompleteStatus. This Task is rejected if the DATAX input does not contain the total patch size. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.			

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Table 4-12. 'PBMc' - Patch Burst Download Complete (continued)

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**
Side Effects	Before this Task completes it will change the I2C target address from the patch address back to the normal value. Upon successful completion of this Task the PD controller will change the MODE register (0x03) to 'APP ' and move to the application mode.
Additional Information	When the CMD1 register goes to 0 check the Output DATAX register for status. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMc' Task.

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4.4.3 'PBMe' - End Patch Burst Mode Download Sequence

Table 4-13. 'PBMe' - Patch Burst Mode Exit

Description	The 'PBMe' Task ends the patch loading sequence. This Task instructs the PD controller to complete the patch loading process.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'PBMe' Task completes after it has ended the patch loading sequence. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.
Side Effects	When the 'PBMe' is successful, the second target address will be restored to the value configured by the ADCINx pins. The PD controller leaves the MODE register (0x03) as 'PTCH' and will wait for the patching process to restart.
Additional Information	If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMe' Task.

4.4.4 'GO2P' - Go to Patch Mode

Table 4-14. 'GO2P' - Forces PD Controller to Return to 'PTCH' Mode and Wait for Patch Over I2C

Description	The 'GO2P' Task causes the PD controller to re-enter the patch mode (MODE = 'PTCH').
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'GO2P' Task completes after the PD controller has re-entered the patch mode. • If the PD controller has re-entered the patch mode and the MODE register reads as 'PTCH'. The 'GO2P' Task is considered rejected if: • The PD controller did not enter the 'APP ' mode without receiving a patch over I2C. • BOOT_STATUS.PatchConfigSource does not read as 3h or 4h.
Side Effects	When the 'GO2P' Task is successful, the MODE register will read as 'PTCH' and the USB PD PHY will be disabled. The PD Controller can temporarily NAK I2C transactions. The host must wait for the IRQ signal to assert (because INT_EVENT1.ReadyForPatch is asserted), and then push the patch as soon as possible.
Additional Information	The 'GO2P' Task must only be used when the ADCINx configuration option NegotiateHighVoltage is used.

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4.5 System Tasks

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4.5.1 'DBfg' - Clear Dead Battery Flag

Table 4-15. 'DBfg' - Clear Dead Battery Flag

Description	The 'DBfg' Task is used to clear the dead battery flag. This Task does not disable the PP_EXT input switch that can have been enabled during dead battery operation.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	The 'DBfg' Task completes after the effects of clearing the Dead Battery Flag are complete.
Side Effects	The Dead Battery Flag causes the PD Controller to take specific actions, so clearing this flag will have side effects. PD Controller 's power input is forced to VBUS until the Dead Battery Flag is cleared, so executing this Task will change PD Controller 's power input.
Additional Information	None

There are several limitations placed on the PD controller while the Dead-Battery Flag is asserted (PowerPathStatus.PowerSource = 10b).

- Fast-Role swap is not supported (on either port).
- A Hard Reset will not be transmitted while in the sink role (on either port).
- VBUS is selected as the main supply for the PD controller, even if the 3.3 V input is present.
- The PD controller will reject PR_Swap requests to become source (on either port).
- The 2nd port in the PD controller that is unconnected will only offer the USB Type-C Default Rp (PortControl.TypeCCurrent is ignored) if it connects as a source.
- A port connected to a source will only act as a Type-C sink regardless of the configuration.
- If no Source Capabilities message is received after the boot process is complete (Status.ActingAsLegacy=11b), the PD controller will not send a Hard Reset until the Dead-Battery Flag is cleared even if the SinkWaitCapTimer expires.

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4.5.2 'I2Cr' - I2C Read Transaction

Table 4-16. 'I2Cr' - Executes I2C Read Transaction on I2Cc

Description	**The 'I2Cr' task can be used to cause the PD controller to read from a specified target address and register offset using a I^2C read transaction through the I2Cc_SDA and I2Cc_SCL pins.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Byte 3: Number of bytes to read from the target.		
	7:0	NumBytes	
	Byte 2: Register offset to use in the I2C read transaction.		
	7:0	RegisterOffset	
	Byte 1: Target Address		
	7	Reserved	
	6:0	Target to use for the transaction.	
OUTPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 2-65: Data Bytes read from the target (in order received)		
	511:0	Data	
	Byte 1: Standard Task Return Code. See also Table 4-1.		
Task Completion	The PD controller completes after it has successfully read the specified number of bytes, or the I^2C transaction terminated for some other reason.		
Side Effects	This task causes the PD controller to issue a command on the I2Cc port. It can result in INT_EVENTx.I2CControllerNACKed being asserted.		
Additional Information	None		

4.5.3 'I2Cw' - I2C Write Transaction

Table 4-17. 'I2Cw' - Executes I2C Write Transaction on I2Cc

Description	**The 'I2Cw' task can be used to cause the PD controller to write a particular I^2C transaction using I2Cc_SDA and I2Cc_SCL.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 5-14: Payload for the I2C transaction		
	Byte 4: Register Offset for the I2C transaction		
	7:0	Register offset	
	Bytes 2-3: Length		
	15:8	Reserved	
	7:0	Number of bytes in the transaction payload.	
	Byte 1: Target Address		
	7	Reserved	
	6:0	Target to use for the transaction.	
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.		
Task Completion	The PD controller maintains a queue of transactions to send on the I2Cc port. If the PD controller has been configured to send transactions upon certain events, it is possible there is a transaction in the queue when the 'I2Cw' task is received. In that case the task will complete successfully after the transaction is inserted into the queue. If the PD controller fails to insert the task into the queue for any reason, the task is rejected. Therefore, when this task is completed successfully it does not guarantee that the I2C transaction is complete. If possible, the host must use the 'I2Cr' 4CC task to confirm the write was successful.		
Side Effects	When successful, this task will cause the PD controller to issue a command on the I2Cc port. This can result in INT_EVENTx.I2CControllerNACKed being asserted.		
Additional Information	If the DATAX register is written with more than 14 bytes, all bytes beyond byte 14 are ignored. The PD controller has a limit on the maximum length of the I^2C write transaction. The 'I2Cw' ommand cannot be sent within 5s from sending a previous 'I2Cw' command. This allows the PD controller to complete all I2C transactions.		

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5.1 PD Controller Application Customization

The PD Controller application binary can be pushed over I2C using the I2Ct port, or the PD controller can read it from an external EEPROM at target address 0x50 on the I2Cc port. The PD Controller application binary provides a way to customize and initialize the settings of the PD Controller. It allows for any register bit accessible through the Host Interface to be changed *before* the PD Controller application starts normal operation, to configure system-related settings that must be correct before any application decision is made. TI provides a GUI tool to create the PD Controller application binary.

5.2 Loading a Patch Bundle

The patch bundle can contain Application Customization data and a Patch binary that modifies the default application firmware in the PD controller. This section will describe how the host can load the patch bundle. The host uses the I2Ct bus for all transactions related to loading the patch bundle. As noted in the flow diagram below, the I2C target address varies depending upon which mode the PD controller is in. The Patch Burst Mode allows the host to push the Patch Bundle to multiple PD controllers simultaneously.

The following flow diagram illustrates the normal successful patch loading process. Other error handling steps can be necessary depending upon the nature of the errors encountered for a particular system. The EC can reset and restart the patch process by issuing a 'PBMe' 4CC Task.

The PD controller can listen for I2C transactions on two unique target addresses on each I2C port. The following table summarizes the target addresses in the different modes of operation. GLOBAL_SYSTEM_CONFIG for the I2C2s bus.

Table 5-1. Use of Target Addresses During Different Modes of Operation

MODE Register Read-Back Value	I2Ct
	Target Address 1
'BOOT'	As configured by ADCINx pins. This is the "Fundamental" I2C target address. BOOT indicates that the PD controller is in the boot stage due to a bad firmware image or incorrect ADCINx settings. APP indicates that the firmware has successfully loaded and is in normal operation. PTCH indicates that the PD controller is waiting for a patch or is in the patch process using the PBMx commands.
'PTCH'(1)	
'APP '(2)	

(1) A successful 'PBMs' Task puts the PD controller into the 'PTCH' mode.
(2) A successful 'PBMc' Task puts the PD controller into the 'APP ' mode.

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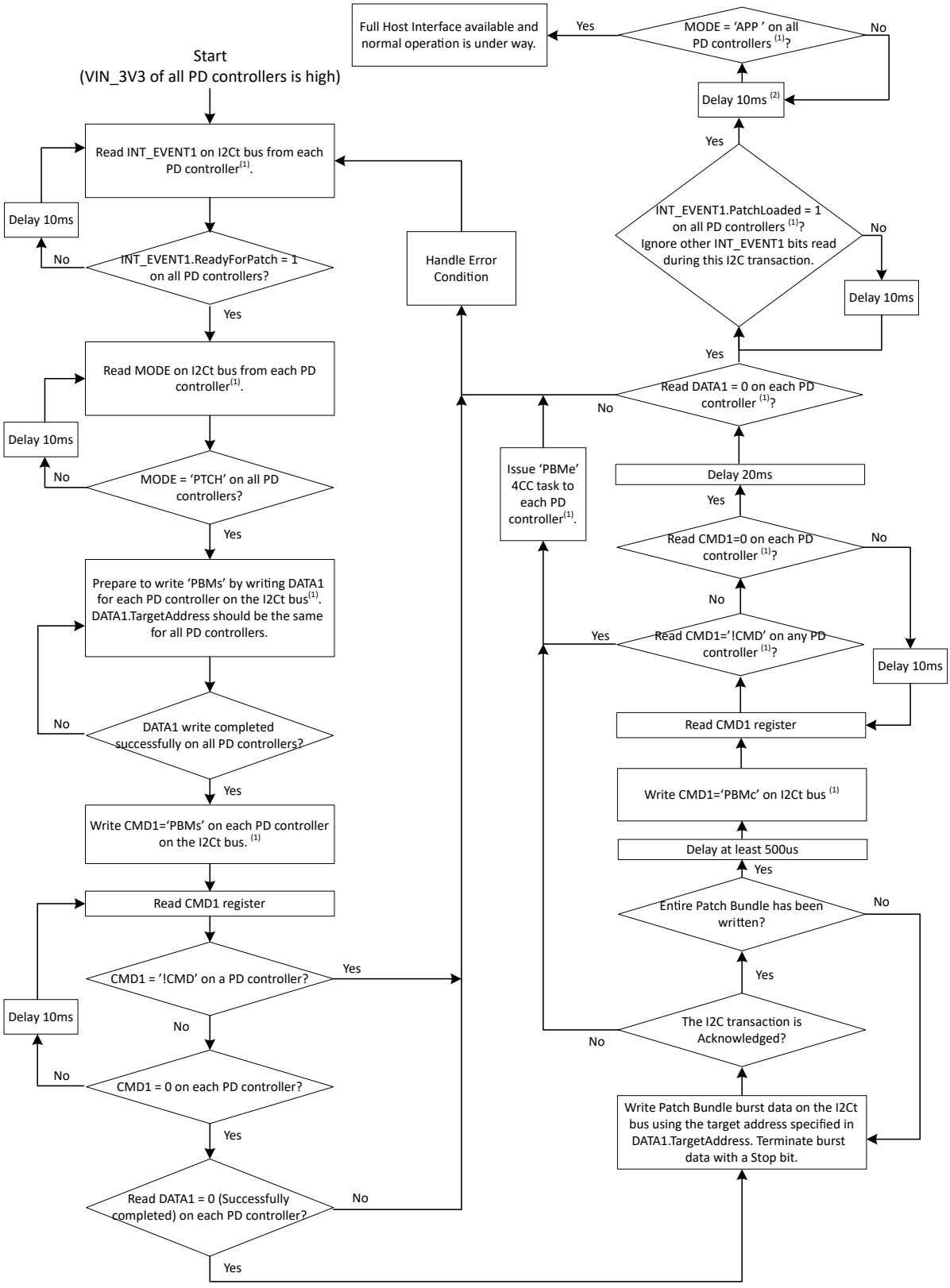

(1) Use the fundamental I2C target address of each PD controller.
(2) This delay before reading the MODE register, is optional but recommended.

Figure 5-1. Flow for Pushing a Patch Bundle Over the I2Ct Bus to Multiple PD Controllers at the Same Time

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While the host is writing the Patch Bundle burst data, the I2C protocol in the following figure must be followed. The host can send the entire Patch Bundle in a single I2C transaction, or it can break it up into multiple transactions. The PD controller increments the pointer into its patch memory space with each byte received on the Patch Target address that was configured by DATA1.TargetAddress as part of the 'PBMs' 4CC Task. The EC can re-issue a 'PBMs' 4CC Task or it can issue a 'PBMe' 4CC Task in order to reset the pointer.

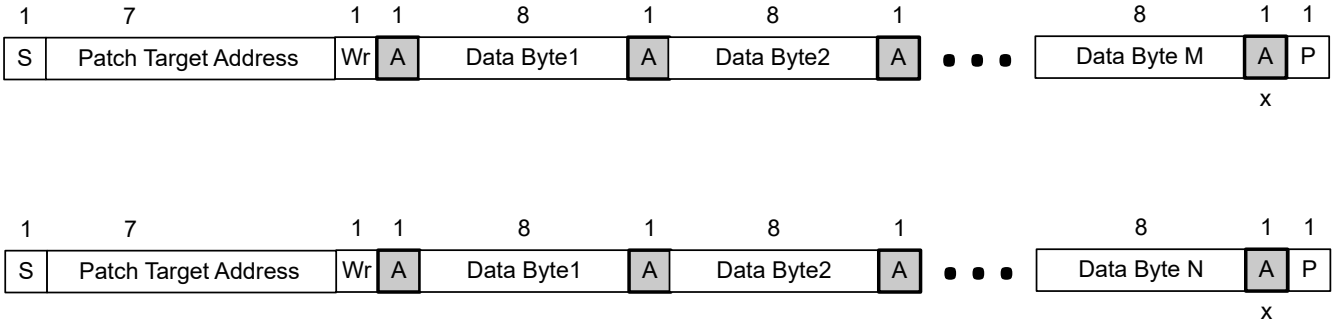

Figure 5-2. Protocol of Patch Bundle Burst Data Assuming it is Broken Into Two Transactions

5.3 GPIO Events

Table 5-2. GPIO Events

Event #	Event Name	I/O	Description
158	WAIT_nPG	I	GPIO from battery charger to indicate to the PD controller can communicate over I2C during a dead battery power up condition.
157	MOISTURE_DETECTED	O	GPIO is asserted when moisture is detected on the SBU1/2 pins. When moisture is no longer detected on the SBU1/2 pins the GPIO will be de-asserted.
156	MOISTURE_NMOS_CONTROL	O	GPIO used to enable the NMOS in the external moisture detection circuit. The GPIO will toggle during moisture detection.
155	MOISTURE_PMOS_CONTROL	O	GPIO used to enable the PMOS in the external moisture detection circuit. The GPIO will toggle during moisture detection.
76	PdNegotiationInProcess	Output	When in source mode, this GPIO is asserted after a Request message is received, before sending the Accept message. The GPIO is de-asserted after the PS_RDY message is sent. When in sink mode, this GPIO is asserted right before sending a Request message, and de-asserted after a PS_RDY message is received. In either mode, the GPIO is de-asserted when a detach occurs.
75	AttachedAsSink	Output	When the PD controller has a port that is connected to a Source, this GPIO will be asserted. The GPIO is de-asserted upon disconnect, hard reset, during power-role swap and during fast-role swap only if none of the ports in the PD controller are connected to a source.
73	EnableSource_Port1	Output	PD controller will assert this GPIO when acting as a source (implicit or explicit contract)
65	Load_Switch_Drive_Port1	Output	When the PD controller enables the PP_EXT1 sinking path, it will pull the selected GPIO low to enable a load-switch. When the PD controller disables the PP_EXT1 sinking path, it will drive the selected GPIO high.
61	Dp_Dm_Mux_Enable_Event_Port1	Output	This GPIO must be used to enable/disable a USB 2.0 D+/D- mux. The GPIO is driven high upon connection, and low upon disconnect on Port1.
50	Debug_Accessory_Mode_Event_Port1	Output	Output: This GPIO is asserted high when a Debug Accessory is attached on Port1.
45	Prevent_DRSwap_To_UFP_Event	Input	When the GPIO is high, the PD controller will reject any DR_Swap messages from the Port Partner requesting to change the data-role from DFP to UFP.

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Table 5-2. GPIO Events (continued)

Event #	Event Name	I/O	Description
44	UFP_Indicator_Event	Output	The GPIO is driven high when the data role of any port in the PD controller is UFP.
43	Barrel_Jack_Event	Input	When this GPIO is high, the PD controller interprets it to mean that a barrel-jack adaptor is connected and the system has Unconstrained power. A falling edge on this GPIO will automatically set PORT_CONTROL.UnconstrainedPower to 0 and TX_SCEDB.SourceInputs[0] to 0. A rising edge on this GPIO will automatically set PORT_CONTROL.UnconstrainedPower to 1 and TX_SCEDB.SourceInputs[0] to 1.
35	Fault_Condition_Active_Low_Event_Port1	Output	Asserts low on an overcurrent event on Port1.
33	Fault_Input_Event_Port1	Input	When set low by the system, Port1 enters the Type-C Error Recovery State. When set high, no action is taken.
29	UFP_DFP_Event_Port1	Output	Output: Asserted high when Port1 is operating as UFP. Asserted low when port is operating as DFP.
13	SourcePDOContractBit2_Port1	Output	Output: Bit2 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
12	SourcePDOContractBit1_Port1	Output	Output: Bit1 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
11	SourcePDOContractBit0_Port1	Output	Output: Bit0 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
10	SourcePDO4Contract_Port1	Output	Output: Asserted high when a Source PDO4 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
9	SourcePDO3Contract_Port1	Output	Output: Asserted high when a Source PDO3 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
8	SourcePDO2Contract_Port1	Output	Output: Asserted high when a Source PDO2 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
7	SourcePDO1Contract_Port1	Output	Output: Asserted high when a Source PDO1 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO1 has been negotiated.
3	Cable_Orientation_Event_Port1	Output	Output: Indicates the plug orientation on Port1. Low when the plug is connected upside-up (CC1 connected to CC in cable) or disconnected. High when plug is connected upside-down (CC2 connected to CC in cable).
1	PlugEvent_Port1	Output	Output: Asserted high when plug event (attached state) has occurred on Port1, otherwise low.
0	NullEvent	NA	No event associated with this GPIO.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2023	*	Initial Release

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