This user’s guide describes the bq25505 evaluation module (EVM), how to perform a stand-alone evaluation and how to allow the EVM to interface with the system and host. The boost charger output is configured to deliver up to 4.2-V maximum voltage to its output, VSTOR, using external resistors. This voltage is applied to the storage element as long as the storage element voltage at VBAT_SEC is above the internally programmed undervoltage of 2 V. The VBAT_OK indicator toggles high when VSTOR ramps up to 3 V and toggles low when VSTOR ramps down to 2.8 V.

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1 Introduction

1.1 EVM Features

- Evaluation module for bq25505
- Ultra-low power boost converter/charger with battery management for energy harvester applications
- Resistor-programmable settings for overvoltage providing flexible battery management
- Programmable push-pull output indicator for battery status (VBAT_OK)
- Test points for key signals available for testing purpose – easy probe hook-up
- Jumpers available – easy to change settings

1.2 General Description

The bq25505 is an integrated energy harvesting Nano-Power management solution that is well suited for meeting the special needs of ultra-low power applications. The product is specifically designed to efficiently acquire and manage the microwatts (µW) to milliwatts (mW) of power generated from a variety of high output impedance (Hi-Z) DC sources like photovoltaic (solar) or thermal electric generators; or with an AC/DC rectifier, a piezoelectric generator. The bq25505 implements a highly efficient, pulse-frequency modulated (PFM) boost converter/charger targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands. Assuming a depleted storage element has been attached, the bq25505 DC-DC boost converter/charger that requires only microwatts of power to begin operating in cold-start mode. Once the boost converter output, VSTOR, reaches ~1.8 V and can now power the converter, the main boost converter can now more efficiently extract power from low voltage output harvesters such as thermoelectric generators (TEGs) or single- and dual-cell solar panels. For example, assuming the Hi-Z input source can provide at least 5 µW typical and the load on VSTOR (including the storage element leakage current) is less than 1 µA of leakage current, the boost converter can be started with VIN_DC as low as 330 mV typical, and once VSTOR reaches 1.8 V, can continue to harvest energy down to VIN_DC ≃ 120 mV.

Hi-Z DC sources have a maximum output power point (MPP) that varies with ambient conditions. For example, a solar panel's MPP varies with the amount of light on the panel and with temperature. The MPP is listed by the harvesting source manufacturer as a percentage of its open circuit (OC) voltage. Therefore, the bq25505 implements a programmable maximum power point tracking (MPPT) sampling network to optimize the transfer of power into the device. The bq25505 periodically samples the open circuit input voltage every 16 seconds by disabling the boost converter for 256 ms and stores the programmed MPP ratio of the OC voltage on the external reference capacitor (C2) at VREF_SAMP. Typically, solar cells are at their MPP when loaded to ~70–80% of their OC voltage and TEGs at ~50%. While the storage element is less than the user programmed maximum voltage (VBAT_OV), the boost converter loads the harvesting source until VIN_DC reaches the MPP (voltage at VREF_SAMP). This results in the boost charger regulating the input voltage of the converter until the output reaches VBAT_SEC_OV, thus transferring the maximum amount of power currently available per ambient conditions to the output.

The battery undervoltage, VBAT_UV, threshold is checked continuously to ensure that the internal battery FET, connecting VSTOR to VBAT_SEC, does not turn on until VSTOR is above the VBAT_UV threshold (2 V). The overvoltage (VBAT_OV) setting initially is lower than the programmed value at startup (varies on conditions) and is updated after the first ~32 ms. Subsequent updates are every ~64 ms. The VBAT_OV threshold sets maximum voltage on VSTOR and the boost converter stops switching when the voltage on VSTOR reaches the VBAT_OV threshold. The open circuit input voltage (VIN_OC) is measured every ~16 seconds in order for the Maximum Power Point Tracking (MPPT) circuit to sample and hold the input regulation voltage. This periodic update continually optimizes maximum power delivery based on the harvesting conditions.
The bq25505 was designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a rechargeable battery, super capacitor, or conventional capacitor. The storage element will make certain constant power is available when needed for the systems. In general, the storage element also allows the system to handle any peak currents that can not directly come from the input source. It is important to remember that batteries and super capacitors can have significant leakage currents that need to be included with determining the loading on VSTOR.

To prevent damage to a customer’s storage element, both maximum and minimum voltages are monitored against the internally programmed undervoltage (VBAT_UV) and user programmed overvoltage (VBAT_OV) levels.

To further assist users in the strict management of their energy budgets, the bq25505 toggles a user programmable battery good flag (VBAT_OK), checked every 64 ms, to signal the microprocessor when the voltage on an energy storage element or capacitor has risen above (OK_HYST threshold) or dropped below (OK_PROG threshold) a pre-set critical level. To prevent the system from entering an undervoltage condition or if starting up into a depleted storage element, it is recommended to isolate the system load from VSTOR by using an NFET to invert the BAT_OK signal so that it drives the gate of PFET, which isolates the system load from VSTOR.

For details, see bq25505 data sheet (SLUSBJ3).

1.3 Design and Evaluation Considerations

This user's guide is not a replacement for the data sheet. Reading the data sheet first will help in understanding the operations and features of this IC. In this document, “secondary rechargeable battery” or "VBAT_SEC” will be used but one could substitute any appropriate storage element.

System Design Tips

Compared to designing systems powered from an AC/DC converter or large battery (for example, low impedance sources), designing systems powered by Hi-Z sources requires that the system load-per-unit time (for example, per day for solar panel) be compared to the expected loading per the same time unit. Often there is not enough real time input harvested power (for example, at night for a solar panel) to run the system in full operation. Therefore, the energy harvesting circuit collects more energy than being drawn by the system when ambient conditions allow and stores that energy in a storage element for later use to power the system. See SLUC461 for an example spreadsheet on how to design a real solar-panel-powered system in three easy steps:

1. Referring the system rail power back to VSTOR
2. Referring the required VSTOR power back to bq255xx input power
3. Computing the minimum solar panel area from the input power requirement

As demonstrated in the spreadsheet, for any boost converter, you must perform a power balance:

\[
P_{\text{out}} / P_{\text{in}} = (V_{\text{STOR}} \times I_{\text{STOR}}) / (V_{\text{in}} \times I_{\text{in}}) = \eta
\]

where \(\eta\) is the estimated efficiency for the same or similar configuration in order to determine the minimum input power needed to supply the desired output power.

This IC is a highly efficient charger for a storage element such as a battery or super capacitor. The main difference between a battery and a super capacitor is the capacity curve. The battery typically has little or no capacity below a certain voltage, whereas the capacitor does have capacity at lower voltages. Both can have significant leakage currents that will appear as a DC load on VSTOR/VBAT_SEC.
1.4 bq25505EVM Schematic

Figure 1 is the schematic for this EVM.

Figure 1. bq25505EVM Schematic
### 1.5 EVM I/O Connections

Table 1. I/O Connections and Configuration for Evaluation of bq25505 EVM

<table>
<thead>
<tr>
<th>REFERENCE DESIGNATOR</th>
<th>DESCRIPTION</th>
<th>COMMENTS / DEFAULT SETTINGS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HEADERS AND TERMINALS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>J1 – VIN</td>
<td>Input source (+)</td>
<td>If VIN_DC is higher than VSTOR and VSTOR is equal to VBAT_OV, the input VIN_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN_DC be higher than 20 Ω and not a low impedance source.</td>
</tr>
<tr>
<td>J2 – VIN/GND</td>
<td>Input source terminal block</td>
<td></td>
</tr>
<tr>
<td>J3 – GND</td>
<td>Input source return (–)</td>
<td></td>
</tr>
<tr>
<td>J4 – VSTOR</td>
<td>Boost charger output (+)</td>
<td></td>
</tr>
<tr>
<td>J5 – VSTOR/GND</td>
<td>Boost charger output terminal block</td>
<td></td>
</tr>
<tr>
<td>J6 – GND</td>
<td>Boost charger return (–)</td>
<td></td>
</tr>
<tr>
<td>J7 – BAT_SEC</td>
<td>Rechargeable storage element connection (+)</td>
<td></td>
</tr>
<tr>
<td>J8 – BAT_SEC/GND</td>
<td>Rechargeable storage element terminal block</td>
<td></td>
</tr>
<tr>
<td>J9 – GND</td>
<td>Rechargeable storage element connection return (–)</td>
<td></td>
</tr>
<tr>
<td>J10 – VBAT_PRI</td>
<td>Non-rechargeable storage element connection (+)</td>
<td>VBAT_PRI is an optional non-rechargeable battery that switches in to the power the system when BAT_SEC drops below the VBAT_OK threshold.</td>
</tr>
<tr>
<td>J11 – VBAT_PRI/GND</td>
<td>Non-rechargeable storage element connection terminal block</td>
<td></td>
</tr>
<tr>
<td>J12 – GND</td>
<td>Non-rechargeable storage element connection return (–)</td>
<td></td>
</tr>
<tr>
<td>J13 – BAT_OK/GND</td>
<td>Battery Status Indicator (+/–)</td>
<td></td>
</tr>
<tr>
<td>J14 – VOR</td>
<td>Output of multiplexing switches, either VSTOR or VBAT_PRI (+)</td>
<td></td>
</tr>
<tr>
<td>J15 – VOR/GND</td>
<td>Output of multiplexing switches terminal block</td>
<td></td>
</tr>
<tr>
<td>J16 – GND</td>
<td>Return for output of multiplexing switches (–)</td>
<td></td>
</tr>
<tr>
<td><strong>TEST POINTS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TP1</td>
<td>Input source, VIN_DC (+)</td>
<td></td>
</tr>
<tr>
<td>TP2</td>
<td>Boost charger switching node</td>
<td></td>
</tr>
<tr>
<td>TP3</td>
<td>Buck converter switching node</td>
<td></td>
</tr>
<tr>
<td>TP4</td>
<td>Boost charger output, VSTOR (+)</td>
<td></td>
</tr>
<tr>
<td>TP5</td>
<td>Rechargeable storage element, VBAT_SEC (+)</td>
<td></td>
</tr>
<tr>
<td>TP6</td>
<td>Non-rechargeable storage element, VBAT_PRI(+)</td>
<td></td>
</tr>
<tr>
<td>TP7</td>
<td>VRDIV node</td>
<td>CAUTION: Providing an additional low impedance current path in parallel with the feedback resistors, for example, with a 10-MΩ scope probe attached, will degrade regulation accuracy.</td>
</tr>
<tr>
<td>TP8</td>
<td>Output return (–)</td>
<td></td>
</tr>
<tr>
<td>TP9</td>
<td>Input return (–)</td>
<td></td>
</tr>
</tbody>
</table>
**Table 1. I/O Connections and Configuration for Evaluation of bq25505 EVM (continued)**

<table>
<thead>
<tr>
<th>REFERENCE DESIGNATOR</th>
<th>DESCRIPTION</th>
<th>COMMENTS / DEFAULT SETTINGS</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1 – VOC_SAMP</td>
<td>VOC_SAMP = external resistors sized to configure the IC to regulate VIN to 75% of VIN_OC.</td>
<td>Uninstalled (NOTE: Do not install if JP4 shunt is installed)</td>
</tr>
<tr>
<td>JP2 - EN</td>
<td>EN = GND enables the IC. EN = BAT_SEC disables the IC.</td>
<td>EN = GND</td>
</tr>
<tr>
<td>JP3 - VREF_SAMP to GND</td>
<td>VREF_SAMP = GND</td>
<td>Uninstalled (NOTE: Providing an additional leakage path for the VREF_SAMP capacitor for example, through a 10-MΩ scope probe attached to VREF_SAMP, will degrade input voltage regulation performance).</td>
</tr>
<tr>
<td>JP4 - VOC_SAMP</td>
<td>VOC_SAMP = 80% configures the IC to regulate VIN to 80% of VIN_OC. VOC_SAMP = 50% configures the IC to regulate VIN to 50% of VIN_OC.</td>
<td>JP4 = 80% (NOTE: Do not install if JP1 shunt is installed)</td>
</tr>
</tbody>
</table>
2  EVM Performance Specification Summary

See Data Sheet “Recommended Operating Conditions” for component adjustments. For details about the resistor programmable settings, see bq25505 data sheet (SLUSBJ3).

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN(DC)</td>
<td>0.13</td>
<td>4.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIN_STARTUP(DC)</td>
<td>330</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>VBAT_OV</td>
<td>4.04</td>
<td>4.18</td>
<td>4.32</td>
<td>V</td>
</tr>
<tr>
<td>VBAT_OK</td>
<td>2.70</td>
<td>2.79</td>
<td>2.88</td>
<td>V</td>
</tr>
<tr>
<td>MPPT</td>
<td>2.89</td>
<td>2.99</td>
<td>3.09</td>
<td>V</td>
</tr>
<tr>
<td>CBAT</td>
<td>100</td>
<td></td>
<td></td>
<td>µF</td>
</tr>
</tbody>
</table>

See SLUC484 spreadsheet tool to assist with modifying the MPPT, VBAT_OV and VBAT_OK resistors for your application.

**CAUTION**

If changing the board resistors or the capacitor on VREF_SAMP (C2), it is important to remember that residual solder flux on a board has a resistivity in the 1–20 MΩ range. Therefore, flux remaining in parallel with changed 1–20 MΩ resistors can result in a lower effective resistances, which will produce different operating thresholds than expected. Similarly, flux remaining in parallel with the VREF_SAMP capacitor provides an additional leakage path, which results in the input voltage regulation set point drooping during the 16-s MPPT cycle. Therefore, it is highly recommended that boards be thoroughly cleaned twice, once after removing the old components and again after installing the new components. If possible, the boards should be cleaned until the wash solution measures ionic contamination greater than 50 MΩ.

3  Test and Measurement Summary

**Test Setup Tips**

Energy harvesting power sources are high impedance sources. A source-meter configured as a current source with voltage compliance set to the harvester's open circuit voltage is the best way to simulate the harvester. When simulating a Hi-Z energy harvester with low output impedance lab power supply, it is necessary to simulate the harvester's impedance with a physical resistor between the supply, VPS, and VIN_DC of the EVM. When the MPPT sampling circuit is active, VIN_DC = VPS = the harvester open circuit voltage (VIN_OC) because there is no input current to create a drop across the simulated impedance (that is, open circuit); therefore, VPS should be set to the intended harvester's open circuit voltage. When the boost converter is running, it draws only enough current until the voltage at VIN_DC droops to the MPPT's sampled voltage that is stored at VREF_SAMP.
The battery (storage element) can be replaced with a simulated battery. Often electronic 4 quadrant loads give erratic results with a “battery charger” due to the charger changing states (fast-charge to termination and refresh) while the electronic load is changing loads to maintain the “battery” voltage. The charging and loading get out of phase and create a large signal oscillation which is due to the 4 quadrant meter. A simple circuit can be used to simulate a battery and can be adjusted for voltage. It consists of load resistor (~10 Ω, 2 W) to pull the output down to some minimum storage voltage (sinking current part of battery) and a lab supply connected to the BAT pin via a diode. The lab supply biases up the battery voltage to the desired level. It may be necessary to add more capacitance across R1.

3.1 Test Setups and Results

3.1.1 Boost Charger Efficiency

The test setup is shown in Figure 2. The specific equipment used for the test results in Figure 3 and Figure 4 is listed below:

1. VIN_DC was connected to a Keithley 2420 source-meter configured as a current source with voltage compliance (clamp) set to the open circuit voltage.
2. VSTOR was connected a Keithley 2420 source-meter configured as a voltage source set to the VSTOR voltage. The current sunk by the source-meter was the output current of the charger.
3. VREF_SAMP was connected to a power supply configured to output the desired input voltage regulation point (that is, the MPPT% times the HiZ source's VOC). No jumper is required on JP4.
Figure 2. Test Setup for Measuring Boost Charger Efficiency

Figure 3. Charger Efficiency versus Input Voltage
3.1.2 Boost Charger Operation during Battery Charging

The test setup is shown in Figure 5. The specific equipment used for the test results in Figure 6 is listed below:

1. VIN_DC and VBAT_SEC are configured as shown in Section 3.1.2.
2. The boost charger inductor current (IL) was measured by using an oscilloscope current probe across a current loop that was inserted in series with inductor L1.
3. VSTOR’s ripple voltage was measured using an oscilloscope voltage probe placed directly across the VSTOR capacitor (C5). The scope probe’s standard ground lead was replaced with short lead.
4. VIN_DC and the LBOOST pin (switching node of the boost charger) were measured by oscilloscope voltage probes connected to TP1 and TP2.
Figure 5. Test Setup for Measuring Charger Operation

Figure 6. Charger Operational Waveforms During Battery Charging
3.1.3 Switching Between Primary and Secondary Batteries

The test setup is shown in Figure 5. The specific equipment used for the test results in Figure 8 is listed below:

1. V<sub>IN_DC</sub>, VBAT_SEC and VBAT_PRI are configured as shown in Section 3.1.2.
2. The function generator and power amplifier simulated VSTOR charging up and discharging.
3. VBAT_SEC, VBAT_PRI, VBAT_OK and VOR were measured with oscilloscope voltage probes at TP5, TP6, J13 and J14, respectively.
Charging a Super Capacitor on VBAT_SEC

The test setup is shown in Figure 9. The specific equipment used for the test results in Figure 10 is listed below:

1. VIN_DC was connected to a Keithley 2420 configured as a 1.0-mA current source with 1.2-V voltage compliance.
2. VBAT_SEC was connected to a 120-mF super capacitor. There were no other loads on VSTOR or VBAT_SEC.
3. VIN_DC, VSTOR and VBAT_SEC were measured with oscilloscope voltage probes connected at TP1, TP4 and TP5 respectively.
Tips for other Tests and Measurements

The quiescent current during main boost operation, which is basically the current from the battery to the IC, is measured at the VSTOR pin. If a source-meter is not available to make the measurement, connect a 100-kΩ resistor to VSTOR and connect a 3-V supply from the other end of this resistor to the ground of the EVM. A 10-MΩ meter can be used to measure the voltage drop across the resistor and calculate the current. No other connections should be made to the EVM and the measurement should be taken after steady state conditions are reached (may take a few minutes). The reading should be much less than 100 nA.
4 Bill of Materials and Board Layout

This section contains the bq25505 bill of materials (BOM) and PCB board layout.

4.1 Bill of Materials

Table 2 lists the BOM for the bq25505EVM.

<table>
<thead>
<tr>
<th>COUNT</th>
<th>RefDes</th>
<th>Value</th>
<th>Description</th>
<th>Size</th>
<th>Part Number</th>
<th>MFR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1</td>
<td>4.7uF</td>
<td>Capacitor, Ceramic Chip, 6.3V, X7R, ±10%</td>
<td>805</td>
<td>C0805C475K9RACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>1</td>
<td>C10</td>
<td>4.7uF</td>
<td>Capacitor, Ceramic Chip, 6.3V, X5R, ±20%</td>
<td>603</td>
<td>GRM188R60J475ME19D</td>
<td>Murata</td>
</tr>
<tr>
<td>0</td>
<td>C11-12</td>
<td>DNP</td>
<td>Capacitor, Ceramic Chip, 6.3V, X5R, ±20%</td>
<td>603</td>
<td>Engineering Only</td>
<td>n/a</td>
</tr>
<tr>
<td>1</td>
<td>C2</td>
<td>0.1u</td>
<td>Capacitor, Ceramic Chip, 50V, X7R, 10%</td>
<td>0603</td>
<td>GRM188R71H010KA01D</td>
<td>Murata</td>
</tr>
<tr>
<td>1</td>
<td>C3</td>
<td>100u</td>
<td>Capacitor, Ceramic Chip, 6.3V, X5R, 20%</td>
<td>1812</td>
<td>GRM43SR60J107ME20L</td>
<td>Murata</td>
</tr>
<tr>
<td>2</td>
<td>C4</td>
<td>4.7uF</td>
<td>Capacitor, Ceramic Chip, 6.3V, X7R, ±10%</td>
<td>805</td>
<td>LMK212B7475KG-T</td>
<td>Taiyo Yuden</td>
</tr>
<tr>
<td>0</td>
<td>C7-9</td>
<td>DNP</td>
<td>Capacitor, Ceramic Chip, 6.3V, X5R, ±20%</td>
<td>603</td>
<td>Engineering Only</td>
<td>n/a</td>
</tr>
<tr>
<td>1</td>
<td>C13</td>
<td>1.0uF</td>
<td>Capacitor, Ceramic Chip, 10V, X5R, ±20%</td>
<td>603</td>
<td>GRM188R61A105MA61D</td>
<td>Murata</td>
</tr>
<tr>
<td>11</td>
<td>J1 J3 J6-7 J9-10 J12-14 J16</td>
<td>PEC02SAAN</td>
<td>Header, Male 2-pin, 100mil spacing,</td>
<td>0.100 inch x 2</td>
<td>PEC02SAAN</td>
<td>Sullins</td>
</tr>
<tr>
<td>5</td>
<td>J2</td>
<td>2.07</td>
<td>Terminal Block, 2-pin, 6-A, 3.5mm</td>
<td>0.27 x 0.25 inch</td>
<td>ED555/2DS</td>
<td>OST</td>
</tr>
<tr>
<td>2</td>
<td>JP1</td>
<td>2.07</td>
<td>Header, Male 2-pin, 100mil spacing,</td>
<td>0.100 inch x 2</td>
<td>PEC02SAAN</td>
<td>Sullins</td>
</tr>
<tr>
<td>2</td>
<td>JP2</td>
<td>2.07</td>
<td>Header, Male 3-pin, 100mil spacing,</td>
<td>0.100 inch x 3</td>
<td>PEC03SAAN</td>
<td>Sullins</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>22uH</td>
<td>Inductor, SMT, 0.65A, 360mΩ</td>
<td>4.0mm x0.4mm x1.0mm x0.8mm</td>
<td>LPS4018-223M</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>2</td>
<td>Q1-2</td>
<td>4.99</td>
<td>MOSFET, Dual PChan, -20V, 1.2A, 190mΩ</td>
<td>CSP 1x1.5mm</td>
<td>CSD75205W1015</td>
<td>TI</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>7.5M</td>
<td>Resistor, Chip, 1/16W, 1%</td>
<td>603</td>
<td>CRCW06037M50FKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>1</td>
<td>R2</td>
<td>5.76M</td>
<td>Resistor, Chip, 1/16W, 1%</td>
<td>603</td>
<td>CRCW0603M76FKEA</td>
<td>Vishay Dale</td>
</tr>
<tr>
<td>2</td>
<td>R3 R5</td>
<td>4.99M</td>
<td>Resistor, Chip, 1/16W, 1%</td>
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4.2 EVM Board Layout

Figure 12 through Figure 14 are the board layouts for this EVM.

Figure 11. EVM PCB Top Silk
Figure 12. EVM PCB Top Assembly
Figure 13. EVM PCB Top Layer
Figure 14. EVM PCB Bottom Layer
As for all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost converter/charger and buck converter could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors should be placed as close as possible to the IC. For the boost charger, the first priority are the output capacitors, including the 0.1-μF bypass capacitor (CBYP), followed by CSTOR, which should be placed as close as possible between VSTOR, pin 19, and VSS, pin 1. Next, the input capacitor, CIN, should be placed as close as possible between VIN_DC, pin 2, and VSS, pin 1. Last in priority is the boost converter inductor, L1, which should be placed close to LBOOST, pin 20, and VIN_DC, pin 2. It is best to use vias and bottom traces for connecting the inductors to their respective pins instead of the capacitors.

To minimize noise pickup by the high impedance voltage setting nodes (VBAT_OV, OK_PROG, and OK_HYST), the external resistors should be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (for example from resistors and CREF), it is recommended to use short traces as well, separated from the power ground traces and connected to VSS pin 15. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The PowerPAD™ should not be used as a power ground return path.

The remaining pins are either NC pins, that should be connected to the PowerPad as shown below, or digital signals with minimal layout restrictions.

In order to maximize efficiency at light load, the use of voltage level setting resistors > 1 MΩ is recommended. However, during board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors or from one end of a resistor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed resistor values. Therefore, it is recommended that no ground planes be poured near the voltage setting resistors. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 Ω. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5X below the measured ionic contamination.

Revision History

Changes from Original (September 2013) to A Revision

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<td>• Changed contents in the bill of materials</td>
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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
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U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user’s authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

• Reorient or relocate the receiving antenna.
• Increase the separation between the equipment and receiver.
• Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
• Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003. Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.
Canada Industry Canada Compliance (French)
Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.
Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio
Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes déetchables
Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.
Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.
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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan.
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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