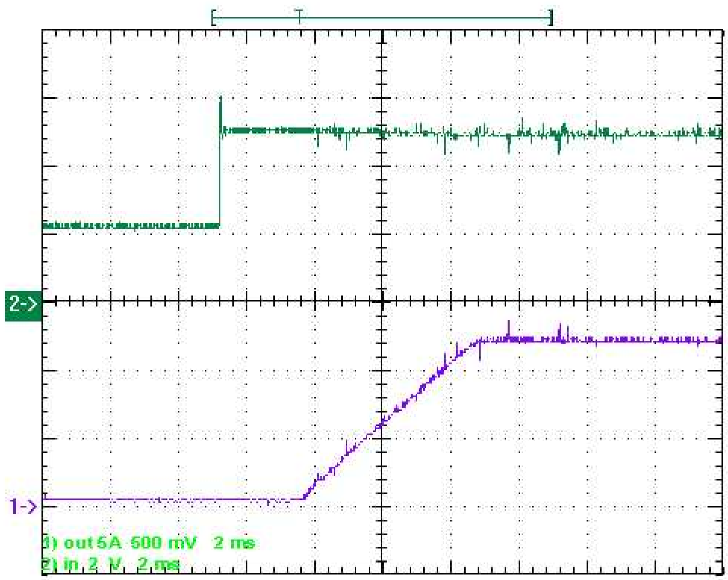
PMP2702 Test Results

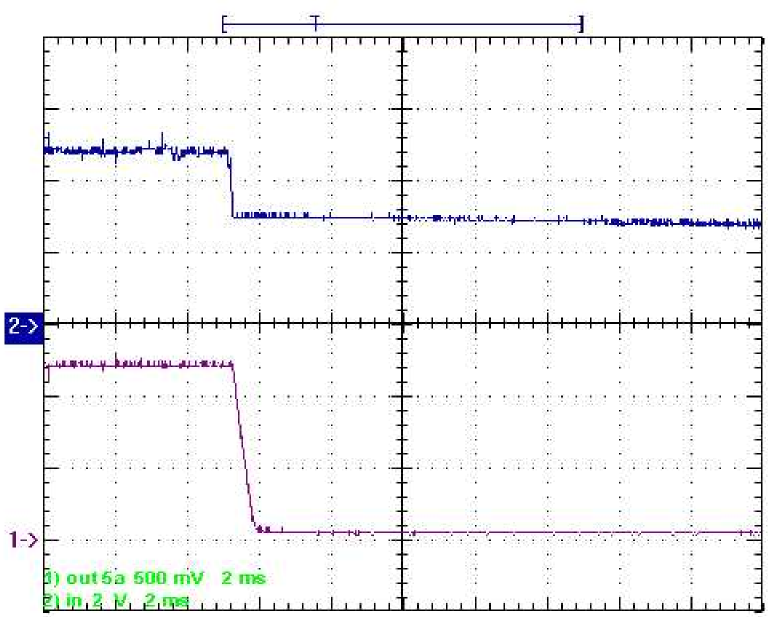
1 Startup

The startup waveform is shown in the figure below. The input voltage is set at 5V, with 5A load on the output.
Channel 1 : Vout
Channel 2 : Vin



2 Shutdown

The shutdown waveform is shown in the figure below. The input voltage is set at 5V, with a 5A load on the output.
Channel 1 : Vout
Channel 2 : Vin



3 Efficiency

The efficiency is shown in the figure below.

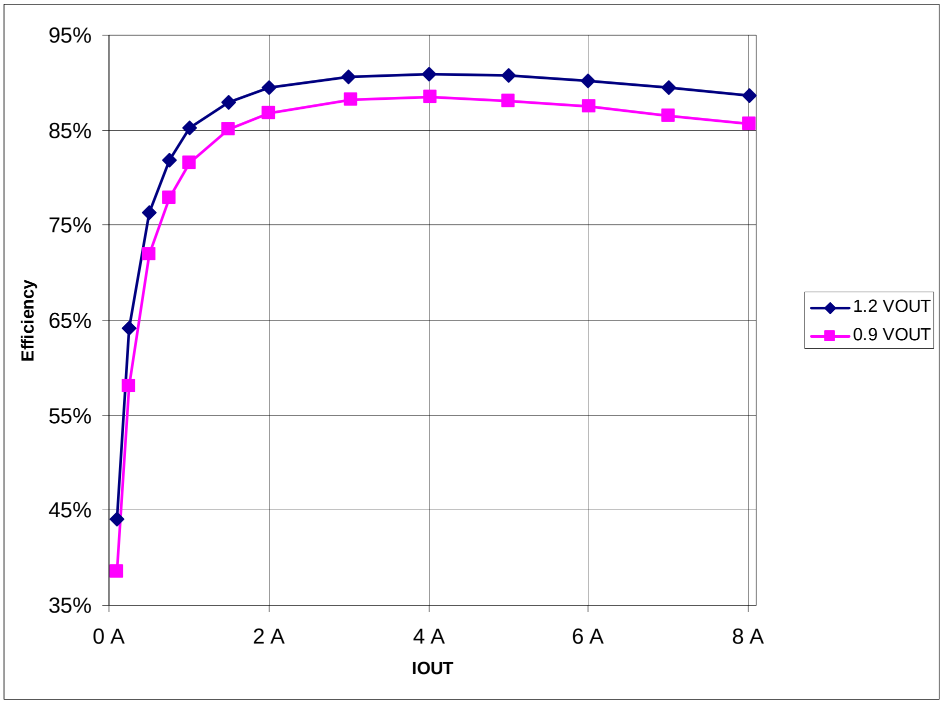


Table for Vout = 1.2V w/ Panasonic ETQP6F1R2HFA, 1.2uH/2.24mOhm:

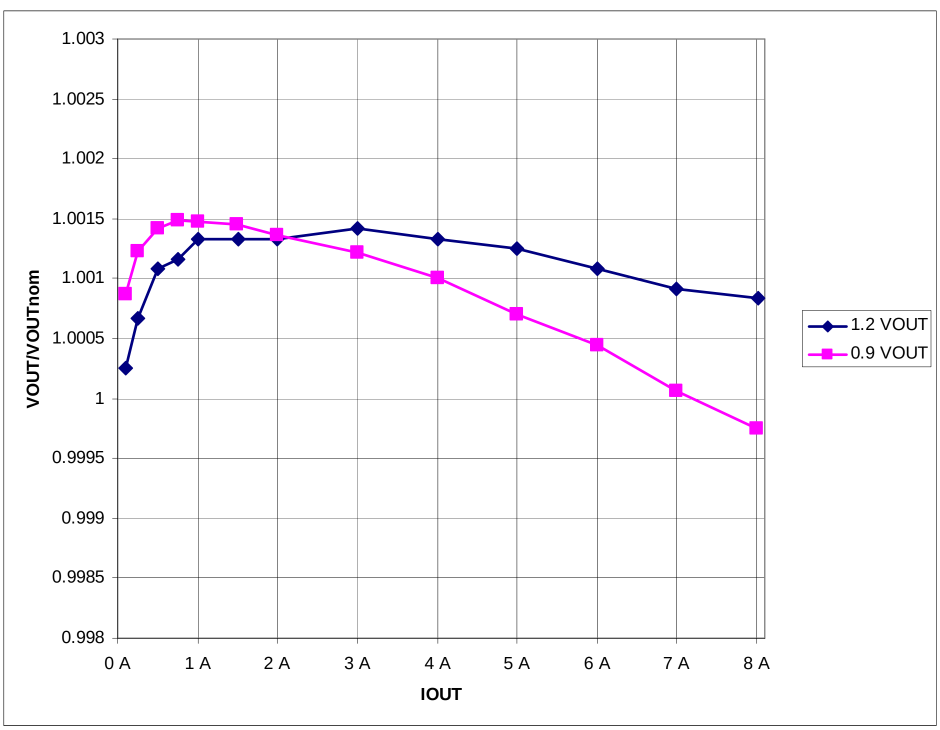
VIN	IIN	PIN	VOUT	IOUTset	IOUT	POUT	Efficiency
5.0003	0.056	0.2800168	1.2003	0.1	0.1028	0.12339	0.440655
5.0168	0.0937	0.4700742	1.2008	0.25	0.251	0.3014	0.641177
5.0104	0.1579	0.7911422	1.2013	0.5	0.5023	0.60341	0.762711
5.0042	0.2201	1.1014244	1.2014	0.75	0.7507	0.90189	0.818841
5.0187	0.283	1.4202921	1.2016	1	1.0072	1.21025	0.852115
5.0061	0.4101	2.0530016	1.2016	1.5	1.502	1.8048	0.879105
4.9932	0.5385	2.6888382	1.2016	2	2.002	2.4056	0.894663
5.0085	0.7952	3.9827592	1.2017	3	3.004	3.60991	0.906383
5.0024	1.0578	5.2915387	1.2016	4	4.002	4.8088	0.908772
5.017	1.319	6.617423	1.2015	5	5	6.0075	0.907831
5.0107	1.595	7.9920665	1.2013	6	6	7.2078	0.901869
5.0026	1.877	9.3898802	1.2011	7	6.997	8.4041	0.895016
4.9977	2.173	10.860002	1.201	8	8.013	9.62361	0.886152

Table for Vout = 900mV w/ Panasonic ETQP6F1R2HFA, 1.2uH/2.24mOhm:

VIN	IIN	PIN	VOUT		IOUT	POUT	Efficiency
5.001	0.0503	0.2515503	0.9008	0.1	0.1078	0.09711	0.386027
4.9983	0.0786	0.3928664	0.9011	0.25	0.2534	0.22834	0.581212
4.9934	0.1285	0.6416519	0.9012	0.5	0.5118	0.46123	0.718823
5.0092	0.1743	0.8731036	0.9014	0.75	0.7542	0.67981	0.778608
5.0044	0.2232	1.1169821	0.9014	1	1.0114	0.91167	0.816187
4.995	0.3196	1.596402	0.9014	1.5	1.507	1.35833	0.850872
5.0064	0.4165	2.0851656	0.9013	2	2.008	1.80977	0.867926
5.0062	0.6172	3.0898266	0.9011	3	3.025	2.72586	0.882204
5.0079	0.8188	4.1004685	0.9008	4	4.025	3.6258	0.884241
5.0082	1.023	5.1233886	0.9005	5	5.009	4.51075	0.880424
5.0079	1.235	6.1847565	0.9002	6	6.011	5.41122	0.874929
5.0065	1.456	7.289464	0.8992	7	7.012	6.30519	0.864973
5.0058	1.681	8.4147498	0.8997	8	8.012	7.20848	0.856648

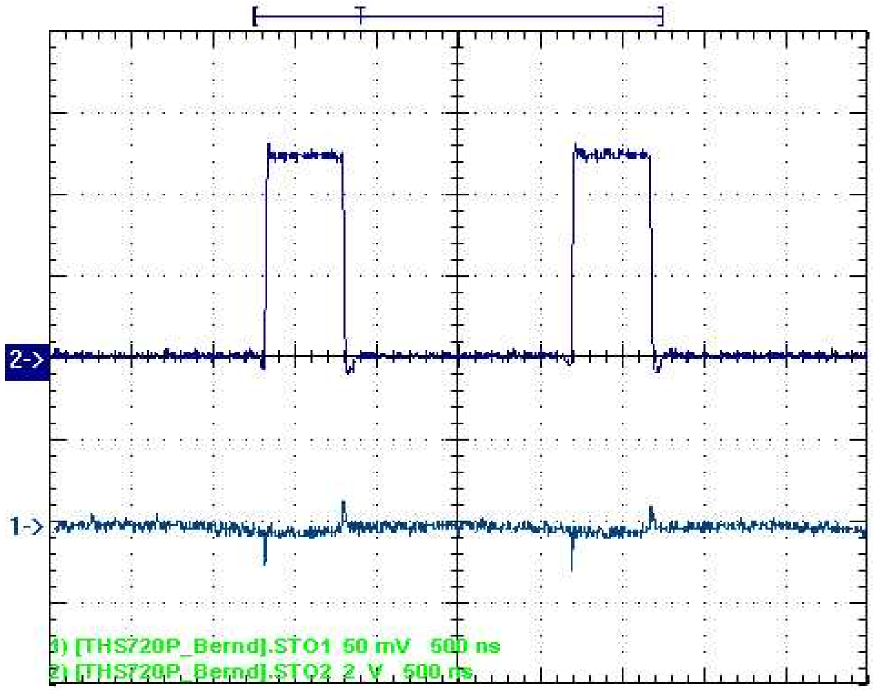
4 Load Regulation

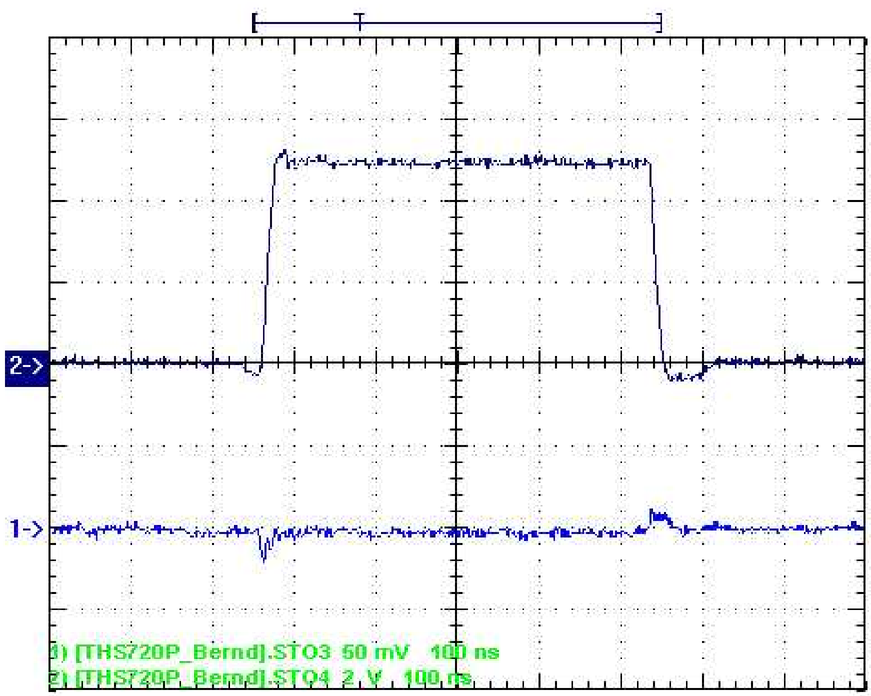
The load regulation is shown in the graph below.



5 Output Ripple Voltage

The output ripple voltage is shown in the figure below. The image was taken with a 5A load. Channel 2 shows waveform at switchnode

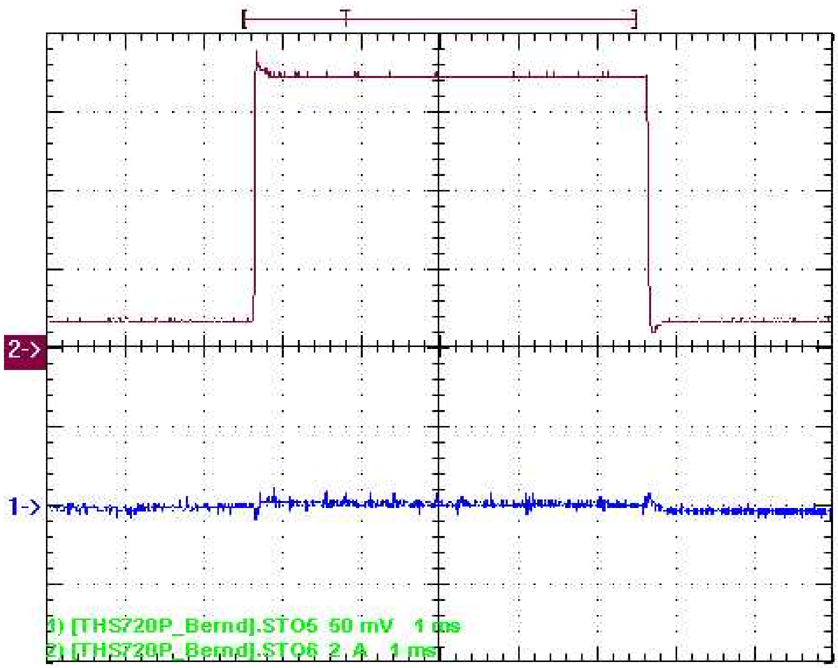


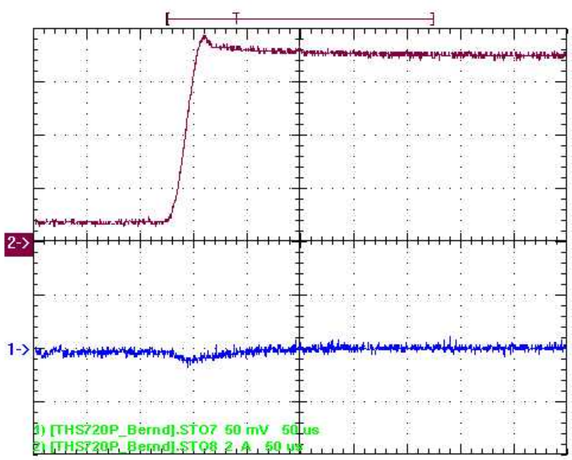


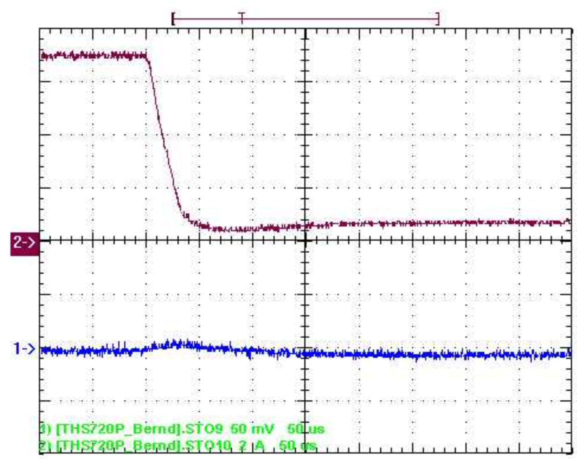
6 Load Transients

The figures below show the response of the 1.2V output to load transients. The input voltage was set to 5V.
Load jump was from 0.7A to 7A with a Dynaload RBL 488 100-120-800

Channel 1 : Vout (AC coupled)
Channel 2 : Load current

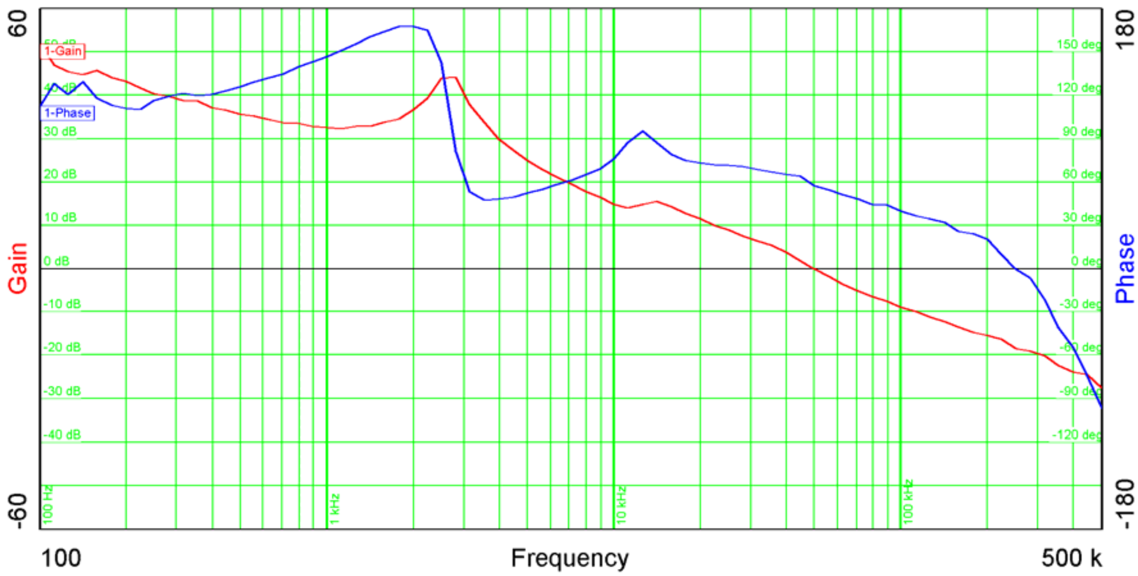






7 Frequency Response

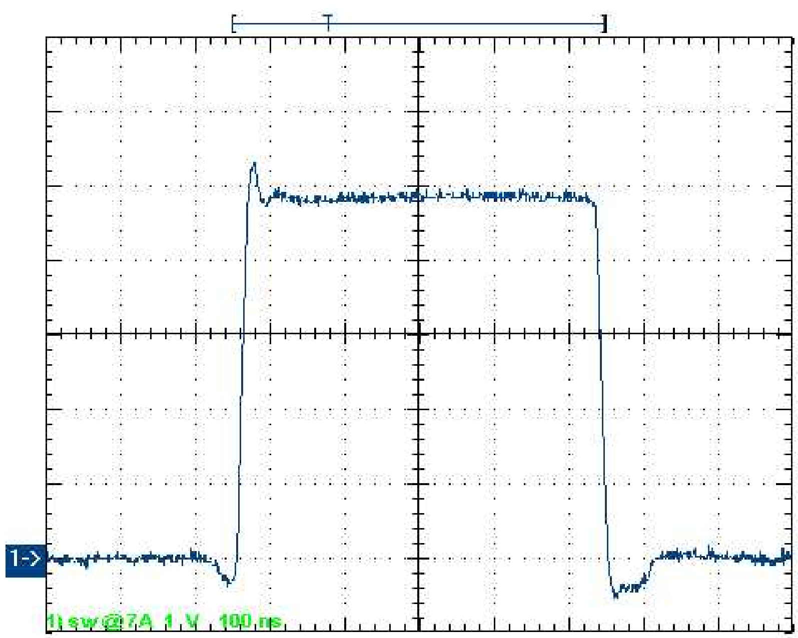
The figure below shows the loop response of the 1.2V output with a 5V input and a 7A load.



fc=50.08kHz with phase 57.51°

8 Miscellaneous Waveforms

The figure below shows the voltage waveform on the switch node of the 1.2V output. This image was captured with a 5V input and a 7A load. (Bandwidth 20% was used)



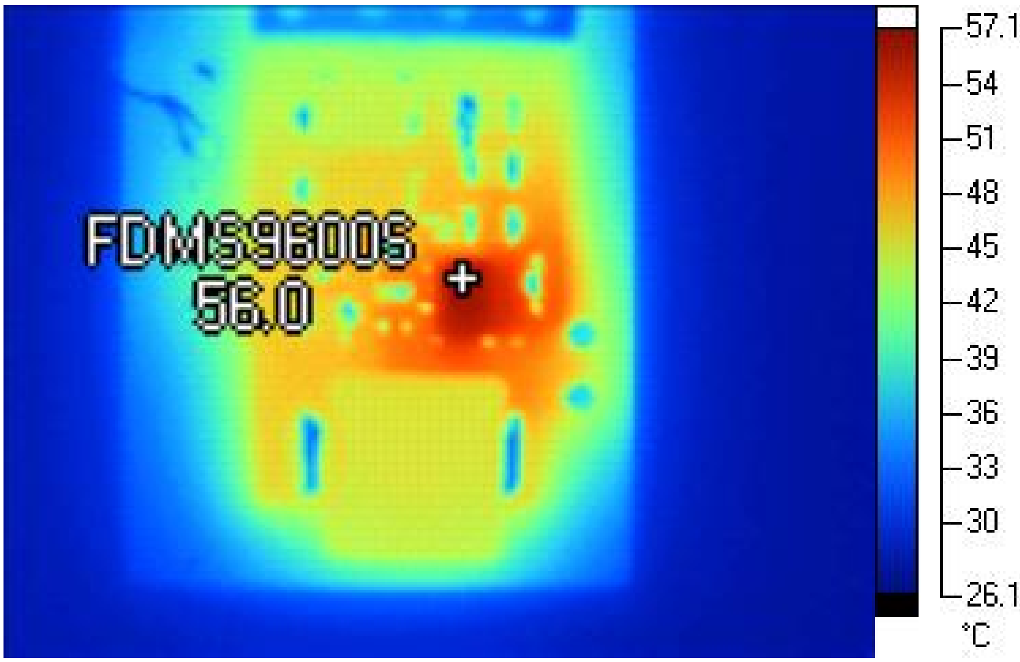
9 Output voltage at different VID Settings

Measurement was performed with 3.5A Load.

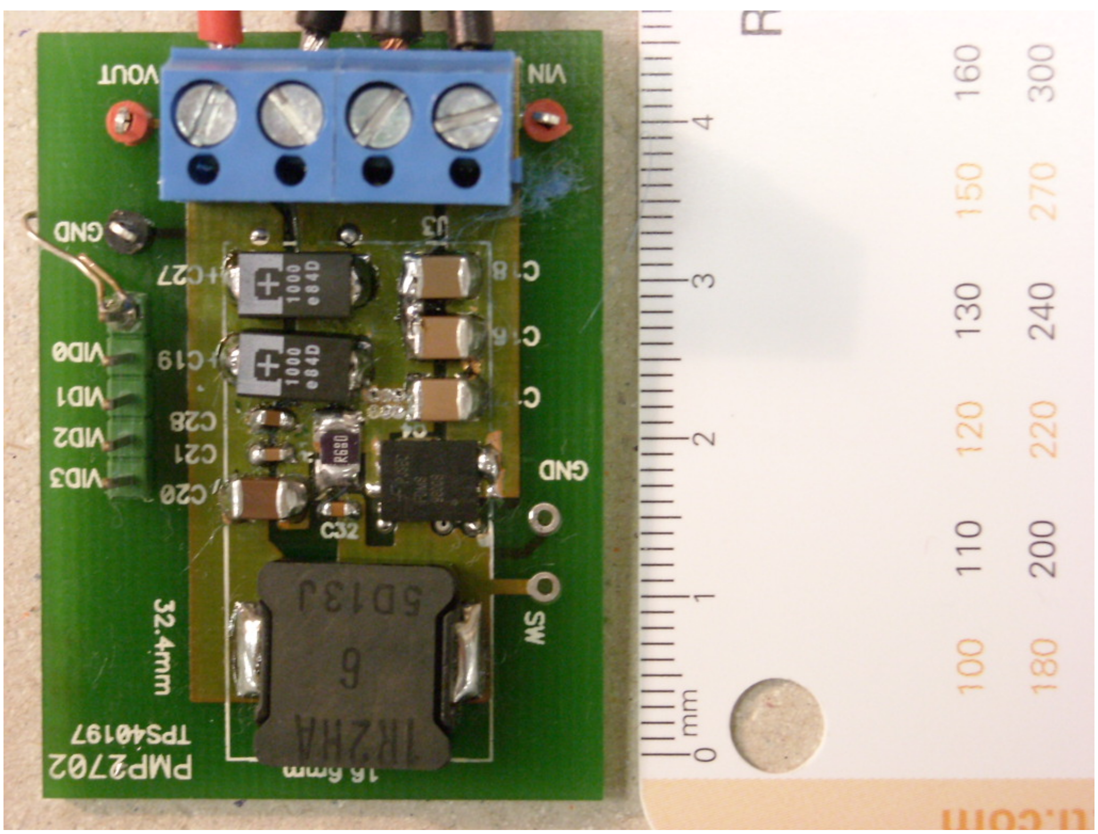
VID3	VID2	VID1	VID0	Vref	Vout
				data sheet	measured
0	0	0	0	0.9	0.9012
0	0	0	1	0.92	0.9214
0	0	1	0	0.94	0.9415
0	0	1	1	0.96	0.9616
0	1	0	0	0.98	0.9816
0	1	0	1	1	1.0016
0	1	1	0	1.02	1.0216
0	1	1	1	1.04	1.0417
1	0	0	0	1.06	1.0617
1	0	0	1	1.08	1.0817
1	0	1	0	1.1	1.1018
1	0	1	1	1.12	1.1218
1	1	0	0	1.14	1.1419
1	1	0	1	1.16	1.1619
1	1	1	0	1.18	1.1820
1	1	1	1	1.2	1.2021

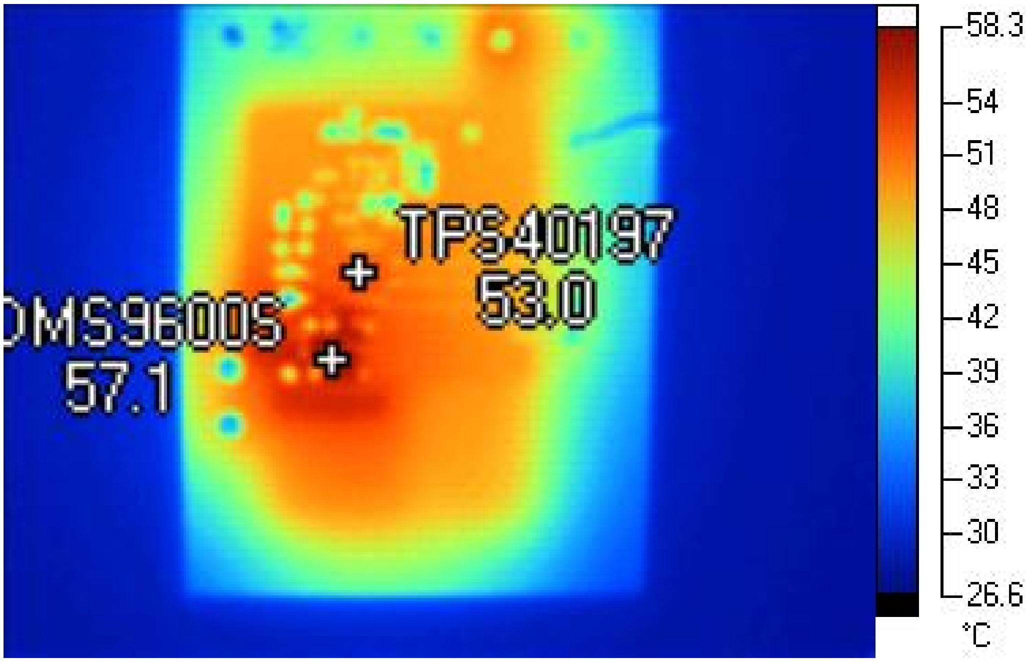
10 Thermal Image

Thermal images were taken at 7A load.

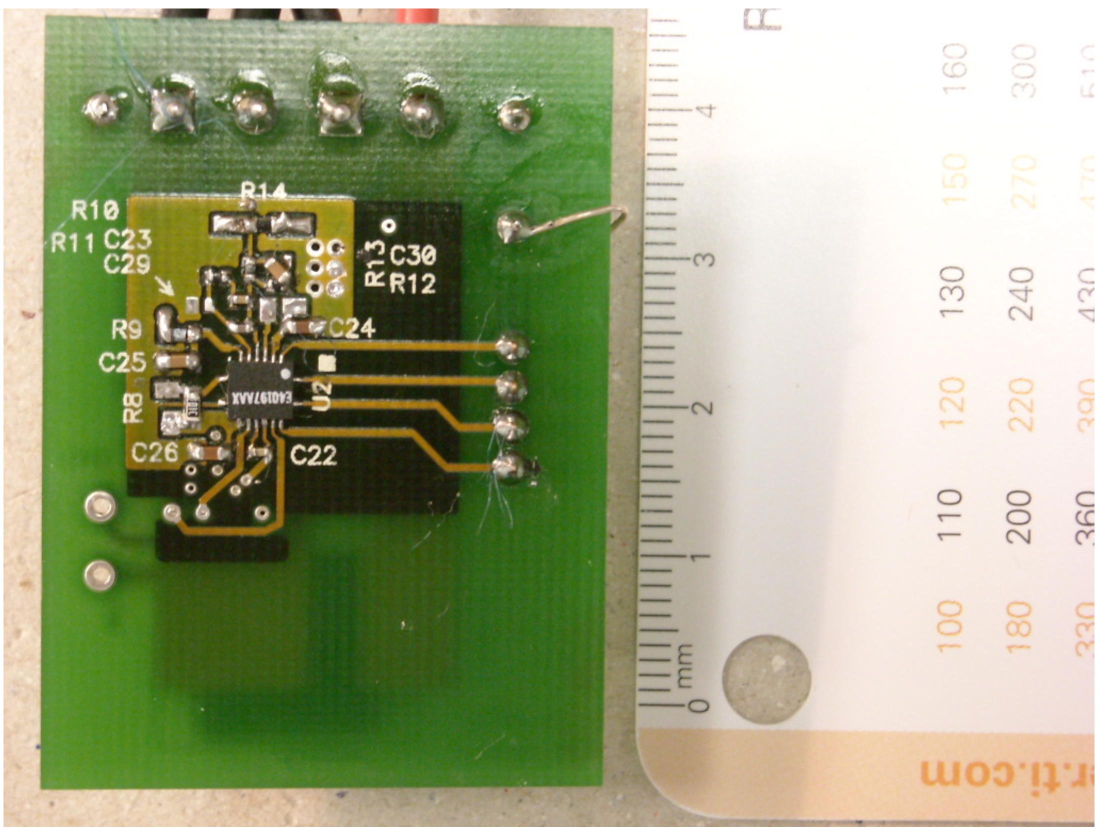


Top Side





Bottom Side



(temperature of dual FET is measured slightly higher at bottom side due to worse convection cooling than by measurement at top side)

dT dual FET Fairchild FDMS9600S = 33K
dT Ctrl. Texas Instruments TPS40197 = 30K

11 Faraday power consumption

1) worst case analysis at 100 degs Celsius done for typical telecom appl,
all eight execution units working, two memory accesses per clock cycle:

IDLE state 3.907W
CPU 0, 75% utilization: 526mW
CPU 1, 50% utilization: 351mW
CPU2, 50% utilization: 351mW
=======================
total max. core pwr: 5.135W
Iccmax at lowest Vcc: 5.71A (at 900mV)

2) a reasonable szenario will be:

IDLE state 3.907W
all cores 50% utilization: 3x 351mW 1.053W
=================================
total core power 4.960W
Icc max at lowest Vcc: 5.51A

3) the real szenario will be lower, expected at best programming code are:
six execution units working, one memory access per clock cycle.

So a design w/ 7Amax current and max effcy in a range 4A to 5.5A
seems to be up to now the best solution.

Summary:

PMP2702 offers at Vout 1.2V in a range 3A to 6A an efficiency **over 90%**, at lowest Vout 900mV still 88%. This results in dT = 33K at maximum load of 7Amps.

For good transient response crossover frequency was set to 1/10 of switching frequency, achieved bw of 50kHz w/ phase margin of 60degs and gain margin of nearly -20dB.

Overall geometry is 32.4mm x 16.6mm, maximum height 5.7mm;
please keep in mind that modules need additional input caps to reach input ripple <100mVpp and need additional output caps (2 x 1000uF) to reach transient requirements.
VID interface is included, any other solution needs EXTERNAL VID interface.

The design was tested at ambient temperature for Iout of 10A continuous for several hrs. w/out any issues.

For series production w/ auto assy geometry could be optimized to 30mm x 15mm, see pics.

For Curie leave out one Cin, one Cout and set inductor to ETQP6F3R2HFA;
geometry will be 25mm x 15mm.

IMPORTANT NOTICE AND DISCLAIMER