# bq78PL116 Technical Reference Manual

# Technical Reference

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# Preface

## 1.1 Read This First

This document discusses the bq78PL116 which is used to build a complete battery-pack gas gauge and protection solution. At minimum read through Chapter 1 to get a sense of what is involved in product development.

The information contained in this document is critical to operation of the bq78PL116. All sections should be read to understand how to appropriately configure the operation of the bq78PL116. Configuration is dependent on pack construction (series and parallel counts), cell type and application.

## 1.2 Notational Conventions

The following notation is used if SBS commands and programmable parameters values are mentioned within a text block:

The reference format for SBS commands is: SBS:Command Name(Command No.), for example: SBS:Voltage(0x09), or SBS:BatteryStatus(0x16):[TCA]

The reference format for programmable parameters values is: Value Name, for example: COV Threshold

## 1.3 Scope and Definitions

The scope of this document is to convey descriptive information on the multiple configuration parameters (thresholds) available in the bq78PL116 to control both basic fuel-gauging operation and safety operation. Multiple parameters are provided for custom configuration of the bq78PL116 to allow flexible use in a variety of 3- to 16-cell Li-Ion applications. (Note that for cell counts greater than four, PowerLAN Dual-Cell Li-Ion Battery Monitor devices, called bq76PL102, need to be connected to the bq78PL116.)

This document includes detail on such parameters, their settings, ranges, and uses. Additional information is included which describes the fuel-gauging algorithm, calibration steps, and similar operational notes to allow a more complete understanding of the usage of this part.

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## 1.4 bq78PL114S12 and bq78PL116 Comparison Chart

There are three similar products available in the PowerLAN Battery Management System Family. They are similar in that they use the same base silicon but, they are different in that they each have unique firmware. The three products are bq78PL114, bq78PL114S12, and bq78PL116. The Technical Reference Manual (SLUU330) of the bq78PL114 describes the differences between the bq78PL114 and bq78PL114S12. The following section serves to explain the differences between the bq78PL114S12 and the bq78PL116. Whenever possible, use the bq78PL116. Or upgrade any bq78PL114 to a bq78PL114S12 via a free firmware download from the TI website.

The bq78PL116 has final firmware resident on the device and does not need firmware download prior to usage.

### *1.4.1 Series Cell Count*

Increased cell count from 12 to 16.

### *1.4.2 Temperature Sensors*

Reduced maximum external temperature count from 12 to 4.

### *1.4.3 Ship Mode*

Fixed ship mode to match description contained within this document.

### *1.4.4 Seal/Unseal*

The bq78PL116 can now be sealed (Level 0) so that only Standard SBData Commands 0x00 to 0x23 and Extended Commands 0x3C to 0x58 can be executed. Two other levels, 1 and 2, are also created. Level 1 is for increasing Level 0 access to include Extended SBData Controls via 0x80 and 0x81. Level 2 is full open access (Unsealed).

### *1.4.5 Default Chemistry*

The default chemistry (CHEM ID) is 107, changed from 101. The initialization of gas gauge parameters like Qmax, Qrem and the Ra table was corrected. If a pack configuration file (.tmap) is loaded for series cell counts above 3, the aforementioned gas gauge parameters are copied into memory for cells 4 to N. (N = number of series cells) One of the primary results is that RSOC will initialize correctly for this default chemistry. In other words, RSOC will not be 0% after a relearn/initialize command. Note that a properly developed .aux file is always needed to correctly initialize the gas gauge of the bq78PL116.

### *1.4.6 SBData Extended Commands(0x3C to 0x58)*

Increased the programmable Extended Command set from 16 to 29. The user can elect to map some of the valuable bq78PL116-specific data values to registers 0x3C – 0x58 and access them through standard SMBus commands. This mapping is specified in a new file type called .sbd. The bqWizard now has a utility that allows users to create these .sbd files.

### *1.4.7 SBS:SpecificationInfo(0x1A)*

Support of VScale and IPScale bits is added. VScale and IPScale can each be either b'0000' or b'0001'. This is needed to allow for reporting voltages above 65535mV and currents beyond ±32768mA.The effects of VScale and IPScale must be reflected in the applicable values of the parameter set.

Version bits are now fully supported. Version can be either b'0010' or b'0011'. This effectively means that the bq78PL116 now supports either PEC or no PEC.

### *1.4.8 SBS:BatteryMode(0x03)*

The CAPACITY_MODE bit is now fully supported. The bq78PL116 reports in either mA and mAHrs or 10mW and 10mWHrs.



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### 1.4.9 Configuration Files

The changes made in the bq78PL116 make the following files of the bq78PL116S12 incompatible with the bq78PL116:

- Parameter Set Files (.ppcsv)
- Production Clone File (.dat)
- Pack Configuration (.tmap)

### 1.4.10 First and Second Level Safety Rules and Charge Control Rules

The timing of the First and Second Level Safety and Charge Control Rules was changed. The set point error decreased from +2.5/-0 seconds down to +1.6/-0 seconds. This does not apply to the Hardware Over Current Charge/Discharge and Hardware Short Circuit Rules.

### 1.4.11 PowerPump

Features were added to the PowerPump algorithm to allow users to force PowerPump to have all cells pump north or all cells pump south. This is controlled through the Algorithm Enable register.

**NOTE:** The Algorithm Enable Register can only be edited by the bqWizard or bq78PL11x API.

TurboPump, also known as SuperPump, was fixed to not allow PowerPump during a safety event.

### 1.4.12 System Present Control Bit

The operation of the System Present Control Bit in the Hardware Configuration register was fixed to match the description in this document. This can decrease the current consumption during Standby mode by shutting off the CHG pin output.

### 1.4.13 Charge Completion

The charge Completion Rule was fixed to correctly look at Transition to Idle Current value when evaluating the Charge Completion FET Activation Time rather than the Transition To Charge Current value.

### 1.4.14 bqWizard 3

The bqWizard was improved to better the user experience and also modified to support the new features of the bq78PL116. See the bqWizard User Guide for specific details on the changes.

### 1.4.15 bq78PL11x API

The Windows .NET API was also modified to support the new features of the bq78PL116. See the bq78PL11x API User Guide for specific details on the changes.

### 1.4.16 LED Startup Indication

There is no LED indication at Power On Reset (POR). The only LED indication is for State of Charge Indication (SOCi) and in the odd case where the boot-loader mode is entered to do a firmware download. Firmware download is not normally required.

### 1.4.17 Lifetime Power

An issue involving the operation of Lifetime Power variable was corrected.

### 1.4.18 Gas Gauging Mode

The gas gauge does not perform calculations based on constant power operation. It bases its calculations on constant current. It can however report capacity related results in either mAHrs or 10mWHrs.


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### 1.4.19 SBData Extended Controls

SBData Extended Controls is a newly documented feature of the bq78PL114S12 and bq78PL116. It allows the SMBus host to modify Safety Thresholds and Timers and make limited configuration changes to the device through standard SMBus commands. The access point in the bq78PL114S12 are commands 0x50 and 0x51. In the bq78PL116 these points are 0x80 and 0x81. A complete description of how this protocol works will be included in an application note.

### 1.4.20 RemCap and RSOC

In bq78PL114S12, RemCap and RSOC may not report correctly due to a delay after entry into Charge from a fully discharged state. This was fixed in bq78PL116.

### 1.4.21 Discharge Simulation

In bq78PL114S12, the discharge simulation does not typically start until the first grid point. This was fixed in the bq78PL116 to coincide with the start of discharge.

## 1.5 Design Flow Overview

The development cycle for a battery management system based on the PowerLAN™ Master Gateway Battery Management Controller is outlined in Figure 1-1. Prototype designs are developed in the laboratory environment using the bqWizard™ software. Once development is complete, the prototype's configuration is saved and used to clone production packs.

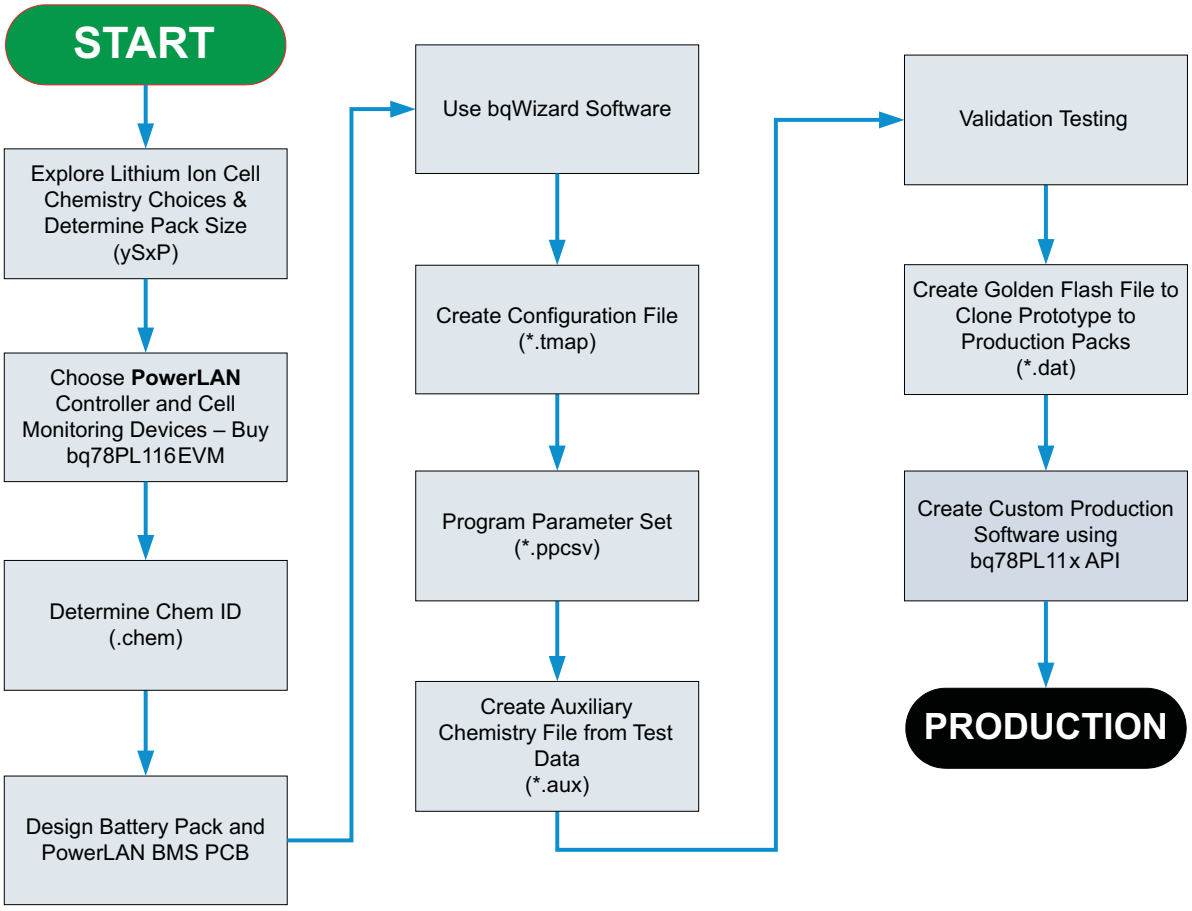


**Figure 1-1. PowerLAN™ BMS Development Cycle**

This introductory section gives an overview of the design flow required for PowerLAN™ Battery Management Systems.



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### 1.5.1 EVM

Use the bq78PL116EVM-001 and the bqWizard™ software to explore the capabilities of the PowerLAN™ devices for 3-to-16 series cell packs. The EVM is ideal for an introduction to the PowerLAN™ architecture and to evaluate PowerPump™ cell balancing. The EVM includes the PowerLAN™ Master Gateway controller – bq78PL116, six PowerLAN™ Dual Cell Monitors – bq76PL102.

At first, use 10-Ω resistors and a power supply to simulator cell voltages; when familiar with the operation of the PowerLAN™ devices, then transition to use of a cell pack.

The bqWizard™ software that is included with the EVM is a powerful data acquisition tool that can log many different system parameters as well as help to generate small-lot production runs.

See the *bq78PL116 EVM User's Guide* (SLUU474) and the *bqWizard™ User's Guide* (SLUU336) for more details.

### 1.5.2 Battery Pack

To take advantage of the advanced-feature set of the PowerLAN™ Master Gateway Controller, the electrical and chemical characteristics of the battery pack must be communicated to the controller prior to use at the production level. This is done through various configuration files loaded by the bqWizard™ software. Three important characteristics are cell chemistry, pack size, and pack construction.

Simple experimentation can be performed without providing full description of the pack. However, some unexpected results may occur if the full characteristics of the pack are not provided.

#### 1.5.2.1 Cell Chemistry

The PowerLAN™ Master Gateway Controller features a gas gauge whose performance is tied to the type of lithium ion cell chemistry used. Each cell chemistry requires that a matching chemistry file (*.chem) be used that accurately characterizes the cell. See the application report *Chemistry Selection for bq78PL116* (SLUA505).

The default chemistry loaded with the firmware is CHEM ID 107. Numerous chemistry files have been developed to date which are accessed through the bqWizard™ software. If the cell being used is not in the library of chemistry files, a characterization test must be performed to generate the chemistry file and subsequent CHEM ID number. For instance, the CHEM ID 0400 represents a $LiFePO_4$ chemistry type. Characterization of cell chemistry and generation of the CHEM ID is done by Texas Instruments Battery Management Application Engineering.

Chemistry data also is used for other advanced features such as PowerPump™ cell balancing and impedance growth calculations.

**CAUTION:** It is only after a chemistry file (.chem) and an auxiliary chemistry file (.aux) are loaded via the bqWizard™ software that the complete cell impedance information is written into the PowerLAN™ controller. Therefore, the auxiliary data collection run and subsequent .aux file must be created for the target pack. If a custom .aux file is not created, the default impedances (107), are used for calculations that require impedance values. This may cause errors if the target cell impedance is different from CHEM ID 107.

#### 1.5.2.2 Pack Size and System Design

Battery pack size is described in terms of series count (y) and parallel count(x). An 8S3P pack means that the battery pack consists of three parallel cells connected in a series of eight cells. If each cell is a nominal 3.7 V and has a capacity of 2200 mAHr, the 8S3P pack is a nominal 29.6 V and with a 6600-mAHr capacity.

Specifying pack size in the PowerLAN™ Gateway Controller's parameter data set determines the number of PowerLAN™ nodes that are created to monitor cell voltage, cell temperature, and coordinate PowerPump™ balancing. The PowerLAN™ Master Gateway Controller monitors up to four series cells. For packs larger than four, a PowerLAN™ Dual Cell Monitor, bq76PL102, is used to monitor every two additional series cells.


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Pack size, current measurement range, state-of-charge indication, and other aspects of the battery management system design are programmed by loading a Configuration File (*.tmap) in the bqWizard™ software. Details of the configuration file operation are found in the application report *What is a .tmap file?* (SLUA542).

#### 1.5.2.3 Pack Construction

The chemistry file previously mentioned describes the operation of the unit cell. An auxiliary chemistry file (*.aux) is needed to change the .chem file so that it represents the cells when they are physically connected together to make up a battery pack. For example, cell strap impedance (length) for each cell connection may not be the same due to mechanical constraints. This is factored into the equivalent cell model to make an application-specific cell model. Pack modeling is accomplished through a data collection test run as described in the application report *Chemistry Selection for the bq78PL116* (SLUA505). The data then is processed by the bqWizard™ software and loaded into the device.

### *1.5.3 Design and Build Prototype Circuitry*

#### 1.5.3.1 System Design

See the application report *bq78PL114 System Design Guidelines* (SLUA537) for details on system design, reference schematic, and PCB layout. The only difference between System Design for bq78PL116 and bq78PL114S12 is that the number of temperature sensors in the system is limited to the four that can be connected to the bq78PL116. And, the bq78PL116 can operate up to 16 series cell packs.

### *1.5.4 Parameter Set*

The parameter set specifies all of the values programmable by the user. The parameters are organized into sections called SBData Static, Charge Control, Cell Balancing, Cell Chemistry, Pack Configuration, Safety Level 1, and Safety Level 2. These sections correspond to the tabbed sections in the bqWizard™ software. Most values can either be edited in the bqWizard™ software or saved to a file (*.ppcsv), edited offline in a spreadsheet program, and then re-loaded into the device.

These parameters govern the operation of the system. Each parameter must be set to match the target battery pack in use. The default parameter set that is included is for a 3S1P pack with CHEM ID 107. The lowest cell count configuration was used as the default because despite the series cell count of the pack connected to the bqWizard it will open and show three cells. If a 16 cell pack was the default, then any pack with fewer cells would cause a communications error upon start up. This also makes it a safe configuration too because if the user attempts to use a pack larger than 3S and neglects to update the parameter set, the pack overvoltage rule (POV) prematurely activates to open the charge MOSFET.

Many safety rules can be deactivated by setting their timer to zero. This allows the reduction of the safety rule set to a minimal level if only basic safety is needed.

### *1.5.5 Validation Testing*

Final test and evaluation of the PowerLAN™ battery management system must only occur with a completely designed system that is representative of the production unit. Using hardware that is properly configured to manage and control the battery pack is critical to achieve the best performance. For instance, a CHEM ID file that does not match the cells under test can result in higher than normal gas gauge inaccuracy.

Thorough performance testing should be conducted prior to making the .dat file. It would not be beneficial if many thousands of packs were made based on an untested .dat clone file.

### *1.5.6 Production Readiness*

#### 1.5.6.1 Golden Flash File (*.dat)

The configuration files customize the PowerLAN™ controller to suit the application needs. These files



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(.tmap, .ppcsv, .chem, .sbd, .aux) are then combined into a single production configuration file called a (.dat) file during the Production Readiness phase. The bqWizard™ software is used to extract the (.dat) file from the PowerLAN™ Master Gateway Controller. The (.dat) file then is used to clone each production pack. This file is often referred to as the *Golden Flash File*. The file is encoded and ensures a level of protection against tampering.

**NOTE:** The .dat file does not contain calibration information. Each device must have its temperature and current measurement systems calibrated.

#### 1.5.6.2 Production Software

The bqWizard™ software is intended for experimentation and development of a prototype system in a laboratory environment. The bq78PL11x API is a Windows™ .NET Application Programming Interface (API). The API is intended to allow users to automate their production flow. Essential tasks such as configuration and calibration of each battery pack can be accomplished using the API and the appropriate software and hardware interfaces.

#### 1.5.6.3 Production Hardware

The SMBus interface to be used in production is the USB-TO-GPIO EVM. This is available through Texas Instruments. This USB adapter provides the communication and control needed to complete the typical production flow. The USB-TO-GPIO is based on Texas Instruments' Universal Serial Bus General-Purpose Device Controller TUSB3210. Schematic, bill of materials, and PCB layout information for the USB-TO-GPIO EVM is available if users wish to incorporate the circuit into their production hardware.


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# First-Level Protection Features

The bq78PL116 supports multilevel safety functions for a variety of battery-pack parameters. The first-level safety protection features are a group of safety thresholds and responses which can be reset and which can occur at various speeds and threshold limits. Tier 1: Typically slow to act, and activation includes opening protection MOSFETs to interrupt current flow in the battery pack. Tier 2: Faster-reacting action, usually a higher threshold is needed to cause the reaction, and activation which includes opening protection MOSFETs to interrupt current flow in the battery pack. Hardware Safety: Very fast reaction, on the order of milliseconds, usually at still-higher activation thresholds which also cause the protection MOSFETs to interrupt current flow in the battery pack. This wide range of battery and system protection features is easily configured or enabled via the integrated data flash. The bq78PL116 does not support the JEITA standard.

Some safety functions are configured using the Hardware Configuration or Algorithm registers. All first level protection features depend on the parameters listed under the "Safety Level 1" tab of the bqWizard software.

Setting threshold values and other configuration parameters can be accomplished using the bqWizard™ graphical user interface (GUI). All times listed throughout this section have a set point tolerance. This is approximately +1.6/–0 seconds, except for Hardware Short Circuit and Hardware Over Current Charge/Discharge. This means that a 10 second time, for instance COV Time, could actually take 10 to 11.6 seconds. This is a function of the accuracy of the firmware timers.

## 2.1 Cell Overvoltage

The bq78PL116 can detect cell overvoltage and protect battery cells from damage.

This condition is evaluated once per second after all cell voltages are measured. The following user-defined parameters govern the behavior of this rule:

(a) COV Threshold: Set in units of mV

(b) COV Time: Set in units of 1 second. Setting to zero disables the function.

(c) COV Recovery: Set in units of mV

(d) COV High-Temperature Adjust: Set in units of 0.1°C

(e) COV High-Temperature Threshold: Set in units of mV

Activation criteria/behavior: When any cell voltage rises above the COV Threshold, the COV Alert Flag (Safety Alert Register, Bit 5) for this condition is set to indicate the presence of the overvoltage condition. If the condition remains true beyond the COV Time, then the COV Alert Flag is cleared and the COV Status flag (Safety Status Register, Bit 5) for this condition is set, and the following safety actions are taken. If the condition clears within the COV Time, then no action is taken, and the COV Alert Flag is cleared. If any cell temperature exceeds the COV High Temperature Adjust, the COV High Temperature Threshold is used instead of the COV Threshold for determining activation.

Activation of this rule exhibits the following behavior:

(a) Charge and precharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:ChargingVoltage(0x15) is set to 0.

(d) SBS:ChargingCurrent(0x14) is set to 0.

(e) BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.



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Deactivation criteria/behavior: When all cell voltages fall below COV Recovery, the following actions are taken:

(a) Charge and precharge MOSFETs are closed.

(b) Safety Status Bit 5, and Bit 2 of the Cell Status Registers for cells in COV are cleared.

(c) SBS:ChargingVoltage(0x15) is set to allow charge.

(d) SBS:ChargingCurrent (0x14) is set to allow charge.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

## 2.2 Cell Undervoltage

The bq78PL116 can detect cell undervoltage and protect battery cells from damage.

This condition is evaluated once per second after all cell voltages are measured. The following user-defined parameters govern the behavior of this rule:

(a) CUV Threshold: Set in units of mV

(b) CUV Time: Set in units of 1 second. Setting to zero disables the function.

(c) CUV Recovery: Set in units of mV

Activation criteria/behavior: When any cell voltage falls below the CUV Threshold, the CUV Alert Flag (Safety Alert Register Bit 7) for this condition is set to indicate the presence of the undervoltage condition. If the condition remains beyond the CUV Time, then the CUV Alert flag is cleared and the CUV Status Flag (Safety Status Register Bit 7) for this condition is set, and safety action is taken. If the condition clears within the CUV Time, then no action is taken, and the alert flag is cleared.

Activation of this rule exhibits the following behavior:

(a) The discharge MOSFET is opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[FD] Fully Discharged bit is set.

Deactivation criteria/behavior: When all cell voltages rise above CUV Recovery, the following actions are taken:

(a) The discharge MOSFET is closed.

(b) Safety-status and alert flags for this condition are cleared.

In cell undervoltage condition, the DSG FET is turned on during charging to prevent overheating of the DSG FET body diode.

## 2.3 Extreme Cell Undervoltage

The bq78PL116 can be programmed to go into an ultra low power state, called Extreme Cell Undervoltage, when certain conditions are present. This state of operation that is not entered in normal cycling of the battery. It is used to gracefully shut down the bq78PL116 in the event that cell voltages drop to an unstable state.

This condition is evaluated once per second after all cell voltages are measured. The following user-defined parameters govern the behavior of this rule:

(a) EUV Threshold: Set in units of mV below 2800. Do not set to above this value as this mode of operation cannot be guaranteed above 2800 mV.

(b) EUV Time: Set in units of 1 second. Setting to zero disables the function.

(c) EUV Recovery: Set in units of mV to 2900. Do not change this parameter as hardware recovery is controlled by the datasheet parameter $V_{startup}$.

Activation criteria/behavior: When any cell voltage falls below the EUV Threshold, the EUV Alert Flag (Safety Alert Register Bit 3) for this condition is set to indicate the presence of the extreme undervoltage condition. If the condition remains beyond the EUV Time, then EUV Safety Flag (Safety Status Bit 3) for this condition is set, and safety action is taken. If the condition rises above EUV Recovery point prior to the expiration of the EUV Time, then the alert condition is cleared.



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Activation of this rule exhibits the following behavior (in no particular order):

(a) The charge and discharge MOSFETs are opened.

(b) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(c) SBS:BatteryStatus(0x16):[FD] Fully Discharged bit is set.

(d) Enter extreme undervoltage low-power state

(e) SMBus Communications stop.

While in the EUV state, all functions cease and the device is in reset. The part recovers when cell voltages rise above the hardware recovery level, see data sheet. The recovery level is specifically controlled by the voltage on the V1 pin. When this occurs, the following actions are taken (in no particular order):

(a) The discharge MOSFET is closed.

(b) Safety-status and alert flags for this condition are cleared.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is cleared

(d) The undervoltage low-power state is exited.

**NOTE:** The EUV condition is not logged to nonvolatile memory.

## 2.4 Pack Overvoltage

The bq78PL116 can detect battery pack overvoltage and protect the battery pack from damage.

This condition is evaluated once per second. The pack voltage is constructed as a summation of the individual cell voltage measurements, which occurs once per second.

The following user-defined parameters govern the behavior of this rule:

(a) POV Threshold: Set in units of mV

(b) POV Time: Set in units of 1 second. Setting to zero disables the function.

(c) POV Recovery: Set in units of mV

Activation criteria/behavior: When the pack voltage rises above the POV Threshold, the POV Alert Flag (Safety Alert Register Bit 8) for this condition is set to indicate the presence of the pack overvoltage condition. If the condition remains beyond the POV Time, then the POV Status Flag (Safety Status Register Bit 8) for this condition is set, and safety action is taken. If the condition clears within the POV Time, then no action is taken, and the alert flag is cleared.

Activation of this rule exhibits the following behavior:

(a) Charge and precharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:ChargingVoltage(0x15) is set to 0.

(d) SBS:ChargingCurrent(0x14) is set to 0.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

Deactivation criteria/behavior: When the pack voltage falls below POV Recovery, the following actions are taken:

(a) Charge and precharge MOSFETs are closed.

(b) Safety-status and alert flags for this condition are cleared.

(c) SBS:ChargingVoltage(0x15) is set to allow charge.

(d) SBS:ChargingCurrent(0x14) is set to allow charge.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

## 2.5 Pack Undervoltage

The bq78PL116 can detect battery pack undervoltage and protect the battery pack from damage.

This condition is evaluated once per second. The Pack Voltage is constructed as a summation of the individual cell voltage measurements, which occurs once per second.



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The following user-defined parameters govern the behavior of this rule:

(a) PUV Threshold: Set in units of mV

(b) PUV Time: Set in units of 1 second. Setting to zero disables the function.

(c) PUV Recovery: Set in units of mV

Activation criteria/behavior: When the pack voltage falls below the PUV Threshold, the PUV Alert Flag (Safety Alert Register Bit 9) for this condition is set to indicate the presence of the undervoltage condition. If the condition remains beyond the PUV Time, then the PUV Status Flag (Safety Status Register Bit 9) for this condition is set, and safety action is taken. If the condition clears within the PUV Time, then no action is taken, and the alert flag is cleared.

Activation of this rule exhibits the following behavior:

(a) The discharge MOSFET is opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[FD] Fully Discharged bit is set.

Deactivation criteria/behavior: When the pack voltage rises above PUV Recovery, the following actions are taken:

(a) The discharge MOSFET is closed.

(b) Safety alert and status flags for this condition are cleared.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is cleared.

## 2.6 Charge Overcurrent – Tier 1

The first level of bq78PL116 overcurrent protection for charge is discussed as follows.

This condition is evaluated once per second after the current measurement is complete.

The following user-defined parameters govern the behavior of this rule:

(a) OC Charge Tier 1 Threshold: Set in units of mA

(b) OC Charge Tier 1 Time: Set in units of 1 second. Setting to zero disables the function.

(c) OC Charge Tier 1 Recovery: Set in units of 1 second

(d) OC Max Attempts: Integer units. Setting to zero causes rule to immediately start trip/try at 255-second intervals; setting to 255 enables continuous retries at intervals equal to OC Charge Tier 1 Recovery.

Activation criteria/behavior: When the current during charge exceeds OC Charge Tier 1 Threshold, the OCC Alert Flag (Safety Alert Register Bit 12) for this condition is set to indicate the presence of an overcurrent condition. If the condition remains beyond the OC Charge Tier 1 Time, then the OCC Status Flag (Safety Status Register Bit 12) for this condition is set, and safety action is taken. If the condition clears within the OC Charge Tier 1 Time, then no action is taken, and the alert flag is cleared.

Activation of this rule exhibits the following behavior:

(a) The charge and precharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:ChargingVoltage(0x15) is set to 0.

(d) SBS:ChargingCurrent(0x14) is set to 0.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.



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Deactivation criteria/behavior: When the OC Charge Tier 1 Recovery time has elapsed, the following actions are taken:

(a) The charge and precharge MOSFETs are closed.

(b) The safety alert and status flags for this condition are cleared.

(c) SBS:ChargingVoltage(0x15) is set to allow charge.

(d) SBS:ChargingCurrent(0x14) is set to allow charge.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

If the *Activation criteria/behavior* condition still exists, then the process repeats for the number of times specified by OC Max Attempts except that the OC Charge Tier 1 Time is not used. The condition only has to be present for one sample time of 1 second. After the maximum number of attempts has been reached, the rule continues to trip/try indefinitely at the maximum recovery time (255 seconds) until the fault is removed.

## 2.7 Discharge Overcurrent – Tier 1

The first level of bq78PL116 overcurrent protection for discharge is described as follows.

This condition is evaluated once per second after the current measurement is complete.

The following user-defined parameters govern the behavior of this rule:

(a) OC Discharge Tier 1 Threshold: Set in units of mA

(b) OC Discharge Tier 1 Time: Set in units of 1 second. Setting to zero disables the function.

(c) OC Discharge Tier 1 Recovery: Set in units of 1 second

(d) OC Max Attempts: Integer units. (This value is set with the Charge Over Current – Tier 1 parameters.)

Activation criteria/behavior: When the current during discharge exceeds OC Discharge Tier 1 Threshold, the OCD Alert Flag (Safety Alert Register Bit 13) for this condition is set to indicate the presence of an overcurrent condition. If the condition remains beyond the OC Discharge Tier 1 Time, then the the OCD Status Flag (Safety Status Register Bit 13) for this condition is set, and safety action is taken. If the condition clears within the OC Discharge Tier 1 Time, then no action is taken, and the alert flag is cleared.

Activation of this rule exhibits the following behavior:

(a) The discharge MOSFET is opened.

(b) The fault is logged into nonvolatile memory.

Deactivation criteria/behavior: When OC Discharge Tier 1 Recovery time has elapsed, the following actions are taken:

(a) The discharge MOSFET is closed.

(b) The safety alert and status flags for this condition are cleared.

(c) SBS:ChargingCurrent(0x14) is set to allow full charge.

If the *Activation criteria/behavior* condition still exists, then the process repeats for the number of times specified by OC Max Attempts except that the OC Discharge Tier 1 Time is not used. The condition only has to be present for one sample time of 1 second. After the maximum number of attempts has been reached, the rule continues to trip/try indefinitely at the maximum recovery time (255 seconds) until the fault is removed.

## 2.8 Charge Overcurrent – Tier 2

The bq78PL116 has a second threshold for overcurrent on charge conditions.

This condition is evaluated once per second after the current measurement is complete.

The following user-defined parameters govern the behavior of this rule:

(a) OC Charge Tier 2 Threshold: Set in units of mA

(b) OC Charge Tier 2 Time: Set in units of 1 second. Setting to zero disables the function.

(c) OC Charge Tier 2 Recovery: Set in units of 1 second

(d) OC Max Attempts: Integer units. Setting to zero causes rule to immediately start trip/try at 255 second intervals; setting to 255 enables continuous retries at intervals equal to OC Charge Tier 1 Recovery.



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(This value is set with the Charge Over Current – Tier 1 parameters.)

Activation criteria/behavior: When the current during charge exceeds OC Charge Tier 2 Threshold, the OCC2 Alert Flag (Safety Alert Register Bit 10) for this condition is set to indicate the presence of an overcurrent condition. If the condition remains beyond the OC Charge Tier 2 Time, then the OCC2 Status Flag (Safety Status Register Bit 10) for this condition is set, and safety action is taken. If the condition clears within the OC Charge Tier 2 Time, then no action is taken, and the alert flag is cleared.

Activation of this rule exhibits the following behavior:

(a) The charge and precharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:ChargingVoltage(0x15) is set to 0.

(d) SBS:ChargingCurrent(0x14) is set to 0.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

Deactivation criteria/behavior: When the OC Charge Tier 2 Recovery time has elapsed, the following actions are taken:

(a) The charge and precharge MOSFETs are closed.

(b) The safety alert and status flags for this condition are cleared.

(c) SBS:ChargingVoltage(0x15) is set to allow charge.

(d) SBS:ChargingCurrent(0x14) is set to allow charge.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

If the *Activation criteria/behavior* condition still exists, then the process repeats for the number of times specified by OC Max Attempts except that the OC Charge Tier 2 Time is not used. The condition only has to be present for one sample time of 1 second. After the maximum number of attempts has been reached, the rule continues to trip/try indefinitely at the maximum recovery time (255 seconds) until the fault is removed.

## 2.9 Discharge Overcurrent – Tier 2

The bq78PL116 provides a second level of overcurrent on discharge detection.

This condition is evaluated once per second after the current measurement is complete.

The following user-defined parameters govern the behavior of this rule:

(a) OC Discharge Tier 2 Threshold: Set in units of mA

(b) OC Discharge Tier 2 Time: Set in units of 1 second. Setting to zero disables the function.

(c) OC Discharge Tier 2 Recovery: Set in units of 1 second

(d) OC Max Attempts: Integer units. (This value is set with the Charge Over Current – Tier 1 parameters.)

Activation criteria/behavior: When the current during discharge exceeds OC Discharge Tier 2 Threshold, the OCD2 Alert Flag (Safety Alert Register Bit 11) for this condition is set to indicate the presence of an overcurrent condition. If the condition remains beyond the OC Discharge Tier 2 Time, then the OCD2 Status Flag (Safety Status Register 11) for this condition is set, and safety action is taken. If the condition clears within OC Discharge Tier 2 Time, no action is taken, and the alert flag is cleared.

Activation of this rule exhibits the following behavior:

(a) The discharge MOSFET is opened.

(b) The fault is logged into nonvolatile memory.

Deactivation criteria/behavior: When the OC Discharge Tier 2 Recovery time elapses, the following actions are taken:

(a) The discharge MOSFET is closed.

(b) The safety alert and status flags for this condition are cleared.

(c) SBS:ChargingCurrent(0x14) is set to allow full charge.



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If the *Activation criteria/behavior* condition still exists, then the process repeats for the number of times specified by OC Max Attempts except that the OC Discharge Tier 2 Time is not used. The condition only has to be present for one sample time of 1 second. . After the maximum number of attempts has been reached, the rule continues to trip/try indefinitely at the maximum recovery time (255 seconds) until the fault is removed.

## 2.10 Hardware Overcurrent Charge

The bq78PL116 provides fast-acting overcurrent detection mechanisms, such as for overcurrent during charge. A selection of delay times and activation thresholds is available. The condition for overcurrent on charge is continuously monitored by hardware. This hardware safety feature is not influenced by the IPScale factor defined in the SBData Specification.

In some applications, it may be desirable to have different thresholds and trip times when in standby mode. The bq78PL116 provides an alternate threshold and time parameter set for when the part is in low-power standby mode. When the bq78PL116 transitions to standby mode, the Hardware LP Charge Threshold and Hardware LP Charge Duration parameters are loaded in place of the respective Hardware OC Charge Threshold and Hardware OC Charge Time parameters. The condition for hardware low-power overcurrent charge is continuously monitored by hardware while the part is in standby mode. If an overcurrent condition is detected, the original hardware overcurrent parameters are restored and the part transitions to active mode. The user must set Hardware LP Overcurrent Charge threshold and duration parameters to be the same as their corresponding Hardware Overcurrent Charge Threshold and Hardware Overcurrent Charge Time parameters if they are not being used.

**Note:** The bq78PL116 uses a 10 mΩ current sense resistor as a default. The resistor value is assignable by the user through the Pack Configuration File (.tmap). The following discussion uses a 10 mΩ resistor to generate the numbers mentioned.

**CAUTION:** All hardware-based safety functions have a minimum activation threshold of 42 mV across the current-sense resistor. For the 10-mΩ current-sense resistor used by the bq78PL116, this corresponds to a 4.2-A minimum threshold.

Setting a register value for a threshold below this limit causes the safety condition to occur at the minimum threshold described above.

The following user-defined parameters govern the behavior of this rule:

(a) Hardware OC Charge Threshold: Set as an integer register value between 0 and 220, where each increment corresponds to a –0.122 mA step from 31.19 A maximum (register value of 0) to 4.2 A minimum (register value of 220).

Example: A register value of 128 sets the OC Charge Threshold limit to 15.53 A. Settings are stable to within 2 step increments or approximately 244 mA. A value of 128 nominally trips at 15.53 A, but could trip as low as 15.3 A or as high as 15.8 A.

**CAUTION:** With the 10-mΩ sense resistor, the register value must never be set above 220, which corresponds to an OC charge threshold of 4.2 A.

(b) Hardware OC Charge Time: Set as an integer register value between 1 and 127, where each increment corresponds to an 830-µs step from 900 µs minimum (register value of 1) to 106 ms maximum (register value of 127).

(c) Hardware LP Charge Threshold: Set as an integer register value between 0 and 220, where each increment corresponds to a –122-mA step from 31.19 A maximum (register value of 0) to 4.2 A minimum (register value of 220).

(d) Hardware LP Charge Duration: Set as an integer register value between 1 and 127, where each increment corresponds to an 830-µs step from 900 µs minimum (register value of 1) to 106 ms maximum (register value of 127).

Example: A register value of 1 sets the OC Charge Time limit to 900 µs, whereas a register value of 63 sets the time limit to 52.6 ms.

(e) Hardware OC Charge Recovery: Set in units of seconds

(f) HOC Max Attempts: Integer units. Setting to zero causes rule to immediately start trip/try at 255 second intervals; setting to 255 enables continuous retries at intervals equal to Hardware OC Charge Recovery.


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Activation criteria/behavior: Hardware is activated when the charge current exceeds Hardware OC Charge Threshold for the Hardware OC Charge Time.

Activation of this rule exhibits the following behavior:

(a) The HOCC Status Flag (Safety Status Register Bit 1) for this function is set.

(b) The fault is logged into nonvolatile memory.

(c) All MOSFETs are opened (hardware controlled).

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(e) SBS:ChargingVoltage(0x15) is set to 0.

(f) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria/behavior: When the Hardware OC Charge Recovery time elapses, the following actions are taken:

(a) All MOSFETs are closed.

(b) The status flag for this condition is cleared.

(c) SBS:ChargingVoltage(0x15) is set to allow charge.

(d) SBS:ChargingCurrent(0x14) is set to allow charge.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

If the *Activation criteria/behavior* condition still exists, then the process repeats for the number of times specified by HOC Max Attempts. After the maximum number of attempts has been reached, the rule continues to trip/try indefinitely at the maximum recovery time (255 seconds) until the fault is removed.

The following table provides details on the hardware overcurrent charge threshold levels. The tolerance value is the amount the actual trip threshold may vary below and above the typical point. Each decrease of 1 in the register value increases the overcurrent charge threshold by an amount corresponding to the step size. If the register value is set for a threshold below the lowest point, the charge overcurrent condition is not detected.

| Device | Sense Resistor (mΩ) | Hardware OC CHG Threshold | HW OC CHG Register Value, Decimal | Hardware Overcurrent Charge Threshold (Amps) | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Tolerance | Step Size |
| bq78PL116 | 10 | Lowest | 220 | 4.04 | 4.28 | 4.53 | ±0.244 | –0.122 |
| | | Highest | 0 | 30.94 | 31.19 | 31.43 | | |
| | 3 | Lowest | 220 | 13.45 | 14.27 | 15.08 | ±0.816 | –0.408 |
| | | Highest | 0 | 103.15 | 103.96 | 104.78 | | |
| | 1 | Lowest | 220 | 40.36 | 42.81 | 45.25 | ±2.446 | –1.223 |
| | | Highest | 0 | 309.44 | 311.89 | 314.33 | | |

Equations to calculate the typical Hardware Overcurrent Charge (HOCC) register value, tolerance, and step size are as follows.

OC Step Size, Amps = $OC_{STEP}$ = –0.3125/Resistor/255.5 = $–1.223 \times 10^{-3}$/Resistor

Register Value, unit-less = Integer[(Threshold in Amps/$OC_{STEP}$ ) + 255]

Threshold in Amps must be greater than the value at a register setting of 220.

Threshold Tolerance, Amps = ±2 × $OC_{STEP}$

## 2.11 Hardware Overcurrent Discharge

The bq78PL116 provides fast-acting overcurrent detection mechanisms, such as overcurrent during discharge. The condition for hardware overcurrent on discharge is continuously monitored by hardware.

In some applications it may be desirable to have different thresholds and trip times when in standby mode. The bq78PL116 provides an alternate threshold and time parameter set for when the part is in low power standby mode. When the bq78PL116 transitions to standby mode, the Hardware LP Discharge Threshold and Hardware LP Discharge Duration parameters are loaded in place of the respective Hardware OC Discharge Threshold and Hardware OC Discharge Time parameters. The condition for hardware



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low-power overcurrent discharge is continuously monitored by hardware while the part is in standby mode. If an overcurrent condition is detected, the original hardware overcurrent parameters are restored and the part transitions to active mode. The user must set Hardware LP Overcurrent Discharge threshold and duration parameters to be the same as their corresponding Hardware Overcurrent Discharge Threshold and Hardware Overcurrent Charge Time parameters if they are not being used.

Note: The bq78PL116 uses a 10-mΩ current sense resistor as a default. The resistor value is assignable by the user through the Pack Configuration File (.tmap). The following discussion uses a 10 milli-ohm resistor to generate the numbers mentioned.

**CAUTION:** All hardware-based safety functions have a minimum activation threshold of 42 mV across the current-sense resistor. For a 10-mΩ current-sense resistor, this corresponds to a 4.2-A minimum threshold.

Setting a register value for a threshold below this limit causes that safety condition never to be detected, regardless of the setting.

The following user-defined parameters govern the behavior of this rule:

(a) Hardware OC Discharge Threshold: Set as an integer register value between 35 and 255, where each increment corresponds to a 122-mA step to 31 A maximum (register value of 255).

Example: A register value of 128 sets the threshold limit to 15.66 A. Settings are stable to within 2 step increments, or approximately 244 mA. A value of 128 nominally trips at 15.66 A, but could trip as low as 15.4 A or as high as 15.9 A.

**CAUTION:** When the 10-mΩ sense resistor, the register value must never be set below 35, which corresponds to an OC discharge threshold of 8.6 A.

(b) Hardware OC Discharge Time: Set as an integer register value between 1 and 127, where each increment corresponds to an 830-µs step from 900 µs minimum (register value of 1) to 106 ms maximum (register value of 127).

(c) Hardware LP Discharge Threshold: Set as an integer register value between 35 and 255, where each increment corresponds to a 122-mA step to 31 A maximum (register value of 255).

(d) Hardware LP Discharge Duration: Set as an integer register value between 1 and 127, where each increment corresponds to an 830-µs step from 900 µs minimum (register value of 1) to 106 ms maximum (register value of 127).

Example: A register value of 1 sets the OC discharge time limit to 900 µs, whereas a register value of 63 sets the time limit to 52.6 ms.

(e) Hardware OC Discharge Recovery: Set in units of seconds

(f) HOC Max Attempts: Integer units. (This value is set with the Hardware Over Current Charge parameters.)

Activation criteria/behavior: Hardware is activated when current exceeds Hardware OC Discharge Threshold limit for Hardware OC Discharge Time.

Activation of this rule exhibits the following behavior:

(a) The HOCD Status Flag (Safety Status Register Bit 0) for this function is set.

(b) The fault is logged into nonvolatile memory.

(c) All MOSFETs are opened (hardware controlled).

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Discharge Alarm bit is set.

(e) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria/behavior: When the Hardware OC Discharge Recovery time elapses, the following actions are taken:

(a) All MOSFETs are closed.

(b) The status flag for this condition is cleared.

(c) SBS:ChargingCurrent(0x14) is set to allow charge.

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Discharge Alarm bit is cleared.

If the *Activation criteria/behavior* condition still exists, then the process repeats for the number of times specified by HOC Max Attempts. After the maximum number of attempts has been reached, the rule continues to trip/try indefinitely at the maximum recovery time (255 seconds) until the fault is removed.


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The following table provides details on the hardware overcurrent discharge threshold levels. The tolerance value is the amount the actual trip threshold may vary below and above the typical point. Each increase of 1 in the register value increases the overcurrent discharge threshold by an amount corresponding to the step size. If the register value is set for a threshold below the lowest point,the discharge overcurrent condition is not detected.

| Device | Sense Resistor mΩ | Hardware OC DSG Threshold | HW OC DSG Register Value, Decimal | Hardware Overcurrent Discharge Threshold (A) | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Tolerance | Step Size |
| bq78PL116 | 10 | Lowest | 35 | 4.04 | 4.28 | 4.53 | ±0.244 | 0.122 |
| | | Highest | 255 | 30.94 | 31.19 | 31.43 | | |
| | 3 | Lowest | 35 | 13.45 | 14.27 | 15.08 | ±0.816 | 0.408 |
| | | Highest | 255 | 103.15 | 103.96 | 104.78 | | |
| | 1 | Lowest | 35 | 40.36 | 42.81 | 45.25 | ±2.446 | 1.223 |
| | | Highest | 255 | 309.44 | 311.89 | 314.33 | | |

Equations to calculate the typical Hardware Overcurrent Discharge (HOCD) register value, tolerance, and step size are as follows.

OC Step Size, Amps = $OC_{STEP}$ = 0.3125/Resistor/255.5 = $1.223 \times 10^{-3}$/Resistor

Register Value, unit-less = Integer [Threshold in Amps/$OC_{STEP}$]

Threshold in Amps must be greater than the value at a register setting of 35

Threshold Tolerance, Amps = ±2 × $OC_{STEP}$

## 2.12 Hardware Short Circuit

The bq78PL116 provides an overcurrent-on-discharge threshold meant to detect short-circuit (very high-discharge) events.

The condition for hardware short circuit is continuously monitored in hardware.

Note: The bq78PL116 uses a 10-mΩ current sense resistor as a default. The resistor value is assignable by the user through the Pack Configuration File (.tmap). The following discussion uses a 10 mΩ resistor to generate the numbers mentioned.

**CAUTION:** All hardware-based safety functions have a minimum activation threshold of 42 mV across the current-sense resistor. For a 10-mΩ current-sense resistor, this corresponds to a 4.2-A minimum threshold. Setting a register value for a threshold below this limit causes that safety condition never to be detected, regardless of the setting.

The following user-defined parameters govern the behavior of this rule:

(a) Hardware Short-Circuit Threshold: Set as an integer register value between 37 and 63, where each increment corresponds to a 1-A step to 31 A maximum (register value of 63).

Example: A register value of 50 sets the threshold limit to 17.9 A. Settings are stable to within 2 step increments, or approximately 2 A. A value of 50 nominally trips at 17.8 A, but could trip as low as 15.8 A or as high as 19.8 A.

**CAUTION:** When the 10-mΩ sense resistor, the register value must never be set below 37, which corresponds to a short-circuit threshold of 4.96 A.

(b) Hardware Short-Circuit Time: Set as an integer register value between 1 and 31, where each increment corresponds to a 104-µs step from 100 µs minimum (register value of 1) to 3.2 ms maximum (register value of 31).

Example: A register value of 2 sets the hardware short-circuit time limit to 200 µs, whereas a register value of 15 sets the time limit to 1.6 ms.

(c) Hardware Short Circuit Recovery: Set in units of seconds

(d) HSC Max Attempts: Integer units. Setting to zero causes the rule to immediately start trip/try at 255 second intervals; setting to 255 enables retry at intervals equal to Hardware Short Circuit Recovery.

Activation criteria/behavior: Hardware activated when current exceeds Hardware Short Circuit Threshold for Hardware Short Circuit Time. Activation of this rule exhibits the following behavior:



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(a) The HSC Status Flag (Safety Register Bit 2) for this function is set.
(b) The fault is logged into nonvolatile memory.
(c) All MOSFETs are opened (hardware controlled).
(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.
(f) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria/behavior: When the Hardware Short Circuit Recovery time elapses, the following actions are taken:

(a) All MOSFETs are closed.
(b) The safety-status flag for this condition is cleared.
(c) SBS:ChargingCurrent(0x14) is set to allow charge.
(d) SBS:ChargingVoltage(0x15) is set to allow charge.
(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

If the *Activation criteria* condition still exists, then the process repeats for the number of times specified by HSC Max Attempts. After the maximum number of attempts has been reached, the rule continues to trip/try indefinitely at the maximum recovery time (255 seconds) until the fault is removed.

The following table provides details on the hardware short circuit threshold levels. The tolerance value is the amount the actual trip threshold may vary below and above the typical point. Each increase of 1 in the register value increases the over short circuit threshold by an amount corresponding to the step size. If the register value is set for a threshold below the lowest point the short circuit condition will not be detected.

| Device | Sense Resistor mΩ | SC Trip Level | HW SC Register Value, Decimal | Hardware Short Circuit Threshold (Amps) | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Tolerance | Step Size |
| bq78PL116 | 10 | Lowest | 37 | 2.98 | 4.96 | 6.94 | ±1.984 | 0.992 |
| | | Highest | 63 | 28.77 | 30.75 | 32.74 | | |
| | 3 | Lowest | 37 | 9.92 | 16.53 | 23.15 | ±6.614 | 3.307 |
| | | Highest | 63 | 95.90 | 102.51 | 109.13 | | |
| | 1 | Lowest | 37 | 29.76 | 49.60 | 69.44 | ±19.842 | 9.921 |
| | | Highest | 63 | 287.70 | 307.54 | 327.38 | | |

Equations to calculate the typical Hardware Short Circuit (HSC) register value, tolerance, and step size are as follows.

OC Step Size, Amps = $OC_{STEP}$ = –0.3125/Resistor/231.5 = 9.921 × $10^{-3}$/Resistor
Register Value, unit-less = Integer [(Threshold in Amps/$OC_{STEP}$)+32]
Threshold in Amps must be greater than the value at a register setting of 37
Threshold Tolerance, Amps = ±2 × $OC_{STEP}$

## 2.13 Overtemperature Charge

The bq78PL116 can be configured to interrupt charge current based on temperature.

This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) OT Charge Threshold: Set in units of 0.1°C
(b) OT Charge Time: Set in units of 2 seconds. Setting to zero disables the function.
(c) OT Charge Recovery: Set in units of 0.1°C

Activation criteria/behavior: During charge, when any cell temperature rises above the OT Charge Threshold, the OTC Alert Flag (Safety Alert Register Bit 14) for this condition is set to indicate the presence of an overtemperature condition. If the condition remains beyond the OT Charge Time, then the OTC Status Flag (Safety Status Register Bit 14) and OTC in the appropriate Cell Status Registers (Bit 4) for this condition is set, and safety action is taken. If the condition clears within the OT Charge Time, then no action is taken, and the alert flag is cleared.


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Activation of this rule exhibits the following behavior:

(a) Charge and precharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[OTA] Over Temperature Alarm bit is set.

(e) SBS:ChargingVoltage(0x15) is set to 0.

(f) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria/behavior: When all cell temperatures fall below OT Charge Recovery, the following actions are taken:

(a) Charge and precharge MOSFETs are closed.

(b) Safety-status and alert flags for this condition are cleared.

(c) SBS:ChargingVoltage(0x15) is set to allow charge.

(d) SBS:ChargingCurrent(0x14) is set to allow charge.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

(f) SBS:BatteryStatus(0x16):[OTA] Over Temperature Alarm bit is cleared.

Note: Although charge likely ceases when the activation of this rule occurs (due to the charge MOSFET being opened), the rule is still considered active until the deactivation criteria is met.

## 2.14 Overtemperature Discharge

The bq78PL116 can be configured to interrupt discharge based on temperature.

This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) OT Discharge Threshold: Set in units of 0.1°C

(b) OT Discharge Time: Set in units of 2 seconds. Setting to zero disables the function.

(c) OT Discharge Recovery: Set in units of 0.1°C

Activation criteria/behavior: During discharge, when any cell temperature rises above the OT Discharge Threshold, the OTD Alert Flag (Safety Alert Register Bit 15) for this condition is set to indicate the presence of an overtemperature condition. If the condition remains beyond the OT Discharge Time, then the OTD Status Flag (Safety Status Register Bit 15) and the OT Flag in the appropriate Cell Status Registers (Bit 4) for this condition is set, and safety action is taken. If the condition clears within the OT Discharge Time, then no action is taken, and the alert flag is cleared.

Activation of this rule exhibits the following behavior:

(a) The discharge MOSFET is opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[OTA] Over Temperature Alarm bit is set.

Deactivation criteria/behavior: When all cell temperatures fall below OT Discharge Recovery, the following actions are taken:

(a) The discharge MOSFET is closed.

(b) Safety-status and alert flags for this condition are cleared.

(c) SBS:BatteryStatus(0x16):[OTA] Over Temperature Alarm bit is cleared.

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

Note: Although discharge likely ceases when the activation of this rule occurs (due to the discharge MOSFET being opened), the rule is still considered active until the deactivation criteria are met.

## 2.15 Host Watchdog Timeout

The bq78PL116 can be configured to require the host system to communicate with the battery periodically, else the battery disables charging and discharging.



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Evaluation Interval. This condition is evaluated once every 2 seconds.

The following user-defined parameter governs the behavior of this rule:

(a) Host Watchdog Timeout: Set in units of 2 seconds. Setting to zero disables the function.

Activation criteria/behavior: When SMBus lines are energized (high) and SMBus communication ceases for Host Watchdog Timeout, the following actions are taken:

(a) All MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) The HWDG Flag (Safety Alert Register Bit 4) for this condition is set.

(d) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(f) SBS:ChargingVoltage(0x15) is set to 0.

(g) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria/behavior: When the presence of SMBus activity is detected, the following actions are taken:

(a) All MOSFETs are closed.

(b) Safety-status flag for this condition is cleared.

(c) SBS:ChargingVoltage(0x15) is set to allow charge.

(d) SBS:ChargingCurrent(0x14) is set to allow charge.

(e) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is cleared.

(f) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

## 2.16 Board Overtemperature

The bq78PL116 has an internal temperature sensor that is used to monitor the board temperature as well as correct for the temperature coefficient of the current measurement system. This sensor is referred to as the board sensor. It is used to determine if the temperature of the circuit board to which it is mounted is above a threshold set by the user.

This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) Board Over Temperature: Set in units of 0.1°C

(b) Board Over Temperature Time: Set in units of 2 seconds. Setting to zero disables the function.

(c) Board Over Temperature Recovery: Set in units of 0.1°C

Activation criteria/behavior: At any time, when the board temperature sensor detects a temperature that is above Board Over Temperature, the BOT Alert Flag (Safety Alert Register Bit 6) for this condition is set to indicate the presence of an overtemperature condition. If the condition remains beyond the Board Over Temperature Time, then the BOT Status Flag (Safety Status Register Bit 6) for this condition is set, and safety action is taken. If the condition clears within the Board Over Temperature Time, then no action is taken, and the alert flag is cleared. Activation of this rule exhibits the following behavior:

(a) The charge, precharge, and discharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(e) SBS:BatteryStatus0x16):[OTA] Over Temperature Alarm bit is set.

(f) SBS:ChargingVoltage(0x15) is set to 0.

(g) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria/behavior: When the board temperature-sensor indication falls below Board Over Temperature Recovery, the following actions are taken:

(a) The discharge MOSFET is closed.

(b) Safety-status and alert flags for this condition are cleared.

(c) SBS:BatteryStatus(0x16):[OTA] Over Temperature Alarm bit is cleared.



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(d) SBS:ChargingVoltage(0x15) is set to allow charge.

(e) SBS:ChargingCurrent(0x14) is set to allow charge.

(f) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is cleared.

(g) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is cleared.

## 2.17 Discharge Undertemperature

The bq78PL116 can be configured to detect undertemperature conditions using the temperature sensors assigned to the cells.

Evaluation Interval. This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) Discharge Under Temperature: Set in units of 0.1°C

(b) Discharge Under Temperature Time: Set in units of 2 seconds. Setting to zero disables the function.

(c) Discharge Under Temperature Recovery: Set in units of 0.1°C

Activation criteria/behavior: During discharge, when any cell temperature drops below the Discharge Under Temperature Threshold, the DUT Alert Flag (Safety Alert1 Register Bit 1) for this condition is set to indicate the presence of an undertemperature condition. If the condition remains beyond the Discharge Under Temperature Time, then the DUT Status Flag (Safety Status1 Register Bit 1) and the CUT Status Flag in the appropriate Cell Status Registers (Bit 5) for this condition is set, and safety action is taken. If the condition clears within the Discharge Under Temperature Time, then no action is taken, and the alert flag is cleared. Activation of this rule exhibits the following behavior:

(a) The discharge MOSFET is opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

Deactivation criteria/behavior: When all cell temperatures rise above Discharge Under Temperature Recovery, the following actions are taken:

(a) The discharge MOSFET is closed.

(b) Safety-status and alert flags for this condition are cleared.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is cleared.

Note: Although discharge likely ceases when the activation of this rule occurs (due to the discharge MOSFET being opened), the rule is still considered active until the deactivation criteria are met.

## 2.18 PowerLAN™ Communications Bus Failure

The PowerLAN network consists of a one wire interface between the PowerLAN node hardware in the bq78PL116 and also the bq76PL102 for series cell counts above 4. The bq78PL116 can detect if the bus fails and uses this rule to alert the SMBus Host.

This condition is evaluated once every 2 seconds.

The following user-defined parameter governs the behavior of this rule:

(a) PowerLAN™ Communications Bus Fail Time: Set in units of 2 seconds. Setting to zero disables the function.

Activation criteria/behavior: If PowerLAN™ communications bus failure is detected, the VLAN Alert Flag (Permanent Disable Alert Register Bit 9) for this condition is set. If the condition exists for longer than the period specified by PowerLAN™ Communications Bus Fail Time, the VLAN Status Flag (Permanent Disable Status Register Bit 9) for this condition is set, and the following actions are taken:

(a) Charge and discharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(e) SBS:ChargingVoltage(0x15) is set to 0.



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(f) SBS:ChargingCurrent(0x14) is set to 0.

(g) Cell balancing is discontinued.

Deactivation Criteria/behavior: The resumption of good PowerLAN communications clears failure condition. The following actions are then taken:

(a) Charge and Discharge MOSFETs are closed.

(b) The status flag for the condition is cleared.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm is cleared.

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm is cleared.

(e) SBS:ChargingVoltage(0x15) is set to Default Charging Voltage.

(f) SBS:ChargingCurrent(0x14) is set to Default Charging Current.

(g) Cell balancing is allowed to continue based on algorithm.



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# Second-Level Protection Features

The bq78PL116 provides features that can be used to indicate a more serious fault via the SPROT output. These outputs can be used to blow an inline fuse to permanently disable the battery pack from charge or discharge activity.

If any second-level protection threshold condition is met, the appropriate alert flag is set. If the threshold condition is cleared within the time limit, the appropriate flag is cleared. But if the threshold condition continues beyond the limit, then the bq78PL116 goes into a permanent failure condition and the appropriate flag is set.

Some safety functions are configured using the hardware configuration or algorithm enable registers. See Section 6.1 for a description of these registers. The parameters that govern the Second Level Protection Features are under the "Safety Level 2" tab in the bqWizard.

The deactivation of any active Second Level Protection rules is through issuance of the Reset Fuse command. This can be done through the bqWizard, user software developed via the bq78PL11x API or using the Extended SBData Controls accessed at Commands 0x80 and 0x81.

## 3.1 Secondary Cell Overvoltage (SOV)

Evaluation Interval. This condition is evaluated once every 2 seconds, although cell voltages are measured every second.

The following user-defined parameters govern the behavior of this rule:

(a) SOV Threshold: Set in units of mV

(b) SOV Time: Set in units of 2 seconds. Setting to zero disables the function.

Activation criteria/behavior: When any cell voltage rises above the SOV Threshold, the SOV Alert Flag (Permanent Disable Alert Register Bit 1) for this condition is set. If any cell voltage exceeds SOV Threshold for SOV Time, the SOV Status Flag (Permanent Disable Status Register Bit 1) for this condition is set and the following permanent actions are taken:

(a) All MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(e) SBS:ChargingVoltage(0x15) is set to 0.

(f) SBS:ChargingCurrent(0x14) is set to 0.

(g) Cell balancing is discontinued.

(h) The SPROT pin is set, and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.2 Secondary Overcurrent (SOC) Charge

Evaluation Interval. This condition is evaluated once every 2 seconds, although current measurements occur every second.

The following user-defined parameters govern the behavior of this rule:

(a) SOC Charge Threshold: Set in units of mA

(b) SOC Charge Time: Set in units of 2 seconds. Setting to zero disables the function.



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Activation criteria/behavior: When battery charge current exceeds the SOC Charge Threshold, the SOCC Alert Flag (Permanent Disable Alert Register Bit 10) for this condition is set. If the condition clears before SOC Charge time elapse, the alert flag is cleared. If the condition remains for longer than SOC Charge Time, the SOCC Status Flag (Permanent Disable Status Register Bit 10) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.
(f) SBS:ChargingCurrent(0x14) is set to 0.
(g) Cell balancing is discontinued.
(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.3 Secondary Overcurrent (SOC) Discharge

Evaluation Interval. This condition is evaluated once every 2 seconds, although current measurements occur every second.

The following user-defined parameters govern the behavior of this rule:

(a) SOC Discharge Threshold: Set in units of mA
(b) SOC Discharge Time: Set in units of 2 seconds. Setting to zero disables the function.

Activation criteria/behavior: When battery discharge current exceeds SOC Discharge Threshold, the SOCD Alert Flag (Permanent Disable Alert Register Bit 11) for this condition is set. If the condition clears before the SOC Discharge Time elapses, then the alert flag is cleared. If the condition remains for longer than SOC Discharge Time, the SOCD Status Flag (Permanent Disable Status Register Bit 11) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.
(f) SBS:ChargingCurrent(0x14) is set to 0.
(g) Cell balancing is discontinued.
(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.4 Secondary Overtemperature (SOT) Charge

Evaluation Interval. This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) SOT Charge Threshold: Set in units of 0.1°C
(b) SOT Charge Time: Set in units of 2 seconds. Setting to zero disables the function.

Activation criteria/behavior: During charge, if any cell temperature exceeds SOT Charge Threshold, the SOTC Alert Flag (Permanent Disable Alert Register Bit 2) for this condition is set. If the condition clears before the SOC Charge Time elapses, then the alert flag is cleared. If the condition remains for longer than SOT Charge Time, the SOTC Status Flag (Permanent Disable Status Register Bit 2) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory
(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.


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(f) SBS:ChargingCurrent(0x14) is set to 0.
(g) Cell balancing is discontinued.
(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.5 Secondary Overtemperature (SOT) Discharge

Evaluation Interval. This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) SOT Discharge Threshold: Set in units of 0.1°C
(b) SOT Discharge Time: Set in units of 2 seconds. Setting to zero disables the function.

Activation criteria/behavior: During discharge, if any cell temperature exceeds SOT Discharge Threshold, the SOTD Alert Flag (Permanent Disable Alert Register Bit 3) for this condition is set. If the condition clears before the SOT Discharge Time elapses, then the alert flag is cleared. If the condition remains for longer than SOT Discharge Time, the SOTD Status Flag (Permanent Disable Status Register Bit 3) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.
(f) SBS:ChargingCurrent(0x14) is set to 0.
(g) Cell balancing is discontinued.
(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.6 Cell Imbalance

Evaluation Interval. This condition is evaluated once every 2 seconds, although cell voltages are measured every second.

The following user-defined parameters govern the behavior of this rule:

(a) Cell Imbalance Current: Set in units of mA
(b) Cell Imbalance Fail Voltage: Set in units of mV
(c) Cell Imbalance Time: Set in units of 2 seconds; range is 0 to 65,535 seconds. Setting to zero disables the function.
(d) OCV Idle Qualifier: Set in units of minutes, range is 0 to 255 minutes.
(e) Cell Imbalance SOC Inhibit: Set in units of one percent (%)

Activation criteria/behavior: When at least one cell has a state-of-charge (SOC) that is above the Cell Imbalance SOC Inhibit, AND battery current (charge or discharge) has been below the Cell Imbalance Current limit for OCV Idle Qualifier, AND the difference between the highest and lowest cell voltage exceeds the Cell Imbalance Fail Voltage, then the CIM Alert Flag (Permanent Disable Alert Register Bit 4) for this condition is set. If all conditions clear before the Cell Imbalance Time elapses, then the alert flag is cleared. If all of these conditions persist longer than the Cell Imbalance Time, then the CIM Status Flag (Permanent Disable Status Register Bit 4) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.
(f) SBS:ChargingCurrent(0x14) is set to 0.
(g) Cell balancing is discontinued.
(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.


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## 3.7 Open Temperature Sensor

Evaluation Interval. This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) Open Temperature Sensor Threshold: Set in units of 0.1°C

(b) Open Temperature Sensor Time: Set in units of 2 seconds. Setting to zero disables the function.

Activation criteria/behavior: When any cell temperature falls below Open Temperature Sensor Threshold, the OTS Alert Flag (Permanent Disable Alert Register Bit 7) for this condition is set. If the condition clears before the Open Temperature Sensor Time elapses, the alert flag is cleared. If the condition remains for longer than Open Temperature Sensor Time, the temperature sensor providing that temperature reading is considered to have failed open. The OTS Status Flag (Permanent Disable Status Register Bit 7) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.

(b) The fault is logged into nonvolatile memory

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(e) SBS:ChargingVoltage(0x15) is set to 0.

(f) SBS:ChargingCurrent(0x14) is set to 0.

(g) Cell balancing is discontinued.

(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.8 Discharge Protection MOSFET Verification

This condition is evaluated once every 2 seconds.

The following user-defined parameters govern the behavior of this rule:

(a) Transition to Discharge Current: Set in units of mA

(b) FET Fail Time: Set in units of 2 seconds. Setting to zero disables both Protection MOSFET Verification functions.

Activation criteria/behavior: If discharge is not permitted (discharge MOSFET is open), but a discharge current is detected that is greater in magnitude than Transition to Discharge Current, then the DFETF Alert Flag (Permanent Disable Alert Register Bit 6) for this condition is set. If this condition clears before FET Fail Time elapses, the alert flag is cleared. If this condition remains for longer than FET Fail Time, then the DFETF Status Flag (Permanent Disable Status Register Bit 6) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.

(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(e) SBS:ChargingVoltage(0x15) is set to 0.

(f) SBS:ChargingCurrent(0x14) is set to 0.

(g) Cell balancing is discontinued.

(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.9 Charge Protection MOSFET Verification

Evaluation Interval. This condition is evaluated once every 2 seconds.

The following user-defined parameters govern the behavior of this rule:

(a) Transition to Charge Current: Set in units of mA

(b) FET Fail Time: Set in units of 2 seconds. Setting to zero disables both Protection MOSFET Verification functions. (This value is set with the Discharge Protection MOSFET Verification parameters.)

Activation criteria/behavior: If charge is not permitted (precharge and discharge MOSFETs are open), but



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a charge current is detected that is greater in magnitude than the Transition to Charge Current, then the CFETF Alert Flag (Permanent Disable Alert Register Bit 5) for this condition is set. If this condition clears before FET Fail Time elapses, the alert flag is cleared. If this condition remains for longer than FET Fail Time, then the CFETF Status Flag (Permanent Disable Status Register Bit 5) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory
(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.
(f) SBS:ChargingCurrent(0x14) is set to 0.
(g) Cell balancing is discontinued.
(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.10 Current Measurement Failure

This condition is evaluated once every 2 seconds, although current measurements occur every second.

The following user-defined parameter governs the behavior of this rule:

(a) Current Measurement Fail Time: Set in units of 2 seconds. Setting to zero disables the function.

Activation criteria/behavior: If the current-measurement system has failed to operate properly by producing multiple errors during a data cycle, the CMF Alert Flag (Permanent Disable Alert Register Bit 8) for this condition is set. If this condition clears before Current Measurement Fail Time elapses, the alert flag is cleared. If the condition exists for longer than the period specified by Current Measurement Fail Time, the CMF Status Flag (Permanent Disable Status Register Bit 8) for this condition is set, and the following actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.
(f) SBS:ChargingCurrent(0x14) is set to 0.
(g) Cell balancing is discontinued.
(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.11 Fuse Failure

This condition is evaluated once every 2 seconds in order to detect the failure of a fuse activation (if utilized).

The following user-defined parameters govern the behavior of this rule:

(a) Fuse Fail Limit: Set in units of mA
(b) Fuse Fail Time: Set in units of 2 seconds. Setting to zero disables the function. Disabling this rule does not disable all of the Secondary Protection Features. Other features can cause the SPROT pin to be set with this feature disabled.

Activation criteria/behavior: If one of the other secondary safety rules has caused the Permanent Disable Condition (SPROT set), and either a charge or discharge current exceeding Fuse Fail Limit has been detected, the FBF Alert Flag (Permanent Disable Alert Register Bit 15) for this condition is set. If the condition clears before the Fuse Fail Time elapses, the alert flag is cleared. If the condition remains longer than Fuse Fail Time, then the status flag for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.


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(d) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(e) SBS:ChargingVoltage(0x15) is set to 0.
(f) SBS:ChargingCurrent(0x14) is set to 0.
(g) Cell balancing is discontinued.
(h) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.12 Impedance Growth

This condition is event-driven and not evaluated on a regular interval. The test checks for abnormal impedance increases in each cell, independent of the other cells.

The following user-defined parameters govern the behavior of this rule:

(a) Current Delta: Set in units of mA
(b) IGR Fail Count: Integer units. Setting to zero disables the function.
(c) IGR Limit: Percentage units. This limit specifies the increase in Normalized Dynamic Impedance from its Initial Value as defined in the Auxiliary Chemistry File (.aux). Setting to a value of 200 would allow increases in Impedance up to 2 times the original value.
(d) Normalized Dynamic Impedance (SOC): Set in units of % of capacity.

Activation criteria/behavior: When the relative state-of-charge (RSOC) is greater than Normalized Dynamic Impedance SOC and a current step greater than Current Delta has occurred, the cell impedance growth rate is calculated for each series-cell element. Rate = (Present NDI / Initial NDI). If the calculated cell impedance growth rate is greater than the IGR Limit, then the cell impedance growth-rate counter is incremented. If the calculated cell impedance growth rate is less than the IGR Limit, then the cell's IGR counter is decremented, without going below zero. If the cell impedance growth-rate counter exceeds the IGR Fail Count, then the following actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) The IGR Status Flag (Permanent Disable Status Register Bit 14) for this condition is set.
(d) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(f) SBS:ChargingVoltage(0x15) is set to 0.
(g) SBS:ChargingCurrent(0x14) is set to 0.
(h) Cell balancing is discontinued.
(i) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.13 Impedance Growth Rate Ratio

This condition is event-driven and not evaluated on a regular interval. The test checks for impedance growth of each cell as compared to the average NDI of the pack.

The following user-defined parameters govern the behavior of this rule:

(a) Current Delta: Set in units of mA (This value is set with the impedance-growth parameters.)
(b) IGR Ratio Fail Count: Integer units. Setting to zero disables the function.
(c) IGR Ratio Limit: Percentage units. This limit specifies the increase in the Normalized Dynamic Impedance of each cell from the average NDI of the cell pack. Setting to a value of 200 would allow increases in Impedance up to 2 times above the pack average.
(d) Normalized Dynamic Impedance (SOC): Set in units of % of capacity.

Activation criteria/behavior: When the relative state-of-charge (RSOC) is greater than Normalized Dynamic Impedance SOC and a current step greater than Current Delta has occurred, the cell impedance growth rate ratio is calculated for each series-cell element. Ratio = (NDI of Cell / Average NDI of Pack). If the calculated cell impedance growth rate ratio is greater than IGR Ratio Limit, then the cell impedance growth-rate ratio counter is incremented. If the calculated IGR Ratio is less than the IGR Ratio Limit, then the IGR Ratio counter is decremented, without going below zero. If the cell impedance growth rate ratio counter exceeds the IGR Ratio Fail Count, then the following actions are taken:

(a) All MOSFETs are opened.


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(b) The fault is logged into nonvolatile memory.
(c) The IGRR Status Flag (Permanent Disable Status Register Bit 13) for this condition is set.
(d) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(f) SBS:ChargingVoltage(0x15) is set to 0.
(g) SBS:ChargingCurrent(0x14) is set to 0.
(h) Cell balancing is discontinued.
(i) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.

## 3.14 Cell-Temperature Rate-of-Rise

This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) Rate Limit Threshold: Set in units of 0.1°C per minute (0.1°C/min.)
(b) Rate Limit Activation Count: Integer units. Setting to zero disables the function.

Activation criteria/behavior: When the calculated cell temperature rate of rise for any cell exceeds the Rate Limit Threshold, then the cell rate-limit counter is incremented, and the condition is logged into nonvolatile memory. If the cell rate limit counter exceeds the Rate Limit Activation Count, then the following actions are taken:

(a) All MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) The ROR Status Flag (Permanent Disable Status Register Bit 12) for this condition is set.
(d) SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set.
(e) SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.
(f) SBS:ChargingVoltage(0x15) is set to 0.
(g) SBS:ChargingCurrent(0x14) is set to 0.
(h) Cell balancing is discontinued.
(i) The SPROT pin is set and the System Fail Flag (Safety Flags Register Bit 15) is set.


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# Charge and Discharge Control and Chemistry

The bq78PL116 allows programmable thresholds for various aspects of both charge and discharge. For example, during charge, the bq78PL116 can report the appropriate charging current needed for the constant charging current and the charging voltage needed for constant-voltage charging per charging algorithm to a smart charger using the *ChargingCurrent* and the *ChargingVoltage* functions. (Actual charging parameters are listed as follows.) Similarly, discharge can be limited due to temperature or various alarm settings, also detailed as follows. All of the parameters that govern the Charge and Discharge Control features are in the "Charge Control" tab of the bqWizard.

Some of the Charge and Discharge Control features, like Charge Completion and Discharge Completion, influence the performance of the gas gauge.

## 4.1 Precharge Voltage Timeout

This condition is evaluated once every 2 seconds, although voltages measurements occur every second.

The following user-defined parameters govern the behavior of this rule:

(a) Precharge Voltage Timeout: Set in units of 2 seconds. (Range is 65,535 seconds maximum.) Setting to zero disables the function.

(b) Precharge Voltage: Set in units of mV

Activation criteria/behavior: During precharge, if any cell voltage fails to reach the limits required to exit the precharge state (i.e., any cell voltage remains below Precharge Voltage) for a period of time equal to precharge voltage timeout, then the PTO Status Flag (Charge Status Register Bit 13) for this condition is set, and the following permanent actions are taken:

(a) Charge and precharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:ChargingVoltage(0x15) is set to 0.

(d) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria: If current greater than Transition to Discharge Current is detected:

(a) Charge and precharge MOSFETs are closed.

(b) SBS:ChargingVoltage(0x15) is set to allow charge.

(c) SBS:ChargingCurrent(0x14) is set to allow charge.

(d) The safety-status flag for this condition is cleared.

## 4.2 Charge Timeout

This condition is evaluated once every 2 seconds.

The following user-defined parameters govern the behavior of this rule:

(a) Charge Duration Timeout: Set in units of 2 seconds. (Range is 65,535 seconds maximum.) Setting to zero disables the function.

NOTE: Other end-of-charge termination values are set with Charge Completion parameters.

Activation criteria/behavior: During charge, if charging continues without a charge completion occurring before Charge Duration Timeout elapses, then the CT Status Flag (Charge Status Register Bit 12) for this condition is set, and the following permanent actions are taken:

(a) All MOSFETs are opened.



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(b) The fault is logged into nonvolatile memory.
(c) SBS:ChargingVoltage(0x15) is set to 0.
(d) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria: If current greater than Transition to Discharge Current is detected:

- Charge and precharge MOSFETs are closed.
- SBS:ChargingVoltage(0x15) is set to allow charge.
- SBS:ChargingCurrent(0x14) is set to allow charge.
- The safety-status flag for this condition is cleared.

## 4.3 Charge-Inhibit Temperature

Evaluation Interval. This condition is evaluated once every 2 seconds after all temperature measurements occur AND only if the Charge Suspend-Temperature rule is not active.

The following user-defined parameters govern the behavior of this rule:

(a) Charge Inhibit Temperature Low: Set in units of 0.1°C
(b) Charge Inhibit Temperature High: Set in units of 0.1°C
(c) Charge Inhibit Recovery Temperature Low: Set in units of 0.1°C
(d) Charge Inhibit Recovery Temperature High: Set in units of 0.1°C

Activation criteria/behavior: If the pack is discharging or in idle and any of the cell temperatures falls below Charge Inhibit Temperature Low or rises above Charge Inhibit Temperature High, then either the CILT of CIHT flag (Charge Status Register Bits 8 and 9 respectively) for this condition is set, and the following actions are taken:

(a) Charge and precharge MOSFETs are opened.
(b) The fault is logged into nonvolatile memory.
(c) SBS:ChargingVoltage(0x15) is set to 0.
(d) SBS:ChargingCurrent(0x14) is set to 0

Deactivation criteria/behavior: When all of the cell temperatures are between Charge Inhibit Recovery Temperature Low and Charge Inhibit Recovery Temperature High, the following actions are taken:

(a) Charge and precharge MOSFETs are closed.
(b) The status flag for this condition is cleared.
(c) SBS:ChargingVoltage(0x15) is set to allow charge.
(d) SBS:ChargingCurrent(0x14) is set to allow charge.

## 4.4 Precharge Voltage and Current

Evaluation Interval. This condition is evaluated once every 2 seconds, although voltage measurements occur every second.

The following user-defined parameters govern the behavior of this rule:

(a) Precharge Voltage: Set in units of mV
(b) Precharge Current: Set in units of mA
(c) Precharge Recovery: Set in units of mV

Activation criteria/behavior: If any cell voltage falls below Precharge Voltage, the PV Status Flag (Charge Status Register Bit 10) for this condition is set, and the following actions are taken:

(a) The charge MOSFET is opened. (Precharge MOSFET remains closed.)
(b) The fault is logged into nonvolatile memory.
(c) SBS:ChargingCurrent(0x14) is set to the defined Precharge Current value.

Deactivation criteria/behavior: When all cell voltages are above Precharge Recovery, then the following actions are taken:

(a) Charge MOSFET is closed.
(b) The status flag for this condition is cleared.


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(c) SBS:ChargingCurrent(0x14) is set to allow charge.

## 4.5 Precharge Temperature

Evaluation Interval. This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) Precharge Temperature: Set in units of 0.1°C

(b) Precharge Current: Set in units of mA. (This value is set with the Precharge Voltage parameters.)

Activation criteria/behavior: If any one of the cell temperatures falls below Precharge Temperature, the PT Status Flag (Charge Status Register Bit 11) for this condition is set, and the following actions are taken:

(a) The charge MOSFET is opened. (Precharge MOSFET remains closed.)

(b) The fault is logged into nonvolatile memory.

(c) SBS:ChargingCurrent(0x14) is set to the defined Precharge Current value.

Deactivation criteria/behavior: When all of the cell temperatures are above Precharge Temperature, then the following actions are taken:

(a) Charge MOSFET is closed.

(b) The status flag for this condition is cleared.

(c) SBS:ChargingCurrent(0x14) is set to allow charge.

## 4.6 Charge Suspend –Temperature

Evaluation Interval. This condition is evaluated once every 2 seconds after all temperature measurements occur.

The following user-defined parameters govern the behavior of this rule:

(a) Charge Suspend Temperature Low: Set in units of 0.1°C

(b) Charge Suspend Temperature High: Set in units of 0.1°C

(c) Charge Suspend Recovery Temperature High: Set in units of 0.1°C

(d) Charge Suspend Recovery Temperature Low: Set in units of 0.1°C

Activation criteria/behavior: If the pack is charging and any one of the cell temperatures falls below Charge Suspend Temperature Low OR rises above Charge Suspend Temperature High, then either the CSLT or CSHT Flag (Charge Status Register Bits 6 and 7 respectively) for this condition is set, and the following actions are taken:

(a) Charge and precharge MOSFETs are opened.

(b) The fault is logged into nonvolatile memory.

(c) SBS:ChargingCurrent(0x14) is set to 0.

Deactivation criteria/behavior: When all of the cell temperatures are above Charge Suspend Recovery Temperature Low AND below Charge Suspend Recovery Temperature High, then the following actions are taken:

(a) Charge and precharge MOSFETs are closed.

(b) The status flag for this condition is cleared.

(c) SBS:ChargingCurrent(0x14) is set to allow charge. Note: Although charge likely ceases when the activation of this rule occurs (due to the charge MOSFET being opened), the rule is still considered active until the deactivation criteria are met.



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## 4.7 Charge Completion

Evaluation Interval. This condition is evaluated once every second after all voltage and current measurements occur. Pack voltage is constructed as a summation of the individual cell-voltage measurements.

The following user-defined parameters govern the behavior of this rule:

(a) Charge Completion Pack Voltage Qualifier: Set in units of mV

(b) Charge Completion Taper Current: Set in units of mA

(c) Charge Completion Time: Set in units of seconds. Setting to zero disables the function.

(d) Charge Completion FET Activation Time: Set in units of seconds. Setting to zero disables the MOSFET activation function, that is, the charge MOSFET is not opened at completion of charge.

(e) Transition to Idle Current: Set in units of mA.

(f) TCA Set SOC Threshold: Set in units of percent (%). (This value is set with the Terminate Charge Alarm (TCA) control parameters.)

(g) FC Set SOC Threshold: Set in units of percent (%). (This value is set with the Fully Charged (FC) bit-control parameters.)

Activation criteria/behavior: If the pack voltage is at or above Charge Completion Pack Voltage Qualifier, and the charge current is below Charge Completion Taper Current but above Charge Completion Taper Current value divided by 2 for a time duration of Charge Completion Time, then the CC Status Flag (Charge Status Register Bit 14) for this condition is set, and the following actions are taken:

(a) If FC Set SOC Threshold is –1, then SBS:BatteryStatus(0x16):[FC] FullyCharged status flag is set.

(b) If TCA Set SOC Threshold is –1, then SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set.

(c) SBS:ChargingVoltage(0x15) is set to 0 after the FETs are opened.

(d) SBS:ChargingCurrent(0x14) is set to 0 after the FETs are opened.

(e) SBS:FullChargeCapacity(0x10) may be updated.

(f) Additional internal capacity updates may be calculated.

(g) SBS:RelativeSOC(0x0d) is set to 100%.

(h) SBS:MaxError(0x0c) may be reset or reduced.

(i) SBS:RemainingCapacity(0x0f) is updated.

(j) SBS:AverageTimeToFull(0x13) is set to 0.

(k) SBS:AbsoluteSOCl(0x0e) is updated.

(l) Timer for Charge Completion FET Activation Time (if non-zero) is started.

If the charge current does not drop below the Transition to Idle Current value before Charge Completion FET Activation Time elapses, then the following action is taken:

(a) Charge and precharge MOSFETs are opened.

Deactivation criteria/behavior: If a discharge current is observed, OR if the charge current drops below the Transition to Idle Current value before the Charge Completion FET Activation Time elapses, then the following actions are taken:

(a) Status condition for this event is cleared.

(b) Charge Completion FET Activation timer is reset.

(c) Charge and precharge MOSFETs are closed.



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## 4.8 Terminate Charge Alarm (TCA) Control

Evaluation Interval. This condition is evaluated once every 2 seconds after all voltage and current measurements occur. Pack voltage is constructed as a summation of the individual cell-voltage measurements.

This condition depends on the following parameters and values calculated elsewhere.

(a) TCA Set SOC Threshold: Set in units of percent (%). Setting to –1 disables this portion of the function, so that the Terminate Charge Alarm bit is set by conditions in the Charge Completion function.

(b) TCA Clear SOC Threshold: Set in units of percent (%). Note: This is the only method that can clear the Terminate Charge Alarm bit.

(c) SBS:RelativeSOC(0x0d)

Activation criteria/behavior: If the TCA Set SOC Threshold is not –1, AND the SBS:RelativeSOC(0x0d) value is greater than or equal to the TCA Set SOC Threshold, then the following action is taken:

(a) The SBS:BatteryStatus(0x16):[TCA] Terminate Charge Alarm bit is set to 1.

If the TCA Clear SOC Threshold is not –1, AND SBS:RelativeSOC(0x0d) value is less than or equal to the TCA Clear SOC Threshold, then the following action is taken:

(a) The Terminate Charge Alarm (TCA) bit in SBS:BatteryStatus(0x16) is cleared to 0.

## 4.9 Fully Charged (FC) Bit Control

Evaluation Interval. This condition is evaluated when once every 2 seconds. Pack voltage is constructed as a summation of the individual cell-voltage measurements.

The following user-defined parameters govern the behavior of this rule:

(a) FC Set SOC Threshold: Set in units of one percent (%). Setting to –1 disables this portion of the function so that so that the Fully Charged bit is set by conditions in the Charge Completion function.

(b) FC Clear SOC Threshold: Set in units of one percent (%). Note: This is the only method that can clear the Fully Charged bit.

Activation criteria/behavior: If the FC Set SOC Threshold is not –1, AND the SBS:RelativeSOC(0x0d) value is greater than or equal to the FC Set SOC Threshold, then the following action is taken:

(a) The SBS:BatteryStatus(0x16):[FC] Fully Charged bit is set to 1.

If SBS:RelativeSOC(0x0d) is equal to or less than FC Clear SOC Threshold, then the following action is taken:

(a) The SBS:BatteryStatus(0x16):[FC] Fully Charged bit is cleared to 0.

## 4.10 Discharge Completion

Evaluation Interval. This condition is evaluated once every second after all voltage and current measurements occur. Pack voltage is constructed as a summation of the individual cell-voltage measurements.

The following user-defined parameters govern the behavior of this rule:

(a) Discharge Completion Pack Voltage Qualifier: Set in units of mV

(b) Discharge Completion Time: Set in units of seconds. Setting to zero disables whole function.

(c) Discharge Completion FET Activation Time: Set in units of seconds. Setting to zero disables the MOSFET activation function, that is, the discharge MOSFET is not opened at completion of discharge.

(d) Transition to Idle Current: Set in units of mA

(e) FD Set SOC Threshold: Set in units of percent (%). (This value is set with the Fully Discharged (FD) Bit Control parameters.)

(f) TDA Set SOC Threshold: Set in units of percent (%). (This value is set with the Terminate Discharge Alarm (TDA) Control parameters.)


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Activation criteria/behavior: If the pack voltage is at or below the Discharge Completion Pack Voltage Qualifier for a time duration of Discharge Completion Time, then the DC Status Flag (Charge Status Register Bit 15) for this condition is set, and the following actions are taken:

(a) SBS:FullChargeCapacity(0x10) may be updated.

(b) Additional internal capacity updates may be calculated.

(c) SBS:RelativeSOC(0x0d) is set to 0%.

(d) SBS:MaxError(0x0c) may be reset or reduced.

(e) SBS:RemainingCapacity(0x0f) is updated.

(f) SBS:AverageTimeToEmpty(0x13) is set to 0.

(g) SBS:AbsoluteSOC(0x0e) is updated.

(h) Timer for Discharge Completion FET Activation Time (if non-zero) is started.

If the discharge current is not reduced below the value of Transition to Idle Current for a time duration of longer than Discharge Completion FET Activation Time after the end of Discharge Completion Time, then the following action is taken:

(a) Discharge MOSFET is opened.

Deactivation criteria/behavior: If a charge current is observed, OR if the discharge current drops below the Transition to Idle Current value before the Discharge Completion FET Activation Time elapses, then the following actions are taken:

(a) Status condition for this event is cleared.

(b) Discharge Completion FET Activation timer is reset.

## 4.11 Terminate Discharge Alarm (TDA) Control

Evaluation Interval. This condition is evaluated once every 2 seconds after all voltage and current measurements occur. Pack voltage is constructed as a summation of the individual cell-voltage measurements.

This condition depends on the following parameters and values calculated elsewhere.

(a) TDA Set SOC Threshold: Set in units of percent (%). Setting to –1 disables this portion of the function.

(b) TDA Clear SOC Threshold: Set in units of percent (%). Setting to –1 disables this portion of the function.

(c) TDA Clear Voltage: Set in units of mV.

(d) TDA Set Voltage Threshold: Set in units of mV of pack voltage

(e) TDA Set Voltage Time: Set in units of 2 seconds. Setting this to zero disables the voltage-based set/clear of the TDA.

(f) SBS:RelativeSOC(0x0d)

(g) Calculated pack voltage

Activation criteria/behavior: If the TDA Set SOC Threshold is not –1, AND the SBS:RelativeSOC(0x0d) value is less than or equal to the TDA Set SOC Threshold, then the following action is taken:

(a) The SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is set to 1.

If the TDA Clear SOC Threshold is not –1, AND the SBS:RelativeSOC(0x0d) value is greater than or equal to TDA Clear SOC Threshold, then the following actions are taken:

(a) The SBS:BatteryStatus(0x16):[TDA] Terminate Discharge Alarm bit is cleared to 0.

If the TDA SET VOLTAGE TIME is non-zero and the pack voltage is below TDA set voltage for TDA SET VOLTAGE TIME, the TDA flag is set.

If the TDA SET VOLTAGE TIME is non-zero and the pack voltage is above TDA CLEAR VOLTAGE, the TDA flag is cleared.



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## 4.12 Fully Discharged (FD) Bit Control

Evaluation Interval. This condition is evaluated once every 2 seconds. Pack voltage is constructed as a summation of the individual cell voltage measurements.

The following user-defined parameters govern the behavior of this rule:

(a) FD Set SOC Threshold: Set in units of one percent (%). Setting to –1 disables this portion of the function.

(b) FD Clear SOC Threshold: Set in units of one percent (%). Setting to –1 disables this portion of the function.

(c) FD Clear Voltage: Set in units of mV.

(d) FD Set Voltage: Set in units of mV of pack voltage

(e) FD Set Voltage Time: Set in units of seconds. Setting this to zero disables the voltage-based set/clear of FD.

Activation criteria/behavior: If the FD Set SOC Threshold is not –1, AND the SBS:RelativeSOC(0x0d) value is less than or equal to the FD Set SOC Threshold, then the following action is taken:

(a) The SBS:BatteryStatus(0x16):[FD] Fully Discharged bit is set to 1.

If the FD Clear SOC Threshold is not –1, AND the SBS:RelativeSOC(0x0d) value is greater than or equal to the FD Clear SOC Threshold, then the following action is taken:

(a) The SBS:BatteryStatus(0x16):[FD] Fully Discharged bit is cleared to 0.

If FD SET VOLTAGE TIME is non-zero, and the pack voltage is below the TDA set voltage for FD SET VOLTAGE TIME, the FD flag is set.

If FD SET VOLTAGE TIME is non-zero and the pack voltage is above FD CLEAR VOLTAGE, the FD flag is cleared.

## 4.13 Overcharge Alarm (OCA) Control

This condition is evaluated once every 2 seconds after all voltage and current measurements occur.

This condition depends on the following parameters and values calculated elsewhere.

(a) Charge Completion Pack Voltage Qualifier: Set in units of mV. (This value is set with the Charge Completion parameters.)

(b) OCA Set Voltage: Set in units of mV

(c) OCA Activation Time: Set in units of 2 seconds

Activation criteria/behavior: If the calculated pack voltage (summation of individual cell voltages) is above the OCA Set Voltage, then the safety-alert flag for this condition is set. If the condition remains longer than OCA Activation Time, then the status flag for this condition is set, and the following action is taken:

(a) The SBS:BatteryStatus(0x16):[OCA] Over Charge Alarm bit is set to 1.

If the calculated pack voltage falls below the Charge Completion Pack Voltage Qualifier, then the following action is taken:

(a) The SBS:BatteryStatus(0x16):[OCA] Over Charge Alarm bit is cleared to 0.

## 4.14 Miscellaneous Control Parameters

The following parameters are used by various charge and discharge functions previously mentioned, but also include uses in various other algorithms.

(a) Transition to Idle Current: Set in units of mA. Used to indicate that the pack has reached an idle level of usage, and is neither being charged or discharged, even if this is a non-zero value.

(b) Transition to Idle Time: Set in units of seconds. Used to gate the transition to Idle to prevent false entry due to short durations of low discharge current.

(c) Transition to Discharge Current: Set in units of mA. Used to indicate that a discharge current has started. (This value is also used by the Discharge Protection MOSFET Verification function.)

(d) Transition to Charge Current: Set in units of mA. Used to indicate that a charge current has started. (This value is also used by the Charge Protection MOSFET Verification function.)


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## 4.15 Remaining Capacity Alarm Status

This condition is evaluated once every 2 seconds after all voltage and current measurements occur.

This condition depends on the following values:

(a) SBS:RemainingCapacity(0x0f) value

(b) SBS:RemainingCapacityAlarm(0x01): Set in units of mAhr or 10 mWhr. Setting to zero disables this alarm function.

Activation criteria/behavior: If value of SBS:RemainingCapacity(0x0f) is equal or less than the value of SBS:RemainingCapacityAlarm(0x01), then the following action is taken:

(a) The Remaining Capacity Alarm bit in SBS:BatteryStatus(0x16):[RCA] is set to 1.

If this condition is not met, and a charge above Transition to Idle Current is detected, then the following actions are taken:

1. The Remaining Capacity Alarm bit in SBS:BatteryStatus(0x16):[RCA] is cleared to 0.

## 4.16 Remaining Time Alarm Status

This condition is evaluated once every 2 seconds after all voltage and current measurements occur.

This condition depends on the following values:

(a) SBS:AverageTimeToEmpty(0x12)

(b) SBS:RemainingTimeAlarm(0x02): Set in units of minutes. Setting to zero disables this alarm function.

Activation criteria/behavior: If value of SBS:AverageTimeToEmpty(0x12) is equal or less than the value of SBS:RemainingTimeAlarm(0x02), then the following action is taken:

(a) The Remaining Time Alarm bit in SBS:BatteryStatus(0x16):[RTA] is set to 1.

If this condition is not met, then the following action are taken:

1. The Remaining Time Alarm bit in SBS:BatteryStatus(0x16):[RTA] is cleared to 0.

## 4.17 Cell Chemistry Configuration

The bq78PL116 has several cell chemistry parameters. These are accessible from the bqWizard™ Cell Chemistry tab. This section describes these parameters.

### *4.17.1 Chemistry ID*

This is the ID of the standard TI chemistry file loaded into the bq78PL116. After a new chemistry file has been uploaded, this parameter changes to indicate the new chemistry file number.

Parameter type: Read-only

Units: Number

Update procedure: The chemistry data and reported version are updated using the bqWizard™ command: Menu → File → Load Chemistry Data. This value can also be updated by loading a Parameter Set File (.ppcsv). It requires that a .chem file matching the number exists in the the Chemistry directory of the bqWizard installation.

### *4.17.2 Tau10*

This is the time constant used for current taper during end of charge.

Parameter type: Read-only

Units: Number

Update procedure: The parameter is updated during a load of an Auxiliary chemistry file (.aux).



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### 4.17.3 Normalized Dynamic Impedance Low Temperature

The normalized dynamic impedance is the impedance due to a step change in current and voltage (ΔV/ΔI) normalized to fixed reference temperature. This parameter is the temperature below which dynamic impedance normalization is not performed.

Parameter type: Read-only

Units: °C

Update procedure: The parameter is updated during a load of an Auxiliary chemistry file (.aux).

### 4.17.4 Normalized Dynamic Impedance High Temperature

This parameter is the temperature above which dynamic impedance normalization is not performed.

Parameter type: Read-only

Units: °C

Update procedure: The parameter is updated during a load of an Auxiliary chemistry file (.aux).

### 4.17.5 Normalized Dynamic Impedance SOC

This is the SOC level above which dynamic impedance normalization is not performed.

Parameter type: Read-only

Units: Percent

Update procedure: The parameter is updated during a load of an Auxiliary chemistry file (.aux).

### 4.17.6 Normalized Dynamic Impedance Gain

This is the weighting factor for new impedance measurements.

Parameter type: Read-only

Units: Number

Update procedure: The parameter is updated during a load of an Auxiliary chemistry file (.aux).

### 4.17.7 FCC Learn Qualifier

The full-charge capacity is learned by evaluating the passed charge between two periods of time where the pack was at rest long enough to allow using the voltage to look up the RSOC in the OCV table. In order to do this learning, the change in RSOC between these idle periods must be greater than the FCC Learn Qualifier.

Parameter type: Read/write

Units: Percent

Update procedure: The parameter can be updated from the bqWizard™ software and exported to the ppcsv parameter file. It is recommended to use the TI-provided default value.

### 4.17.8 Cycle Fade

Generally, the capacity fade is tracked by the FCC learning. In a situation where this is not possible, an estimate is made using the Cycle Fade parameter. For any cycle (defined as an accumulated discharge equal to the design capacity) which did not involve an update in FCC, the capacity is derated by the Cycle Fade parameter.

Parameter type: Read/write

Units: Percent

Update procedure: The parameter can be updated from the bqWizard™ software and exported to the ppcsv parameter file. It is recommended to use the TI-provided default value.


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### 4.17.9 Min OCV Slope

Estimation of RSOC from the open-circuit voltage during idle periods is held off if the slope of the mV-to-RSOC table is less than this parameter.

Parameter type: Read/write

Units: 2 mV per % of RSOC

Update procedure: The parameter can be updated from bqWizard™ software and exported to the ppcsv parameter file. It is recommended to use the TI-provided default value.

### 4.17.10 OCV Idle Qualifier

OCV Idle Qualifier is the time qualifier that must be satisfied before the cell voltages can be considered to represent a true OCV value.

Parameter type: Read/write

Units: Minutes

Update procedure: The parameter can be updated from the bqWizard™ software and exported to the ppcsv parameter file. It is recommended to use the TI-provided default value.

### 4.17.11 Stale FCC Timeout

If the time since the previous rest period (and associated RSOC estimation) is greater than the Stale FCC timeout, the earlier RSOC estimate is discarded and the gas gauge algorithm does not use it for FCC update.

Parameter type: Read/write

Units: Minutes

Update procedure: The parameter can be updated from bqWizard™ software and exported to the ppcsv parameter file. It is recommended to use the TI-provided default value.

### 4.17.12 Default Charging Voltage

This is the voltage to be reported by the gauge over the SBdata bus during normal charging conditions.

Parameter type: Read/write

Units: Volts
NOTE: Per the Smart Battery Specification, the units are not affected by the setting of the VScale bits in SpecificationInfo().

Update procedure: The parameter can be updated from the bqWizard™ software and exported to the ppcsv parameter file. It must be set to correspond to the battery pack design requirements.

### 4.17.13 Default Charging Current

This is the charging current to be reported by the gauge over the SBdata bus during normal charging conditions.

Parameter type: Read/write

Units: mA
NOTE: Per the Smart Battery Specification, the units are not affected by the setting of the IPScale bits in SpecificationInfo().

Update procedure: The parameter can be updated from the bqWizard™ software and exported to the ppcsv parameter file. It must be set to correspond to the battery pack design requirements.

### 4.17.14 Capacity Algorithm

This parameter defines the load to use in pack capacity calculations.

0 → C/5



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1 → Present current
2 → User-defined current
3 → Average current (default)

Parameter type: Read/write

Units: Hexadecimal number

Update procedure: The parameter can be updated from the bqWizard™ software and exported to the ppcsv parameter file. It must be set to correspond to the battery pack design requirements.

### 4.17.15 User Rate

This is the discharge rate to be used when Capacity_Algorithm = 2.

Parameter type: Read/write

Units: mA

Update procedure: The parameter can be updated from the bqWizard™ software and exported to the ppcsv parameter file. It must be set to correspond to the battery pack design requirements.


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# SBData Dynamic, Static and Extended

The bq78PL116 provides Standard and Extended SBData as defined in this section. The Standard SBData is defined in the SBData Specification. The Extended data is specific to the bq78PL116.

## 5.1 SBData Static and Dynamic

The standard SBData commands are located at addresses 0x00 to 0x23. The following section describes any clarifications or exceptions to the bq78PL116's support of these commands. If the command is not listed it is supported as described in the SBData Specification.

Smart Battery Data Specification, version 1.1 http://smartbattery.org/specs/sbdat110.pdf

### *5.1.1 BatteryMode(0x03)*

The default value is 0x6001.

Internal Charge Controller bit is set to 1 because the bq78PL116 are charge controllers in the sense that they perform Precharge control and can also control the ON/OFF of charge under safety conditions.

The Charge Controller Enabled bit is read only and set to 0 (default). The write capability is not supported.

The only bit that is writable by the SMBus host is the Capacity Mode bit. CAPACITY_MODE bit 15 is fully supported. The bq78PL116 reports in either mA and mAHrs (Bit=0) or 10mW and 10mWHrs (Bit=1).

### *5.1.2 AtRate(0x04)*

This command is not supported.

### *5.1.3 AtRateTimeToFull(0x05)*

This command is not supported.

### *5.1.4 AtRateTimeToEmpty(0x06)*

This command is not supported.

### *5.1.5 AtRateOK(0x07)*

This command is not supported.

### *5.1.6 Voltage(0x09)*

When the user elects to set the VScale bits in the SpecificationInfo(0x1A) Command to 0001 it means that the reported Voltage(0x09) is actual pack mV divided by ten. This allows pack voltages greater than 65535mV to be reported. If VScale is set to 0000, then Voltage(0x09) is actual pack mV.

It is the responsibility of the SMBus Host Controller to interpret this value correctly.

### *5.1.7 Current(0x0A)*

When the user elects to set the IPScale bits in the SpecificationInfo(0x1A) Command to 0001 it means that the reported Current(0x0A) is actual mA divided by ten. This allows pack currents greater than ±32768mA to be reported. If IPScale is set to 0000, then Current(0x0A) is actual pack mA.


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It is the responsibility of the SMBus Host Controller to interpret this value correctly.

### 5.1.8 AverageCurrent(0x0B)

When the user elects to set the IPScale bits in the SpecificationInfo(0x1A) Command to 0001 it means that the reported AverageCurrent(0x0B) is actual mA divided by ten. This allows pack currents greater than ±32768mA to be reported. If IPScale is set to 0000, then AverageCurrent(0x0A) is actual pack mA.

It is the responsibility of the SMBus Host Controller to interpret this value correctly.

### 5.1.9 MaxError(0x0C)

At start of the device or after an initialization command, the value is 10. It is set to 1 when capacity learning takes place. The value increases by 1/20 for each cycle that goes by without learning. If it ever gets > 100, the CONDITION_FLAG bit of BatteryMode() is set.

### 5.1.10 RemainingCapacity(0x0F)

The range 0 to 32767 mAHrs or 0 to 32767 10mWHrs is supported.

When the user elects to set the IPScale bits in the SpecificationInfo(0x1A) Command to 0001 it means that the reported RemainingCapacity(0x0F) is the actual value divided by ten for mAHrs.

If the user elects to set the VScale bit in SpecificationInfo(0x1A) to 0001 and report RemainingCapacity(0x0F) in 10mWHrs, then the reported RemainingCapacity(0x0F) is the actual divided by 10, or 100mWHrs. VScale has no influence on RemainingCapacity(0x0F) when reporting in mAHr mode.

If both IPScale and VScale are set to 0001 and reporting is in 10mWHrs, then the reported value will actually be in 1000mWHrs.

It is the responsibility of the SMBus Host Controller to interpret this value correctly.

### 5.1.11 FullChargeCapacity(0x10)

The range 0 to 32767 mAHrs or 0 to 32767 10mWHrs is supported.

When the user elects to set the IPScale bits in the SpecificationInfo(0x1A) Command to 0001 it means that the reported FullChargeCapacity(0x10) is the actual value divided by ten for mAHrs.

If the user elects to set the VScale bit in SpecificationInfo(0x1A) to 1 and report FullChargeCapacity(0x10) in 10mWHrs, then the reported FullChargeCapacity(0x10) is the actual divided by 10, or 100mWHrs. VScale has no influence on reporting FullChargeCapacity(0x10) in mAHr mode.

If both IPScale and VScale are set to 0001 and reporting is in 10mWHrs, then the reported value will actually be in 1000mWHrs.

It is the responsibility of the SMBus Host Controller to interpret this value correctly.

### 5.1.12 SpecificationInfo(0x1A)

Bits 0 to 3 (Revision) are set to 0001 by the bq78PL116.

Bits 4 to 7 (Version) are set to 0011 by the bq78PL116.

Bits 8 to 11 (VScale) are set to 0000 by default by the bq78PL116. These bits can be set to 0001 through a Pack Configuration File (.tmap) generated by the bqWizard. No other values are supported. Doing so causes the reported pack voltage as well as values that depend on Pack Voltage (mWHrs)to be divided by 10. Further, any Parameter Set value that depend on Pack voltage must be first divided by 10 before entering into the register.

Bits 12 to 15 (IPScale) are set to 0000 by default by the bq78PL116. These bits can be set to 0001 through a Pack Configuration File (.tmap) generated by the bqWizard. No other values are supported. Doing so causes the reported pack current as well as values that depend on Pack Current (mAHrs, mWHrs) to be divided by 10.



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Further, any Parameter Set value that depends on Pack Current must be first divided by 10 before entering into the register. This table summarizes the parameters effected by IPScale and/or VScale.

| Parameter Description | Default Value | Default VScale = 0000 IPscale = 0000 UNITS | User Defined VScale = 0001 IPscale = 0000 UNITS | User Defined VScale = 0000 IPscale = 0001 UNITS | User Defined VScale = 0001 IPscale = 0001 UNITS |
|---|---|---|---|---|---|
| Pre-Charge Current | 240 | mA | mA | mA/10 | mA/10 |
| Charge Completion Taper Current Qualifier | 120 | mA | mA | mA/10 | mA/10 |
| Transition to Idle Current | 50 | mA | mA | mA/10 | mA/10 |
| Transition to Discharge Current | –75 | mA | mA | mA/10 | mA/10 |
| Transition to Charge Current | 75 | mA | mA | mA/10 | mA/10 |
| User Rate | 480 | mA | mA | mA/10 | mA/10 |
| Current Delta | 100 | mA | mA | mA/10 | mA/10 |
| OC Charge Tier 1 Threshold | 4800 | mA | mA | mA/10 | mA/10 |
| OC Discharge Tier 1 Threshold | –7200 | mA | mA | mA/10 | mA/10 |
| OC Charge Tier 2 Threshold | 5200 | mA | mA | mA/10 | mA/10 |
| OC Discharge Tier 2 Threshold | –9600 | mA | mA | mA/10 | mA/10 |
| Cell Imbalance Current | 50 | mA | mA | mA/10 | mA/10 |
| SOC Charge Threshold | 6000 | mA | mA | mA/10 | mA/10 |
| SOC Discharge Threshold | –12000 | mA | mA | mA/10 | mA/10 |
| Fuse Fail Limit | 50 | mA | mA | mA/10 | mA/10 |
| Remaining Capacity Alarm (CAPACITY_MODE=0) | 480 | mAh | mAh | mAh/10 | mAh/10 |
| Remaining Capacity Alarm (CAPACITY_MODE=1) | 480 | 10mWHrs | 100mWHrs | 10mWHrs | 1000mWHrs |
| Design Capacity (CAPACITY_MODE=0) | 2400 | mAh | mAh | mAh/10 | mAh/10 |
| Design Capacity (CAPACITY_MODE=1) | 2592 | 10mWh | 100mWHrs | 10mWh | 1000mWHrs |
| Design Voltage | 10800 | mV | mV/10 | mV | mV/10 |
| Charge Completion Pack Voltage Qualifier | 12300 | mV | mV/10 | mV | mV/10 |
| Discharge Completion Pack Voltage Qualifier | 9300 | mV | mV/10 | mV | mV/10 |
| FD Set Voltage | 9300 | mV | mV/10 | mV | mV/10 |
| FD Clear Voltage | 9600 | mV | mV/10 | mV | mV/10 |
| TDA Set Voltage Threshold | 9600 | mV | mV/10 | mV | mV/10 |
| TDA Clear Voltage | 11100 | mV | mV/10 | mV | mV/10 |
| OCA Set Voltage | 12900 | mV | mV/10 | mV | mV/10 |
| POV Threshold | 12750 | mV | mV/10 | mV | mV/10 |
| POV Recovery | 12300 | mV | mV/10 | mV | mV/10 |
| PUV Threshold | 8400 | mV | mV/10 | mV | mV/10 |
| PUV Recovery | 9300 | mV | mV/10 | mV | mV/10 |

Note that the First Level Hardware Current safety rule settings are not effected by the IPScale value.

### 5.1.13 ManufacturerName(0x20)

The 32 bytes maximum includes the null termination character.

### 5.1.14 DeviceName(0x21)

The 32 bytes maximum includes the null termination character.

### 5.1.15 DeviceChemistry(0x22)

The 32 bytes maximum includes the null termination character.

### 5.1.16 Summary

A summary of the Standard SBData Commands is shown in the following table:


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| Slave Functions | Code | Access | Size In Bytes | Min Value | Max Value | Units |
|---|---|---|---|---|---|---|
| ManufacturerAccess | 0x00 | r/w | 2 | 0x0000 | 0xFFFF | word |
| RemainingCapacityAlarm | 0x01 | r/w | 2 | 0 | 65535 | mAh or 10mWh |
| RemainingTimeAlarm | 0x02 | r/w | 2 | 0 | 65535 | minutes |
| BatteryMode | 0x03 | r/w | 2 | 0x0000 | 0xE383 | bit flags |
| Temperature | 0x08 | r | 2 | 0 | 65535 | 0.1°K |
| Voltage | 0x09 | r | 2 | 0 | 65535 | mV |
| Current | 0x0a | r | 2 | –32768 | 65535 | mA |
| AverageCurrent | 0x0b | r | 2 | –32768 | 32767 | mA |
| MaxError | 0x0c | r | 1 | 0 | 100 | percent |
| RelativeStateOfCharge | 0x0d | r | 1 | 0 | 100 | percent |
| AbsoluteStateOfCharge | 0x0e | r | 1 | 0 | 100+ | percent |
| RemainingCapacity | 0x0f | r | 2 | 0 | 32767 | mAh or 10mWh |
| FullChargeCapacity | 0x10 | r | 2 | 0 | 32767 | mAh or 10mWh |
| RunTimeToEmpty* | 0x11 | r | 2 | 0 | 65534 | minutes |
| AverageTimeToEmpty | 0x12 | r | 2 | 0 | 65534 | minutes |
| AverageTimeToFull | 0x13 | r | 2 | 0 | 65534 | minutes |
| ChargingCurrent | 0x14 | r | 2 | 0 | 65534 | mA |
| ChargingVoltage | 0x15 | r | 2 | 0 | 65534 | mV |
| BatteryStatus | 0x16 | r | 2 | 0x0000 | 0xDBFF | bit flags |
| CycleCount | 0x17 | r | 2 | 0 | 65535 | count |
| DesignCapacity | 0x18 | r | 2 | 0 | 65535 | mAh or 10mWh |
| DesignVoltage | 0x19 | r | 2 | 0 | 65535 | mV |
| SpecificationInfo | 0x1a | r | 2 | 0x0031 | 0x1131 | unsigned int |
| ManufactureDate | 0x1b | r | 2 | – | – | unsigned int |
| SerialNumber | 0x1c | r | 2 | 0x0000 | 0xFFFF | number |
| ManufacturerName | 0x20 | r | 32 | – | | string |
| DeviceName | 0x21 | r | 32 | – | | string |
| DeviceChemistry | 0x22 | r | 32 | – | | string |
| ManufacturerData | 0x23 | r | 14+1 | – | | data |

## 5.2 Extended SBData Commands

The Commands 0x3C to 0x58 can be assigned to a multitude of parameters that are specific to the bq78PL116. These parameters can provide a richer detail of information that goes far beyond the original SBData Commands. For instance, the PowerPump Net Pumping variable can be monitored to create a cell state of health algorithm. The user accesses these parameters using the applicable transactions defined in the SMBus Specification. The Extended SBData Commands are read only.

A utility within the bqWizard software allows the user to select the values that should fill these 29 registers. The bqWizard creates a unique configuration file (*.sbd) that is then loaded to the bq78PL116. The default set of parameters is shown in the following table.

| Slave Functions | Code | Access | Size In Bytes | Units |
|---|---|---|---|---|
| Cell voltage 1 | 0x3c | r | 2 | mV |
| Cell voltage 2 | 0x3d | r | 2 | mV |
| Cell voltage 3 | 0x3e | r | 2 | mV |
| Cell voltage 4 | 0x3f | r | 2 | mV |
| Cell voltage 5 | 0x40 | r | 2 | mV |
| Cell voltage 6 | 0x41 | r | 2 | mV |
| Cell voltage 7 | 0x42 | r | 2 | mV |
| Cell voltage 8 | 0x43 | r | 2 | mV |
| Cell voltage 9 | 0x44 | r | 2 | mV |
| Cell voltage 10 | 0x45 | r | 2 | mV |
| Cell voltage 11 | 0x46 | r | 2 | mV |
| Cell voltage 12 | 0x47 | r | 2 | mV |


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| Slave Functions | Code | Access | Size In Bytes | Units |
|---|---|---|---|---|
| Cell voltage 13 | 0x48 | r | 2 | mV |
| Cell voltage 14 | 0x49 | r | 2 | mV |
| Cell voltage 15 | 0x4a | r | 2 | mV |
| Cell voltage 16 | 0x4b | r | 2 | mV |
| Internal Temperature | 0x4c | r | 2 | 0.1°K |
| External Temperature 1 | 0x4d | r | 2 | 0.1°K |
| External Temperature 2 | 0x4e | r | 2 | 0.1°K |
| External Temperature 3 | 0x4f | r | 2 | 0.1°K |
| External Temperature 4 | 0x50 | r | 2 | 0.1°K |
| Safety Status | 0x51 | r | 2 | Bit wise |
| Permanent Fail Status | 0x52 | r | 2 | Bit wise |
| Charge Status | 0x53 | r | 2 | Bit wise |
| Lifetime Maximum Pack Voltage | 0x54 | r | 2 | mV |
| Lifetime Maximum Cell Voltage | 0x55 | r | 2 | mV |
| Lifetime Maximum Charge Current | 0x56 | r | 2 | mA |
| Lifetime Maximum Discharge Current | 0x57 | r | 2 | mA |
| Lifetime Maximum Temperature | 0x58 | r | 2 | 0.1°K |


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# Pack Configuration and Dynamic Registers

## 6.1 Configuration Registers

The hardware configuration and algorithm enable registers allow specific controls to be enabled or disabled.

### 6.1.1 Hardware Configuration Register (Read/Write)

**Table 6-1. bq78PL116 Hardware Configuration Register**

| Bit # | Description | Details |
|---|---|---|
| 0 | Disp 0 | 0x00 = Reserved,<br>0x01 = LED (Default)(1),<br>0x10 = LCD,<br>0x11 = EPD |
| 1 | Disp 1 | |
| 2 | Reserved, not used | Cleared to 0 |
| 3 | Reserved, not used | Cleared to 0 |
| 4 | Reserved, internal use | Reserved, set to 0x11 |
| 5 | Reserved, internal use | |
| 6 | EPD Polarity | 0=black segments on white background (default)<br>1=white segments on black background. |
| 7 | Reserved, internal use | Cleared to 0 |
| 8 | EFCI_D_Sense | 0 = Turn off DSG FET when EFCID pin is low.<br>1 = Turn off DSG FET when EFCID pin is high.<br>Default configuration is EFCI_D_Sense = 1 and EFCID pin = low. |
| 9 | EFCI_C_Sense | 0 = Turn off CHG FET when EFCIC pin is low.<br>1 = Turn off CHG FET when EFCIC pin is high.<br>Default configuration is EFCI_C_Sense = 1 and EFCIC pin = low. |
| 10 | Sense 0 | Sense Resistor<br>0x00 = Reserved, 0x01 = 10 mΩ (Default),<br>0x10 = 3 mΩ, 0x11 = 1 mΩ |
| 11 | Sense 1 | |
| 12 | Reserved, not used | – |
| 13 | System present FET control | When = 0, the CFET and PFET are on in standby mode (default).<br>When = 1, the CFET and PFET are turned off when the part is in standby mode. |
| 14 | Reserved, not used | Cleared to 0 |
| 15 | Reserved, not used | Cleared to 0 |

(1) Five LEDs or display segments are supported: Each indicates 20% of SBS:RelativeSOC(0x0d)


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### 6.1.2 Algorithm Enable Register (Read/Write)

**Table 6-2. bq78PL116 Algorithm Enable Register**

| Bit # | Description | Details |
|---|---|---|
| 0 | PumpAlgorithm 0 | See Table 6-3 |
| 1 | PumpAlgorithm 1 | See Table 6-3 |
| 2 | Pump Mode | See Table 6-3 |
| 3 | WIRED | When = 0, disables all safety, pumping, and data writes (default).<br>When = 1, safety, pumping, and data writes are enabled. |
| 4 | Reserved, not used | – |
| 5 | Inhibit Pump During Charge | When = 0, cell balancing is enabled during charge (default).<br>When = 1, inhibit cell balancing during charge. |
| 6 | Inhibit Pump During Discharge | When = 0, cell balancing is enabled during discharge (default),<br>When = 1, inhibit cell balancing during discharge. |
| 7 | Turbo 0 | Enables SuperPump mode when nonzero and no current is flowing and no safety rules are active. Temperature measurements are suspended for n cycles while SuperPump is active where n = 0x0001 through 0x1111. After n suspended cycles a temperature measurement is always taken. Default value is 0x0000, turbo mode = off. |
| 8 | Turbo 1 | |
| 9 | Turbo 2 | |
| 10 | Turbo 3 | |
| 11 | Reserved, not used | Cleared to 0 |
| 12 | Force DFET | Direct control of discharge pack protection MOSFET (See bit 15). When = 1, FET is turned on. |
| 13 | Force CFET | Direct control of charge pack protection MOSFET (See bit 15). When = 1, FET is turned on. |
| 14 | Force PFET | Direct control of precharge pack protection MOSFET (See bit 15). When = 1, FET is turned on. |
| 15 | Inhibit safety rules | When = 0, enables safety rules.<br>When = 1, disables safety rules and allows MOSFETs to be directly controlled using bits 12–14 (default). |

**Table 6-3. Pumping (Balancing) Algorithm Table**

| Pump Mode | PumpAlgorithm(1:0) | Function |
|---|---|---|
| **NORMAL** | | |
| 1 | 00 | Reserved, not used |
| 1 | 01 | State-of-charge pumping algorithm |
| 1 | 10 | Open-circuit-voltage pumping algorithm (default) |
| 1 | 11 | Terminal-voltage pumping algorithm |
| **TESTING** | | |
| 0 | 00 | Reserved |
| 0 | 01 | All Cells Pump North |
| 0 | 10 | All Cells Pump South |

### 6.1.3 bq78PL116 System Control Register (Read/Write)

**Table 6-4. bq78PL116S12 System Control Register**

| Bit # | Description | Details |
|---|---|---|
| [14:0] | Reserved, not used | Cleared to 0 |
| 15 | Pump Disable | When = 0, cell balancing, pumping are enabled.<br>When = 1, disables all cell balancing, pumping (default). |



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## 6.2 Pack Configuration

The parameters that grouped in the Pack Configuration Section and typically configure the firmware to match the pack are defined below.

### 6.2.1 Parallel Count

This is the number of parallel cells in the pack. This parameter can only be set by loading a Pack Configuration File (.tmap).

### 6.2.2 Expected Number of Cells

This is the number of series cells in the pack. This parameter can only be set by loading a Pack Configuration File (.tmap).

### 6.2.3 Actual Number of Cells

This is the number of series cells found by the bq78PL116. This parameter is written by the firmware. A mismatch between this register and the Expected Number of Cells register triggers a rebuild of the PowerLAN network.

### 6.2.4 Maximum Number of Cells

This is fixed at 16 for the bq78PL116.

### 6.2.5 Max Number of Temperatures

This is fixed at 5 for the bq78PL116. It indicates four external sensors, connected to XT1, XT2, XT3 and XT4, and one internal sensor of the bq78PL116.

### 6.2.6 Sense Resistor

This is the value of the current sense resistor in micro-Ohms. This value is specified by user in the Pack Configuration File (.tmap). The configuration file allows one of three sense resistors to be selected. The selection process is done by first writing the Sense 0 and Sense 1 bits in the Hardware Configuration Register and then doing a relearn/initialize command.

### 6.2.7 EPD Refresh Period

See the Chapter on Display. This value is written by the user using a Pack Configuration File (.tmap) in units of minutes.

### 6.2.8 EPD Pump Time

See the Chapter on Display. This is directly written by the user in units of cycles.

### 6.2.9 EPD Write Time

See the Chapter on Display. This is directly written by the user in units of cycles.

### 6.2.10 Display Driver Frequency

This is the display driver frequency directly set by the user. The allowable range is 20 to 50 Hz.

### 6.2.11 FW Build

This is fixed in the bq78PL116 to 717. This is the particular build of FW 6000.

### 6.2.12 Firmware Version

This is fixed in the bq78PL116 to 6000.


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### 6.2.13 Firmware CRC

This is the Cyclical Redundancy Check value for the firmware in the bq78PL116.

### 6.2.14 Data CRC

This is the Cyclical Redundancy Check for the data stored in the bq78PL116.

### 6.2.15 Current Delta

This parameter can be directly set by the user. The default is 100mA and should stay at that level. It is the change in current needed to perform different impedance measurements like Normalized Dynamic Impedance (NDI).

### 6.2.16 Access Level

This is the present access level of the bq78PL116. There are three access levels:

- Sealed, Level 0: This allows access to Standard SBData Commands from 0x00 to 0x23 and also the Extended Data Commands at 0x3C to 0x58.
- Partially Unsealed, Level 1: This allows everything in Level 0 and also access to read and change Safety Level 1 and 2 Timers and Limits.
- Unsealed, Level 2: This allows full access to the bq78PL116. This is the default access level at which the device ships.

The access level is changed by the user through commands in the bqWizard.

## 6.3 Pack Dynamic

The pack parameters that are grouped in the Pack Dynamic section that are dynamically updated by the firmware are defined below.

### 6.3.1 Board Temperature

The source of this temperature is the sensor inside of the bq78PL116. This value is used in the Board Over Temperature Safety Feature.

### 6.3.2 Pack Passed Current

This is considered an internal gas gauge variable that is the accumulated current that has passed through the sense resistor. This value is range limited to -32768mAHrs and +32767 mAHrs. When the value reaches one of the limits it rolls over to zero.

### 6.3.3 Cycle Since Learn

This is the number of cycles since a qualified Qmax learning event took place.

### 6.3.4 Epoch Hour

It is the number of hours since the last relearn/initialize command was executed.

### 6.3.5 Number of Rebuilds

It indicates the number of times that the bq78PL116 tried to build the PowerLAN network. Ideally, this number is always zero indicating an errorless PowerLAN.

### 6.3.6 Number of Polls

Number of Polls indicates the number of PowerLAN polls by the bq78PL116. Each number indicates an instance of the one second poll interval. This number is incrementing even if polling is not active on the SMBus.



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### 6.3.7 Number of Poll Errors

The Number of Poll Errors is a record of the number of PowerLAN bus poll errors that have occurred.


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# Operating Modes and Ranges

The bq78PL116 has three main modes of operation: Normal, Stand-By and Ship. There are also a temporary operating mode within Normal mode that is controlled by the status of the Wired Bit and the Safe Disconnect Command.

## 7.1 Normal Mode

During normal operation, the bq78PL116 takes *Current*, *Voltage* and *Temperature* measurements, performs calculations, does PowerPump cell balancing, updates SBS data, and makes protection and status decisions at regular intervals. Within the Normal Operating Mode are two sub modes called Wired/Unwired and Safe Disconnect. These are described below.

### *7.1.1 Wired / Un-Wired*

The Algorithm Enable register bit 3 is the Wired status of the bq78PL116. The default setting is 0, called Un-Wired. When set to a 1 it indicates that the bq78PL116 is Wired.

Wired means that all of the cell "wire" connections are securely mated to bq78PL116 and bq76PL102s, if in system. The bq78PL116 spends its normal operating life Wired.

Un-Wired means that these same connections are not complete. This is the case during construction or disassembly of a battery pack. While Un- Wired, the bq78PL116 has restricted operational capability. The primary restriction is flash memory writes. It is not safe to remove power from the bq78PL116 while Wired.

The bqWizard and the bq78PL11x API both contain commands to conveniently toggle the Wired Bit.

### *7.1.2 Safe Disconnect*

Whenever power to the bq78PL116 and bq76PL102s (if present) is to be removed, the command called safe disconnect must be issued.

This Command puts the bq78PL116 in a safe mode prior to power removal. One of the primary tasks it performs is to shut off PowerPump. This mode of operation after the Safe Disconnect Command is issued only lasts twenty seconds. At which time, the mode stops and the bq78PL116 returns to Normal Mode if power is not removed. The user must again issue Safe Disconnect and remove power within twenty seconds.

The bqWizard and the bq78PL11x API both contain commands to conveniently issue the Safe Disconnect Command.

The Safe Disconnect Command is not needed when simply disconnecting the SMBus connections.

## 7.2 Battery Pack Removed Mode/System-Present Detection

### *7.2.1 Battery Pack Removed*

The bq78PL116 interprets SMBus signals remaining low for 4 seconds as removal of the battery pack from the load (host).


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### 7.2.2 System-Present FET Control

The system-present detection system can optionally open FETs when the pack is removed from the host.

Optional FET control is activated by setting the SYSTEM PRESENT FET CONTROL bit in the HARDWARE CONFIGURATION register. If this bit is cleared, all FETs remain on while the pack is removed from the host.

When the SYSTEM PRESENT FET CONTROL bit is set, only the discharge FET remains on when the host system is not present.

Note 1: All FETs are opened while in ship mode, regardless of system-present configuration.

Note 2: The host system relies on power from the pack for SMBus operation. Therefore, when using SMBus as the means of detecting system presence, the discharge FET must remain on.

## 7.3 Standby Mode

The bq78PL116 goes into standby mode when the SMBus signals are not pulled high, no current flow exists, no safety rules are active, and no cell balancing is required. In standby mode, the bq78PL116 periodically checks the safety rules, detects any change in SMBus status, senses current flow, checks for pushbutton pressed if implemented, and checks for cells out of balance. Any of these events causes the device to exit standby mode. The LP threshold settings replace the normal hardware trip settings while in standby mode. See the *bq78PL116 PowerLAN™ Master Gateway Battery Management Controller With PowerPump™ Cell Balancing* data sheet (SLUSAB8A) for electrical specifications.

Parameters:

(a) Hardware LP Discharge Threshold: This current threshold determines when the discharge (DSG) MOSFET is opened when in standby mode.

(b) Hardware LP Discharge Duration: This is the duration that Hardware LP Discharge Threshold current must be observed before the discharge (DSG) MOSFET is opened while in standby mode.

(c) Hardware LP Charge Threshold: This current threshold determines when the charge (CHG) MOSFET is opened when in standby mode.

(d) Hardware LP Charge Duration: This is the duration that Hardware LP Charge Threshold current must be observed before the charge (CHG) MOSFET is opened while in standby mode.

Entrance Criteria: The device can enter standby mode when all of the following criteria are satisfied.

(a) Pack is removed from host computer.

(b) No safety events are pending or active.

(c) Fuse is not blown.

(d) Balancing is not required.

(e) Pushbutton is not pressed.

(f) No LED patterns are being displayed. See Table 12-2 for bq78PL116 display operation.

Exit criteria: The device exits standby mode when one or more of the following criteria is satisfied.

(a) SMBus host activity, SMBus SMBCLK and SMBDAT pins.

(b) Pushbutton pressed

(c) Safety issue detected

(d) Current flow greater than Transition to Discharge Current or Transition to Charge Current is detected.

Mode behavior: While in standby mode, the bq78PL116 behaves as follows:

(a) Tests for pack insertion at 2-second intervals (SMBus activity or SYSTEM PRESENT pin)

(b) Tests for button press at 2-second intervals

(c) Tests for current flow at 2-second intervals

(d) Runs all measurements for a duration of 4 seconds every 10 minutes

(e) Tests for safety conditions at 10-minute intervals for a duration of 4 seconds

(f) Assesses need for balancing at 10-minute intervals for a duration of 4 seconds

(g) Hardware safety circuitry remains active, but is set to the LP levels. There is no HW SC LP setting. See Section 2.10 and Section 2.11.



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## 7.4 Ship Mode

Ship mode is an ultralow-power state where all functionality is periodically suspended except for an internal timer. The MOSFETs are always open in ship mode when in this ultralow-power state. This mode is not entered in normal operation. It is intended that the device be put into this mode after factory configuration and test and prior to shipment.

Ship Mode has an entrance and exit criteria and a mode behavior that is periodic based on the internal timer mentioned above.

**Entrance Criteria:** The device can enter Ship mode when all of the following criteria are satisfied.

(a) Ship mode is set.
(b) SMBus lines (Clock, Data) remain low and stay low for 2–4 seconds.
(c) A First or Second Level Safety Condition is not present or pending.
(d) A permanent failure condition is not present, SPROT output is low.
(e) Cell balancing is not required.
(f) Pushbutton is not being pressed or serviced.
(g) When configured for LED display, no pattern is being displayed.

**Exit criteria:** There are two ways that the device can exit ship mode: permanent and temporary.

**Permanent Exit criteria:**
The permanent exit is intended to be a single event. This would be when a shipped pack is first used in the application.
The device can be made to permanently exit ship mode when the SMBus lines (Clock, Data) are pulled high for 2–4 seconds. The only way to re-enter ship mode is to then set the Ship Bit and satisfy the Entrance Criteria.

**Temporary Exit from Ship Mode:**
The PowerLAN Master Gateway controller will perform the following tasks on a periodic basis while in Ship mode. This is considered a temporary exit from ship mode or its modal behavior.

1. Tests for SMBus activity at two second intervals. This is the check for a permanent exit criteria mentioned above. (SMBus pins detected as high.)
2. Tests for SOCi push button press at two second intervals. If a push button is detected, the SOCi display will be serviced and the device is put into Active Mode until the SOCi display timer is elapsed.
3. Active mode is entered for a minimum of 10–12 seconds at a six minute interval. During this time:
   (a) First and Second Level Safety rules are evaluated. An active safety rule keeps the device in Active mode until the safety rule violation is cleared.
   (b) PowerPump Cell Balancing is performed if necessary. A cell imbalance will keep the device in Active mode until the cells return to balance as determined by the Minimum Cell Differential for Balancing parameter value.

## 7.5 Operating Current Range

Three operating current ranges are supported with the bq78PL116. They are selected by changing the bits 10 and 11 in the Hardware Configuration register and then issuing a relearn/initialize command. This allows the pack designer to optimize for packs operating between 11A and 110A. Table 7-1 details the operating conditions available to the user as a function of the selected sense resistor.

Two maximum operating capacities are supported, 32,767 mAh and 327,760 mAh.


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## Table 7-1. bq78PL116 Operating Current and Capacity Ranges

| Sense Resistor (mΩ) | Current Resolution (mA) | Maximum Discharge Current (A) | Maximum Charge Current (A) | Hardware Safety Short-Circuit Discharge Threshold (A) | | Hardware Safety Overcurrent Charge and Discharge Threshold (A) | | SBS Reported Data | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min [(1)] | Max [(1)] | Min [(1)] | Max [(1)] | Maximum Capacity (Ah) | Maximum Current (A) | Specification Info IPScale [Bits 15:12] |
| 10 | 1 | –11.2 | 10.08 | –4.96 | –30.75 | 4.28 | 31.19 | 32.767 | ±32.767 | 0 |
| 3 | 1 | –26 | 26 | –16.5 | –102.5 | 14.27 | 103.9 | 32.767 | ±32.767 | 0 |
| 1 | 10[(2)] | –111 | 100 | –49.6 | –307.5 | 42.8 | 311.8 | 327.67[(2)] | ±327.67 | 1 |

(1) Typical values

(2) Battery capacity resolution is 10mAhr and current resolution is 10mA.



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# Calibration

## 8.1 Cell Voltage Calibration

The bq78PL116 part is calibrated at the factory for cell voltage. No calibration by the customer is required to achieve data sheet accuracy ratings. Cell voltage offset and gain correction for cells 1 to 4 are stored in the bq78PL116.

### *8.1.1 Cell Voltage Calibration Data Transfer*

Systems that have five or more series cells require the use of one or more bq76PL102 Dual Cell Monitor devices. The cell voltage calibration information for each bq76PL102 is stored internally. This calibration information (offset and gain) must be transferred down to the bq78PL116 for cell voltage measurement. This is done by selecting the command to Load a Configuration File (.tmap) and Relearn from the bqWizard™ File menu. This can also be accomplished via the bq78PL116 API by Loading the production clone file (.dat) and then issuing a Commit command. The cell voltage calibration information from the bq76PL102s is sent to the bq78PL116 whenever the Relearn/Initialize command is issued.

Three or four series cell applications do not include bq76PL102s and therefore do not require any cell voltage calibration data transfer.

## 8.2 Temperature Sensor Calibration

Temperature calibration must be performed as part of the PCB manufacturing flow. Because performance is based on the sensors attached to the bq78PL116 and the internal sensor, each system must be calibrated. One calibration file cannot be loaded to many packs.

Temperature calibration should be done after a Configuration File (.tmap) is loaded and relearned. In other words, all cell voltages must be reading within specifications and the desired temperature sensor mapping must be established before temperature calibration can occur.

Temperature calibration is performed using a single known temperature in a certain range (18°C to 30°C). The bqWizard™ software or bq78PL11x API communicates the value to the bq78PL116 and it applies an offset correction to its temperature calculation.

## 8.3 Current Calibration

Current calibration must be performed as part of the PCB manufacturing flow. Because performance is based on the sense resistor attached to the bq78PL116, each system must be calibrated. One calibration file cannot be loaded to many packs.

Current calibration occurs after temperature calibration is completed. The current measurement system uses device temperature as a parameter in its current calculation.

An offset correction based on the system is obtained when the user applies an open circuit to the pack terminals and alerts the bq78PL116 via the bqWizard™ calibration utility or through the bq78PL11x API. A gain correction based on the system is obtained when the user applies an average load current at the pack terminals and alerts the bq78PL116 via the bqWizard™ calibration utility or through the bq78PL11x API. The applied current for gain correction can be –32000 mA to +32000 mA.

NOTE: For systems that use the 1-mΩ resistor, the current value entered for gain correction is the actual current divided by 10.


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## 8.4 Calibration File

The calibration information of the device can be saved in a unique calibration file (.cal). This information is exclusive to the system in which it was calibrated. The file contents are encoded and are not intended to be readable, except by the firmware. The offsets for cell voltage, temperature and current are stored and the gain corrections for cell voltage and current are also stored. Creation of the file is through the bqWizard™ software or the bq78PL11x API.

Possible uses of the file are to restore a calibration that may have been lost. A single calibration file cannot be used to calibrate multiple packs.

**NOTE:** A single calibration file cannot be used on multiple bq78PL116s.



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# SMBus Communications

The SMBus port of the bq78PL116 communicates Standard and Extended SBData Commands and Controls to the SMBus Host. This is done on pins SMBCLK and SMBDAT and referenced to the system ground. The bq78PL116's Extended Data and Extended Controls capability provides the user with a wealth of information and control for state of the art battery management.

## 9.1 SMBus and SBData

The bq78PL116 uses SMBus v1.1 with master-mode to communicate the information described in the Smart Battery Data Specification (SBData v1.1). Refer to the SMBus and SBData Specifications. System Management (SMBus) Specification, version 1.1 http://smbus.org/specs/ Smart Battery Data Specification, version 1.1 http://smartbattery.org/specs/sbdat110.pdf

## 9.2 SMBus On and Off States

The bq78PL116 detects an SMBus off state when SMBC and SMBD are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

## 9.3 bq78PL116 Slave Address

The bq78PL116 uses the address 0x16 as a default. The user can change the address using a Pack Configuration File (.tmap) that can be made by the Pack Configuration Utility in the byWizard.

## 9.4 PEC

The SpecificationInfo(0x1A) Command bits 4…7 call out the PEC support. The bq78PL116 supports transmission with and without a PEC included.

## 9.5 Broadcasts to Smart Charger and Smart Battery Host

The bq78PL116 does not support broadcasts to a smart charger or smart battery host.


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# Gas Gauging and Chemistry

The bq78PL116 measures individual cell voltages, pack voltage, temperatures, and current as inputs to an algorithm used to determine capacity of the battery pack.

## 10.1 Introduction

The bq78PL116 gas-gauging algorithm uses open-circuit voltage (OCV) when the system is in a relaxed state along with charge integration when the system is under load conditions to determine State of Charge (SOC) and Chemical Capacity (Qmax). It acquires dynamic cell impedance at times of load current change and updates the Battery Impedance Profile during normal battery usage. It further uses the Battery Impedance Profile along with SOC and Qmax to determine SBS:FullChargeCapacity(0x10) and SBS:RelativeStateOfCharge(0x0d) specific for the average load of a given application.

## 10.2 Basic Measurements

The gas-gauging calculations depend on several basic measurements provided by the measurement subsystem of the bq78PL116. These are:

- Synchronous measurements of cell voltages and pack current
- An independent continual coulomb count of passed charge
- Individual cell temperatures
- Various derived parameters such as average current, dynamic cell impedance, etc.

### *10.2.1 Pack Current and Charge*

The instantaneous pack current reflected by the voltage across the current-sense resistor is acquired by a continuously running delta-sigma modulator. This single bit stream is used to produce both charge and current by appropriate decimation. Bit-stream accumulation over a 2-second window (box car) results in passed-charge increments for coulomb counting. Decimation of the bit stream using an 80-ms tapered window results in the basic current reading. The window is triggered synchronously with similar windows for cell-voltage measurement. Current and voltage readings are updated every second. To minimize ADC offset and offset drift, the ADC input is commutated every second under firmware control. (Current readings are derived from two contiguous windows positioned across the commutation instance).

In addition, there is a one-time, board-level calibration of residual offset and gain for current and coulomb readings. (Independent calibration parameters are used for current and coulomb readings). The coulomb reading only is subject to a snap-to-zero before use in the GG algorithm. The coulomb counter resolution is approximately 1 mC or 0.000278 mAh. Current reported as SBS:Current(0x0a) in mA is based on the coulomb reading after snap-to-zero. Current flow in the discharge direction is reported as negative.

### *10.2.2 Cell Voltage*

All cell voltages are updated every second using 80-ms measurement windows synchronous with the current measurements. Each cell has its own ADC. Cell voltages are compensated for ADC offset and ADC gain. Cell voltages are reported in mV by SBS:VCELLx(0x3c–0x3f) for cells 1 to 4 and by SBS:VCELLx(0x40–0x4b) for cells 5 to 16.

### *10.2.3 Cell Temperatures*

Temperatures external to the bq78PL116 are sensed by means of forward voltage drop of a dual diode


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(excitation current ~50 µA). Temperature voltages are acquired every 2 seconds using an 80-ms measurement window. Readings are compensated for ADC offset and ADC gain. In addition, there is a one-time, board-level, room-temperature calibration of diode offset. (The temperature coefficient of the dual diode is known, a priori, from characterization.) SBS:Temperature(0x08) is updated based on the maximum cell temperature and reported in 0.1°K units.

## 10.3 Gas Gauge Terms and Notational Convention

This section identifies some important gas gauge terms a notational convention used during the gas gauge operation presentation.

### *10.3.1 Conventions*

A certain convention is used to describe some of the gas gauge parameters and variables. X(n, t) is an array variable called “X” that is “n” elements long. “n” typically represents the number of series cells, n=1, 2, 3, 4, …. The “t” symbolizes the value of the variable at an instance in time. The time component of a variable is often used to enhance the explanation of algorithms. If a variable does not have an (n,t) it is a constant or a generic representation.

### *10.3.2 Open Circuit Voltage (OCV)*

The OCV estimate is a function of SOC and temperature. The bq78PL116 uses the TI standard cell chemistry files as the initial inputs for gas gauging.

### *10.3.3 Design Capacity*

Design Capacity is a parameter in the data set. It is not changed by the gas-gauging algorithms, but is used in the determination of Absolute State of Charge.

### *10.3.4 Qmax*

The chemical capacity of the individual cells is referred to as QMAX(n). This is the amount of capacity which could be extracted from the cell under a relatively low load if it were fully charged. The PowerLAN gas gauging algorithm uses the cell with the lowest QMAX when calculating the pack capacity.

### *10.3.5 Qrem*

The capacity remaining at some intermediate charge is referred to as QREM(n).

### *10.3.6 FullChargeCapacity(0x10)*

The capacity of a fully charged pack under the specified load until Discharge Completion Pack Voltage Qualifier is reached by Voltage(0x09) is referred to by FullChargeCapacity(0x10), or commonly FCC . Note that this is not available on a cell basis.

### *10.3.7 RemainingCapacity(0x0F)*

The remaining capacity of the pack at the present state of charge under the specified load is referred to as Remaining Capacity (0x0F), or commonly RemCap. The specified load is determined by the user by setting the Capacity Algorithm parameter.

### *10.3.8 RelativeStateOfCharge (0x0D)*

The RelativeStateOfCharge (0x0D), or commonly RSOC, is defined as the ratio of the RemCap to the FCC.

## 10.4 State and Mode Definitions

Central to the behavior of the gas gauge are current-flow states and reporting modes.



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### 10.4.1 Current Flow State

The pack resides in one of three current-flow states: Charge, Idle or Discharge. Transition between states occurs when the following conditions are met:

- Idle: Entered when the Absolute Current is less than the Transition to Idle Current for a Time longer than Transition to Idle Time.
  - A condition within Idle Mode is Cell Relaxation. This condition is entered when in idle for a time longer than OCV Idle Qualifier Time.
- Discharge: Entered when the Current is greater than the Transition to Discharge Current
- Charge: Entered when the Current is greater than the Transition to Charge Current.

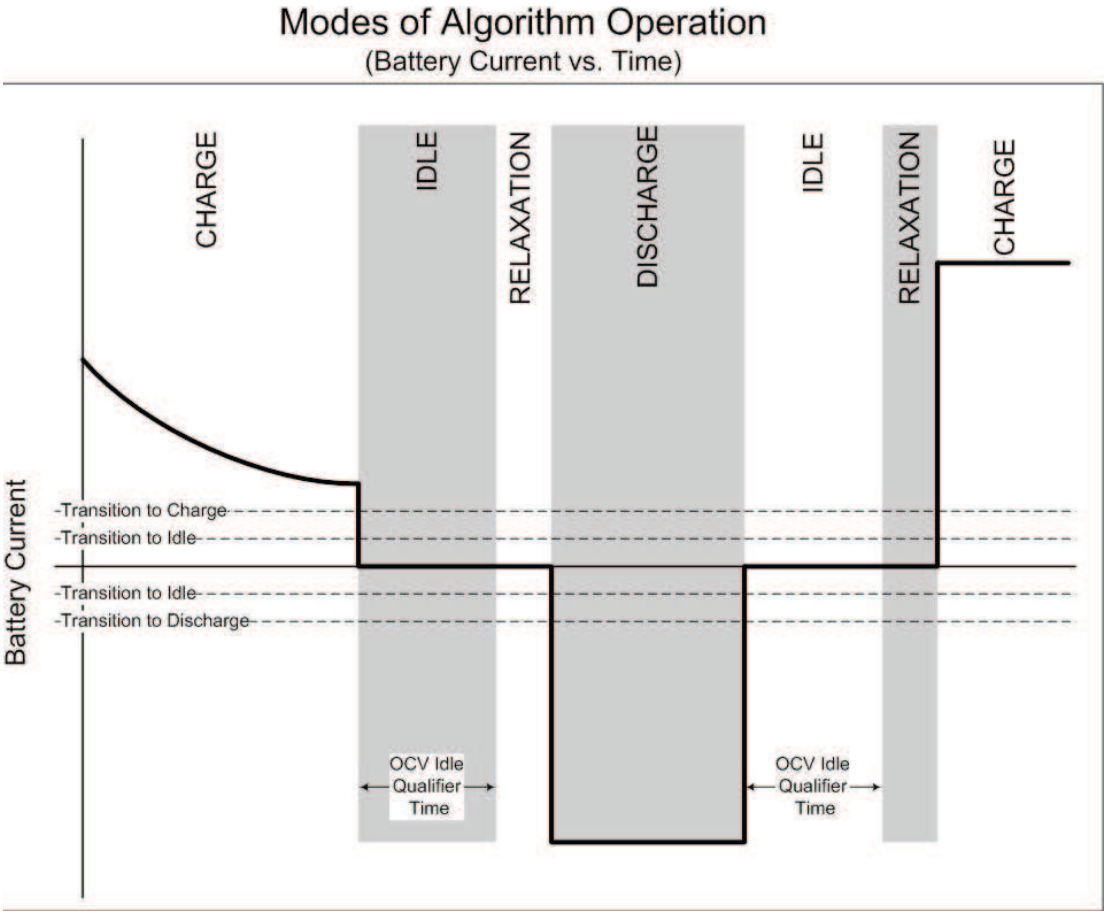


**Figure 10-1. Gas Gauge Algorithm Modes of Operation**

### 10.4.2 Reporting Modes

The reporting of the predicted remaining capacity, SBS:RemainingCapacity(0x0f), and time to empty, SBS:RunTimeToEmpty(0x11) depends on the mode configured:

- Current mode: Assumes the load continues as a constant current over the predicted remaining time to empty. SBS:RemainingCapacity(0x0f) is reported in mAh.
- Power Mode: Assumes the load continues as a constant current over the predicted remaining time to empty. SBS:RemainingCapacity(0x0f) is reported in mWh. The average time to full, SBS:AverageTimeToFull(0x13), prediction always assumes CC/CV charging and is not affected by reporting mode.


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## 10.5 Gas-Gauge Behavior

### 10.5.1 Update of $Q_{MAX}$

$Q_{MAX}$ is learned from the change in SOC and Passed Charge between two qualified points in time, P1 and P2. Loosely speaking, the points occur during a time when two consecutive relaxation periods are separated by a period of current flow. The first point occurs during the first relaxation period. Then there is a charge or discharge period that meets a certain minimum change in SOC. Then the second point is during the second relaxation period.

The first qualification of P1 and P2 is that the local slope of the OCV table around each point must be greater than the Min OCV Slope parameter. This parameter is typically set to 2mV/% RSOC. Second, P1 is deleted if the time since its acquisition > Stale FCC Timeout. This parameter is typically set to 2880 minutes, or 48 hours. Lastly, the absolute value of the change in SOC since the last learning point must be at least equal to the FCC Learn Qualifier in order for $Q_{MAX}$ learning to take place. This parameter is typically 30% of Design Capacity. There is no temperature restriction on the calculation of $Q_{MAX}$.

If the above conditions are met, estimates of $Q_{MAX}$ updates are calculated as follows:

$$\left[Q_{MAX}(n,P2)\right]_{EST} = \frac{\Delta Q}{SOC(n,P1) - OSC(n,P2)} \quad (1)$$

This estimate is used to update the actual $Q_{MAX}$ with a weighting function which is proportional to the change in SOC between the two points. Following an update, Passed Charge (ΔQ) is reset to zero, and the initial leaning point, P1, is replaced by P2.

For cases where the above conditions are not present to drive a $Q_{MAX}$ update, a parameter called Cycle Fade is used to estimate the change in $Q_{MAX}$ after each cycle is counted.

$$Q_{MAX}(n, t+1) = (1\text{-CycleFade}) \times \text{CycleCount(0x17)} \times Q_{MAX}(n,t) \quad (2)$$

The CycleFade parameter is typically set to 0.05%. The cycle count is incremented when an accumulated discharge equal to the Design Capacity parameter is met.

### 10.5.2 Update of Chemical State of Charge (SOC)

Calculations are dependent on the operating mode. While in Idle Mode, cell relaxation is achieved after the OCV Idle Qualifier Time has elapsed. This parameter is typically set to 30 minutes. Relaxation triggers the calculation of $Q_{REM}$ for each cell. The OCV voltage for each cell is used to look up the SOC which would result in that voltage. This SOC is then used to obtain an estimate of the $Q_{REM}$ value, called $[Q_{REM}]_{EST}$. Because the quality of this estimate will depend on the flatness of the OCV curve at the measured voltage, the actual $Q_{REM}$ value is updated using the estimate and an update factor which is inversely proportional to the slope of the OCV curve. These calculations are summarized below:

- SOC(n, t) = f(OCV Table, T(n, t)), where T(n, t) is the cell temperature and the OCV vs. SOC table is predefined by the Chemistry File (.chem)
- $[Q_{REM}(n, t)]_{EST} = Q_{MAX}(n, m) \times SOC(n, t)$, $Q_{MAX}(n, m)$ is the chemical capacity of the cell determined at the time “m” – which could be equal to “t” or some time in the past.
- $Q_{REM}(n)$ = Smoothing Function with inputs $Q_{REM}(n)$, $[Q_{REM}(n, t)]_{EST}$, OCV Slope.

These calculations persist every minute during the cell relaxation phase of Idle Mode. It is assumed that the Idle current is low (zero) during Relaxation and does not contribute significantly to IR loss.

While in Charge or Discharge Mode, SOC(n) is calculated every two seconds as a function of the passed charge(ΔQ) during that time:

$$Q_{REM}(n,t+1) = Q_{REM}(n,t) + \Delta Q \quad (3)$$

$$SOC(n) = \frac{Q_{REM}(n)}{Q_{MAX}(n)} \quad (4)$$



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### 10.5.3 Update of Resistance

The dynamic impedance of each cell, DI(n), is derived from the changes in pack current, Δ I, and resultant changes in cell voltage, Δ V(n), between two successive sets of synchronous measurements.

$$DI(n) = \frac{\Delta V(n)}{\Delta I} \quad (5)$$

DI updates can occur during charge or discharge modes. (Dynamic Impedance is named HF Impedance in the bqWizard software.) The reading is qualified for minimum change in current, specified by Current Delta, and represents the real impedance in the range 1–10 Hz. The Current Delta parameter is typically set to 100 mA. By using this approach, impedance is found directly without assumptions about the correctness of $Q_{MAX}$, SOC, and OCV table. The dynamic impedance is used both in safety rules (impedance growth) and also gas gauging to update the $R_a$ table.

DI calculations are only qualified by the Current Delta parameter. Updates to the impedance parameters stored in flash memory are qualified by SOC and temperature. The single value stored in data flash memory for each cell is DI(n) normalized to 0°C, called Normalized Dynamic Impedance or NDI(n).

$$NDI(n) = \overline{DI(n)}\Big|_{T=0°C} \quad (6)$$

The parameters Normalized Dynamic Impedance Low Temperature and Normalized Dynamic Impedance High Temperature set the temperature range under which NDI updates occur. This range is typically 20 to 30 °C. The Normalized Dynamic Impedance SOC parameter sets the SOC upper limit for NDI updates. This parameter is typically set to 15% and NDI calculations are not performed above this value. The individual NDI estimates based on qualified DI readings are used to update the stored NDI values using a smoothing function which reduces the impact of noisy estimates. Lastly, the new NDI value is compared to the last time NDI was calculated. If there is not an increase in NDI, then the Ra table update is not performed. This filter is in place because cell impedance does not normally decrease with time.

The $R_a$ table consists of 15 values of cell impedance, stored in milli-Ohms, that are a function of cell SOC. Each series cell can have a different $R_a$ table depending on its measured performance. Each entry in the table is referred to as a grid point, N, where N = 0 to 14. The lowest SOC grid point is N = 14 and the highest SOC grid point is a N = 0. Spacing between grid points are in 11.1% increments of SOC until 23.3% SOC, and then 3.2% increments of SOC until approximately 0%.

The $R_a$ table is updated by applying a weighted ratio of the normalized dynamic impedance change. The effective result is a change to the terms below 30% SOC. The Ra terms above 30% have no meaningful update due to the shape of the weighting factor vector.

The process looks like this:

$$R_a(n,t) = R_a(n,0) + (NDI(n,t) – NDI(n,0)) \times \beta \times Weight(RSOC) \quad (7)$$

Where NDI(n, t) – NDI(n, 0) represents the change in NDI of cell n from initial value to the present value. The scaling factor, β, is a gain defined by Normalized Dynamic Impedance Gain. The default value is set to 32 in the Auxiliary Chemistry File (.aux). The user creates the .aux file through an offline learning cycle test described in Application Note – *Chemistry Selection for the bq78PL114* (SLUA505). If it is set to zero, no updates will be done. The Weight function implements the shaped update. This satisfies the fact that the impedance growth is greater at the lower SOC values that at higher values. This weighting function is a fixed value as defined by the firmware.

If a qualified NDI measurement cannot be completed and the cycle count is incremented, then another relationship is used to determine NDI(n, t). The relationship is a function of CycleCount(0x17) and takes the form of the following:

$$NDI(n,t)\ \alpha + \sigma \times \log(CycleCount(0x17)) \quad (8)$$

This is an empirical relationship that models expected cell impedance growth. The parameters “α” and “σ” define the empirical relationship and are fixed by the firmware.


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### 10.5.4 Update of FullChargeCapacity(0x10) & RemainingCapacity(0x0F)

The prediction of capacity consists of two components: Discharge Simulation and Coulomb Counting. The Discharge Simulation is used for estimating both RemainingCapacity(0x0F) and FullChargeCapacity(0x10). The simulations are not run continually and are only performed on the cell with the lowest $Q_{MAX}$.

An update to FCC and RemCap is performed whenever the following happens:

- There is a change to the Charge or Discharge state,
- If there is a change of $Q_{MAX}$ during Idle and at grid points during discharge. Grid points refers to the fifteen points that make up the Impedance vs. SOC table stored in the Chemistry File.
- Every 10th $Q_{REM}$ update in the Relaxation Period of the Idle State.

A continuous estimate of RemCap is provided during charge and discharge by Coulomb Counting between grid point simulations.

The Discharge Simulation can be described by the following iterative process:

1. Calculate: $SOC(m + 1) = SOC(m) + \Delta S \times m$
   - Where m = 0, 1, 2, 3, …
   - ΔS = step size of SOC equal to 1%.
   - SOC(0) is 0%.
2. Calculate: $V(n) = OCV(SOC(m + 1), T) – I \times R_a(SOC(m + 1), T)$
   - Use cell with lowest $Q_{MAX}$. Call this cell $V(n)_{LOW}$
3. Evaluate: V(n) LOW > (Discharge Completion Pack Voltage Qualifier / N). N = series cell count.

   (a) If True, then go to step 4.
   (b) If False, then go to step 1.
4. Calculate new Capacity values (when appropriate):

   (a) $RemainingCapacity(0x0F)_t = RemainingCapacity(0x0F)_{t-1} – (\Delta S \times m \times Q_{MAX})$
   (b) $FullChargeCapacity(0x10)_{NEW} = (100\% - \Delta S \times m) \times Q_{MAX}$

“t-1” and “t” in step 4a refers to the last time RemCap was calculated and the present value, respectively. The current used in step 2 of the discharge simulation is determined by the bottom two bits of the Capacity Algorithm parameter as shown in the following table.

| Parameter Value | Current used in Discharge/Charge Simulation | Current Used in Idle Simulation |
|---|---|---|
| 0x00 | DesignCapacity(0x18) / 5 | DesignCapacity(0x18) / 5 |
| 0x01 | Present value of Current(0x0A) | Zero |
| 0x02 | User Rate | User Rate |
| 0x03 | AverageCurrent(0x0B) | Last Discharge Average |

In most cases, setting the parameter to 0x03 makes the most sense, since it will follow the actual load without too much fluctuation. Last Discharge Average is updated at the end of a qualified discharge by computing the average current of the last discharge. In order to prevent spurious data from extremely short discharges, at least one grid point must be crossed for the discharge to qualify for updating the Last Discharge Average.

### 10.5.5 Example

As a concrete example, assume a room temperature (25°C) constant current discharge of a typical cell. Figure 10-2 shows the OCV and Impedance for the cell at this temperature and as a function of RSOC.



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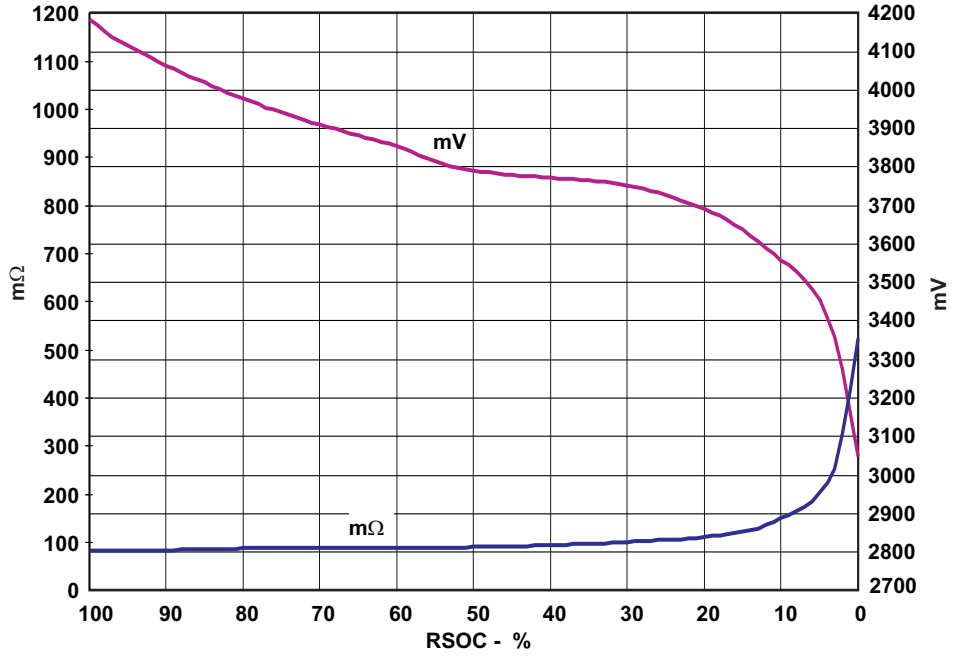


**Figure 10-2. OCV and Impedance at 25°C**

In Figure 10-3, the effect of the IR drop on the OCV is shown at two currents – 1 Amp and – 4 Amps. This clearly shows the shift of the terminal RSOC point to the left (higher RSOC) for higher currents. The relationship between the RSOC ranges used to calculate FCC and RemCap is also shown for the – 4 Amp simulated discharge. In this case, the present value of RSOC – used in the calculation of RemCap – is shown as 75%.

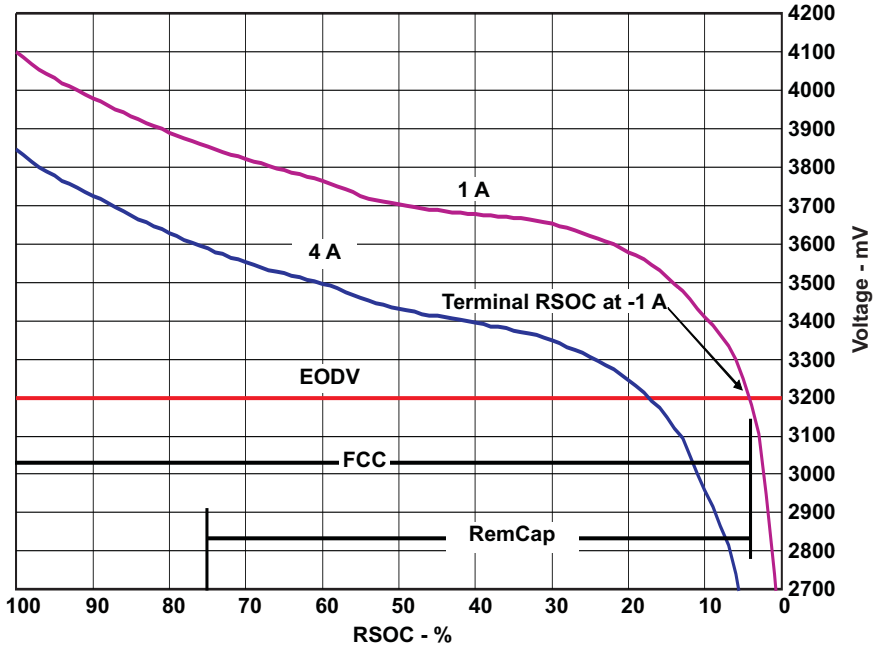


**Figure 10-3. Discharge Simulation at 25 °C and 1 and 4 Amps Discharge Curves**

Based on Figure 10-3, the – 1 Amp discharge simulation would stop at around 4% RSOC. Assuming a $Q_{MAX}$ of 2200 mAHrs and a present RSOC of 75%, RemCap would then be calculated as:

RemainingCapacity(0x0F)= (75% x 2200) – (4% x 2200) = 1562 mAHrs


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When FCC is calculated at the start of discharge, it would appear as follows:

FullChargeCapacity(0x10)= (100% x 2200) – (4% x 2200) = 2112 mAHrs

Because the cell impedance is a function of both RSOC and temperature, both are taken into account when performing the simulated discharge. Figure 10-4 shows the OCV and impedance at 0°C and Figure 10-5 shows the effect on the simulation.

Using the – 4 Amp, 0°C discharge data of Figure 5, RemCap would be

RemainingCapacity(0x0F)= (75% x 2200) – (54% x 2200) = 462 mAHrs

And, FCC if calculated at the start of discharge would be

FullChargeCapacity(0x10)= (100% x 2200) – (54% x 2200) = 1012 mAHrs

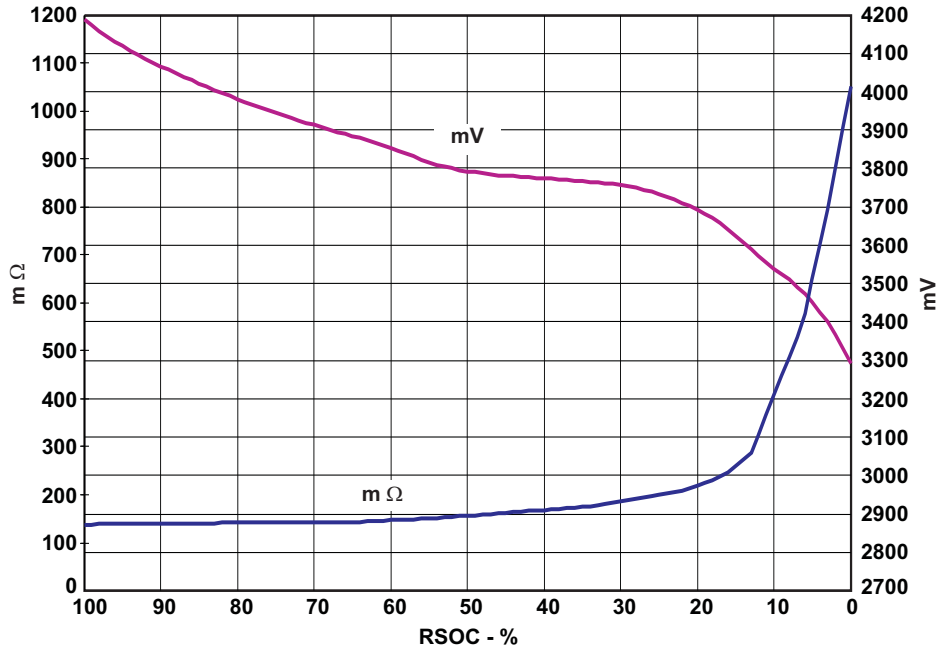


**Figure 10-4. OCV and Impedance at 0°C**



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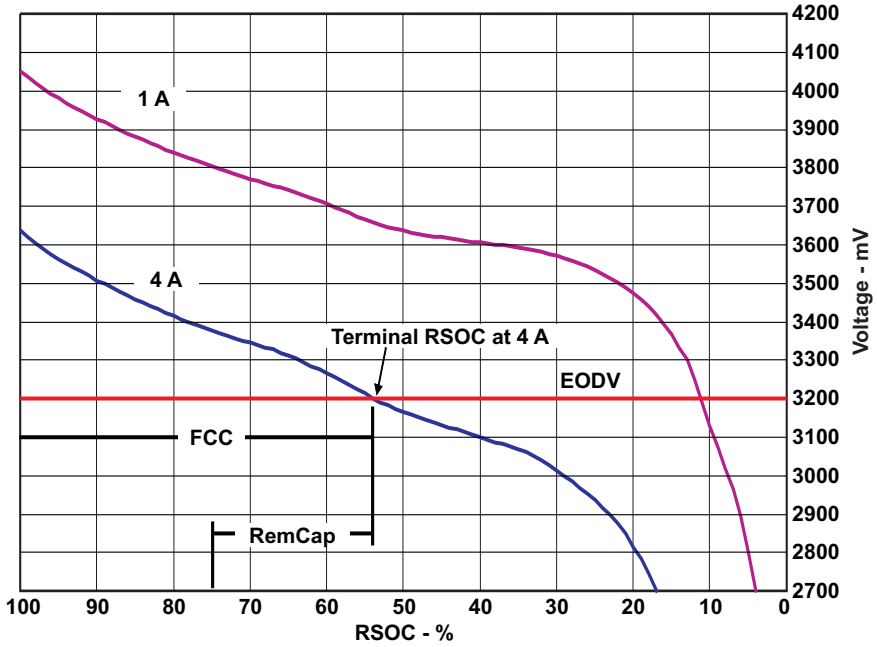


**Figure 10-5. Discharge Simulation at 0°C and – 1 and – 4 Amps Discharge**

### *10.5.6 Update of RelativeStateofCharge(0x0D)*

RelativeStateofCharge() is a function of RemCap and FCC. The definition is as follows:

$$\text{RSOC(0x0D)} = \frac{\text{RemainingCapacity(0x0F)}}{\text{RemainingCapacity(0x10)}} \quad (9)$$

Therefore, whenever either RemCap or FCC is updated, RSOC is updated.

### *10.5.7 Update of Max Error(0x0C)*

At initialization the value is 10. Maximum value is 100. It is set to 1 when capacity learning ($Q_{MAX}$) takes place. The value increases by 5% for each cycle that goes by without learning. If it ever gets to 100, the CONDITION_FLAG bit of BatteryMode() is set.

### *10.5.8 Update of RunTimeToFull (0x05)*

Another simulation is used to determine the RunTimeToFull(0x05) (RTTF) during charge mode. This is based on the assumption that the charge will take place in two consecutive periods – constant current and constant voltage. The time to full will be the sum of the time spent in each of these two conditions. This simulation uses the following parameters:

- Default Charging Voltage – Because the simulation is run on a single cell basis, the cell charging voltage is determined by dividing this parameter by the number of series cells
- Default Charging Current
- Charge Completion Taper Current Qualifier – this is one of the criteria that determines Charge Completion.
- Tau10 – this is the taper time constant (read from the .aux file)

The simulation is based on cell data, not pack data and the cell with the lowest $Q_{MAX}$ is used as this will be the cell which gets fully charged. $Q_{MAX}$ is an indication of the cell's capacity. The cell with the lowest capacity compared to the others will "fill up" first given that the same charge current is applied to all cells. A new simulation is run at each grid point crossing. Between simulations, the RTTF value is updated by subtracting the elapsed time since the last simulation.


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### 10.5.8.1 Determination of $RSOC_{TAPER}$

The $RSOC_{TAPER}$ is the RSOC at the point where the OCV of the cell plus the IR drop due to the charging current and cell impedance will be equal to the charging voltage. Beyond this point, the current will taper off and the voltage will be constant.

$$V_{CH} = V_{IR} + V_{OCV} \quad (10)$$

$$V_{OCV} = V_{CH} - V_{IR} \quad (11)$$

This voltage, $V_{OCV}$, and the OCV vs SOC table of the chemistry file are used to determine the Taper RSOC. In the following Figure 10-6, the point in time that the above calculations seek is marked with "RSOC Taper."

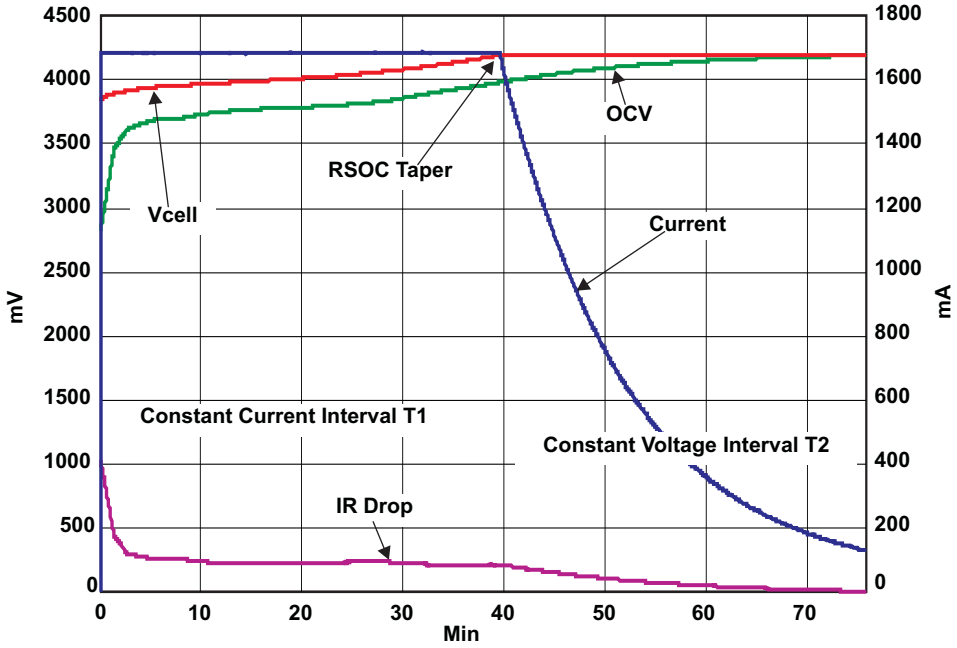


**Figure 10-6. Battery Charge Profile**

### 10.5.8.2 Constant Current Interval ($T_1$)

The Constant Current Interval ($T_1$) is the time that the present value of the current will take to discharge a capacity equal to the difference between capacity based on the present $RSOC_T$ and $RSOC_{TAPER}$. Because the $Q_{MAX}$ value is in mAh and the TTF is to be presented in minutes, there is a multiplier of 60. That is:

$$T_1 = 60 \times \frac{(RSOC_{TAPER} - RSOC_T) \times Q_{MAX}(lowest)}{Current_0} \quad (12)$$

### 10.5.8.3 Constant Voltage Interval ($T_2$)

The Constant Voltage Interval ($T_2$) is the period beyond the $RSOC_{TAPER}$ point where the current starts an exponential decay until the Charge Completion criteria are satisfied. The current follows this exponential function at the time of the calculation ($T_0$):

$$Current(T) = Current(T_0) \times e^{\frac{-10x(T_1 - T)}{Tau_{10}}} \quad (13)$$



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If $T_0$ is the time of the calculation and $T_{CC}$ is the time when the current is equal to Charge Completion Taper Current Qualifier, or $Current_{CC}$, this can be used to solve for the time to get to the end of charge.

$$T_2 = (T_{CC} - T_0) = \frac{Tau_{10}}{10} \times \log\left(\frac{Current}{Current_{CC}}\right) \quad (14)$$

If the RSOC is not yet at the RSOCTAPER, T2 is equal to the maximum value of this equation using Default Charging Current instead of using the present value of Current.

### 10.5.9 RunTimeToEmpty(0x11)

The value of RunTimeToEmpty(0x11) is calculated as follows:

$$RunTimeToEmpty(0x11) = \frac{RemainingCapacity(0x0F)}{Current(0x0A)} \quad (15)$$

It is updated whenever RemainingCapacity is updated.


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# PowerPump Cell Balancing

## 11.1 Cell Balancing

The bq78PL116 can use PowerPump™ cell balancing to decrease the differences in imbalanced cells at any time: while at rest, while charging, or while discharging. By maintaining cell-to-cell balance, pack performance is increased and cells are not excessively overcharged or overdischarged.

This increases overall pack energy by preventing premature charge termination. More Information can be found in the "PowerPump Balancing " Application Report (SLUA524).

The automatically operated algorithm determines the amount of charge needed to fully charge each cell. See the algorithm configuration register (Section 6.1.2) for balancing-algorithm options.

Parameters used for cell balancing:

1. Minimum Cell Differential for Balancing: Set in units of mV

   When the difference in voltage between any two cells exceeds the Minimum Cell Differential for Balancing value, then PowerPump™ cell balancing is activated.
2. Discharge Completion Voltage Qualifier: Set in units of mV. The lower cut off for cell balancing is governed by the following equation. It must be true for PowerPump to occur.
   (Lowest Cell – Discharge Completion Voltage Qualifier / Series Cell Count) > Minimum Differential for Balancing. There is no upper cell voltage cutoff for PowerPump.

The bq78PL116 supports the following configurable cell balancing features:

(a) SuperPump mode. When enabled, this allows 60%–70% pump, cell balancing, availability when there are no active safety events and current is not flowing.

(b) Disable cell balancing during discharge.

(c) Disable cell balancing during charge.

(d) All Cells Pump North or South. This is a feature for production test only.

SuperPump mode is turned off or is blocked from being enabled when:

- Any current flow (charge/discharge) is detected.
- A safety event becomes active with the following exceptions:
  - Overtemperature charge
  - Overtemperature discharge
  - Host watchdog timeout
  - Charge-inhibit temperature
  - Precharge voltage
  - Precharge temperature
  - Charge suspend – temperature (high and low)
  - Charge completion
  - Discharge completion
  - Charge timeout
  - Precharge voltage timeout
  - Board overtemperature
  - Discharge undertemperature



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During SuperPump cycle, temperature reading is suspended for the number of temperature measurement cycles selected when SuperPump mode was enabled. Temperature measurements are normally taken at 2s intervals. When in SuperPump mode, temperature measurements are suspended for 2 × (n + 1) seconds where n = the value between 1 and 15 programmed into the bq78PL116 Algorithm Register bits [10:7].

While in SuperPump mode, Temperature ROR Safety rule checking is postponed until 4 seconds has elapsed since the last SuperPump cycle.

Table 11-1 summarizes the percentage of time that pumping is active as a function of the Algorithm Register bits Turbo[3:0] suspended temperature measurement count settings. The greatest increase in pumping availability occurs at low settings between 0001b and 0100b. As the count is increased the curve flattens out, and no significant improvement is observed. The entries in the table are nominal values.

**Table 11-1. bq78PL116 Pumping Availability vs Algorithm Enable Register Bits Turbo[3:0]**

| Turbo[3:0] | 8 Cells | 10 Cells | 12 Cells |
|---|---|---|---|
| 0000 (default) | 42% | 38% | 32% |
| 0001 | 55% | 50% | 47% |
| 0010 | 59% | 55% | 52% |
| 0011 | 62% | 58% | 53% |
| 0100 | 63% | 59% | 56% |
| 0101 | 64% | 60% | 57% |
| 0110 | 65% | 61% | 58% |
| 1000 | 66% | 62% | 59% |
| 1010 | 66% | 62% | 60% |

### *11.1.1 Net Pumping*

Each cell has a Net Pumping statistic. This unit-less statistic records the pumping activity of the cell during every second. If the cell has PowerPump activity during the one second period then its Net Pumping statistic is incremented if it was pumped to or decremented if it did the pumping. Net pumping statistics are zeroed after a Charge Completion happens.



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# Display Operation

## 12.1 Display Operation

Pins LED1 to LED5 are configured to drive five LEDs in sequence when the pushbutton switch is activated. Each LED represents 20% State-of-Charge, using the value contained in SBS:RelativeStateOfCharge(0x0d). The LEDs light to indicate the SOC within 3 seconds of pressing the button, and LED illumination is maintained for at least 2 seconds (see Table 12-1). If the button is held down continuously, the LED indication turns off after 2 seconds and stays off unless the button is released and pushed again. LED1 is the least-significant and LED5 is the most-significant. A battery that is at or below 20% RSOC only has LED1 on. When the bq78PL116 is configured for EPD or LCD, only SEG1 is on. A battery that is above 80% RSOC has all five LEDs on, or in the case of EPD or LCD configuration, all five segments are on.

**Table 12-1. Status-of-Charge (SOC) Indication**

| SOC | Indication |
|---|---|
| SOC > 80% | 5 segments on |
| 60% < SOC ≤ 80% | 4 segments on |
| 40% < SOC ≤ 60% | 3 segments on |
| 20% < SOC ≤ 40% | 2 segments on |
| SOC ≤ 20% | 1 segments on |

During flash reprogramming, the LEDs indicate the progress of the code download. The LEDs also indicate a failed download if it occurs. An LED pattern is present during power-on reset and any subsequent reset.

the bq78PL116 is configurable to drive LED, liquid crystal (LCD), and electronic paper (EPD) type displays. See Table 6-1.

An EPD is a static display that only consumes power when it is being updated and does not require periodic refreshing. See EPD reference schematic in the bq78PL116 datasheet.

Table 12-2 summarizes display activity vs device operating mode. Table 8-4 describes display related pins and their operation as a function of selected display type.

The bq78PL116 EPD driver periodically updates the display whenever there is a change. An external power supply having a nominal 15-V output powers the display. A lower voltage may be used depending on the display and system qualification requirements. This increases the display write time. A voltage multiplier or charge pump power supply can be used to generate the required 15V. See EPD reference schematic in the bq78PL116 data sheet. It is advised to validate system design and configuration with the display vendor.

The bq78PL116 pulses the EPD display signals every time the display is updated. This occurs for the time defined in EPD Pump Time parameter. During this pump time, the TP signal can be used to drive a voltage multiplier or charge pump circuit to generate the display voltage. When EPD Pump time parameter is set to zero no pulsing occurs and the display subsystem must obtain its power from the cell stack or a separate voltage regulator connected to the cell stack.


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**Table 12-2. bq78PL116 Display Activity vs Device Operating Mode**

| Operating Mode | LED | LCD | EPD |
|---|---|---|---|
| Active / Normal | Enabled (push button) | Enabled | Enabled |
| Standby | Enabled (push button) | Enabled | Enabled |
| Ship | Enabled (push button) | Disabled | Enabled |
| Extreme Cell Undervoltage Shutdown | Disabled | Disabled | Enabled(1) |

(1) In EPD mode no display refresh occurs when the device is in Extreme Cell Undervoltage Shutdown mode

**Table 12-3. bq78PL116 Display Pin Operation As Function Of Display Type**

| Pin | LED | EPD | LCD |
|---|---|---|---|
| **PSH/BP/TP** | **PSH - Pushbutton.detect for LED display** | **TP -Top Plane and charge pump drive.** | **BP -LCD Backplane** |
| FIELD | – | Field segment | – |
| LED1/SEG1 | LED1 | SEG1 | SEG1 |
| LED2/SEG2 | LED2 | SEG2 | SEG2 |
| LED3/SEG3 | LED3 | SEG3 | SEG3 |
| LED4/SEG4 | LED4 | SEG4 | SEG4 |
| LED5/SEG5 | LED5 | SEG5 | SEG5 |

### 12.1.1 Display Parameters

The following parameters located in the Pack Configuration section are used for configuring display operation:

1. EPD Pump Time: Set in units of cycle counts. (Number of Display Driver Frequency cycles). A value of 0 disables the pumping function. Default = 120 cycles.
2. EPD Write Time: Set in units of cycle counts. (Number of Display Driver Frequency cycles). Default = 90 cycles.
3. Display Driver Frequency: Set in units of Hz. This is the LCD refresh frequency or the EPD charge pump frequency. Default = 30Hz.
4. EPD Global Refresh Period. Set in units of minutes. Default = 1440min.

### 12.1.2 bq78PL116 Bootloader LED Patterns

The display is also used to show the progress of firmware downloads. Note that EPD- and LCD-type displays are not supported for firmware downloads. During firmware download, an LCD or EPD may show random patterns. Also see Table 6-1, *bq78PL116 Hardware Configuration Register*.

LED order is from left to right (leftmost = LED5, rightmost = LED1).

Note: For the bq78PL116, the following sequence is followed by a second sequence in which all LEDs are turned on and then off after a brief period. This sequence does not occur with the bq78PL116.

**Table 12-4. bq78PL116 Bootloader LED Patterns**

| Seq. | Event | Pattern 1 LED[5..1] | Pattern 1 LED[5..1] |
|---|---|---|---|
| 1 | In bootloader mode-1(1) | ■ □ ■ □ ■ | □ ■ □ ■ □ |
| 2 | In bootloader mode-2(1) | □ □ ■ □ ■ | □ ■ □ ■ □ |
| 3 | Code downloading | Binary counting | |
| ■ = Off; □ = On | | | |

(1) Pattern-1 and -2 cycles every 15 seconds

Application-code-driven patterns (gas gage) are described somewhere else.



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# Lifetime and Safety History Data

For forensic purposes, the bq78PL116 saves lifetime and safety history in flash memory.

## 13.1 Safety History

The bq78PL116 records the most recent 10 occurrences of any activation of a safety rule or a reset. The safety events correlate with the rules described in this document.

A safety event is recorded with its name and the value that caused the event. The time stamp, FET status, fuse status, temperature, and current at the time of the event are also recorded. The record of the event is based on the last measurement prior to the event. The time stamp resolution is one hour. In the case of a voltage event, the number of the cell with the maximum value and the number of the cell with the minimum value are also recorded along with their respective voltages. The recorded temperature is always from the sensor with the highest temperature. Hardware Current Safety events happen so fast (millisecond time base) that the actual current that caused the event cannot be recorded by the firmware that samples on a one second basis.

The bqWizard™ software permits the safety events to be saved as standard CSV text files. The file also contains the firmware version, the bqWizard™ version, a time stamp, and device epoch hour. The epoch hour is the time from last reset. The Extended SBData Command mapping feature of the bq78PL116 can be used to access these LifeTime data values while in system over the SMBus. Some of these values are already mapped to the Extended Area (0x3c to 0x58) by default.

## 13.2 Lifetime Data

The extrema of the pack measurement data is recorded in Flash memory and referred to as Lifetime data. These parameters are considered valuable for possible forensic analysis that may take place in the event that a pack is returned to the manufacturer.

### *13.2.1 Lifetime Minimum Pack Voltage*

This is a record of the minimum pack voltage in mV. This is subject to the setting of the VScale bit in SpecificationInfo(0x1A).

### *13.2.2 Lifetime Maximum Pack Voltage*

This is a record of the maximum pack voltage in mV. This is subject to the setting of the VScale bit in SpecificationInfo(0x1A).

### *13.2.3 Lifetime Minimum Cell Voltage*

This is a record of the minimum cell voltage in mV amongst of the series cells.

### *13.2.4 Lifetime Maximum Cell Voltage*

This is a record of the maximum cell voltage in mV amongst of the series cells.

### *13.2.5 Lifetime Maximum Charge Current*

This is a record of the maximum charge current in mA. This is subject to the setting of the IPScale bit in SpecificationInfo(0x1A).


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### 13.2.6 Lifetime Maximum Discharge Current

This is a record of the maximum discharge current in mA. This is subject to the setting of the IPScale bit in SpecificationInfo(0x1A).

### 13.2.7 Lifetime Delivered Amp Hours

This is a record of the cumulative delivered Amp-Hrs of the pack. This is subject to the setting of the IPScale bit in SpecificationInfo(0x1A). If the CAPACITY_MODE bit is set in the BatteryMode(0x03) command, then this register is reported in 10mWHrs.

### 13.2.8 Last Discharge Average

This is a record of the average discharge in mA of the last discharge. This is subject to the setting of the IPScale bit in SpecificationInfo(0x1A).

### 13.2.9 Lifetime Minimum Temperature

This is a record of the minimum recorded temperature.

### 13.2.10 Lifetime Maximum Temperature

This is a record of the maximum recorded temperature.

### 13.2.11 Lifetime Maximum Power

This is a record of the maximum recorded power in Watts. This is subject to the setting of the IPScale and VScale bits in SpecificationInfo(0x1A).

### 13.2.12 Initializing Lifetime Values

The Lifetime values and Last Discharge Average are initialized after the first measurement cycle takes place after the first application of power. Subsequent power cycles do not repeat. This same process is followed when a relearn/initialize command is executed.

| Parameter | Initialized Value |
|---|---|
| Lifetime Minimum Pack Voltage | Present Value |
| Lifetime Maximum Pack Voltage | Present Value |
| Lifetime Minimum Cell Voltage | Present Value |
| Lifetime Maximum Cell Voltage | Present Value |
| Lifetime Maximum Cell Charge Current | Present Value |
| Lifetime Maximum Cell Discharge Current | Present Value |
| Lifetime Delivered Amp Hours | 0 |
| Last Discharge Average | User Rate |
| Lifetime Minimum Temperature | Present Value |
| Lifetime Maximum Temperature | Present Value |
| Lifetime Maximum Power | Present Value |


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# Safety and Status Register Definitions

## A.1 FET Status

The purpose of the FET Status register is to monitor the Pack Disconnect Control outputs. A bit set to one means the control pin is high (On). A bit cleared to zero indicates that the control output is low (Off).

| FET Status | | | | |
|---|---|---|---|---|
| Bit | 0 | 1 | 2 | 3–15 |
| Name | DEFET | CFET | PFET | RESERVED |

DFET: DSG Pin Status
CFET: CHG Pin Status
PFET: PRE Pin Status

## A.2 Safety Alert

The purpose of a Safety Alert is to indicate that the threshold of a particular Safety condition has been exceeded but, the condition has not lasted long enough to latch and cause the Safety Rule to be active. Alerts happen prior to the event status being set. A bit set to 1 means the alert condition is present. A bit set to zero means the condition is not present. The bit stays latched while the safety feature is active and clears when the safety feature clears.

| Safety Alert | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| Name | HOCD | HOCC | HSC | EUV | HWDG | COV | BOT | CUV | POV | PUV | OCC2 | OCD2 | OCC | OCD | OTC | OTD |

HOCD: Hardware Over Current Discharge
HOCC: Hardware Over Current Charge
HSC: Hardware Short Circuit
EUV: Extreme Cell Under Voltage
HWDG: Host Watchdog Alert
COV: Cell Over Voltage
BOT: Board Over Temperature
CUV: Cell Under Voltage
POV Pack Over Voltage
PUV: Pack Under Voltage
OCC2: Over Current Charge Tier 2
OCD2: Over Current Discharge Tier 2
OCC: Over Current Charge
OCD: Over Current Discharge
OTC: Over Temperature Charge
OTD: Over Temperature Discharge


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## A.3 Safety Status

The purpose of the Safety Status register is to see the status of most of the First Level Safety features. A bit set to 1 means the condition is active. A bit set to zero means the condition is not active.

| Safety Status | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| Name | HOCD | HOCC | HSC | EUV | HWDG | COV | BOT | CUV | POV | PUV | OCC2 | OCD2 | OCC | OCD | OTC | OTD |

HOCD: Hardware Over Current Discharge
HOCC: Hardware Over Current Charge
HSC: Hardware Short Circuit
EUV: Extreme Cell Under Voltage
HWDG: Host Watchdog Alert
COV: Cell Over Voltage
BOT: Board Over Temperature
CUV: Cell Under Voltage
POV Pack Over Voltage
PUV: Pack Under Voltage
OCC2: Over Current Charge Tier 2
OCD2: Over Current Discharge Tier 2
OCC: Over Current Charge
OCD: Over Current Discharge
OTC: Over Temperature Charge
OTD: Over Temperature Discharge

## A.4 Safety Alert1

The purpose of Safety Alert1 is to indicate that a particular threshold for a First Level Safety Rule has been exceeded but, the condition has not lasted long enough to latch and cause the Safety Rule to be active. A bit set to 1 means the alert condition is present. A bit set to zero means the condition is not present. The Alert bit stays latched while the safety feature is active and clears when the safety feature clears.

| Safety Alert1 | | | |
|---|---|---|---|
| Bit | 0 | 1 | 2–15 |
| Name | Reserved | DUT | RESERVED |

DUT: Discharge Under Temperature

## A.5 Safety Status1

The purpose of the Safety Status1 register is to see the status of the Discharge Under Temperature Safety Feature. A bit set to 1 means the condition is present. A bit set to zero means the condition is not present.

| Safety Status1 | | | |
|---|---|---|---|
| Bit | 0 | 1 | 2–15 |
| Name | Reserved | DUT | RESERVED |

DUT: Discharge Under Temperature


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## A.6 Permanent Disable Alert

The purpose of the Permanent Disable Alert is to indicate that the threshold for a particular Second Level Safety Rule has been exceeded but, the condition has not lasted long enough to latch and cause the Safety feature to be active. A bit set to 1 means the alert condition is present. A bit set to zero means the condition is not present. The Alert bit stays latched while the safety feature is active and clears when the safety feature clears.

| Permanent Disable Alert | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| Name | Reserved | SOV | SOTC | SOTD | CIM | CFETF | DFETF | OTS | CMF | VLAN | SOCC | SOCD | ROR | IGRR | IGR | FBF |

SOV: Secondary Over Voltage
SOTC: Secondary Over Temperature Charge
SOTD: Secondary Over Temperature Discharge
CIM: Cell Imbalance
CFETF: Charge FET Fail
DFETF: Discharge FET Fail
OTS: Open Temperature Sensor
CMF: Current Modulator Fail
VLAN: Virtual Local Area Network
SOCC: Secondary Over Current Charge
SOCD: Secondary Over Current Discharge
ROR: Cell Rate of Rise
IGRR: Impedance Growth Rate Ratio
IGR: Impedance Growth Rate
FBF: Fuse Blow Failure

## A.7 Permanent Disable Status

The purpose of the Permanent Disable Status is to see the status of the Second Level Safety Features. A bit set to 1 means the condition is active. A bit set to zero means the condition is not active.

| Permanent Disable Status | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| Name | Reserved | SOV | SOTC | SOTD | CIM | CFETF | DFETF | OTS | CMF | VLAN | SOCC | SOCD | ROR | IGRR | IGR | FBF |

SOV: Secondary Over Voltage
SOTC: Secondary Over Temperature Charge
SOTD: Secondary Over Temperature Discharge
CIM: Cell Imbalance
CFETF: Charge FET Fail
DFETF: Discharge FET Fail
OTS: Open Temperature Sensor
CMF: Current Modulator Fail
VLAN: Virtual Local Area Network
SOCC: Secondary Over Current Charge
SOCD: Secondary Over Current Discharge
ROR: Cell Rate of Rise
IGRR: Impedance Growth Rate Ratio
IGR: Impedance Growth Rate
FBF: Fuse Blow Failure


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## A.8 Charge Alert

The purpose of the Charge Alert is to indicate that thresholds for the Charge and Discharge Control feature have been exceeded but, the condition has not lasted long enough to latch and cause the feature to be active. A bit set to 1 means the alert condition is present. A bit set to zero means the condition is not present. The Alert bit stays latched while the Charge Control feature is active and clears when the Charge Control feature clears.

| Charge Alert | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 0–5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| Name | Reserved | CLST | CSHT | CILT | CIHT | PV | PT | CT | PTO | CC | DC |

CSLT: Charge Suspend Low Temperature
CSHT: Charge Suspend High Temperature
CILT: Charge Inhibit Low Temperatureer
CIHT: Charge Inhibit High Temperature
PV: Pre-Charge Voltage
PT: Pre-Charge Temperature
CT: Charge Timeout
PTO: Pre-Charge Timeout
CC: Charge Completion
DC: Discharge Completion

## A.9 Charge Status

The purpose of the Charge Status is to see the status of the Charge and Discharge Control features. A bit set to 1 means the condition is active. A bit set to zero means the condition is not active.

| Charge Status | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 0–5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| Name | Reserved | CLST | CSHT | CILT | CIHT | PV | PT | CT | PTO | CC | DC |

CSLT: Charge Suspend Low Temperature
CSHT: Charge Suspend High Temperature
CILT: Charge Inhibit Low Temperatureer
CIHT: Charge Inhibit High Temperature
PV: Pre-Charge Voltage
PT: Pre-Charge Temperature
CT: Charge Timeout
PTO: Pre-Charge Timeout
CC: Charge Completion
DC: Discharge Completion


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## A.10 Cell Status (1, 2, 3, 4, 5, 6–16)

The purpose of the Cell Status is to see the status each cell relating to PowerPump, Voltage and temperature extrema. A bit set to 1 means the condition is active. A bit set to zero means the condition is not active.

| Safety Alert | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6–15 |
| Name | North | South | OV | UV | OT | UT | Reserved |

North: Cell is Pumping North
South: Cell is Pumping South
OV: Cell is in an Over Voltage condition
UV: Cell is in an Under Voltage condition
OT: Cell is in an Over Temperature Condition
UT: Cell is in an Under Temperature Condition


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# bq78PL116 Default Parameter Set

The following table contains the default values for the bq78PL116 parameters. The bq78PL116 firmware download has a default configuration for three cells in series. It is the responsibility of the BMS Design engineer to ensure that the parameters are configured according to the desired pack configuration and cell manufacturer's requirements.

## B.1 bq78PL116 Default Parameters

| bq78PL116 Parameter | Units | Value |
|---|---|---|
| <SBData Static> | 1 | |
| Manufacturer Name | | TEXAS INSTRUMENTS |
| Device Name | | bq78PL116 |
| Device Chemistry | | LI ION 2400mAHrs |
| Manufacturer Data | | 0E4D616E20446174612020202020200000000000000000000000000000000000000000 |
| Serial Number | | 1 |
| Manufacture Date | | 0x3CFF |
| Design Voltage | mV | 10800 |
| Battery Mode | | 0x6001 |
| Remaining Time Alarm | Minutes | 10 |
| Remaining Capacity Alarm | mAh/10mWh | 480 |
| | | |
| <Charge Control> | 3 | |
| Pre-Charge Temperature | Kelvin | 273 |
| Pre-Charge Voltage | mV | 3000 |
| Pre-Charge Recovery | mV | 3100 |
| Pre-Charge Current | mA | 240 |
| Charge Inhibit Temperature Low | Kelvin | 273 |
| Charge Inhibit Temperature High | Kelvin | 318 |
| Charge Inhibit Recovery Temperature Low | Kelvin | 278 |
| Charge Inhibit Recovery Temperature High | Kelvin | 313 |
| Charge Suspend Temperature Low | Kelvin | 278 |
| Charge Suspend Recovery Temperature Low | Kelvin | 283 |
| Charge Suspend Temperature High | Kelvin | 333 |
| Charge Suspend Recovery Temperature High | Kelvin | 328 |
| Charge Completion Pack Voltage Qualifier | mV | 12300 |
| Charge Completion Taper Current Qualifier | mA | 120 |
| Charge Completion Time | Seconds RDTE | 4 |
| Charge Completion FET Activation Time | Seconds RDTE | 0 |
| Discharge Completion Pack Voltage Qualifier | mV | 9300 |
| Discharge Completion Time | Seconds RDTE | 4 |
| Discharge Completion FET Activation Time | Seconds RDTE | 0 |
| Discharge Under Temperature | Kelvin | 263 |
| Discharge Under Temperature Recovery | Kelvin | 273 |


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| bq78PL116 Parameter | Units | Value |
|---|---|---|
| Discharge Under Temperature Time | Seconds RDTE | 2 |
| FC Set SOC Threshold | % | -1 |
| FC Clear SOC Threshold | % | -1 |
| FD Set SOC Threshold | % | -1 |
| FD Clear SOC Threshold | % | -1 |
| FD Set Voltage | mV | 9300 |
| FD Clear Voltage | mV | 9600 |
| FD Set Voltage Time | Seconds | 0 |
| Transition to Idle Current | mA | 50 |
| Transition to Idle Time | Seconds | 30 |
| Transition to Discharge Current | mA | -75 |
| Transition to Charge Current | mA | 75 |
| Design Capacity mAh | mAHrs | 2400 |
| Design Capacity 10mWh | 10mWh | 2592 |
| TDA Set SOC Threshold | % | -1 |
| TDA Set Voltage Threshold | mV | 9600 |
| TDA Set Voltage Time | Seconds | 0 |
| TDA Clear SOC Threshold | % | -1 |
| TDA Clear Voltage | mV | 11100 |
| TCA Set SOC Threshold | % | -1 |
| TCA Clear SOC Threshold | % | -1 |
| OCA Set Voltage | mV | 12900 |
| OCA Activation Time | Seconds RDTE | 2 |
| | | |
| <Cell Balancing> | 5 | |
| Minimum Cell Differential For Balancing | mV | 10 |
| | | |
| <Cell Chemistry> | 6 | |
| Chemistry ID | | 107 |
| FCC Learn Qualifier | % | 30 |
| Cycle Fade | % | 0.05 |
| Min OCV Slope | mV/% RSOC | 2 |
| OCV Idle Qualifier | Minutes | 60 |
| Stale FCC Timeout | Minutes | 2880 |
| Default Charging Voltage | mV | 12600 |
| Default Charging Current | mA | 1680 |
| Capacity Algorithm | | 0x0003 |
| User Rate | mA | 480 |
| | | |
| <Pack Configuration> | 7 | |
| Hardware Configuration | | 0x0731 |
| Algorithm Enable | | 0x8006 |
| System Control | | 0x8000 |
| EPD Pump Time | Cycle Counts | 120 |
| EPD Write Time | Cycle Counts | 70 |
| Display Driver Frequency | Hz | 30 |
| Product Sub ID | | 0 |
| Current Delta | mA | 100 |
| | | |
| <Safety Level 1> | 8 | |
| COV Threshold | mV | 4250 |
| COV Recovery | mV | 4100 |


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| bq78PL116 Parameter | Units | Value |
|---|---|---|
| COV High Temperature Threshold | mV | 4250 |
| COV High Temperature Adjust | Kelvin | 323 |
| COV Time | Seconds | 2 |
| CUV Threshold | mV | 2900 |
| CUV Recovery | mV | 3100 |
| CUV Time | Seconds | 1 |
| POV Threshold | mV | 12750 |
| POV Recovery | mV | 12300 |
| POV Time | Seconds | 2 |
| PUV Threshold | mV | 8400 |
| PUV Recovery | mV | 9300 |
| PUV Time | Seconds | 2 |
| EUV Threshold | mV | 2500 |
| EUV Time | Seconds | 2 |
| EUV Recovery | mV | 2900 |
| OC Charge Tier 1 Threshold | mA | 4800 |
| OC Charge Tier 1 Recovery | Seconds | 6 |
| OC Charge Tier 1 Time | Seconds | 2 |
| OC Discharge Tier 1 Threshold | mA | -7200 |
| OC Discharge Tier 1 Recovery | Seconds | 6 |
| OC Discharge Tier 1 Time | Seconds | 2 |
| OC Charge Tier 2 Threshold | mA | 5200 |
| OC Charge Tier 2 Recovery | Seconds | 8 |
| OC Charge Tier 2 Time | Seconds | 2 |
| OC Discharge Tier 2 Threshold | mA | -9600 |
| OC Discharge Tier 2 Recovery | Seconds | 10 |
| OC Discharge Tier 2 Time | Seconds | 1 |
| OC Max Attempts | | 3 |
| Hardware OC Charge Threshold | | 211 |
| Hardware OC Charge Recovery | Seconds | 10 |
| Hardware OC Charge Time | Count | 60 |
| Hardware OC Discharge Threshold | | 98 |
| Hardware OC Discharge Recovery | Seconds | 10 |
| Hardware OC Discharge Time | Count | 37 |
| HOC Max Attempts | | 3 |
| Hardware Short Circuit Threshold | | 47 |
| Hardware Short Circuit Recovery | Seconds | 10 |
| Hardware Short Circuit Time | Count | 3 |
| HSC Max Attempts | | 3 |
| OT Charge Threshold | Kelvin | 323 |
| OT Charge Recovery | Kelvin | 318 |
| OT Charge Time | Seconds RDTE | 2 |
| OT Discharge Threshold | Kelvin | 333 |
| OT Discharge Recovery | Kelvin | 323 |
| OT Discharge Time | Seconds RDTE | 2 |
| Board Over Temperature | Kelvin | 358 |
| Board Over Temperature Recovery | Kelvin | 338 |
| Board Over Temperature Time | Seconds RDTE | 2 |
| Hardware LP Discharge Threshold | | 32 |


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| bq78PL116 Parameter | Units | Value |
|---|---|---|
| Hardware LP Discharge Duration | | 127 |
| Hardware LP Charge Threshold | | 220 |
| Hardware LP Charge Duration | | 127 |
| Host Watchdog Timeout | Seconds RDTE | 0 |
| | | |
| <Safety Level 2> | 9 | |
| SOV Threshold | mV | 4350 |
| SOV Time | Seconds RDTE | 8 |
| Cell Imbalance Current | mA | 50 |
| Cell Imbalance Fail Voltage | mV | 500 |
| Cell Imbalance Time | Seconds | 180 |
| Cell Imbalance SOC Inhibit Threshold | % | 30 |
| SOC Charge Threshold | mA | 6000 |
| SOC Charge Time | Seconds RDTE | 2 |
| SOC Discharge Threshold | mA | -12000 |
| SOC Discharge Time | Seconds RDTE | 2 |
| SOT Charge Threshold | Kelvin | 343 |
| SOT Charge Time | Seconds RDTE | 2 |
| SOT Discharge Threshold | Kelvin | 343 |
| SOT Discharge Time | Seconds RDTE | 2 |
| Open Temperature Sensor Threshold | Kelvin | 233 |
| Open Temperature Sensor Time | Seconds RDTE | 2 |
| FET Fail Time | Seconds RDTE | 2 |
| Fuse Fail Limit | mA | 50 |
| Fuse Fail Time | Seconds RDTE | 0 |
| VLAN Fail Time | Seconds RDTE | 4 |
| Current Measurement Fail Time | Seconds RDTE | 10 |
| Pre-Charge Voltage Timeout | Seconds RDTE | 900 |
| Charge Duration Timeout | Seconds RDTE | 14400 |
| IGR Limit | | 200 |
| IGR Fail Count | | 0 |
| IGR Ratio Limit | | 120 |
| IGR Ratio Fail Count | | 255 |
| Rate Limit Threshold | | 200 |
| Rate Limit Activation Count | | 0 |


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# Glossary

| | |
|---|---|
| ADC | Analog-to-digital converter |
| Alert | A warning set by the bq78PL116 |
| Bit | A single binary digit in an SBS command or data-flash value which can be changed by the user |
| CC | Constant current (may also indicate coulomb counting) |
| CHG FET | Charge FET |
| COV | Cell overvoltage |
| CV | Constant voltage |
| CUV | Cell undervoltage |
| DSG FET | Discharge FET, connected to the DSG pin; used to enable or disable discharging |
| EFCI | External FET control input – allows control of pack-protection MOSFETs |
| FC | Fully charged |
| FD | Fully discharged |
| Flag | A single bit in an SBS command or data-flash value which is set by the bq78PL116 and indicates a status change |
| LED | Light-emitting diode |
| Li-Ion | Lithium-ion |
| NDI | Normalized dynamic impedance. This is the dynamic impedance due to a step change in current and voltage (ΔV/ΔI), normalized to a fixed reference temperature. |
| OC | Overcurrent |
| OCA | Overcharge alarm |
| OCV | Open-circuit voltage |
| PEC | Packet error checking |
| POV | Pack overvoltage |
| PRES | System-present flag |
| PUV | Pack undervoltage |
| Qmax | Maximum chemical capacity |
| RCA | Remaining Capacity Alarm |
| RDTE | Round down to even; the time value is an integral multiple of two seconds. |
| ROR | Rate of rise |
| RSOC | Relative state-of-charge |
| SBS | Smart battery system |
| SMBus | System-management bus |
| SOC | Safety overcurrent |
| SOC | State of charge |
| SOT | Safety overtemperature |
| TCA | Terminate charge alarm |
| TDA | Terminate discharge alarm |


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