Texas Instruments

# 48 V to 3.3 V Forward Converter with Active Clamp Reset Using the UCC2897 Active Clamp Current Mode PWM Controller

Reference Design

# Reference Design PR265A 48V to 3.3V Forward Converter with Active Clamp Reset Using the UCC2897 Active Clamp Current Mode PWM Controller

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## 1 Introduction

The UCC2897 reference design is an active clamp reset forward converter providing a 3.3-V regulated output at 30 A of load current, operating from a 48-V input. The design operates over the entire 36-V to 72-V telecom input range, and is able to fully regulate down to zero load current. The module uses the UCC2897 current mode active clamp PWM controller for effectively demonstrating the active clamp transformer reset technique.

Benefits of the active clamp include a control driven transformer reset scheme allowing zero voltage switching (ZVS) to increase overall efficiency, lower drain-to-source voltage stress, extended duty cycle beyond 50% and reduced electromagnetic radiated emissions. Combined with synchronous rectification, the design operates at 250 kHz and exhibits a peak efficiency of 93%, with a full load efficiency of over 91%. The design displays many features that might be typical of a more complex design, yet its compact board layout and low component count make it elegantly simple.

## 2 Description

The UCC2897 controller provides advanced active clamp control features such as programmable maximum duty cycle clamp, programmable dead time between the two primary switches and the ability to drive either a P-channel, or N-channel MOSFET in either a high-side or low-side active clamp configuration. The UCC2897 also allows the ability to start-up directly from the 48-V telecom bus voltage, eliminating the need for external start-up circuitry. It includes programmable soft-start, internal slope compensation for peak current-mode control, internal low-line and high-line voltage sensing, internal bidirectional syncronizable clock input, cycle-by-cycle current limiting and short-circuit current protection, and a robust 2-A sink/source TrueDrive™ internal gate drive circuit. The result is a highly efficient design loaded with features, requiring very few external components.

The TrueDrive™ output architecture of UCC2897 uses TI's unique TrueDrive™ Bipolar/CMOS hybrid output technology. To the user, this simply means ultra-fast rise and fall times by providing the highest possible drive current where it is needed most, at the MOSFET Miller plateau region.

The UCC2897 is available in a 20-pin TSSOP package for applications where absolute minimal board space is required.

This UCC2897 reference design highlights the many benefits of using the UCC2897 active clamp current mode PWM controller. This document provides the schematic, component list, assembly drawing, artwork and test set up necessary to evaluate the UCC2897 in a typical telecom application. More detailed design information can be found in references[1] and [2].

## 2.1 Applications

The UCC2897 is designed to be used in isolated telecom 48-V input systems requiring high efficiency and high power density for very-low-output voltage, high current converter applications, including:

- Server Systems
- Datacom
- Telecom
- DSPs, ASICs, FPGAs

## 2.2 Features

- ZVS transformer reset using active clamp technique in forward converter
- All surface mount components, double sided half brick (2.2”x2.28”x0.5”)
- Low−side active clamp with programmable dead time for ZVS
- Current Mode Control with bi−directional sync function
- Internal PWM slope compensation
- Start up directly from telecom input voltage
- Synchronous rectifier output stage allows high efficiency operation
- Programmable soft start
- Up to 30Adc output current
- Regulation to zero load current
- Non−latching, cycle by cycle over−current and short circuit protection
- Non−latching, Input under−voltage protection
- Non−latching, Input over−voltage protection
- 1500-V isolation primary to secondary

# 3 UCC2897 Reference Design Electrical Performance Specifications

The UCC2897 reference design electrical perofmance specifications are listed in Table 1.

**Table 1. Performance Specification Summary**

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Input voltage range | | | 36 | 48 | 72 | V |
| No load input current | $V_{IN}$ = 36 V, | $I_{OUT}$ = 0 A | | 75 | 100 | mA |
| Input undervoltage limit | | | | 35 | | V |
| Input overvoltage limit | | | | 73 | | |
| Maximum input current | $V_{IN}$ = 36 V, | $I_{OUT}$ = 30 A | | 3.00 | 3.25 | A |
| Input voltage ripple | $V_{IN}$ = 72 V, | $I_{OUT}$ = 30 A | | 1.50 | 1.75 | $V_{P-P}$ |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output voltage | 36 V < $V_{IN}$ < 72 V, | 0 A < $I_{OUT}$ < 30 A | 3.25 | 3.30 | 3.35 | V |
| Output voltage regulation | Line regulation<br>$I_{OUT}$ = 0 A | 36 V < $V_{IN}$ < 72 V | | 0.003% | 0.01% | |
| | Load regulation<br>0 A < $I_{OUT}$ < 30 A | $V_{IN}$ = 48 V | | 0.06% | 0.1% | |
| Output voltage ripple | $V_{IN}$ = 48 V, | $I_{OUT}$ = 30 A | | 30 | 35 | $mV_{P-P}$ |
| Output load current | 36 V < $V_{IN}$ < 72 V | | 0 | | 30 | A |
| Output current limit | | | | 32 | | |
| **CONTROL LOOP CHARACTERISTICS** | | | | | | |
| Switching frequency | | | 225 | 250 | 265 | kHz |
| Control loop bandwidth | 36 V < $V_{IN}$ < 72 V, | $I_{OUT}$ = 10 A | 5 | | 7 | |
| Phase margin | | | 50 | | 60 | ° |
| Peak efficiency | $V_{IN}$ = 36 V | | | 93% | | |
| Full load efficiency | $V_{IN}$ = 48 V, | $I_{OUT}$ = 30 A | | 91% | | |

# 4 PR265A Schematic

A schematic of the UCC2897 reference design is shown in Figure 1. Terminal block J1 is the 48-V input voltage source connector and terminal block J8 is the output and return for the 3.3-V output voltage.

On the primary side, U1 is the UCC2897 shown with the necessary discrete circuitry for setting up the controller to operate at 250 kHz with the maximum duty clamp set for 0.65. The design is programmed to start at $V_{IN}$=36 V, as determined by R11 and R12 and shut down at $V_{IN}$=73 V, as determined by R30 and R31. To minimize power dissipation in the current sense, a current-sense transformer, T1 is used. Q2 is the primary switching MOSFET and is selected based upon $V_{DS}$ and low $R_{DS(on)}$. Q1 is the AUX (active reset) MOSFET and is selected based upon preferred package only, with only minor consideration given for $R_{DS(on)}$ and $Q_G$. Since the active clamp used in this design is low-side referenced, Q1 must be a P-channel type MOSFET. Finally, C9 is the clamp capacitor ($C_{CL}$) used to maintain a constant dc voltage. The input voltage is subtracted from the clamp voltage to allow transformer reset during the active clamp period.

High efficiency is achieved using self-driven synchronous rectification on the secondary side. Q3 and Q4 are placed in parallel and make up the forward synchronous rectifier (SR), while the reverse SR is made up of the parallel combination of Q5 and Q7. The PCB is able to accommodate a third parallel reverse SR, which may be needed if the frequency is increased beyond 250 kHz or if the load current is increased beyond 30 A. The output inductor L1 has a coupled secondary, referenced to the primary side, used to provide bootstrapping voltage to U1. A stable bias for the optocoupler, U2 is provided by the series pass regulator made up of D6, Q6 and some associated filtering. Additional soft start circuitry for the secondary is available through C21, R33, R34, R35 and Q9. This simple circuit helps to control the output voltage at start up, only until D7 and its associated circuitry are in steady state operation.

Scope jacks J2 and J3 allow the user to measure the gate-to-source and drain-to-source signals for Q2, the primary MOSFET. J4 and J5 allow convenient access to the gate drive signals of each SR on the secondary side. J6 and J7 are available allowing the option of using a network analyzer to non−invasively measure the control to output loop gain and phase.

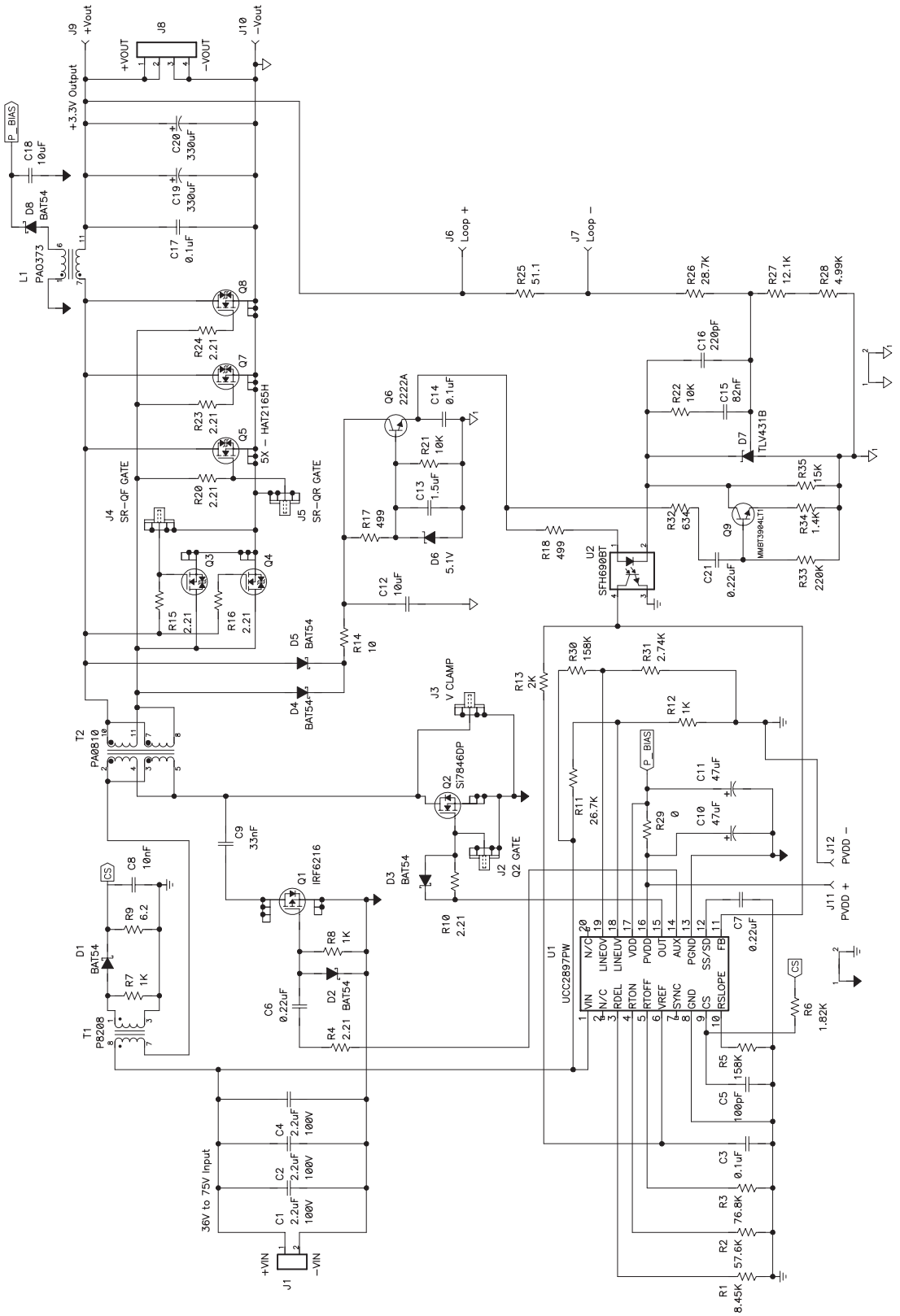


**Figure 1. PR265A Schematic**

# 5 Test Set Up

Figure 2 shows the basic test set up recommended to evaluate the UCC2897 reference design.

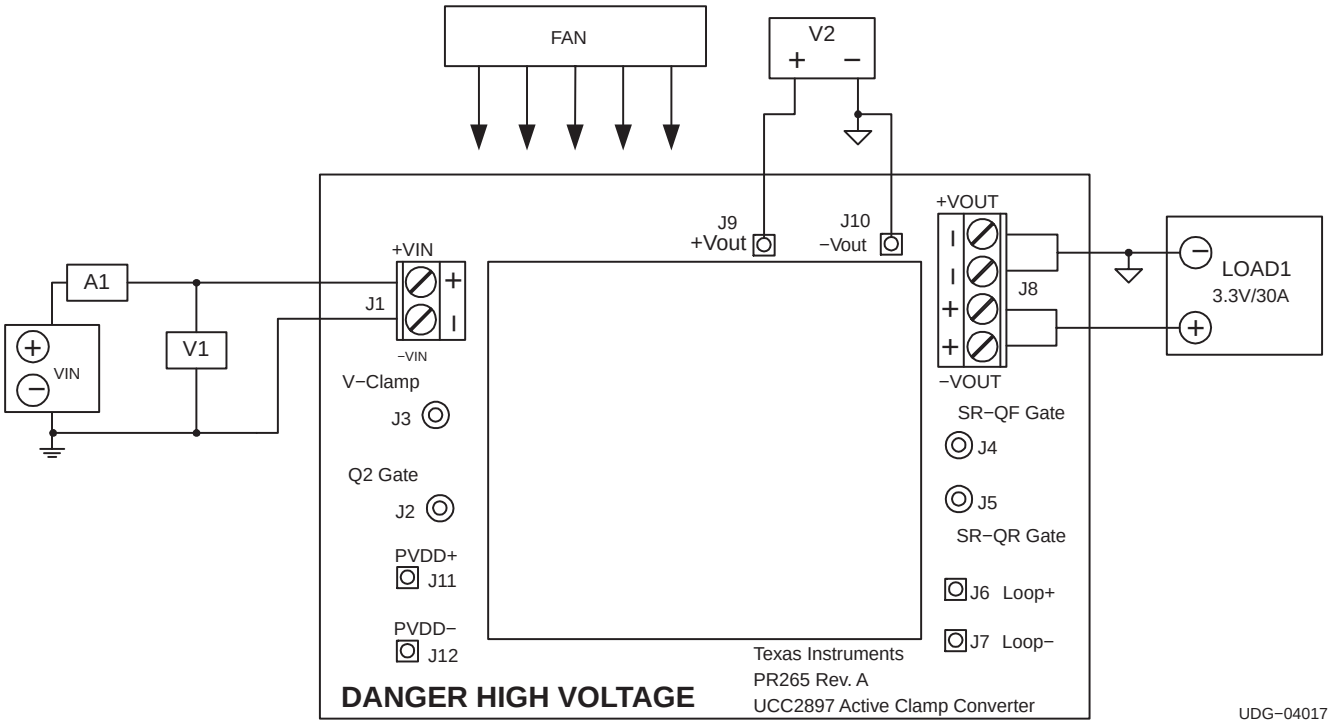


**Figure 2. PR265A Recommended Test Setup**

## 5.1 Output Load (LOAD1)

For the output load to $V_{OUT}$, a programmable electronic load set to constant current mode and capable of sinking 0 to 30 Adc, shall be used. For convenience, $V_{OUT}$ can be monitored by connecting a dc voltmeter, V2, to J9 and J10. For highest accuracy, such as gathering efficiency data, $V_{OUT}$ should be measured directly across the output capacitor.

## 5.2 DC Input Source ($V_{IN}$)

The input voltage shall be a variable DC source capable of supplying between 0 Vdc and 75 Vdc at no less than 3.5 Adc, and connected to J1 and A1 as shown in figure 2. For fault protection to the unit, good common practice is to limit the source current to no more than 3.5 Adc for a 36 V input. A dc ammeter, A1 should also be inserted between $V_{IN}$ and J1 as shown in Figure 2. For highest accuracy, such as gathering efficiency data, $V_{IN}$ should be measured directly across the input capacitor.

## 5.3 Recommended Wire Gauge

The connection between the source voltage, $V_{IN}$ and J1 can carry as much as 3.25 Adc. The minimum recommended wire size is AWG #20 with the total length of wire less than 8 feet (4 feet input, 4 feet return). The connection between J8 and LOAD1 can carry as much as 30 Adc. The minimum recommended wire size is AWG #16, with the total length of wire less than 8 feet (4 feet output, 4 feet return).

### 5.4 External PVDD DC Power Supply (Optional)

The design allows for separate VDD and PVDD, allowing the gate drive voltage amplitude to be separately biased from the rest of the device. By removing R29, the gate drive voltage for Q1 and Q2 can be derived from an external dc power supply applied to J11 and J12. Be cautious not to exceed the maximum gate-to-source voltage rating ($V_{GS(max)}$ = 20 V) of Q1 and Q2. Do not connect an external dc power supply to J11 and J12 when R29 is installed.

### 5.5 Network Analyzer (Optional)

A network analyzer can be connected directly to J6 and J7. The UCC2897 reference design provides a 51.1 resistor (R25) between the output and the voltage feedback to allow easy non-invasive measurement of the control to output loop response.

### 5.6 Fan

Most power converters include components that can be hot to the touch when approaching temperatures of 60°C. Because this design is not enclosed to allow probing of circuit nodes, a small fan capable of 200 to 400 LFM is recommended to reduce component temperatures when operating at or above 50% maximum rated load current.

## 6 Power Up/Down Test Procedure

The following test procedure is recommended primarily for power up and shutting down the reference design board. Whenever the unit is running above an output load of 15  Adc, the fan should be turned on.

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the unit. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the dc input source, $V_{IN}$, it is advisable to limit the source current from $V_{IN}$ to 5 A maximum. Make sure $V_{IN}$ is initially set to 0 V and connected to J1 as shown in Figure 2.
3. Connect the ammeter A1 (0 A to 10 A range) between $V_{IN}$ and J1 as shown in Figure 2.
4. Connect voltmeter (can optionally use voltmeter from $V_{IN}$ source if available), V1 across J1 as shown in Figure 2.
5. Connect LOAD1 to J8 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0 Adc before $V_{IN}$ is applied.
6. Connect voltmeter, V2 across J9 and J10 as shown in Figure 2.
7. Increase $V_{IN}$ from 0 V to 36 Vdc.
8. Observe that $V_{OUT}$ is regulating when $V_{IN}$ is at 36 V.
9. Increase $V_{IN}$ to 48 V.
10. Increase LOAD1 from 0 A to 15 Adc.
11. Turn on fan making sure to blow air directly on the unit.
12. Increase LOAD1 from 15 Adc to 30 Adc.
13. Decrease LOAD1 to 0 A.
14. Decrease $V_{IN}$ from 48 Vdc to 0 V.
15. Shut down $V_{IN}$.

# 7 UCC2897 Reference Design Performance Data

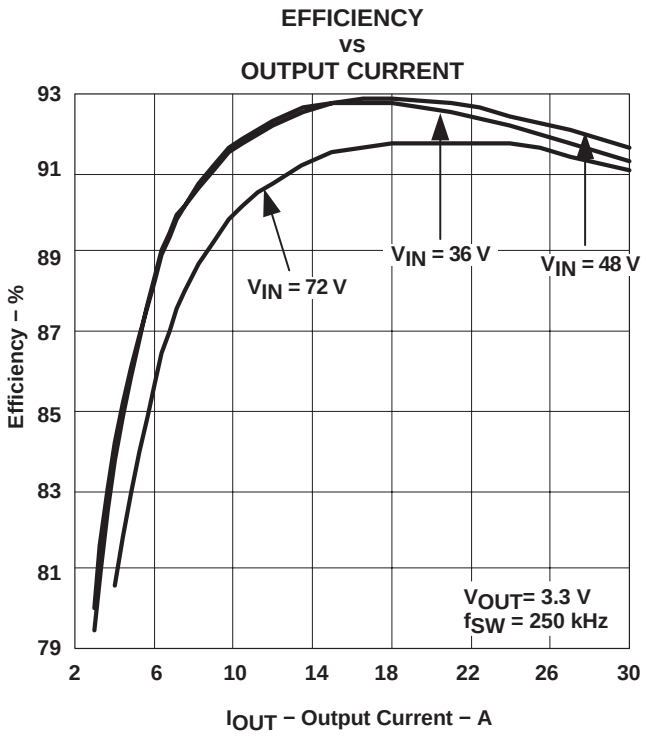


**Figure 3**

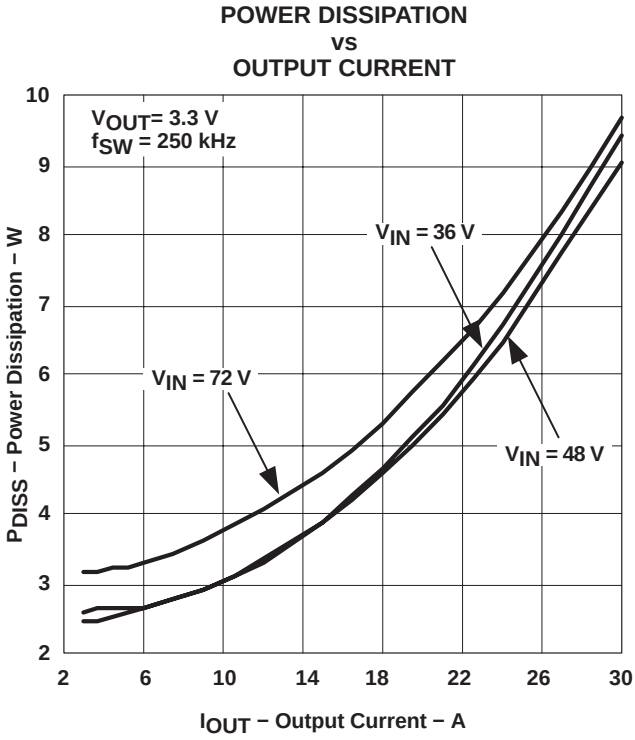


**Figure 4**

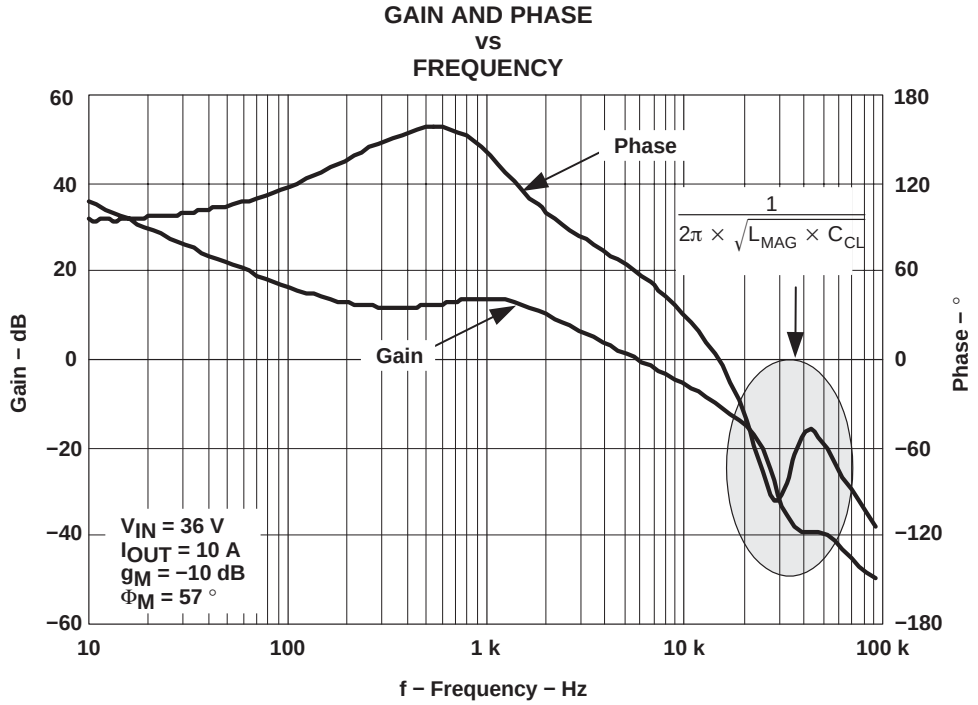


**Figure 5. Control Loop**

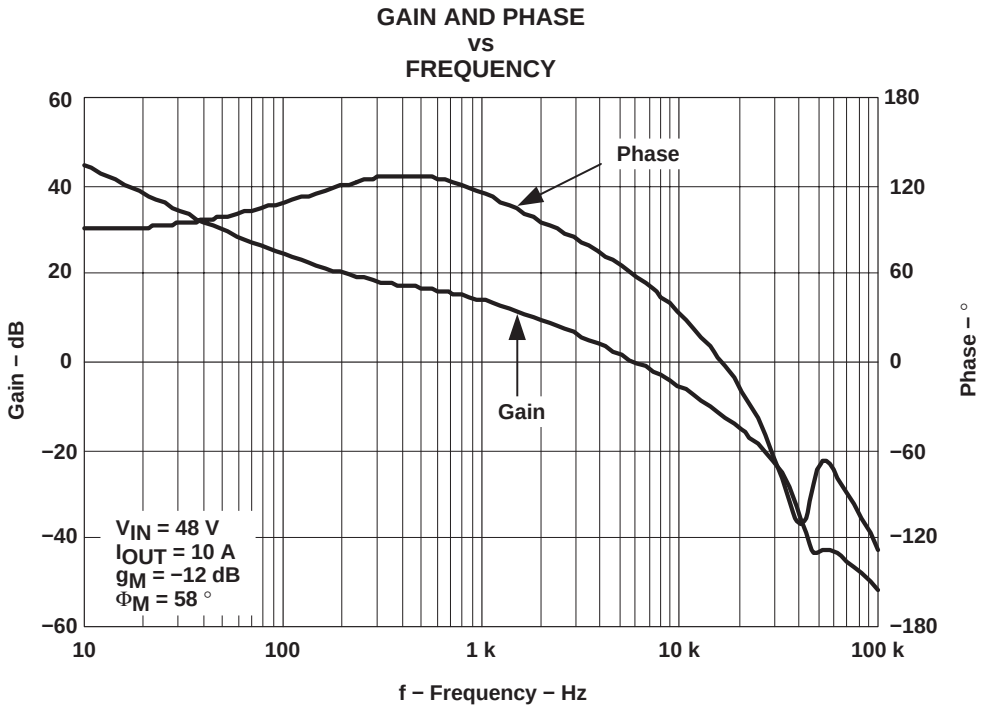


**Figure 6. Control Loop**

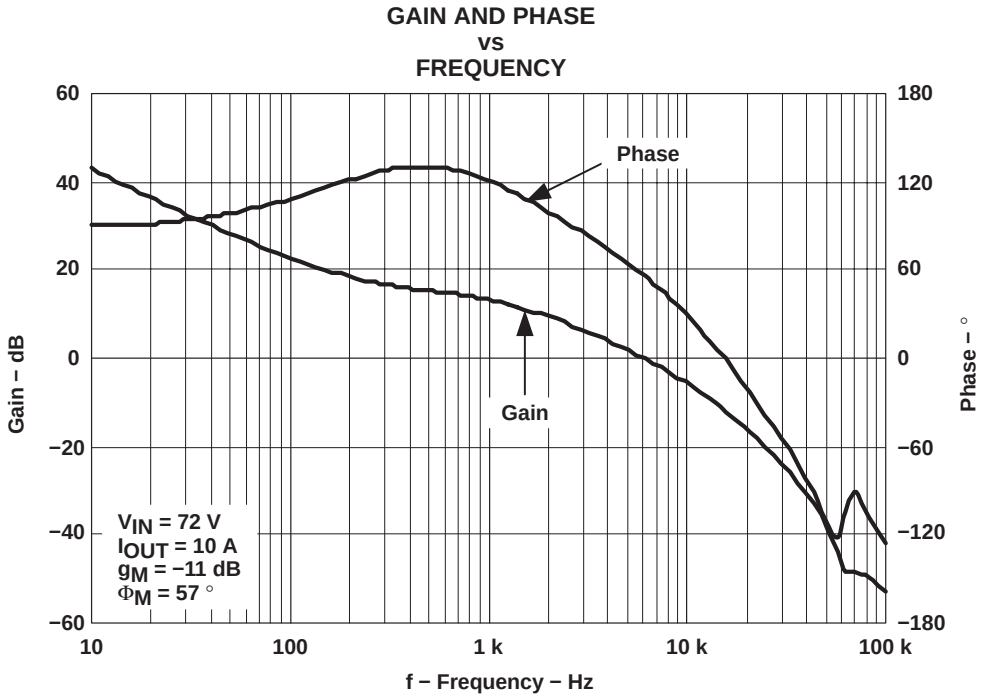


**Figure 7. Control Loop**

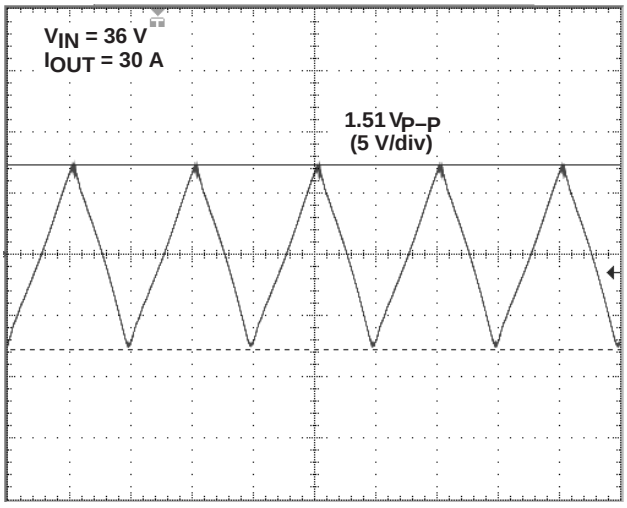


**Figure 8. Input Ripple Voltage**

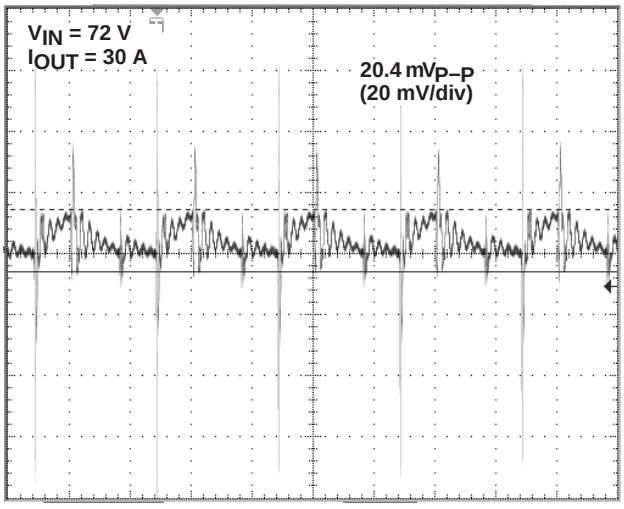


**Figure 9. Output Ripple Voltage**

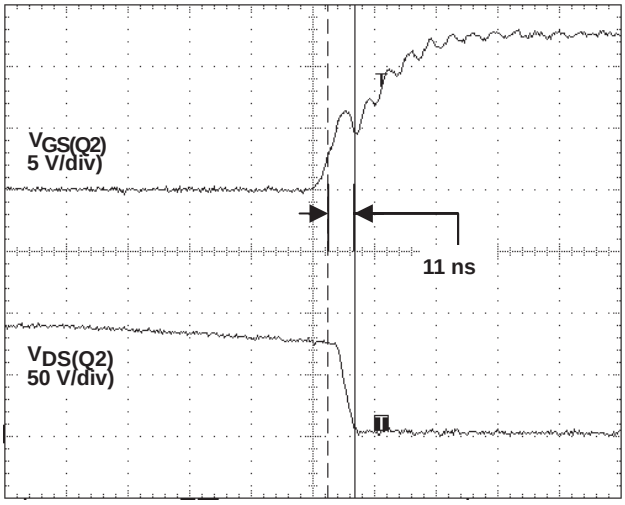


**Figure 10. Main FET (Q2) Turn-On**

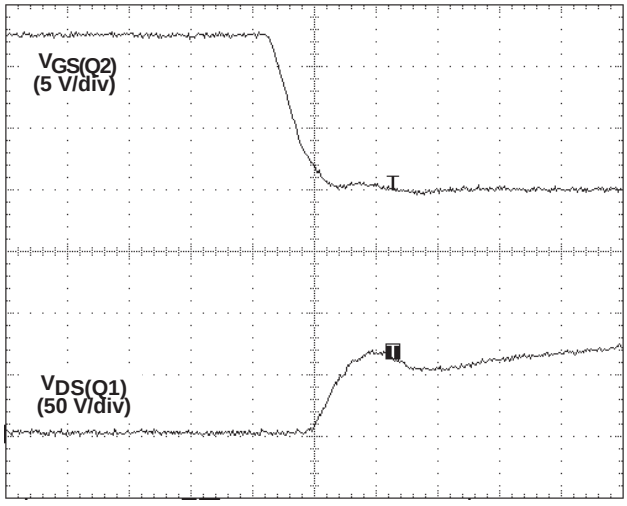


**Figure 11. Main FET (Q2) Turn-Off**

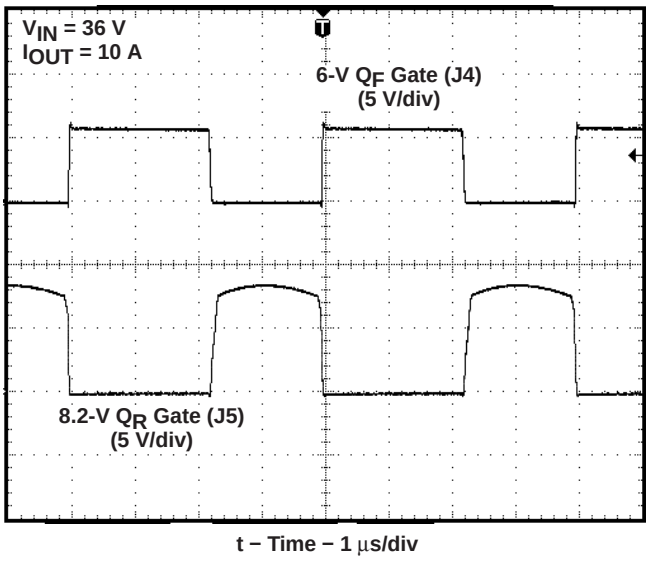


Figure 12. SR Gate Drive

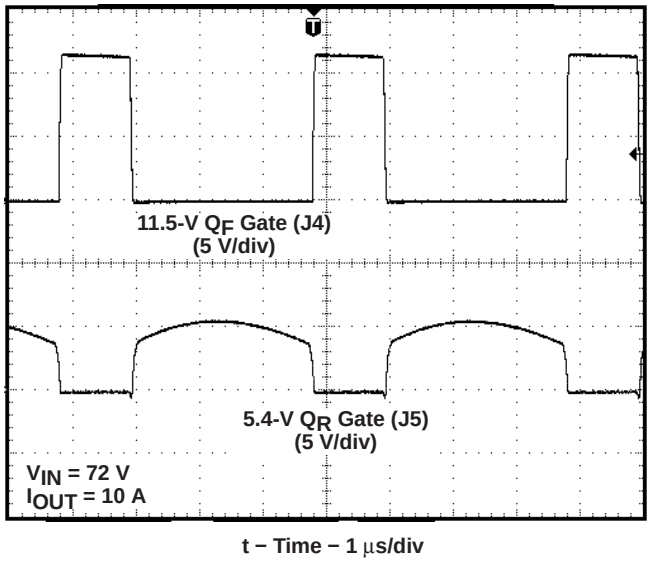


Figure 13. SR Gate Drive

# 8 Suggested Design Improvements

Once the design was built and tested, several areas of improvement were noticed and have been noted below. Component reference designations in the following notes refer to the schematic of Figure 1.

## 8.1 Main MOSFET ZVS

In Figure 10, the main MOSFET, Q2 is shown not to turn-on at zero voltage as indicated by the 11-ns overlap between $V_{GS}$ and $V_{DS}$. Increasing the delay time, adding an external inductor in series with the transformer primary and adding a saturable reactor in series with the transformer secondary each had no effect on moving the turn-on voltage closer to ZVS. It is believed that the forward synchronous MOSFET (Q3, Q4) is conducting for a portion of the dead-time period when ZVS should be occurring. During the set delay period, the resonant energy is circulating through the transformer primary. If the secondary is energized for even a brief portion of the ZVS period, then the stored resonant inductive energy necessary for discharging the resonant capacitance will be lost as it is inadvertently coupled to the secondary. This seems to be a natural consequence of using self driven SR in the active clamp forward converter. A possible design improvement might be to drive both synchronous rectifiers with a control driven solution instead of a transformer driven approach. Decreasing the transformer primary magnitizing inductance may also help Q2 ZVS.

## 8.2 Soft-Start of $V_{OUT}$

The output voltage is found to overshoot during initial turn-on only. When power is initially transferred from the primary to the secondary, there is a brief period of time required for the converter secondary side to charge the optocoupler biasing circuitry and TLV431 feedback circuitry. During this time the converter output starts to rise, but since the TLV431 can only sink current, the PWM is not yet receiving any feedback voltage from the secondary. For low output voltage designs this is a problem since the converter output rises quickly to the regulation point (and beyond) before the feedback circuitry is fully operational. To prevent this overshoot it is necessary to control the rate of rise of the output from the secondary side as well as through the primary side soft start. Start-up performance is improved when the feedback circuitry is pre-biased, but this requires a dedicated secondary-side voltage level that must be regulating prior to the UCC2891 converter. The TLV431 is a popular choice for feedback compensation, but it may not be the best choice for low voltage converters. Another better approach is to use an operational amplifier with a precision voltage reference. This solution would outperform the TLV431 because the error amplifier can now source current necessary to drive the optocoupler. Improved secondary side control during start-up is another advantage since the rise rate of the reference voltage could also be independently controlled.

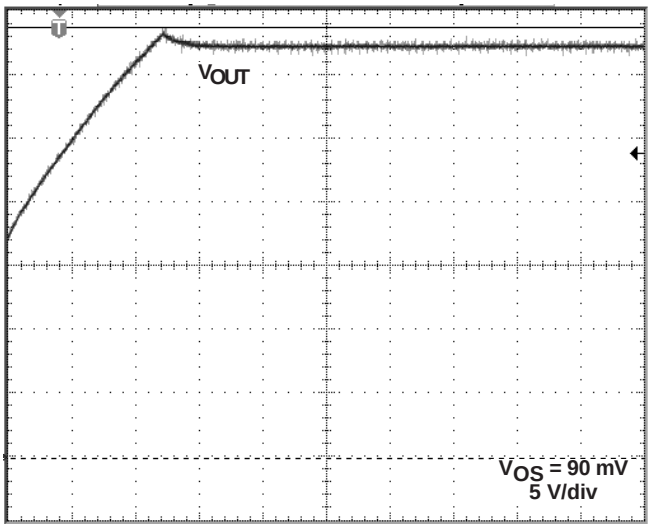


**Figure 14. $V_{OUT}$ Start-Up Overshoot**

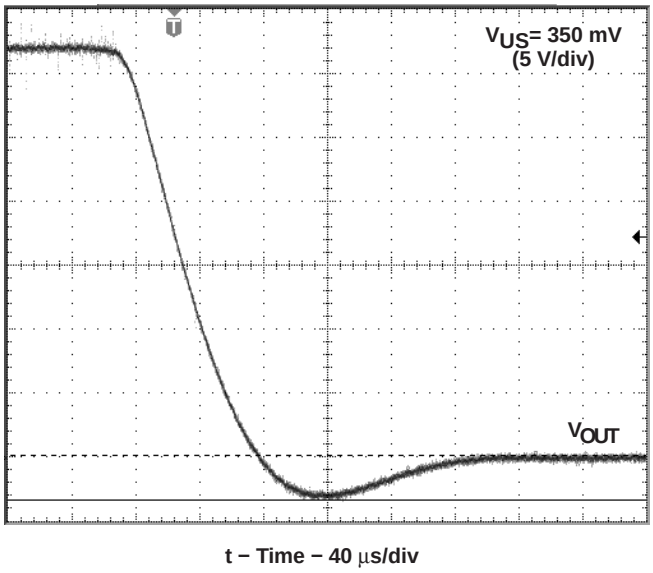


**Figure 15. $V_{OUT}$ Shut-Down Undershoot**

# 9 PR265A Assembly Drawing and Layout

Figure 17 through Figure 23 show the top and bottom-side component placement, as well as device pin numbers where necessary. A four-layer PCB was designed using the top and bottom layers for signal traces and component placement along with an internal ground plane. The PCB dimensions are 3.6″ x 2.7″ with a design goal of fitting all components within the industry standard half-brick format, as outlined by the box dimensions 2.28″ x 2.20″ shown in Figure 18. All components are standard OTS surface mount components placed on the both sides of the PCB. The copper-etch for each layer is also shown.

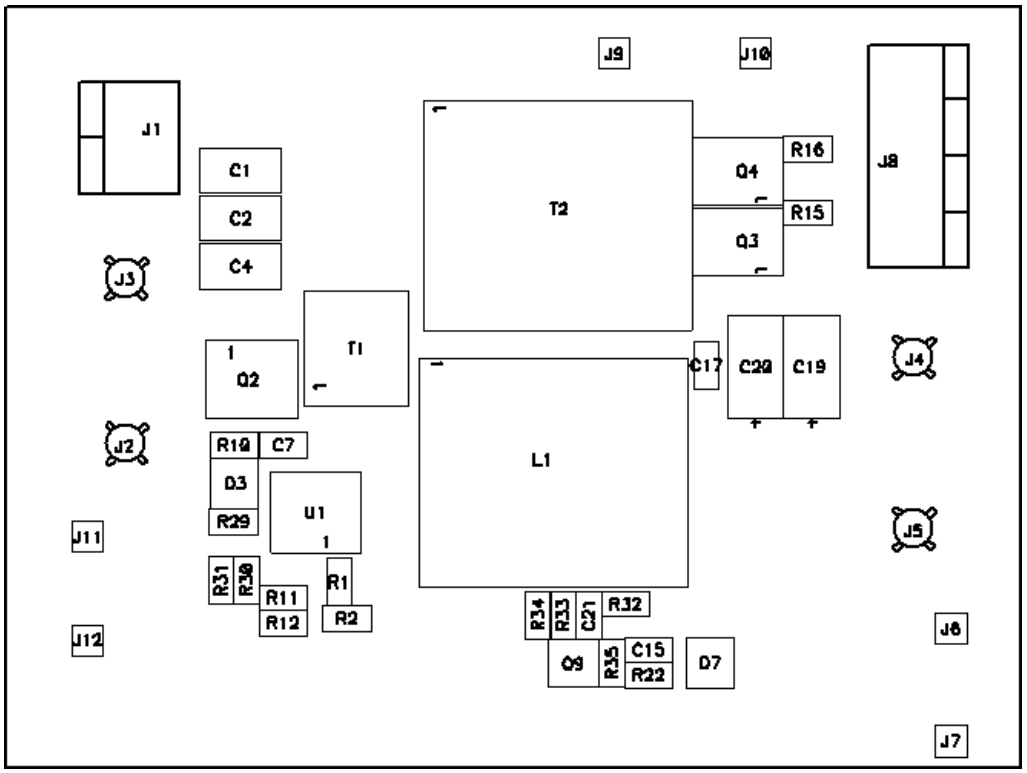


**Figure 16. Top Side Component Assembly**

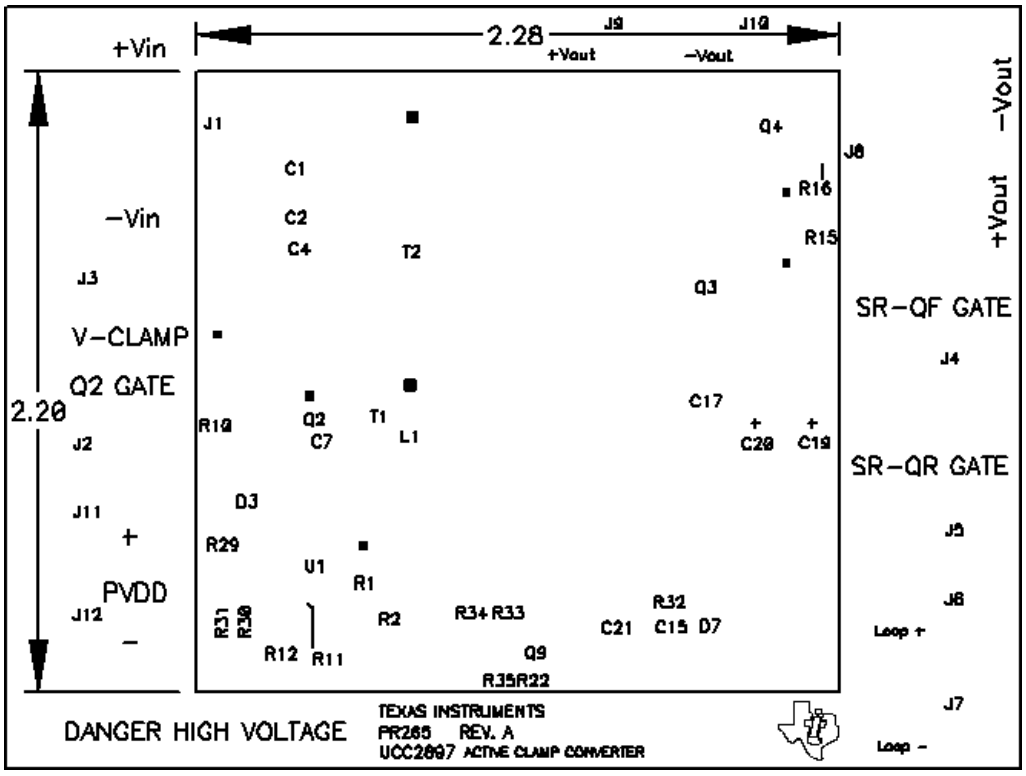


**Figure 17. Top Side Silk Screen**

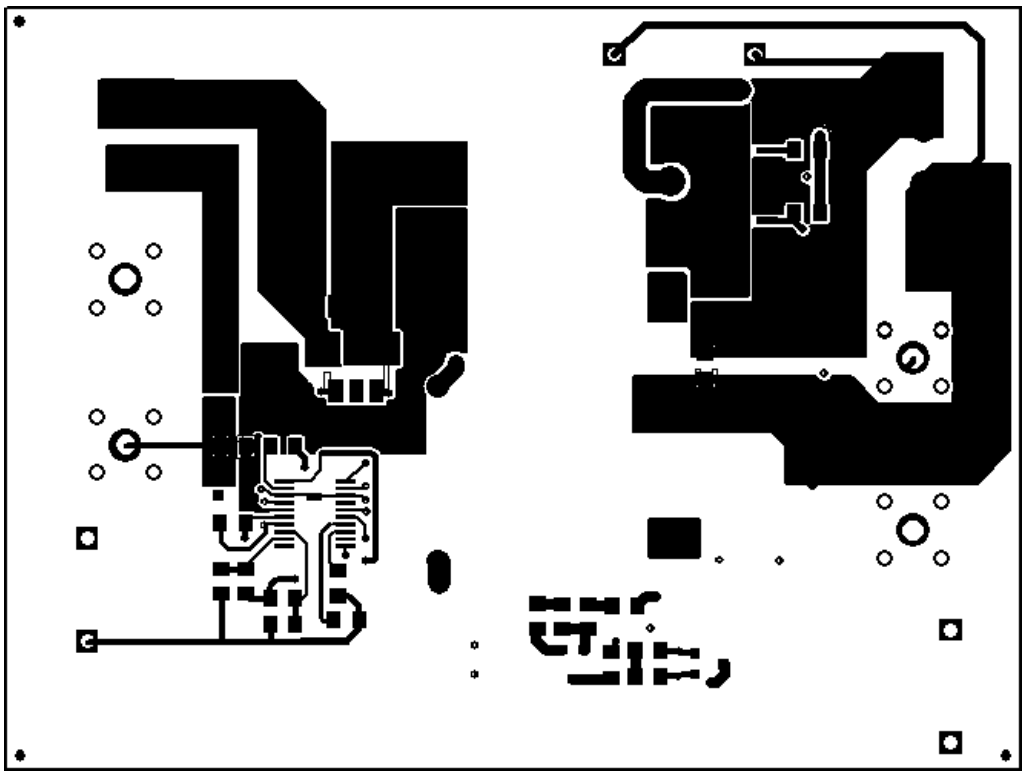

**Figure 18. Top Signal Trace Layer**

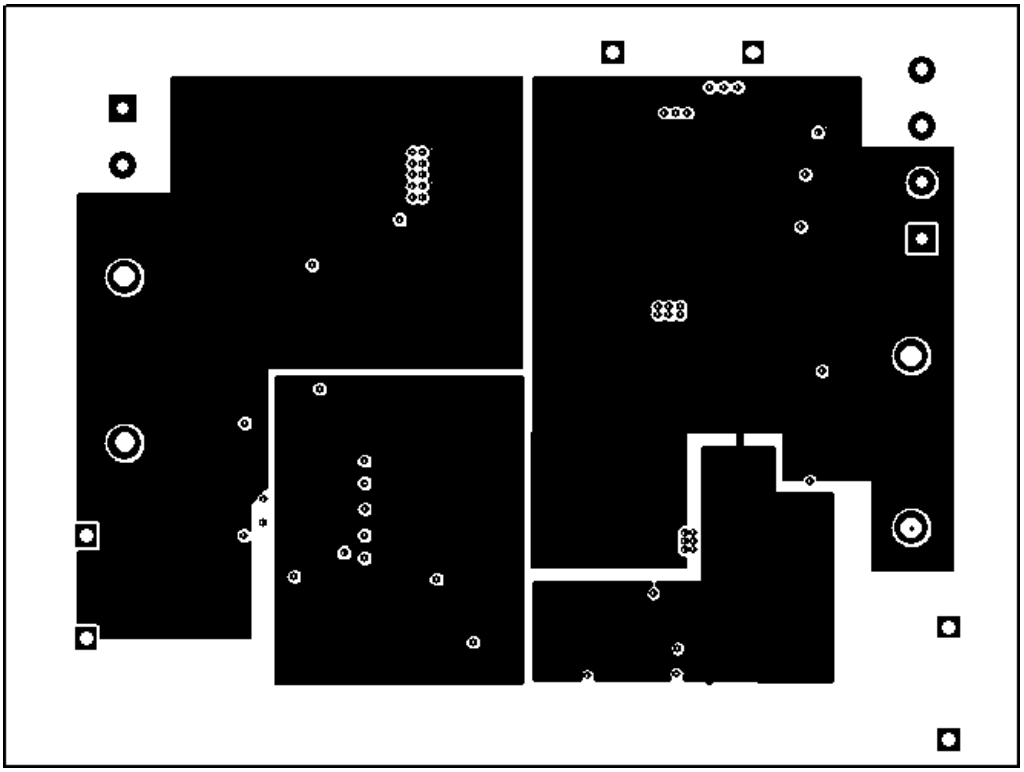

**Figure 19. Internal Split Ground Plane**

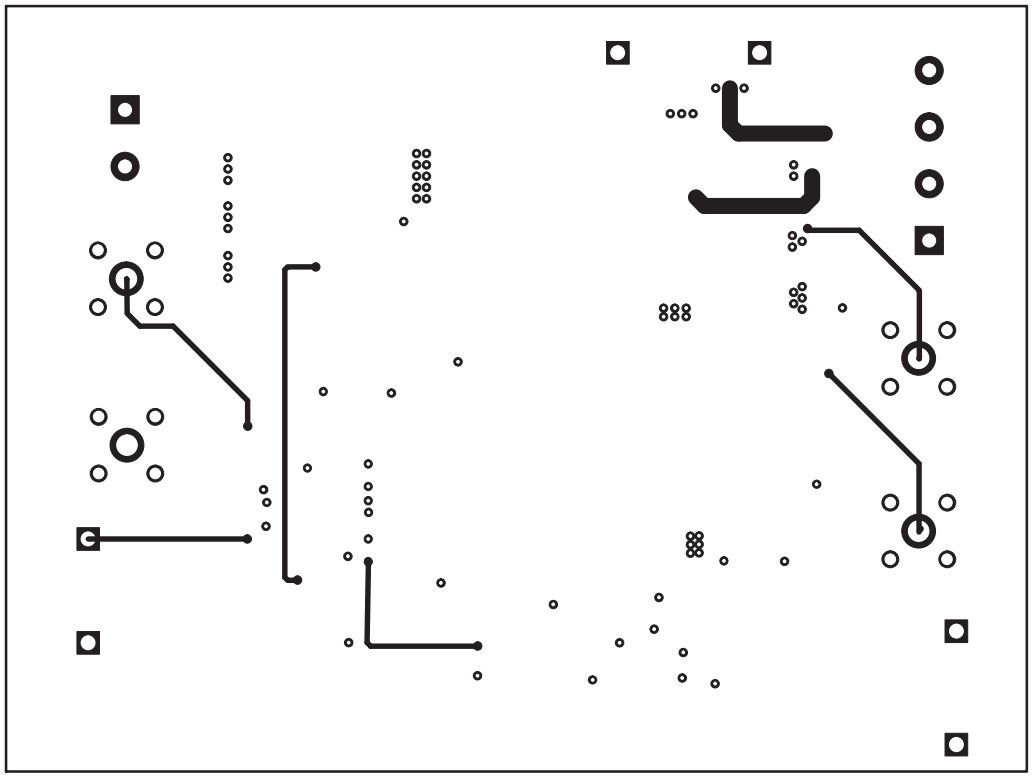

**Figure 20. Internal Signal Trace Layer**

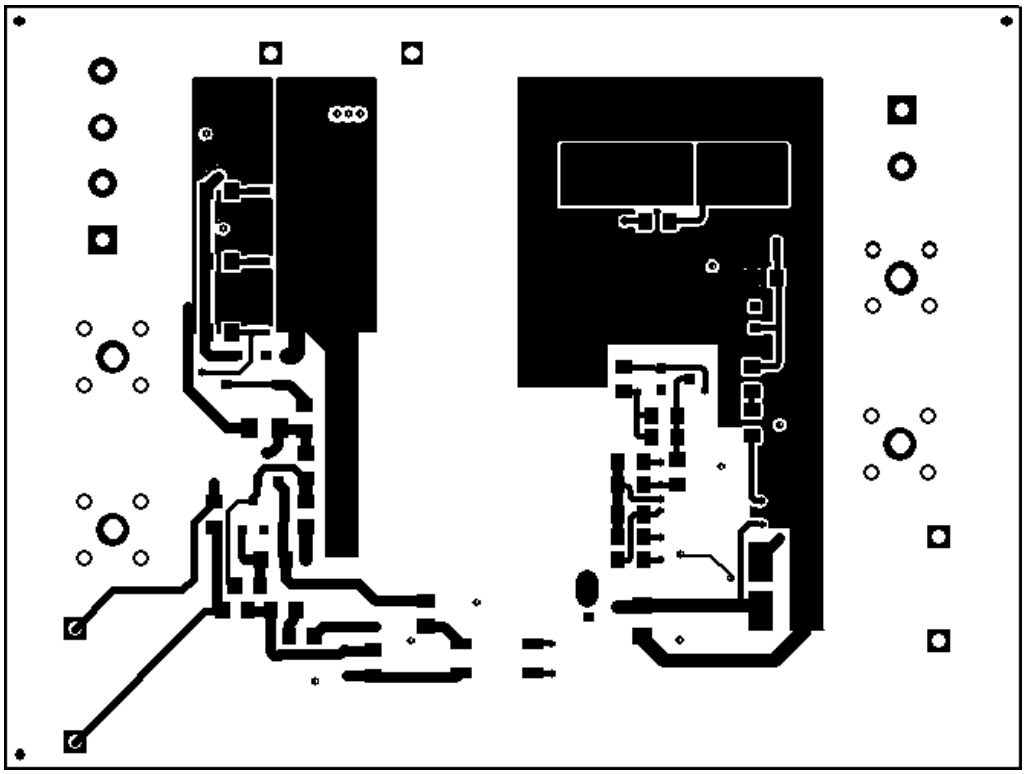

**Figure 21. Bottom Signal Trace Layer**

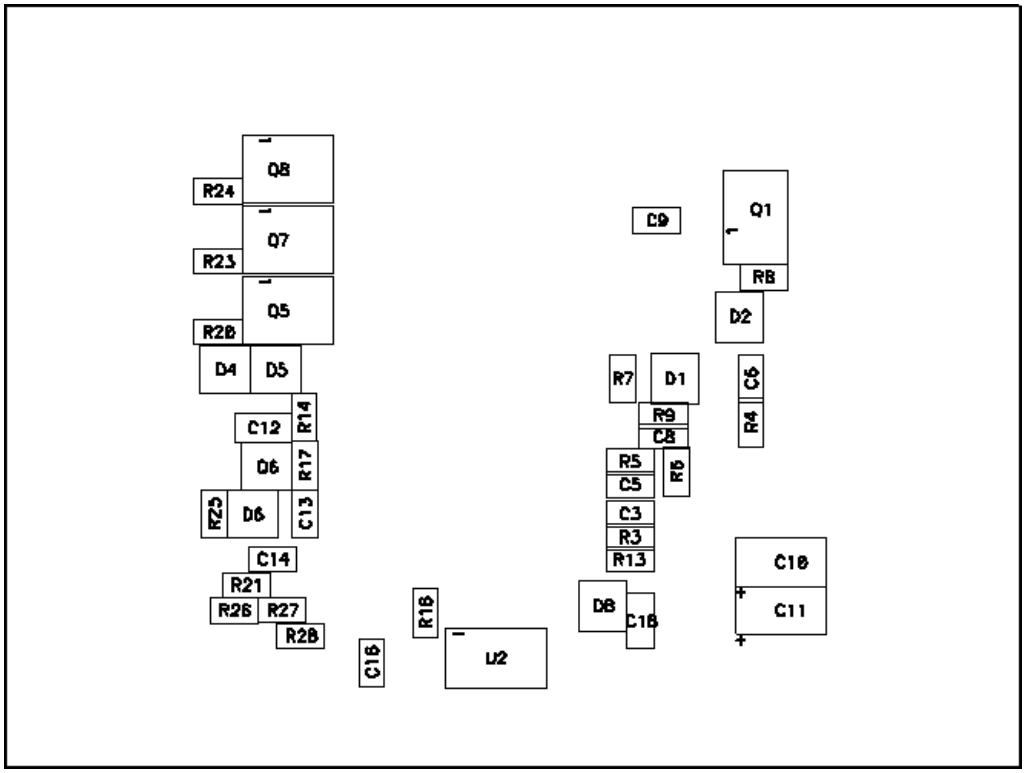


**Figure 22. Bottom Side Component Assembly**

# 10 List of Materials

**Table 2. List of materials**

| REFERENCE DESIGNATOR | QTY | DESCRIPTION | SIZE | MFR | PART NUMBER |
|---|---|---|---|---|---|
| C1, C2, C4 | 3 | Capacitor, ceramic, 2.2 µF, 100 V, X7R, 20% | 1812 | TDK | C4532X7R2A225M |
| C3, C14, C17 | 3 | Capacitor, ceramic, 0.1 µF, 50 V, X7R, 20% | 805 | Vishay | VJ0805Y104MXAA |
| C5 | 1 | Capacitor, ceramic, 100-pF, 50 V, NPO, 10% | 805 | Vishay | VJ0805A101KXAA |
| C6, C7, C21 | 3 | Capacitor, ceramic, 0.22 µF, 50 V, X7R, 20% | 805 | TDK | C2012X7R1H224M |
| C8 | 1 | Capacitor, ceramic, 10 nF, 50 V, X7R, 20% | 805 | Vishay | VJ0805Y103MXAA |
| C9 | 1 | Capacitor, ceramic, 33 nF, 100 V, X7R, 20% | 805 | Vishay | VJ0805Y333MXBA |
| C10, C11 | 2 | Capacitor, tantalum Chip, 47 µF, 16V | C | Vishay | 595D476X9016C2T |
| C12, C18 | 2 | Capacitor, ceramic, 10 µF, 16 V, X5R, 20% | 1206 | TDK | C3216X5R1C106M |
| C13 | 1 | Capacitor, ceramic, 1.5 µF, 10 V, X5R, 20% | 805 | TDK | C2012X5R1A155M |
| C15 | 1 | Capacitor, ceramic, 82 nF, 50 V, X7R, 10% | 805 | Vishay | VJ0805Y823KXAA |
| C16 | 1 | Capacitor, ceramic, 220 pF, 50 V, NPO, 10% | 805 | Vishay | VJ0805A221KXAA |
| C19, C20 | 2 | Capacitor, POSCAP, 330 µF, 6.3 V, 20% | 7343 (D) | Sanyo | 6TPD330M |
| D1, D2, D3, D4, D5, D8 | 6 | Diode, schottky, 200 mA, 30 V | SOT23 | Vishay | BAT54 |
| D6 | 1 | Diode, zener, 5.1 V, 350 mW | SOT23 | Vishay | BZX84C5V1 |
| D7 | 1 | Adjustable precision shunt regulator, 0.5% | SOT23 | ON Semi | TLV431BSN1T1 |
| L1 | 1 | Inductor, 2 µH, 1 pri, 1 sec | .920×0.78 | Pulse | PA0373 |
| J1 | 1 | Terminal block, 2 pin, 15 A, 5.1mm | 0.40×0.35 | OST | ED500/2DS |
| J2, J3, J4, J5 | 4 | Adaptor, 3.5 mm probe clip (or 131 5031 00) | 3.5 mm | Tektronix | 131−4244−00 |
| J6, J7, J9, J10, J11, J12 | 6 | Printed circuit pin, 0.043 hole, 0.3 length | 0.043 | Mill−Max | 3103-1-00-15-00-00-0X-0 |
| J8 | 1 | Terminal block, 4 pin, 15 A, 5.1mm | 0.80×0.35 | OST | ED500/4DS |
| Q1 | 1 | MOSFET, P-channel, 150 V, 2.2 A, 240 mΩ | SO8 | IR | IRF6216 |
| Q2 | 1 | MOSFET, N-channel, 150 V, 6.7 A, 50 mΩ | PowerPak S08 | Vishay | Si7846DP |
| Q3, Q4, Q5, Q7 | 4 | MOSFET, N-channel, 30 V, 55 A, 2.5 mΩ | LFPAK | Renesas | HAT2165H |
| Q8 | 0 | MOSFET, N-channel, 30 V, 55 A, 2.5 mΩ | LFPAK | Renesas | HAT2165H |
| Q6 | 1 | Bipolar, NPN, 40 V, 600 mA, 225 mW | SOT23 | Vishay | MMBT2222A |
| Q9 | 1 | Bipolar, NPN, 40 V, 200 mA, 0.3 W | SOT23 | ON Semi | MMBT3904LT1 |
| R1 | 1 | Resistor, chip, 8.45 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−8451−F |
| R2 | 1 | Resistor, chip, 69.8 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−6982−F |
| R3 | 1 | Resistor, chip, 88.7 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−8872−F |
| R4, R10, R15, R16, R20, R23, R24 | 7 | Resistor, chip, 2.21 Ω, 1/10W, 1% | 805 | Vishay | CRCW0805−2R21−F |
| R5, R30 | 2 | Resistor, chip, 158 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−1583−F |
| R6 | 1 | Resistor, chip, 1.82 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−1821−F |
| R7, R8, R12 | 3 | Resistor, chip, 1 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−1001−F |
| R9 | 1 | Resistor, chip, 6.04 Ω, 1/10W, 1% | 805 | Vishay | CRCW0805−6R04−F |
| R11 | 1 | Resistor, chip, 26.7 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−2672−F |
| R13 | 1 | Resistor, chip, 2 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−2001−F |
| R14 | 1 | Resistor, chip, 10 Ω, 1/10W, 1% | 805 | Vishay | CRCW0805−10R0−F |
| R17, R18 | 2 | Resistor, chip, 499 Ω, 1/10W, 1% | 805 | Vishay | CRCW0805−4990−F |
| R21, R22 | 2 | Resistor, chip, 10 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−1002−F |
| R25 | 1 | Resistor, chip, 51.1 Ω, 1/10W, 1% | 805 | Vishay | CRCW0805−51R1−F |
| R26 | 1 | Resistor, chip, 28.7 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−2872−F |
| R27 | 1 | Resistor, chip, 12.1 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−1212−F |
| R28 | 1 | Resistor, chip, 4.99 kΩ, 1/10W, 1% | 805 | Vishay | CRCW0805−4991−F |
| R29 | 1 | Resistor, chip, 0 Ω, 1/10−W | 805 | Vishay | CRCW0805−0000−Z |
| R31 | 1 | Resistor, chip, 2.74 kΩ, 1/10−W, 1% | 805 | Vishay | CRCW0805−2741−F |

| REFERENCE DESIGNATOR | QTY | DESCRIPTION | SIZE | MFR | PART NUMBER |
|---|---|---|---|---|---|
| R32 | 1 | Resistor, chip, 634 Ω, 1/10−W, 1% | 805 | Vishay | CRCW0805−6340−F |
| R33 | 1 | Resistor, chip, 220 kΩ, 1/10−W, 1% | 805 | Vishay | CRCW0805−2202−F |
| R34 | 1 | Resistor, chip, 1.4 kΩ, 1/10−W, 1% | 805 | Vishay | CRCW0805−1401−F |
| R35 | 1 | Resistor, chip, 15 kΩ, 1/10−W, 1% | 805 | Vishay | CRCW0805−1502−F |
| T1 | 1 | Transformer, current sense, 10−A, 1:100 | 118800 | Pulse | P8208 |
| T2 | 1 | Transformer, high-frequency planar | Planar | Pulse | PA0810 |
| U1 | 1 | IC, current mode active clamp PWM controller | PW20 | TI | UCC2897PW |
| U2 | 1 | IC, phototransistor, CTR 100%−300% | SOP4 | Vishay | SFH690BT |
| −− | 1 | PCB, 3.6″ × 2.7″ × 0.093″ | | Any | PR265B |

# 11 References

1. UCC2897 Current Mode Active Clamp PWM Controller, Datasheet, (SLUS591A)
2. Designing for High Efficiency with the UCC2891 Active Clamp PWM Controller, Application Note, Steve Mappus, (SLUA299)

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