UC3578 Telecom Buck Converter Reference Design

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ABSTRACT

The UC3578 is a PWM controller with an integrated high-side floating gate driver. It is used in buck stepdown converters and regulates a positive-output voltage. Intended for a distributed power system, this device allows operation from 14-V to 72-V input, which includes the prevalent telecom bus voltages. The output duty cycle of the UC3578 can vary between 0% and 90% for operation over the wide input voltage and load conditions. This Reference Design describes a simple solution for a buck converter operating from an input of 15 V to 72 V with an N-channel MOSFET switching transistor. Using this switch configuration requires a gate potential higher than the input source, generally requiring an auxiliary supply or a transformer. The UC3578 provides a regulated floating gate drive voltage for an N-channel MOSFET that allows for cost-effective design of buck stepdown regulators with power levels in the tens of watts. A complete converter with schematic, bill of materials, and performance results is presented to produce a 5-V, 35-W output from a 48-V source.

Contents

1 Introduction

This reference guide describes a simple solution for a buck converter operating from an input of 15 V to 72 V with an N-channel MOSFET switching transistor. Using this switch configuration requires a gate potential higher than the input source, generally requiring an auxiliary supply or a transformer. The UC3578 provides a regulated floating gate drive voltage for an N-channel MOSFET that allows for cost-effective design of buck stepdown regulators with power levels in the tens of watts. A complete converter with schematic, bill of materials, and performance results is presented to produce a 5-V, 35-W output from a 48-V source.

Distributed power systems have come into widespread use in communications and related industries over the last decade. In these systems the electrical power distribution network has been changed from one central power supply with cables or busses to a number of smaller power processing units which are placed throughout the host system. The usual intent is to bring the power processing closer to the subsystems where the power is used. The advantages of distributed power as delineated in *Distributed Power Systems*[1], along with much information on distributed power architectures and applications.

However, the cost of the modules has historically been relatively high compared to design solutions using discrete components. This Reference Design introduces the UC3578 integrated circuit and highlights its use in a 48-V to 5-V buck regulator. Utilizing this approach results in a 35-W converter that is a fraction of the cost of a comparable module.

The UC3578 is used to simplify the design of the single switch PWM buck converter by incorporating a floating high-side driver that allows the use of an external N-channel MOSFET switch. Its bipolar manufacturing process allows operation from the prevalent bus voltage of 48-Vdc, with allowable inputs up to 72-Vdc. Higher output current is possible because there is no preset internal switch current limit as used in control devices that incorporate an onboard switch. These options allow the user to configure a low-cost high-power buck regulator suitable for many applications.

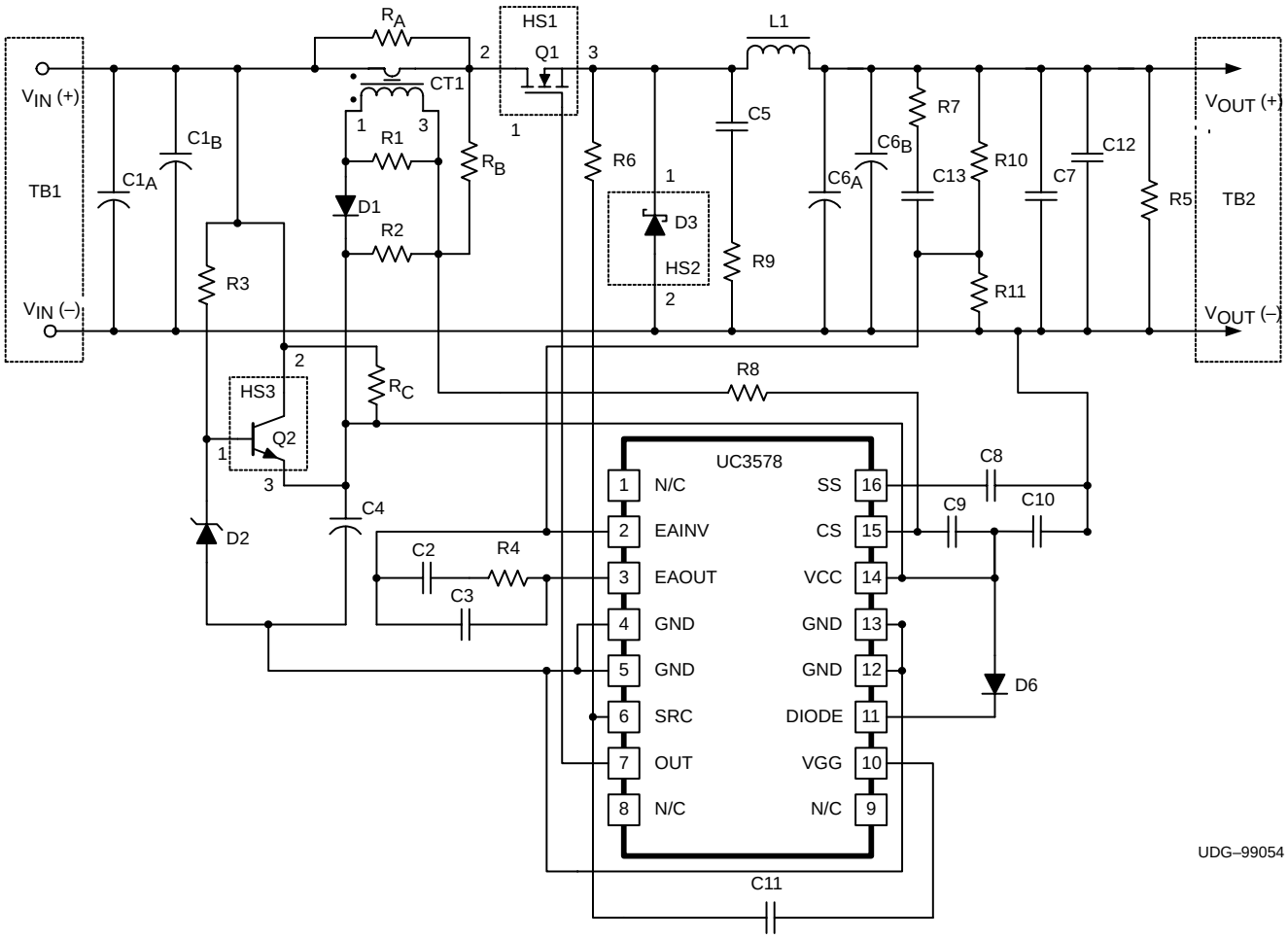

Figure 1. UC3578 Typical Application

2 Operation

2.1 Specifications.

This reference design featuring the UC3578 has been developed to illustrate the capabilities of the UC3578. The design is targeted at the telecom converter market and has the following specifications:

- V_{IN} = 48 V (nominal)
- 38.4 V < V_{IN} < 57.6 V
- V_{OUT} = 5 V, ±2%
- Output ripple, < 50 mV at 100 kHz
- I_{OUT} = 7 A
- P_{OUT} = 35 W

2.2 Schematic

A schematic diagram for the telecom buck converter meeting these specifications is shown in Figure 1. The components Q1, D3, L1, and C6 perform the power handling tasks. C1 serves as a filter to handle the input ripple current. The UC3578 provides the control circuitry for orderly startup, switch protection, regulation, and high-side power MOSFET drive. These functions are discussed in detail in the following sections, along with selection of power components. Alternate components R_A, R_B, and R_C shown on the schematic are used to evaluate circuit options as described in Section 4.2, *Resistive Current Sense Applications*. For further information on the UC3578 and its specifications, consult the datasheet (TI Literature No. SLUS341) or contact the TI Product Infromation Center.

2.3 Circuit Description

2.3.1 UC3578 Housekeeping and Control Circuits

Undervoltage lockout (UVLO) is employed to disable device operation until VCC reaches 11 V, and exhibits a 2-V hysteresis. After the UVLO threshold is exceeded, a soft-start cycle is initiated with 45-μA charging current supplied to the capacitor on pin 16. When the soft-start pin reaches approximately 1.2 V, the narrow soft-start pulses begin to appear on the output, increasing in width until pin 16 reaches 5 V. The internal oscillator is fixed at 100 kHz, a frequency that has proven to be a good compromise between small size and efficiency. The internal architecture of the UC3578 is configured for voltage-mode control. The onboard error amplifier is a voltage amplifier with the non-inverting input tied to an internal 2-V reference. Resistors R10 and R11 form a voltage divider to provide feedback information to the inverting terminal, pin 2. Control loop compensation components R4, R7, C2, C3, and C13 are used to shape the overall closed loop response.

2.3.2 Gate Drive Circuit

Gate-drive power for Q1 is provided by a voltage VGG on C11 which is charged through D6 when the switch Q1 is off, and the freewheel diode D3 is conducting. Circuitry internal to the UC3578 regulates VGG to 14 Vdc. When VGG is applied to the gate of Q1, turning it on, the source flies up close to V_{IN}, carrying the floating driver and VGG with it. During the switch on-time, D6 prevents VGG from discharging into V_{IN}. Resistor R6 serves two purposes. First, it adds damping to the L-C circuit formed by trace inductance and switch gate-to-source capacitance. Second, it serves to limit current flow into the substrate of the device when the SRC node (pin 6) is driven below ground when D3 begins conduction. It is essential that D3 is a Schottky diode so that the SRC pin is not pulled more than 0.6 V below ground. A snubber consisting of C5 and R9 is also placed across D3 to reduce high-frequency ringing.

2.3.3 Current Limiting Circuitry

CT1 and associated circuitry R1, D1, and R2, sense input current between V_{IN} and the drain of switch Q1. In the UC3578 the current sense input, pin 15, has a –0.5-V threshold with respect to VCC, pin 14. R2 is chosen to develop this signal when the current limit threshold is reached. Under full load conditions, the input current during Q1 on-time reaches a peak of 7 A plus one-half D_I, the ripple current. This normal peak current is 7 A + 0.875 A = 7.875 A. Headroom of at least 20% is allowed for transient conditions so the current-limit trip point is set for a peak current of 10 A. The selection of the burden resistor for the current transformer is calculated:

$$R2 = \frac{0.5\ V}{I_{PK}} \times \frac{N2}{N1} = \frac{0.5\ V}{10\ A} \times \frac{100}{1} = 5\ \Omega \quad (1)$$

Circuit delays in the device cause an effective LEB (leading edge blanking) period of approximately 150 ns before the circuit responds to an overcurrent condition. This allows suppression of leading-edge spikes from rectifier ringing and/or the inductive effects of the sensing circuit. When the desired current-limit point is reached, the UC3578 discharges the soft-start capacitor on pin 16 and initiates a soft-restart cycle to minimize fault power. Components R8 and C9 have been included to form a high-frequency filter to reduce the switching noise that reaches the current limit comparator.

2.4 Power Circuit Design

2.4.1 Power Switch Q1

The UC3578 integrated high-side driver allows the user to benefit from the low conduction losses and lower prices of the N-channel MOSFET as compared to a P-channel device. In the telecom buck converter, Q1 must block the full input voltage in every cycle, so the voltage rating must be greater than 57.6 V. Since the ratings for MOSFETs generally step from 60 V to 100 V, select a member of the IRF520, IRF530, IRF540 family which is rated for 100 V. This requires estimation of the conduction and switching losses following the guidelines in reference [2].

2.4.2 Duty Cycle

In order to estimate the size of the heatsink required for Q1, the duty cycle must be determined. The simplified transfer function of an ideal buck regulator is given as:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

where D is the duty cycle of the power switch Q1.

Reference [3] presents a more detailed equation derived from the volt-second balance across the output inductor during the switch ON and OFF times. Comparison between these two methods yields the values shown in Table 1.

Table 1. Duty Cycle Comparison

	Low Line 38.4 V	Nominal Line 48 V	High Line 57.6 V
Q1 ideal dc	13.0%	10.4%	8.7%
Q1 realistic dc	15.3%	12.2%	10.0%

These results show an error of approximately 15% between the two calculations.

2.4.3 IRF520, IRF530, IRF540 Comparison [4]

All three of the candidate MOSFETs could handle the peak and continuous current required by the buck telecom application. In order to choose the *best* fit for this example, the total power loss was calculated following the procedures in [2] using the realistic duty cycles found above. Graphs presented for Q1 show power loss (in watts) versus switching frequency for low-, nominal-, and high-line conditions in Figures 2, 3, and 4. In all three cases the IRF530 yielded the lowest approximate losses and is the best choice for the telecom converter. The IRF540 losses were higher in all cases because of the large switching losses. At low line the IRF520 losses grew because of increasing conduction losses.

There are several available heatsinks that have a 40°C rise with 3 W to 4 W of power dissipation. This decision is made depending on the form factor of the application and the availability or lack of forced air.

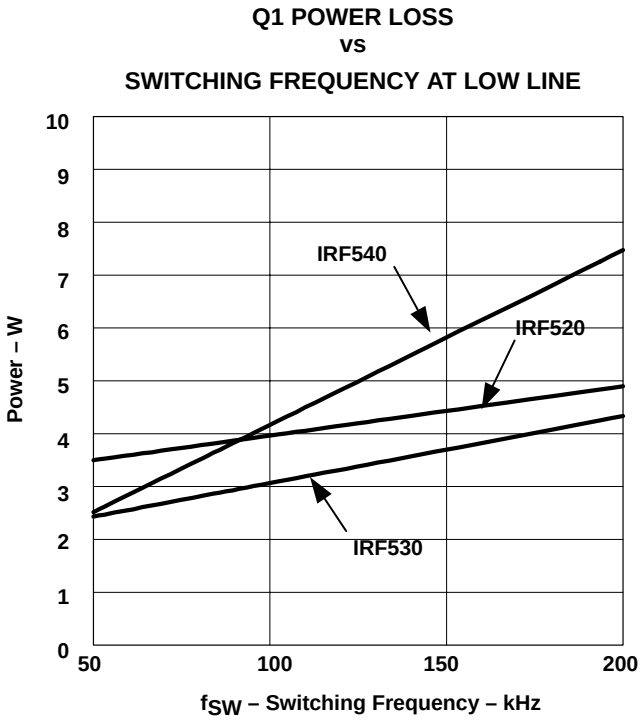

Figure 2.

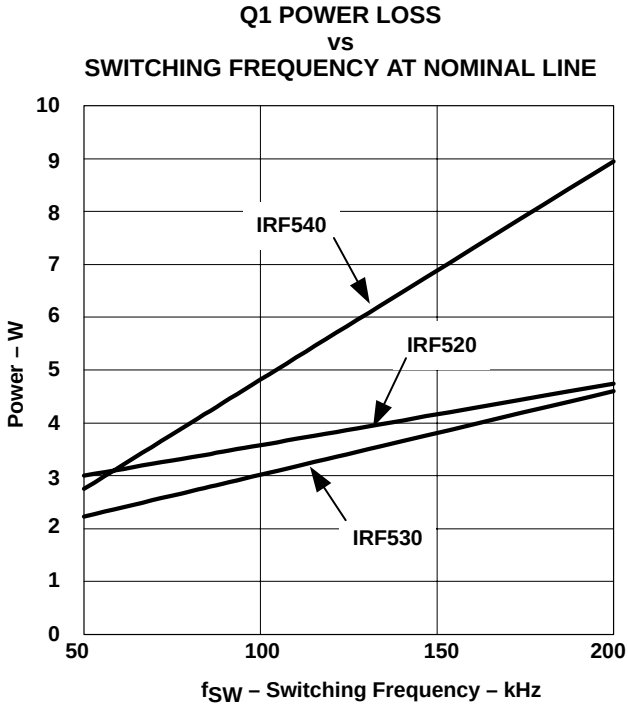

Figure 3.

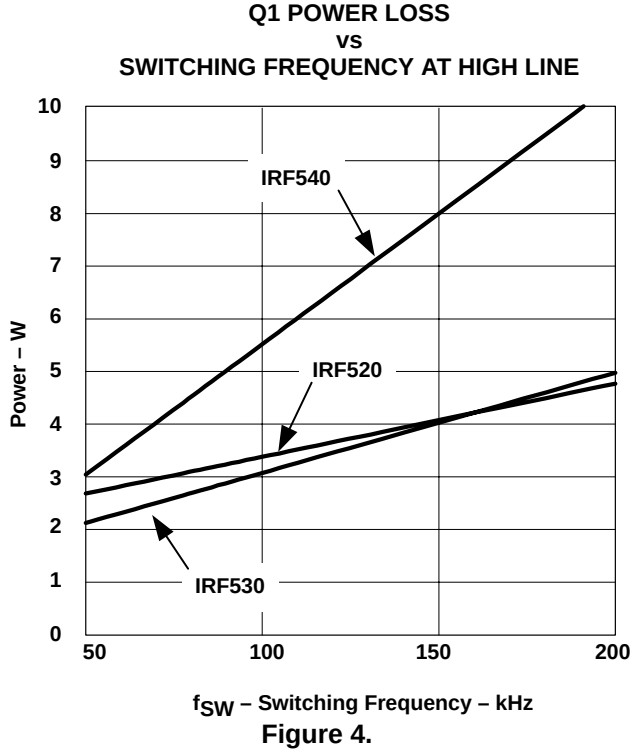

Figure 4.

2.4.4 Diode D3

D3 is a Schottky diode used to carry the freewheeling current, and should have a voltage rating larger than the maximum input voltage with a safety margin. The power dissipation is approximately 3.7 W[2]. Since V_{IN} may range up to 57.6 Vdc in this application a 100-V Schottky diode is specified, the MBR10100[5]. The same heatsink specified for Q1is also used for D3.

2.5 Output Inductor Selection

The output filter of the buck regulator can be optimized around many parameters. These include transient response, output ripple voltage, physical size, temperature rise, and other factors including availability and cost of parts. This design has been undertaken with the goal of obtaining good electrical performance using commercially available parts. Setting the ripple current in the circuit to 25% of the full load current results in a ripple current ΔI of 1.75 A. Using the basic inductor equation:

$$V = L \times \frac{\Delta I}{\Delta T}, \tag{3}$$

which, when rearranged to find the inductance and substituting the appropriate values, yields the minimum inductor value:

$$L = \frac{\left(V_{IN} - V_{Q1} - V_{OUT}\right) \times T_{ON(max)}}{\Delta I}$$
$$= \frac{(38.2\ V - 1.7\ V - 5\ V) \times 1.44\ \mu\ sec}{1.75\ A} = 26\ \mu H \tag{4}$$

Several vendors list inductors in this range which are capable of handling 7 A. In order to have an inductance over 26 μH at full load, the no load inductance may be considerably higher. Many available choices are based on low cost powdered iron that can have a *soft* saturation characteristic as its current is varied from minimum to maximum. In this case the inductor value decreases as the dc load current increases. The designer must ensure that the full-load inductor value is known to predict the ripple voltage on the output. The winding resistance of the inductor is generally noted, in order for the power loss to be calculated. Part #CTX50–5–52, rated 50 μH, is selected for this example. It has a series resistance of 0.021 Ω, and an inductance of at least 32.5 μH at 10 A.

2.5.1 Choosing the Output Capacitor

The output capacitor choice can strongly affect the regulator size and cost. For the battery charger in the Application Note, *Implementing Multi-State Charge Algorithm with the UC3909 Switchmode Lead-Acid Battery Charger Controller*[2], the output capacitor is selected for its ability to handle the inductor ripple current and to provide filtering in the absence of the battery. Output ripple voltage and transient capability were not a major concern because the battery swamps out the effect of the output filter capacitor. In buck regulators that drive sensitive electronic loads, the ripple voltage and transient capability become major factors in choosing the output capacitors, along with ripple current capability. To ensure margin for specification compliance, the output voltage ripple calculations are made using 37.5 mV as a limit, which is 75% of the 50-mV requirement.

Equation (5) from *Magnetics Definitions and Equations*[6] allows calculation of the RMS ripple current flowing through the output capacitor.

$$I_{RIP} = \frac{\Delta I}{\sqrt{12}} = \frac{1.75\ A}{3.46} = 0.505\ A \quad (5)$$

If capacitors were ideal and had no parasitic resistance or inductance, equation (6) would define the capacitance needed to carry the specified amount of ripple current with the stated voltage ripple at a fixed frequency:

$$C = \frac{\Delta I}{8 \times f \times \Delta V} = \frac{1.75\ A}{8 \times 100\ kHz \times 0.0375\ V} = 58.3\ \mu F \quad (6)$$

In real applications, the capacitor ESR plays a major role in determining the output ripple voltage. In this example, calculate the maximum ESR allowed to stay within the ripple voltage specification by using the ripple current calculated with an inductance of 32.5 μH:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{0.0375\ V}{1.4\ A} = 27\ m\Omega \quad (7)$$

The output capacitor chosen must have the following attributes:

- voltage rating 20% greater than 5V
- ripple current capability over 0.505A (5)
- minimum value of 58.3 μF (6)
- ESR below 28 mΩ at temperatures of interest (7)

The options available to the designer are as follows:

- Bulk capacitance: use one or more capacitors from one of the three applicable classes (Aluminum Electrolytic, Tantalum, or Organic Semiconductor) to meet the minimum capacitance and maximum ESR requirements.
- Fit capacitors to handle the inductor ripple current and then add a secondary L-C filter to meet the output voltage ripple requirements.

Table 2 shows electrical parameters and normalized costs for the various capacitor technologies that are candidates for the output filter in this 100-kHz buck converter. The cost figures were taken for a quantity of 1000 pieces through normal distribution channels. The total cost factor is based on the number of capacitors needed in parallel to reach the ESR goal of 27 mΩ. In this example, the Total Cost Factor of 1 is assigned to the use of two 2200-μF aluminum electrolytic capacitors. The ripple current is over 1 A for any one capacitor of the types mentioned, so the specific ratings are not given. It is evident that these choices reveal severe tradeoffs between cost and size of the buck converter. Option 2, incorporating a secondary L-C ripple filter, is not investigated in this presentation.

Table 2. Capacitor Technology Comparison

MANUFACTURER	PART NUMBER	TYPE	VOLTAGE	VALUE	ESR (m)	QTY	TOTAL COST FACTOR
Panasonic	HFQ Series ECA–OJFQ222[7]	AI EI	6.3 V	2200 μF	0.042	2	1.00
Sanyo	SA Series 6SA330Ml[8]	OS	6.3 V	330 μF	0.025	1	1.45
AVX TPS	Series TPSE337M006R0100[9]	Tantalum	6 V	330 μF	0.100	4	8.70

Another factor worthy of mention pertains to the transient loads that the power supply may be subjected to in its application. Solutions that utilize the smaller capacitance values may have larger transient deviations because these load changes must propagate through the L1–C6 output filter. A larger capacitor would have more stored energy to supply the load while the inductor current climbs to the larger value of load current. The telecom buck converter incorporates two aluminum electrolytic output capacitors to minimize costs while providing a large value of reservoir capacity to handle load transients. For comparison, the design was also configured and stabilized with one capacitor to demonstrate the smallest practical size solution.

2.6 Control Loop Stability Considerations

2.6.1 Aluminum Electrolytics

In the UC3578 circuit design, the filter components have been chosen as follows:

Output capacitors $C6_A$,$C6_B$:	total 4400 μF, ESR approximately 0.021 Ω
Output inductor L1:	32.5 μH for 10 A rating

These values allow the designer to calculate the output corner frequency as:

$$F_{LC} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{4400\ \mu F \times 32.5\ \mu H}} = 421\ Hz \quad (8)$$

Due to the capacitor ESR, Figure 5, the output filter capacitors contribute a power circuit zero at a frequency of:

$$F_Z = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (9)$$

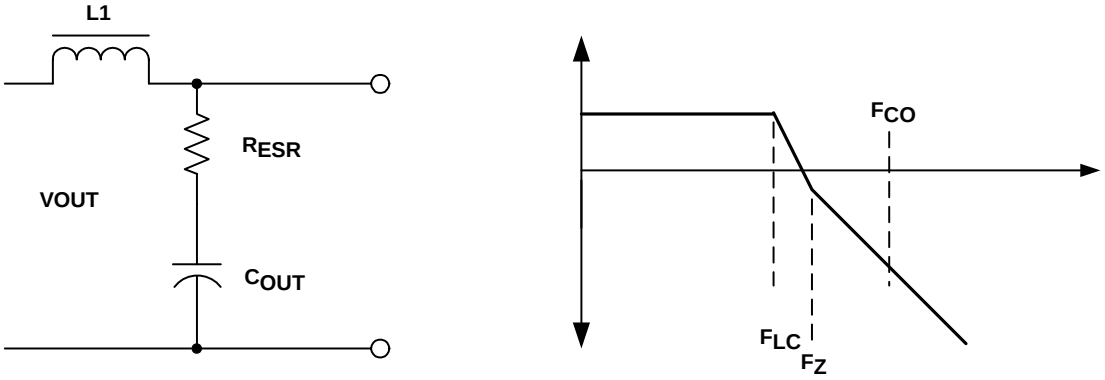

Figure 5. Output Filter with R_{ESR} and Bode Plot.

The gain falls with a –2 slope after the L-C filter resonance, and this is converted to a –1 slope at the frequency where the capacitor ESR equals the capacitive impedance, F_Z. This slope continues through the desired unity gain crossover frequency, F_{CO}, of 10 kHz.

The UC3578 error amplifier should be tailored to have flat gain in this region to maintain the –1 slope for stable operation (see *Closing the Feedback Loop*[10]), and this can be achieved as shown in Figure 6 using an amplifier (see *Practical Techniques for Analyzing, Measuring, and Stabilizing Feedback Control Loops in Switching Regulators and Converters*[11]) with a zero-pole pair.

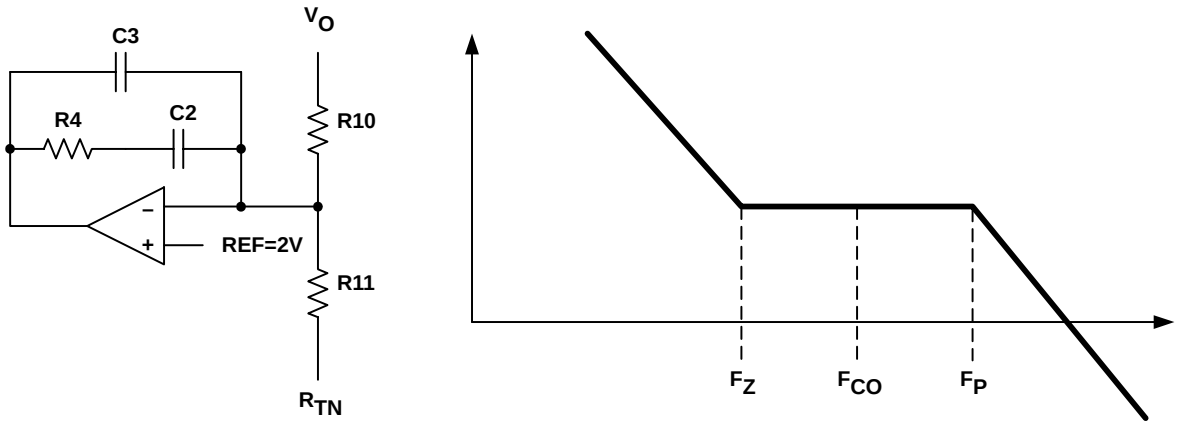

Figure 6. Error Amplifier with Zero-Pole Pair

This amplifier configuration has been fully analyzed in *Practical Techniques for Analyzing, Measuring, and Stabilizing Feedback Control Loops in Switching Regulators and Converters*[11] to yield a pole at the origin that sets the initial –1 slope, a zero at $F_Z = 1/2\ \pi \times (R4 \times C2)$, and a pole at $F_P = 1/2\ \pi \times (R4 \times C3)$. The zero turns the gain slope from –1 to 0 before the unity gain crossover frequency of 10 kHz is reached, and the pole turns the slope from 0 to –1 to roll off the gain at high frequencies. A summary of the circuit component selections is given in Table 3.

2.6.2 OSCON Capacitors

The circuit was also built using an OSCON output capacitor.

Output capacitor:	330 μF, ESR 0.025W
Output inductor:	32.5 μH

This yielded a new output corner frequency of:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{LC}} = \frac{1}{2\pi \sqrt{30\ \mu H \times 330\ \mu F}} = 1.6\ kHz \qquad (10)$$

In the OSCON capacitor circuit the ESR zero at 19.3 kHz is beyond the crossover frequency of 12.5 kHz, so the output filter characteristic exhibits a –2 slope throughout this region, as shown in Figure 7.

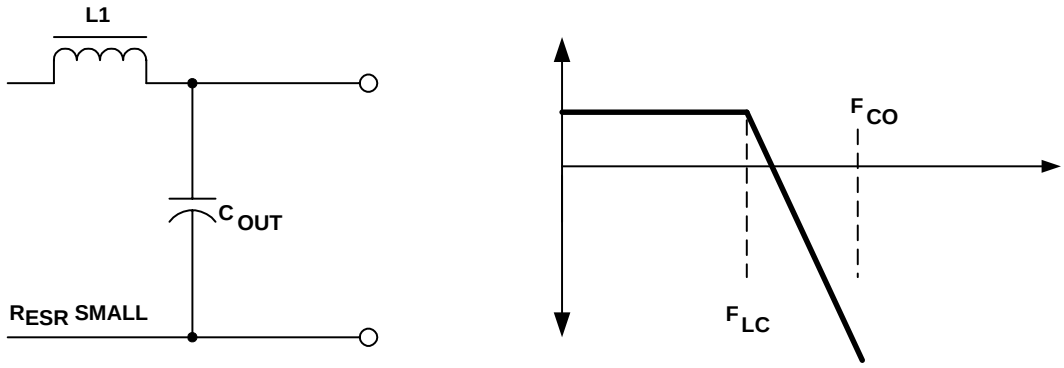

Figure 7. Output Filter with Negligible R_{ESR}

For this situation the error amplifier must provide a +1 slope during the crossover region to convert the overall loop slope to –1. This requires an amplifier with two pole-zero pairs with the schematic and characteristic shown in Figure 8.

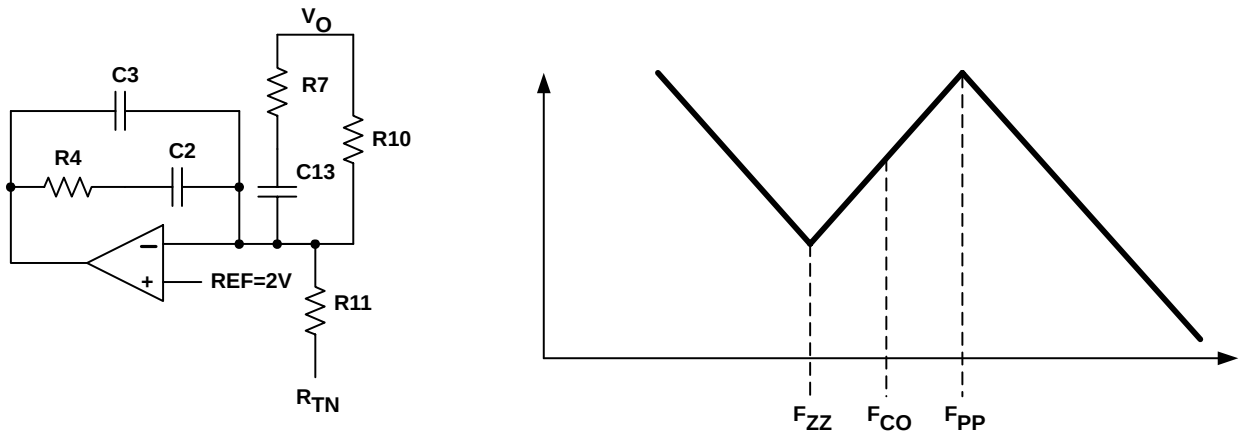

Figure 8. Error Amplifier with Two Pole-Zero Pairs

Table 3. Control Loop Configuration Comparing the Use of Aluminum Electrolytic Capacitors and OSCON Capacitors

COMPONENT	CONFIGURATION	
	ALUMINUM ELECTROLYTIC CAPACITORS	OSCON CAPACITOR
Filter cutoff, F_{LC}	421 Hz	1.6 kHz
ESR zero, F_Z	1.81 kHz	19.3 kHz
Modulator gain	23 dB	–
Sampling gain	–8 dB	–8 dB
Crossover frequency chosen, F_{CO}	10 kHz	12.5 kHz
Error amplifier gain at F_{CO}	23 dB	–
Error amplifier zero frequency	1.54 kHz	–
Error amplifier 1st zero frequency	–	1.2 kHz
Error amplifier 2nd zero frequency	–	1.5 kHz
Error amplifier 1st pole	–	Origin
Error amplifier 2nd pole	–	19.3 kHz
Error amplifier 3rd pole	–	50 kHz
C2	2000 pF	6.8 nF
C3	85 pF (used 100 pF)	470 pF
C13	not used	1.5 nF
R4	47 kΩ	20 kΩ
R7	not used	2.2 kΩ
R10	8.25 kΩ	69.8 kΩ
R11	–	46.4 kΩ

2.6.3 Output Capacitor Summary

The UC3578 could be implemented with various output capacitor technologies. The aluminum provide the lowest cost solution with a good transient response due to the large bulk capacitance. The OSCON family provides the smallest solution with an acceptable transient response at a higher cost. Both versions may be implemented and stabilized on an evaluation board; it is left for the designer to determine the best configuration for any particular application.

3 Thermal Considerations In High-Voltage Applications

The UC3578 voltage regulator is able to operate from an input voltage range of 14 Vdc to 72 Vdc. However, thermal considerations play a limiting role in the application of the UC3578 device as the supply voltage is increased. The package rating information allows calculation of the junction temperature rise for various power dissipation levels. For example, the 16-pin DP SOIC power lead frame has a thermal resistance Δja of 58°C/W on a 5 square inch FR4 PC board with one-ounce copper. The maximum allowable power at 70°C is calculates as:

$$P_D = \frac{(150^o\,C - 70^o\,C)}{58^o\,C/W} = 1.38\ W \tag{11}$$

For the 16-pin plastic batwing package, the allowable power is 1.6 W at 70°C. At 150°C, no power dissipation is allowed, and at 70°C the differences between the two packages is shown in Figure 9. Operation is permitted only to the left of the line representing a particular package; to the right, the maximum junction temperature is exceeded. Reliability is enhanced as the operating point is moved farther left from the line.

In the application using the DP package, the input supply voltage is limited to approximately 40 Vdc because of power dissipation (approximately 1 W) in the device package. It becomes obvious that the key to using the UC3578 in the 48-Vdc input application is to find a way to dissipate the excess bias power external to the control device. Methods to accomplish this are presented in this application note.

3.1 Bias Current Components

At this point it is appropriate to discuss the three components of the bias currents feeding the circuit; namely I_{VCC}, I_{VGG}, and I_{GATE}. I_{VCC} is the quiescent current drawn to power the entire chip except for the floating gate driver VGG. Current I_{VGG} supplies the driver section quiescent current through an external diode. The current needed to drive the external MOSFET, I_{GATE}, is supplied through the external diode and VGG regulator. The power related to I_{VCC} and I_{VGG} is dissipated internally to the UC3578, however, this is not the case for I_{GATE}. The only power loss internal to the device due to I_{GATE} comes from conduction of the totem pole driver section while the MOSFET gate is being charged and discharged.

I_{GATE} varies with the choice of the power MOSFET used as the buck switch. The IRF530 was selected to minimize the heatsink size needed in the circuit layout. The total gate charge, which must be supplied to drive this device, is 26nC (see *HEXFET Power MOSFET Designer's Manual*[4]). This requires a current of:

$$I_{GATE} = Q_G \times f_S = 26\ nC \times 100\ kHz = 2.6\ mA \tag{12}$$

At V_{BIAS} = 14 V this represents a power loss of 36-mW, and only a small portion of this is dissipated in the integrated circuit. This loss is small in comparison to that due to I_{VCC} and I_{VGG} and is not included in calculations for junction temperature for the device.

Maximum specifications for I_{VCC} and I_{VGG} are given in the Power Management Products Data Book (TI Literature No. SLUD003) as $I_{VCC(max)}$ = 14 mA and $I_{VGG(max)}$ = 10.5 mA. ICC varies with temperature and VCC as given in Figure 10. In the 48-Vdc circuit, the goal is to regulate VCC as V_{IN} increases. This reduces the power dissipated in the UC3578 to levels which allow operation at V_{IN} = 48 Vdc with a reasonable maximum junction temperature.

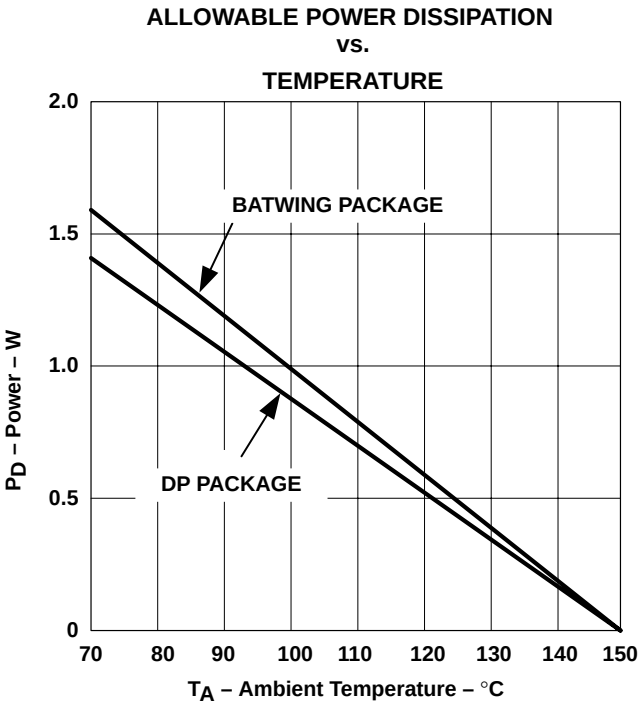

Figure 9.

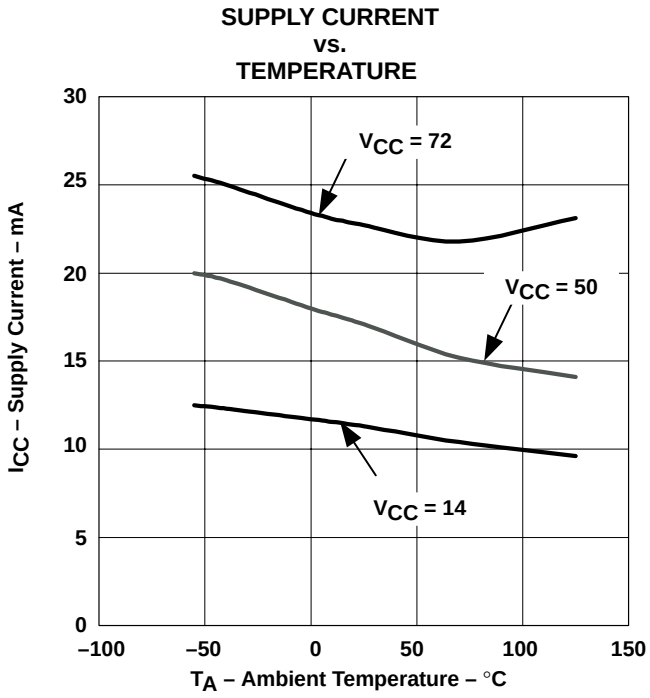

Figure 10.

4 Comparison Of Input Supply Methods

Two methods are considered to limit the voltage available to supply bias power to the UC3578.

- Series dropping resistor
- VCC voltage regulator

The series resistor can be utilized in the lowest cost applications and works best when the supply voltage variation is relatively small. The resistor must be sized to allow the maximum required current at the minimum input voltage. In this case

$$R_{LIM} = \frac{\left(V_{IN(min)} - VCC\right)}{\left(I_{VCC} + I_{VGG} + I_{GATE}\right)} = \frac{38.4\ V - 14\ V}{14\ mA + 10.5\ mA + 2.6\ mA} = 900\ \Omega \quad (13)$$

Note that I_{GATE} was included because the associated voltage must be dropped on the resistor even though very little of this power is dissipated in the device. As the input is increased to $V_{IN(max)}$ = 57.6 V, the drop across R_{LIM} remains essentially constant because the ICC increase seen with higher VCC is offset by the ICC decrease at higher junction temperature.

$$V_{R(LIM)} = 27.1\ mA \times 820\ \Omega = 22.2\ V, \quad (14)$$

and

$$VCC = V_{IN(max)} - V_{R(LIM)} = 57.6\ V - 22.2\ V = 35.4\ V \quad (15)$$

The UC3578 power dissipation is:

$$P_D = VCC \times \left(I_{VCC} + I_{VGG}\right) = 35.4\ V \times 24.5\ mA = 0.87\ W \quad (16)$$

At high V_{IN} calculate the UC3578 temperature rise is:

$$\Delta T_{ja} = \Theta_{ja} \times P_D = 50^{o}C/W \times 0.87\ W = 43.5^{o}C \quad (17)$$

This is a significant improvement over the datasheet example in which VCC was limited to 40 V.

4.1 Input Voltage Regulator

The VCC voltage regulator in Figure 1 consists of Q2, R3, and D2. D2 is a 16-V zener diode connected from the base of Q2 to ground, so the bias voltage on the emitter of Q2 is regulated to one diode drop below the zener, or approximately 15 V. R3 is selected to bring D2 into conduction and also provide base current to Q2. A power MOSFET could also be used by increasing the zener diode value to offset the drop of the gate-to-source threshold voltage. A current regulator was not chosen for this application because the VCC level supplied to the chip would vary as ICC changes with temperature, possibly necessitating the addition of a second zener to clamp VCC to a fixed level.

Under these conditions with VCC = 15 V the power dissipated in the device is:

$$P_D = VCC \times \left(I_{VCC} + I_{VGG}\right) = 15\ V \times 24.5\ mA = 0.37\ W \quad (18)$$

With this power dissipation, the junction temperature rise is:

$$\Delta T_{ja} = \Theta_{ja} \times P_D = 50^{o}C/W \times 0.37\ W = 18.5^{o}C \quad (19)$$

This allows room to increase the maximum ambient temperature to the full industrial range or to raise the allowable V_{IN} range upward to 72-Vdc(max), as long as the junction temperature and allowable power dissipation are monitored. Keep in mind that the bias voltage regulator should be sized to handle 1 W of power at V_{IN} of 57.6 V.

4.2 Resistive Current Sense Applications

Alternate circuits that use the UC3578 at lower input voltages and/or reduced ambient temperatures often are able to fit a current-sense resistor in place of the current transformer. In this case, the filter formed by R8 and C9 is more critical to provide a clean waveform because there is no current transformer with associated filtering action to reduce the noise produced during the switching operation.

To use the circuit in a resistive current-sense application, configure the circuit as follows:

Remove Components	Populate Components
CT1, R1, R2, D1, Q3, R3, D2	R_A, R_B, R_C

R_A is selected to produce 0.5 V when input current limiting has reached the current limit activation level. R_B is a low value jumper (≤10 Ω) to tie the current-sense signal into the filter components R8 and C9. R_C is also a low-value jumper (≤10 Ω) to provide bias directly to the device from V_{IN}.

4.3 Other Considerations

The UC3578 is capable of operating at a duty-cycle as low as approximately 6%. Below this level, the controller begins to skip pulses to maintain the output at the desired value. Figure 11 gives an approximate V_O versus V_{IN} calculated using the ideal duty-cycle equation. This is used to give a worst-case estimate because it has been shown that the realistic duty cycle runs a little longer than the ideal duty-cycle because of the effect of parasitic circuit components.

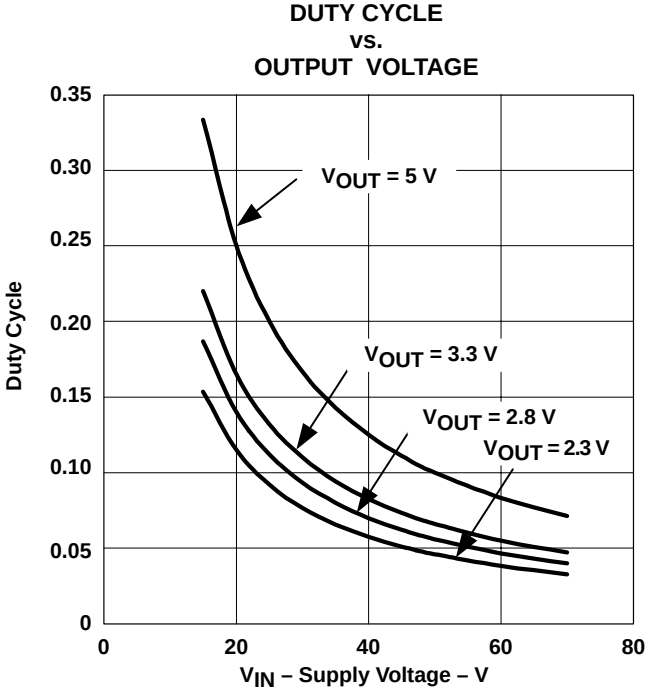

Figure 11.

4.4 Evaluation Board Performance

An evaluation board was built and tested using the parts list given. Typical efficiencies are given in Table 4. for the operating conditions listed.

Table 4. Typical UC3578 Evaluation Board Efficiencies

SUPPLY VOLTAGE (V_{IN})	SUPPLY CURRENT (I_{IN})	OUTPUT VOLTAGE (V_{OUT})	OUTPUT CURRENT (I_{OUT})	INPUT POWER (W_{IN})	OUTPUT POWER (W_{OUT})	EFFICIENCY
25 V	0.61 A	4.92 V	2.5 A	15.25 W	12.30 W	81%
35 V	0.45 A	4.92 V	2.5 A	15.75 W	12.30 W	78%
35 V	0.91 A	4.91 V	5.0 A	31.85 W	24.55 W	77%
48 V	0.35 A	4.91 V	2.5 A	16.80 W	12.28 W	73%
48 V	0.69 A	4.91 V	5.0 A	33.12 W	24.55 W	74%
48 V	0.97 A	4.91 V	7.0 A	46.56 W	34.37 W	74%

A load transient from 2.5 A to 5.0 A was applied to the evaluation board to compare the two output capacitor configurations discussed in the stability section. Figure 12 shows the transient response with two 2200-µF aluminum electrolytic capacitors installed. The maximum undershoot is 70 mV. In Figure 13 a single 330-µF OSCON capacitor was fitted in place of the two aluminum electrolytic capacitors. Noting that the scales have changed, the maximum undershoot is now near 220 mV. The importance of performance, cost, and size tradeoffs must be evaluated to make the most appropriate output capacitor selection.

TRANSIENT RESPONSE WITH TWO 2200 µF ALUMINUM ELECTROLYTIC CAPACITORS

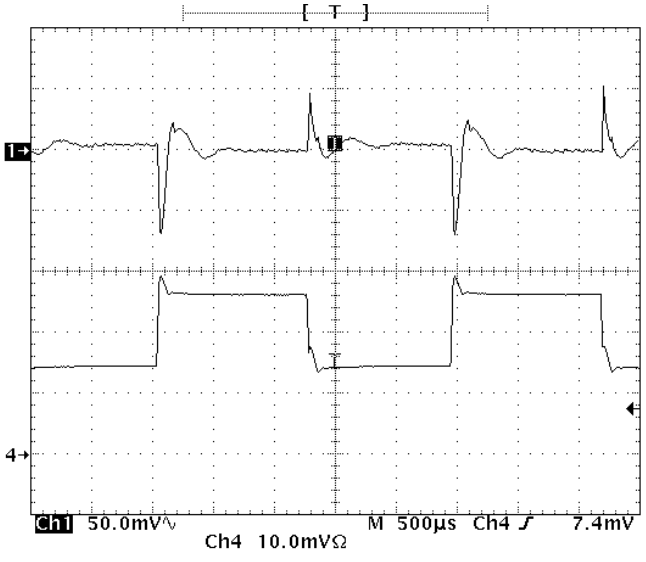

Figure 12.

TRANSIENT RESPONSE WITH A SINGLE 330 µF OSCON CAPACITOR

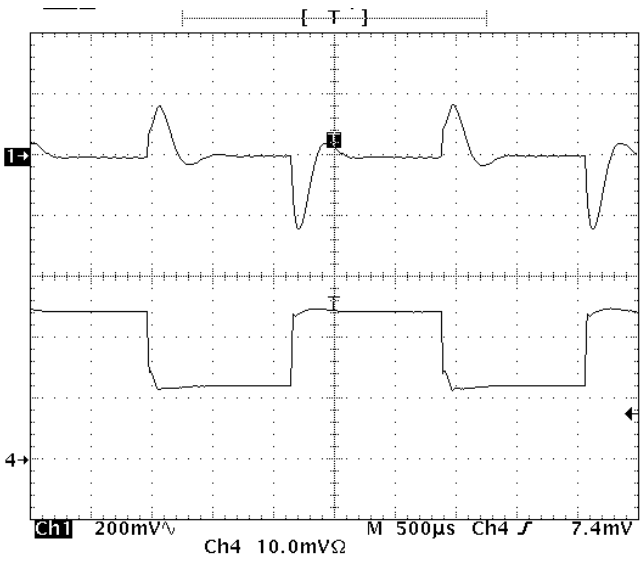

Figure 13.

5 Summary

The UC3578 Buck Stepdown Voltage Regulator provides the power supply designer with an integrated circuit controller that incorporates a floating high-side driver capable of operating at input voltages up to 72-Vdc. This Reference Design explains the power losses associated with using this high-voltage device, and suggests circuit configurations to relieve the thermal load. In addition, the circuit can be adapted to evaluate resistive current sense versions by making a few simple component changes.

Table 5. Evaluation Board List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
$C1_A$, $C1_B$	220 μF, 63 V, aluminum capacitor	Panasonic	ECA–1JFQ221
C2	2200 pF, 50 V, ceramic capacitor		
C3	100 pF, 50 V, ceramic capacitor		
C4	47 μF, 50 V, aluminum capacitor		
C5	680 pF, 50 V, ceramic capacitor		
$C6_A$,$C6_B$	2200 μF, 6.3 V, aluminum capacitor	Panasonic	ECA–OJFQ222
C7,C10,C12	0.1 μF, 50 V, ceramic capacitor		
C8	0.01 μF, 50 V, ceramic capacitor		
C9	470 pF, 50 V, ceramic capacitor		
C11	1 μF, 50 V, ceramic capacitor		
C13	See text for use		
CT1	Current transistor, 100:1	Magnetek Triad	CST306–2A
D1	75 V, 200 mA, switching diode		1N4148
D2	16 V, zener diode, 1W		1N4745A
D3	100 V, 10 A, Schottky diode		MBR10100
D6	75 V, 200 mA, switching diode		1N4148
HS1	Q1 heatsink	Thermalloy	7020B–MT
HS2	D3 heatsink	Thermalloy	7020B–MT
HS3	Q2 heatsink	Aavid	579302B00000
L1	30 μH, 10A, inductor	Coiltronics	CTX 50–5–52
R1	200 Ω, 1/4W, 5%, resistor		
R2	5 Ω, 1/4W, 1%, resistor		
R3	15 kΩ, 1/4W, 5%, resistor		
R4	47 kΩ, 1/4W, 5%, resistor		
R5	330 Ω, 1/4W, 5%, resistor		
R6	10 Ω, 1/4W 5%, resistor		
R7	See text for use		
R8	470 Ω, 1/4W, 5%, resistor		
R9	51 Ω, 1W, 5%, resistor		
R10	8.25 kΩ, 1/4W, 1%, resistor		
R11	5.62 kΩ, 1/4W, 1%, resistor		
R_A	See text for use		
R_B	See text for use		
R_C	See text for use		
Q1	100 V, 0.16 Ω, N-channel, MOSFET	IR	IRF530
Q2	250 V, 1 A, NPN transistor		TIP47
U1	Buck stepdown voltage regulator	Texas Instruments	UC3578N
TB1, TB2	Terminal block, 2 position, 5 mm spacing		

6 References

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For more complete information, pin descriptions and specifications for the UC3578 Telecom Buck Converter, please refer to the UC3578 datasheet (TI Literature No. SLUS341) .

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