TUSB8040 Design Guide

User's Guide

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TUSB8040 Design Notes and Recommendations

1 General Recommendations

1.1 Part Placement

1. If possible, place all active components on the top layer of the board stack up.
2. Place the crystal as close as possible to the TUSB8040 device and on the top layer of the board stack up to avoid the use of any vias in the clock trace.
3. Place the voltage regulators as far away as possible from the TUSB8040, the crystal, and the differential pairs.
4. Place the TUSB8040 device apart from the USB connectors (if possible).
5. Place the SuperSpeed transmit differential pair capacitors as close as possible to the USB connector pins. The ESD protection device (if used) should also be placed as close as possible to the USB connectors.
6. In general, the bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators as possible.

1.2 Board Layout Considerations

1.2.1 PFP – Plastic Quad FlatPack

- The TUSB8040 package has 0.5-mm (~20 mil) pin pitch. The TUSB8040 REV B EVM is routed on 4 layers: signal, power, ground, and signal. This 4 layer board still meets requirements of 0.062 thickness ±.010.
- The TUSB8040 has a thermal pad of 4.3 x 5.4 ±0.4 mm (170 mil x 213 mil) that must be connected to ground through a system of vias.
- All vias on the board should be solder masked to avoid any potential issues with thermal pad layouts.

1.2.2 Impedance

The differential pair traces for each USB port (USB_DP_XX / USB_DM_XX, USB_SSTXP_XX / USB_SSTXM_XX, USB_SSRXP_XX / USB_SSRXM_XX) must be designed with a characteristic impedance of 90 Ω ±10% between the complementary signals (i.e. + and -). The width and spacing of the differential pair traces can be modified to achieve the characteristic impedance of 90 Ω and may differ depending on the PCB stack up and materials used. The differential traces on the TUSB8040 REV B EVM are 5.5 mils wide with 6 mil spacing from a pin pad that is approximately 8.5 mils wide.

The remaining traces should be as close as possible to 50 Ω characteristic impedance. To meet this impedance requirement the traces on the EVM are 6.0 mils wide. Due to constraints from routing the differential pairs, board stack up and board thickness requirements, the board fabricator may not be able to get to precisely exactly 50 Ω, in those cases maintaining impedances within ±20% of 50 Ω is acceptable.

1.3 Critical Signals

1. Differential pair signals
2. External crystal signals
3. Power and ground signals (particularly VBUS and Earth GND)

Important rules for the routing of these critical signals are:

- Run all critical signals on a signal plane adjacent to a solid ground plane layer if possible.
- Never cross power/ground plane boundaries with critical signals, particularly at a 90 degree angle.
- Avoid 90 degree turns in traces, use 45 degree turns or use bevels instead.
- Keep digital signals away from the differential pairs and the crystal circuitry.
- See following sections for more information on the routing of critical signals.

2 Crystal

The XI terminal of the TUSB8040 requires a crystal input or an external clock source to the 1.8-V input. Since a 24-MHz crystal is used on the TUSB8040 REV B EVM, the other side of the crystal is attached to the XO terminal and the ground connections of the load capacitors are attached to VSS_OSC.

Care should be taken in the layout of the crystal to reduce noise and jitter. The crystal should be located as close as physically possible to the TUSB8040 XI / XO terminals. This connection should be short and direct.

3 USB Interface

The USB ports of the TUSB8040 device are attached to USB 3.0 connectors. These port connectors allow the hub to communicate to downstream USB 3.0 devices in SuperSpeed or downstream USB 2.0 devices in High-speed or Full-speed or Low-speed. The upstream connection allows simultaneous SuperSpeed and High-speed connections. The connection speed determination is done automatically by the TUSB8040.

3.1 Differential Pair Signals

Notes on routing differential pair signals:

1. Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for SS differential pair signals and USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.
2. Match the etch lengths of the differential pair traces (i.e. DP and DM or SSRXP and SSRXM or SSTXP and SSTXM). There should be less than 5 mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
3. Route the differential pair traces parallel to one another and close together as much as possible. The traces should be symmetrical.
4. Try to match the etch lengths of the differential pair groups to each other (i.e. match the length of the SSRX pair to that of the SSTX pair). The USB 2.0 differential pair length does not need to match the SSRX and SSTX pairs.

NOTE: To minimize crosstalk, it is recommended that the spacing between the TX and RX signal pairs for each interface be five times the width of the trace (5W rule). For instance, on the TUSB8040 REV B EVM there is 27.5 mils of space between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs is maximized as much as possible and ground-fill is placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

5. There should be a general keep out region of at least 20 mils around the differential pairs so that signals, components or power/ground planes are not routed close to the differential pairs. The exception is at the TUSB8040 device.
6. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make

sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close to the TUSB8040 device as possible.

7. Do not place power fuses across the differential pair traces.
8. It is preferable to route the differential pair signals directly from the port to the via under the TUSB8040 without disruption. On the TUSB8040 REV B EVM, the differential pair signals “fly-by” the ESD protection devices so that no stubs are created. Depending on board layout, this may not always be possible.
9. The differential pairs should be routed over a solid ground plane. This ground plane should run under the entire trace length from the TUSB8040 (or via) to the pins of the USB connectors and extend past the traces by 10 mils. Avoid routing differential pairs at 90 degrees angles over power plane edges.
10. In order to route the differential pairs of the TUSB8040 to the USB connectors, it is necessary on the downstream ports to cross the SSTX pair and the SSRX pair. To avoid using multiple sets of vias, the vias were carefully placed on the TUSB8040 REV B EVM so that the crossover was inherent in the board design and then both pairs of signals (along with the USB 2.0 differential pair) were routed on the bottom layer (see Figure 1).
11. To ease routing, the polarity of the SS differential pairs can be swapped. This means that SSTXP can be routed to SSTXM or SSRXM can be routed to SSRXP.

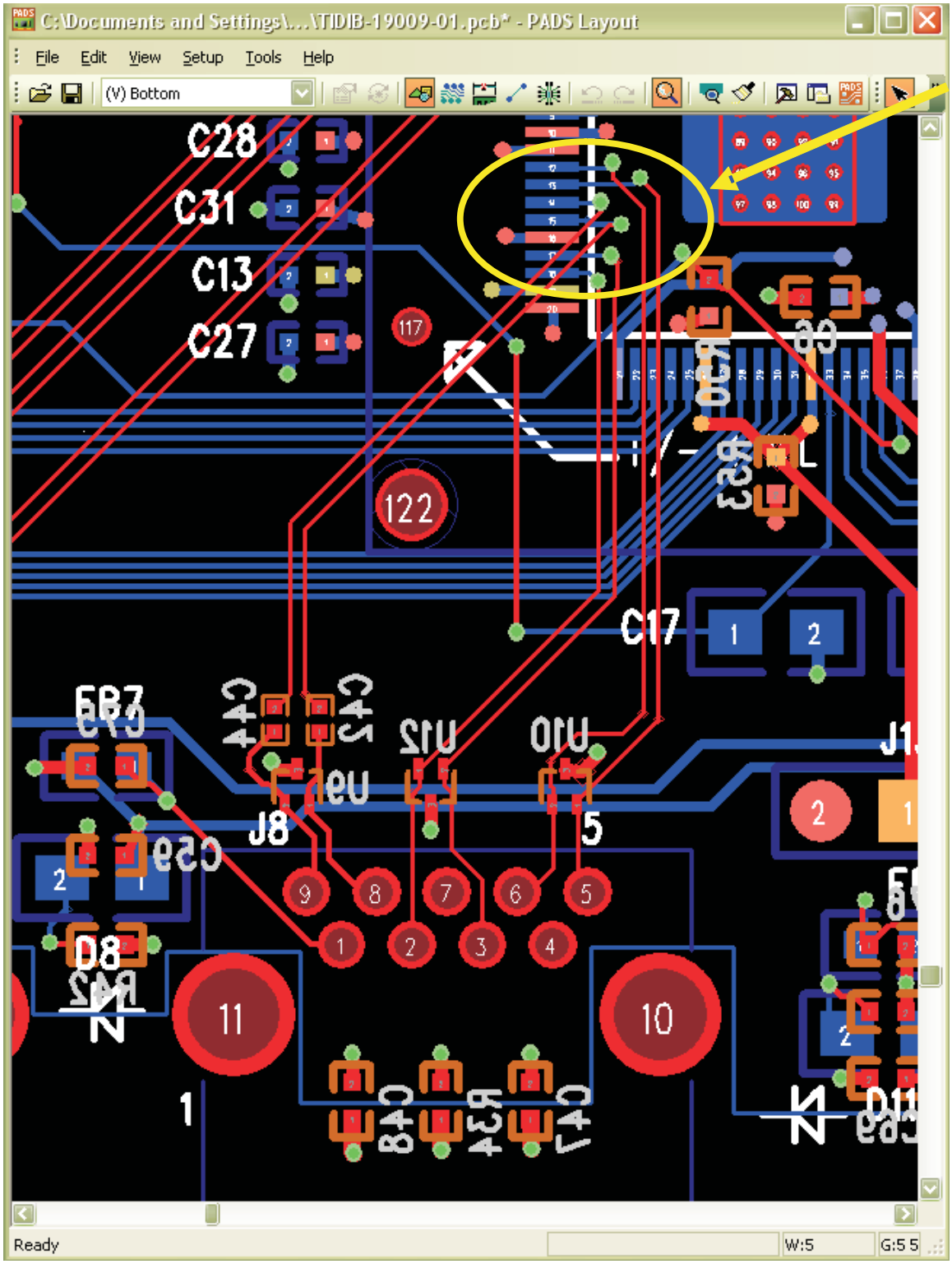


Figure 1. Using Via Placement to Cross the SSTX and SSRX Pairs

3.2 Port Connectors

Most TUSB8040 customers will be using thru-hole USB 3.0 standard connectors with mounting pegs that are soldered into the board for more rigid connections. The thru-hole connectors allow differential pairs to be routed on the bottom layer of the EVM without requiring any vias to the top layer at the connector. Routing on the bottom layer of the EVM to the thru-hole connector can reduce the stub length caused by the thru hole pins.

The outside shield of the connector should be tied to chassis ground to provide a low impedance path to the chassis ground for ESD current. If galvanic isolation is required, the outside shield should be isolated from digital ground with a parallel combination of a 1M Ohm resistor and capacitors of 0.1 µF and 0.001 µF.

Pins 4 and 7 of the USB 3.0 connector should be connected to digital ground. Both of these pins should be connected directly to the board ground plane as close to the connector as possible.

The TUSB8040 REV B EVM incorporates placeholder pull down resistors on the downstream ports SS TX signals that are not populated. These are for lab test purposes only and should not be duplicated in standard applications.

4 TUSB8040 Reset Terminals

Asserting the TUSB8040 GRSTZ pin low resets the TUSB8040. The GRSTZ signal should be held low for a minimum of 3 ms from the time that the power supplies reach the minimum required supply voltage (90% of nominal) and the crystal is active to ensure a valid reset. An external delay capacitor of 0.1 µF – 1 µF along with the internal pull-up resistor can be used to generate the power on reset pulse, the voltage ramp of the implementation will dictate the capacitor value needed. An alternative to this passive reset is to actively drive GRSTZ low using external circuitry for the minimum reset time following power on.

5 TUSB8040 Miscellaneous Terminals

The USB_R1 and USBR1_RTN terminals require a precision resistor. A 9.09 kΩ ±1% resistor should be placed in parallel across these terminals, as close to the device as possible.

While the TUSB8040 REV B EVM utilizes external pull up and pull down resistors on the following terminals, there are inherent pull ups and pull downs implemented within the TUSB8040.

NOTE: The internal pull up and pull down resistors of the TUSB8040 have a nominal value of 22 kΩ (150 µA at 3.3 V). If using an external pull up on a terminal that has an internal pull down resistor, TI recommends using a value of 7.5 kΩ or smaller. Or if using an external pull down on a terminal that has an internal pull up resistor, TI recommends using a value of 7.5 kΩ or smaller.

FULLPWRMGMTZ_SMBA1— Full power management is enabled and reported in the USB descriptors when a 4.7-kΩ pull-down is placed on this terminal and sampled at power-on reset. This pin also acts as the interface for the SMBA1 signal when a SMBus host is connected to the TUSB8040. The TUSB8040 has an internal pull up on this terminal, the TUSB8040 defaults to a non full power management state which is the lowest cost implementation with no active downstream port switching.

SMBUSz— The I^2C interface mode is enabled by default via the internal pull up resistor on this terminal. If a 4.7-kΩ pull-down is placed on this terminal and sampled at power-on reset, SMBUS mode is enabled.

PWRON0Z_BATEN— Battery charging on the downstream ports is disabled by default via the internal pull down resistor on this terminal. If a 4.7-kΩ pull-up is placed on this terminal and sampled at power on reset, battery charging on the downstream ports is enabled. This signal also acts at the active low power enable/disable for the downstream port power switches.

OVERCUR0Z— An over-current event is reported to the TUSB8040 by the downstream port power controller circuitry using this terminal. The TUSB8040 has an internal pull up on this terminal to avoid any unexpected over-current reporting.

SDA_SMBDAT and SCL_SMBCLK— Provide a serial EEPROM interface. On the EVM, these pins are routed to a serial EEPROM socket with 1-kΩ pull-up resistors installed on both signals. If the TUSB8040 is being used in SMBUS mode, then these signals become the data and clock signal respectively. The TUSB8040 has internal pull downs on these terminals.

The SDA_SMBDAT terminal is sampled at the deassertion of reset to determine if SuperSpeed low power states U1 and U2 are disabled. If SDA_SMBDAT is high, U1 and U2 low power states are disabled. If SDA_SMBDAT is low, U1 and U2 low power states are enabled. This provides the TUSB8040 the ability to work with USB 3.0 devices that do not implement the low power states per the USB 3.0 specification. If the optional EEPROM or SMBUS is implemented, the value of the u1u2Disable bit of the Device Configuration Register determines if the low power state U1 and U2 are enabled.

6 Power

6.1 TUSB8040 Power

VDD11 and VDDA11 should be implemented as a single power plane, as should VDD33, VDDA33 and VDDA33_OSC.

- The VDD11 terminals of the TUSB8040 supply 1.1-V power to the core of the TUSB8040. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the 1.1-V power rail can affect the voltage provided to the device due to the high current draw on the power rail. The output of the 1.1-V votlage regulator may need to be adjusted to account for this or a ferrite bead with low DC resistance (less than 0.05 Ω) can be selected.
- The VDD33 terminals of the TUSB8040 supply 3.3-V power rail to the I/O of the TUSB8040. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10-µF capacitor or 1-µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB8040 power pins as possible with an optimal grouping of two of differing values per pin.

6.2 Downstream Power

The downstream port power, VBUS, must be supplied by a source capable of supplying 5 V and up to 900 mA per port. Downstream port power switches can be controlled by the TUSB8040 signals. It is also possible to leave the downstream port power always enabled.

A large bulk low-ESR capacitor of 22 µF or larger is required on each downstream port's VBUS to limit in-rush current.

The ferrite beads on the VBUS pins of the downstream USB port connections are recommended for both ESD and EMI reasons. A 0.1-µF capacitor on the USB connector side of the ferrite provides a low impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

6.3 TUSB8040 Ground

It is recommended that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB8040 and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

Appendix A TUSB8040 REV B EVM Bill of Materials

This appendix contains the TUSB8040 REV B EVM BOM (see Table 1).

Table 1. Bill of Materials

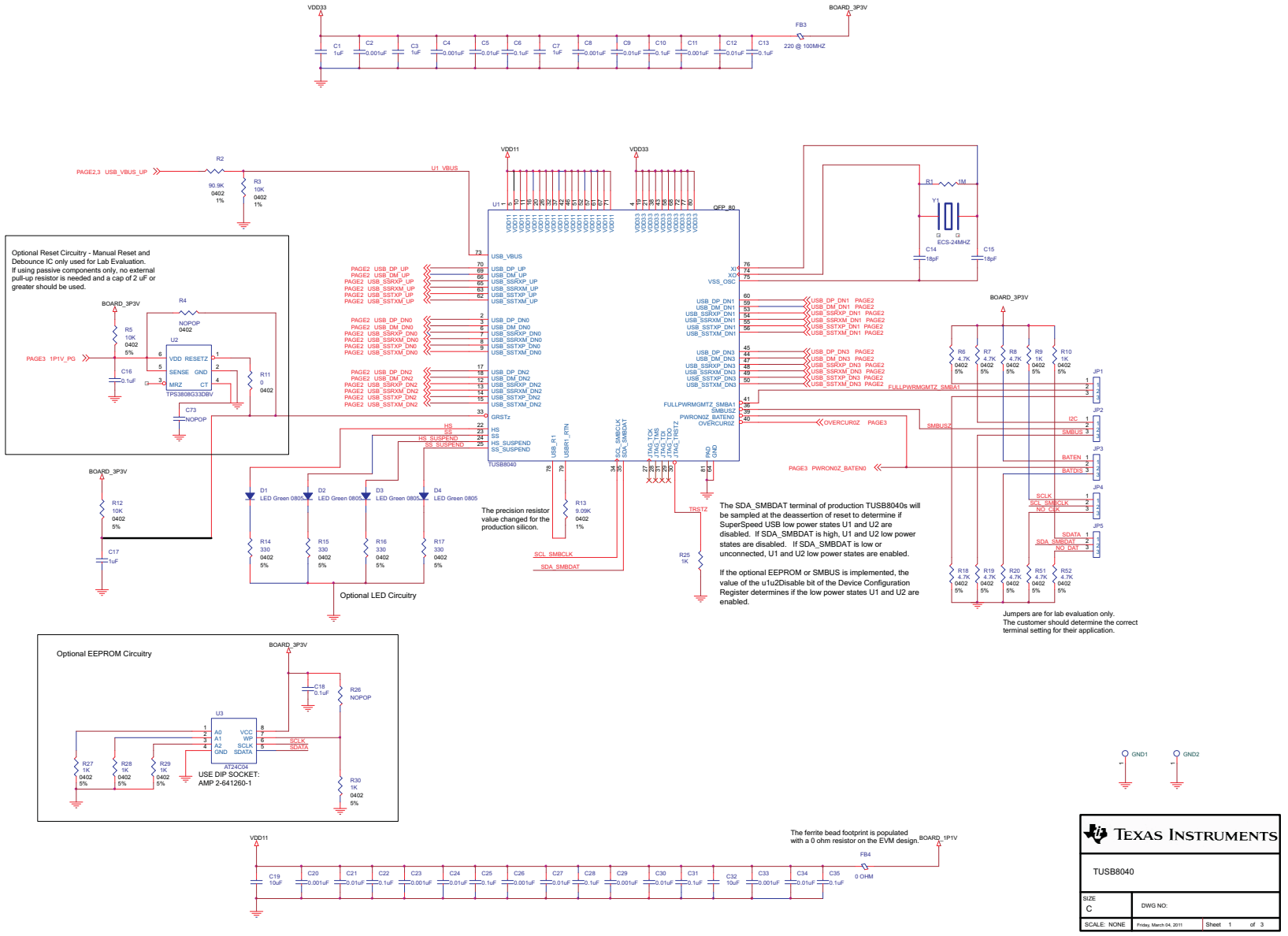
Item	Quantity	Reference	Part	MFR	Part Number	Pkg
1	4	C1,C3,C7,C17	1 µF	TDK	C2012X7R1A105K	805
2	14	C2,C4,C8,C11,C20,C23,C26,C29,C33,C40,C46, C48,C54, C56	0.001 µF	TDK	C1005X7R1H102K	402
3	9	C5,C9,C12,C21,C24,C27,C30,C34,C66	0.01 µF	AVX	0402YC103KAT2A	402
4	25	C6,C10,C13,C16,C18,C22,C25,C28,C31,C35, C39,C45,C47,C53,C55,C58,C59,C61,C65,C67, C69,C74,C75,C76,C77	0.1 µF	Yageo	CC0402KRX5R6BB104	402
5	10	C37,C38,C41,C42,C43,C44,C49,C50,C51,C52	0.1 µF	TDK	C0603X5R0J104M	201
6	2	C14,C15	18 pF	AVX	04025A180JAT2A	402
7	8	C19,C32,C36,C57,C63,C64,C71,C72	10 µF	Kemet	T491A106M006AT (Tantalum)	1206
8	4	C60,C62,C68,C70	150 µF	Kemet	B45197A2157K409 (Tantalum)	7343
9	4	R4,R26,R47,C73	NOPOP			402
10	11	D1,D2,D3,D4,D5,D6,D7,D8,D9,D10,D11	LED Green 0805	Lite On	LTST-C171GKT	805
11	5	FB3,FB6,FB7,FB8,FB9	220 at 100-MHz Ferrite Bead	Murata	BLM18PG221SN1D	603
12	7	JP1,JP2,JP3,JP4,JP5,JP7,JP8	Head 1x3 (HDR3X1 M .1)	3M	961103-6404-AR	HDR3X1 M 0.1" TH
13	1	J6	USB3_TYPEB_CONNECTOR	FoxConn	UEB1112C-2AK1-4H	9_RA_TH_B
14	4	J7,J8,J9,J10	USB3_TYPEA_CONNECTOR	FoxConn	UEA1112C-4HK1-4H	9_RA_TH_A
15	1	J11	2.1-mm x 5.5-mm DC Power Jack	CUI Inc.	PJ-202AH (PJ-002AH)	2.1-mm x 5.5-mm
16	6	R1,R31,R33,R34,R35,R36	1M	Rohm Semiconductor	MCR01MZPJ105	402
17	1	R2	90.9K 1%	Rohm Semiconductor	MCR01MZPF9092	402
18	3	R5,R12,R38	10K	Rohm Semiconductor	MCR01MZPJ103	402
19	1	R3	10K 1%	Rohm Semiconductor	MCR01MZPF1002	402
20	9	R6,R7,R8,R18,R19,R20,R39,R51,R52	4.7K	Rohm Semiconductor	MCR01MZPJ472	402
21	7	R9,R10,R25,R27,R28,R29,R30	1K	Rohm Semiconductor	MCR01MZPJ102	402
22	1	R11	0	Rohm Semiconductor	MCR01MZPJ000	402
23	11	R14,R15,R16,R17,R32,R37,R41,R42,R43,R45, R46	330	Rohm Semiconductor	MCR01MZPJ331	402
24	2	R40,R44	37.4K	Vishay / Dale	CRCW040237K4FKED	402
25	1	R48	1.87K	Vishay / Dale	CRCW04021K87FKED	402
26	1	R49	4.99K	Vishay / Dale	CRCW04024K99FKED	402
27	1	U1	TUSB8040 - USB 3.0 Hub	Texas Instruments	TUSB8040	80QFP
28	1	U2	TPS3808G33DBV - Voltage Supervisor	Texas Instruments	TPS3808G33DBV	6DBV
29	1	U3	AT24C04 / SOCKET - I^2C EEPROM	Atmel / Tyco	AT24C04A-10PU-1.8 / 2-641260-1	8DIP/8SOIC SOCKET
30	15	U4,U5,U6,U7,U8,U9,U10,U11,U12,U13,U14,U15, U16, U17,U18	TPD2EUSB30 - USB ESD Protection	Texas Instruments	TPD2EUSB30	3DRT
31	2	U19,U21	TPS2560DRC - USB Power Switch	Texas Instruments	TPS2560DRC	10SON
32	1	U20	TPS78633KTT - 3.3-V Voltage Regulator	Texas Instruments	TPS78633KTT	DDPAK-5

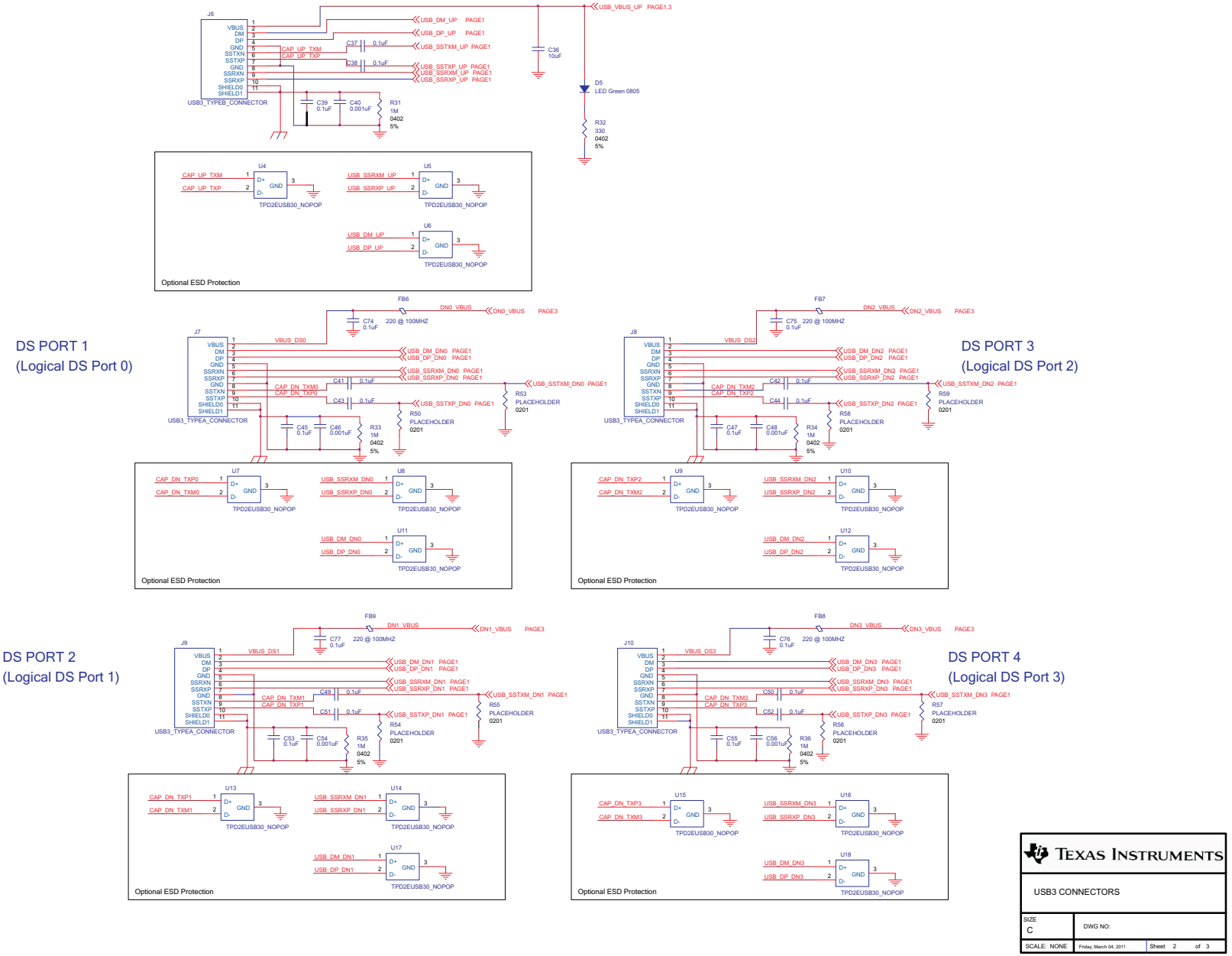
Table 1. Bill of Materials (continued)

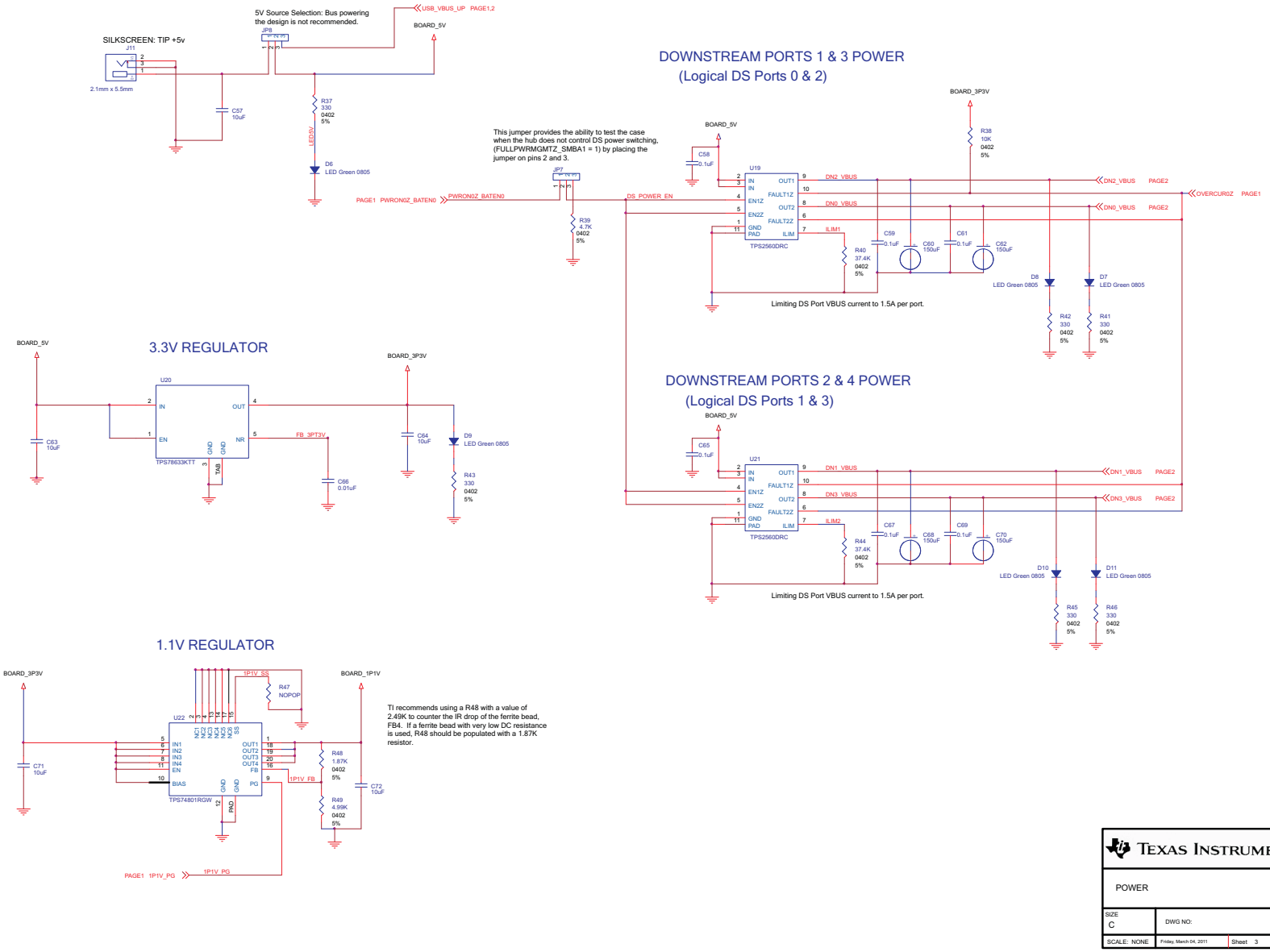
Item	Quantity	Reference	Part	MFR	Part Number	Pkg
33	1	U22	TPS74801RGW - 1.1-V Voltage Regulator	Texas Instruments	TPS74801RGW	20VQFN
34	1	Y1	ECS-24-MHz Crystal	ECS	ECX-53B (ECS-240-20-30B-TR)	5-mm x 3.2-mm
35	8	R50,R53,R54,R55,R56,R57,R58,R59	PLACEHOLDER			201
36	1	R13	9.09K1%	Vishay / Dale	CRCW04029K09FKED	402
37	1	FB4	0 Ω	Rohm Semiconductor	MCR03EZPJ000	603

Appendix B TUSB8040 REV B EVM Schematics

This appendix contains the TUSB8040 REV B EVM schematics.







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