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TSW3085EVM ACPR and EVM Measurements



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Design Resources

[Design Zip File](#)

[DAC3482](#)

[LMK04806](#)

[TRF3705](#)

[TSW1400](#)

[TSW3100](#)

Simulations, PCB, Gerber, BOM

Product Folder

Product Folder

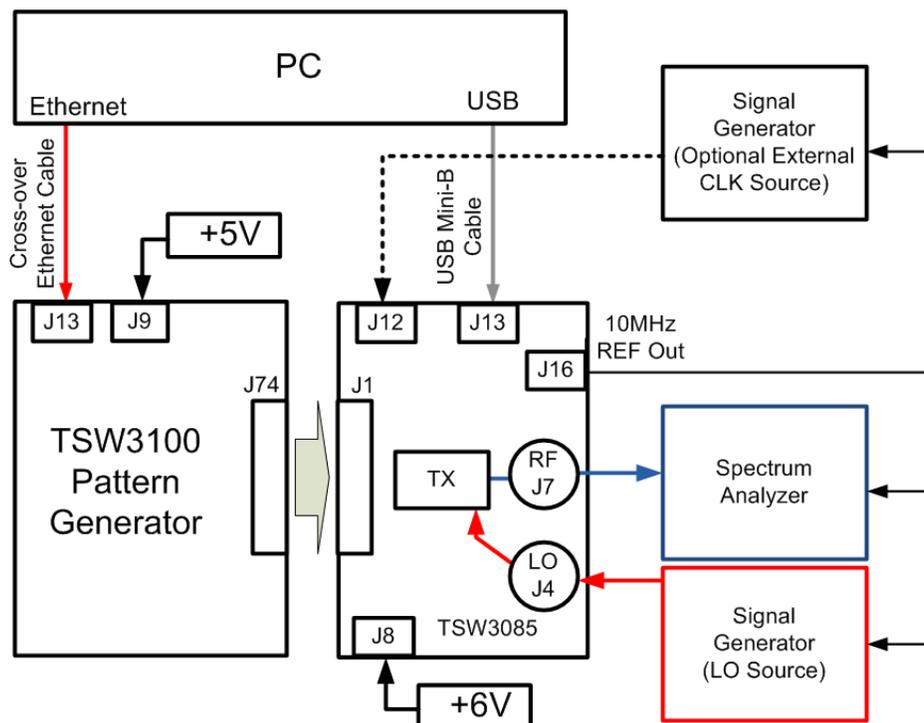
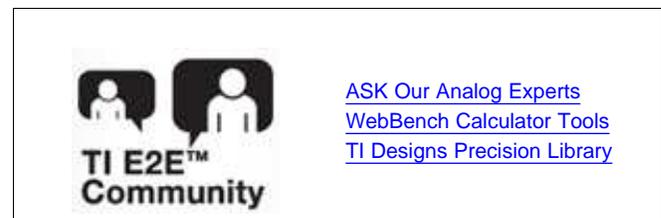
Product Folder

Tool Folder

Tool Folder

Design Description

This reference design discusses the use of the TSW3085EVM with the TSW3100 pattern generator to test adjacent channel power ratio (ACPR) and error vector magnitude (EVM) measurements of LTE baseband signals. By using the TSW3100 LTE GUI, patterns are loaded into the TSW3085EVM which is comprised of the DAC3482, TRF3705, and LMK04806B.



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1 Introduction

This application report discusses the use of the TSW3085EVM with the TSW3100 pattern generator to test adjacent channel power ratio (ACPR) and error vector magnitude (EVM) measurements of LTE baseband signals. By using the TSW3100 LTE GUI, patterns can be loaded into the TSW3085EVM which is comprised of the DAC3482, TRF3705, and LMK04806B.

Measuring ACPR and EVM performance of an LTE baseband signal is important because the amount of interference in the transmitted signal must be minimized in order for the data transmitted to be received clearly. Power transmitted in a desired channel can result in undesirable transmitted power in adjacent channels, and because regulations are set to allow transmission in specific bandwidths, this interference must meet minimum requirements.

The cause of power being transmitted in adjacent channels is from non-linearities of the signal chain; hence, linearity of the signal chain in transmitter systems is very important. Also important to the transmitter and receiver is the measure of EVM, which indicates the in-band signal to noise ratio and can be seen on a constellation plot. The deviation away from the ideal location for the constellation point is the EVM, usually measured in percentage, and can be caused by factors such as carrier leakage, image rejection ratio for 0 IF, clock, phase, and local oscillator (LO) noise.

As a solution for precise signal transmitting and receiving, the LMK04806B clock of the TSW3085EVM provides a clean clock in order for EVM measurements to remain low, while providing acceptable ACPR measurements using the DAC3482. Using a Rohde and Schwarz signal analyzer for demodulation of LTE signals, verification of EVM and ACPR is presented to verify that the TSW3085EVM provides exceptional testing of receive signal chain hardware.

2 TSW3085EVM Overview

The TSW3085 evaluation module contains the DAC3482 digital-to-analog converter, the LMK04806B clock, and the TRF3705 quadrature modulator. The 16-bit DAC3482 is capable of up to 16x interpolation and a sampling rate of 1.25GSPS. The LMK04806B clock generator and jitter cleaner uses cascaded PLLs and VCOs to provide a low-cost jitter cleaner as well as clock rates capable of up to 1536 MHz. Lastly, the TRF3705 modulator provides IF to RF upconversion, and the TSW3085EVM allows for measurements directly after the modulator or as a direct RF output after the power amplifier.

As shown in [Figure 1](#), the TSW3100 board is on the left and the TSW3085EVM is on the right. The connection in the middle that links the boards is the LVDS interface. The TSW3100 uses an Ethernet cable for loading the pattern from the computer using the LTE GUI and a USB-to-Ethernet adapter. Ensure that both boards have correct power connected, where 5 V is connected to the TSW3100 and 6 V is connected to the TSW3085. The TSW3085 is loaded using a USB-to-mini-USB cable from the computer. Lastly, the configuration of signals to and from the TSW3085 board are the optional external clock, LO, and RF output. The optional external clock set to 614.4 MHz is only used for testing the performance compared to the LMK04806B clock performance. The LO is set to 2 GHz and the RF output is the output LTE signal transmitted.

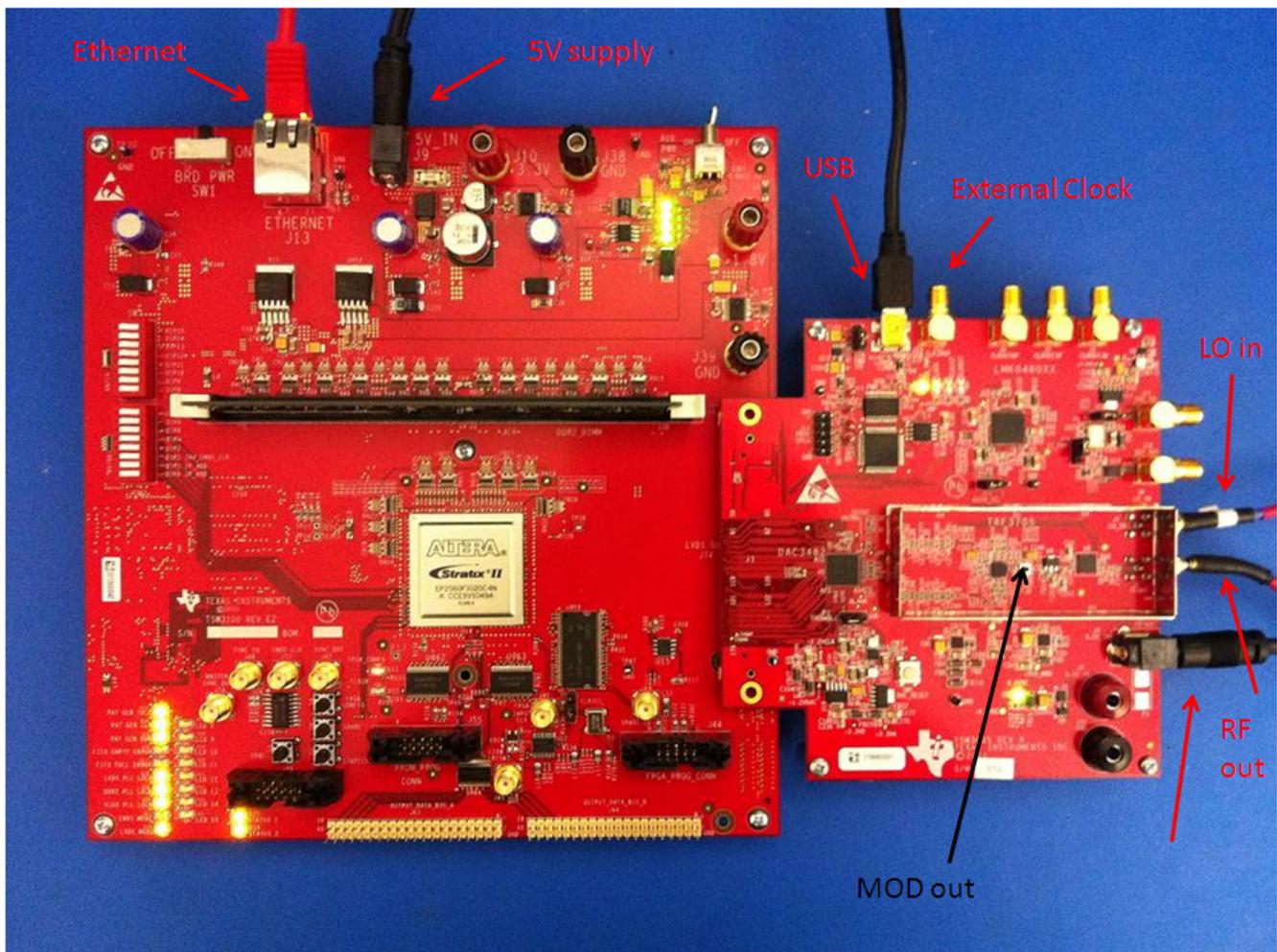


Figure 1. TSW3100 and TSW3085 Board Configuration

Figure 2 shows the internal blocks of components that are tested with the TSW3085EVM. Notice that the connections of USB, 6VDC, PLL1 REF_IN, LO_IN, and RF_OUT are also the same connections highlighted in Figure 1. PLL1 REF_IN is the external clock that overrides the LMK04806B clock source when selected as such in the GUI.

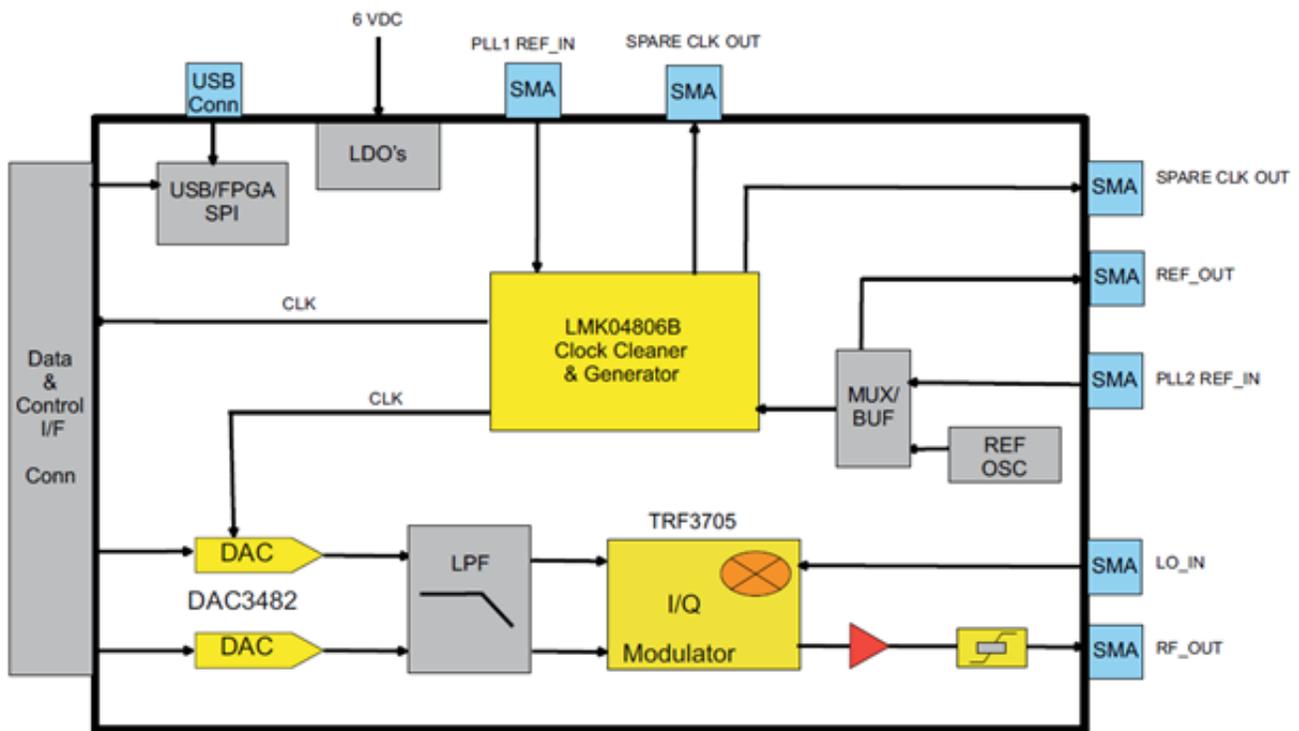


Figure 2. TSW3085 Block Diagram

Figure 3 shows the setup for testing LTE baseband signals using the TSW3085EVM with the TSW3100EVM with the onboard 10-MHz reference oscillator. Figure 4 shows the setup of devices when using an external 10-MHz reference oscillator. Notice that in both setups an optional external clock can be connected to J12. If the LMK04806B is to be used, then do not connect a signal generator to J12. For the onboard 10-MHz reference oscillator, a 10-MHz reference is taken from J16 and supplied to all external reference connections on the back of all test equipment. Jumpers JP4 and JP5 must be set to 1-2 for the onboard reference oscillator option as shown in the Figure 3 setup. Also ensure that all test equipment is set to external reference mode. For the setup in Figure 4, jumpers JP4 and JP5 are now set to pins 2-3, and the SMA connector J16 is no longer used. Instead, a signal generator is connected to J11 which is supplying the external 10-MHz reference. This signal generator is set to internal reference mode, while the signal generator for the LO source as well as the signal analyzer is set to external reference mode. The signal generator used for the external 10-MHz reference routes a reference from the back to the external reference connectors on the LO signal generator and signal analyzer.

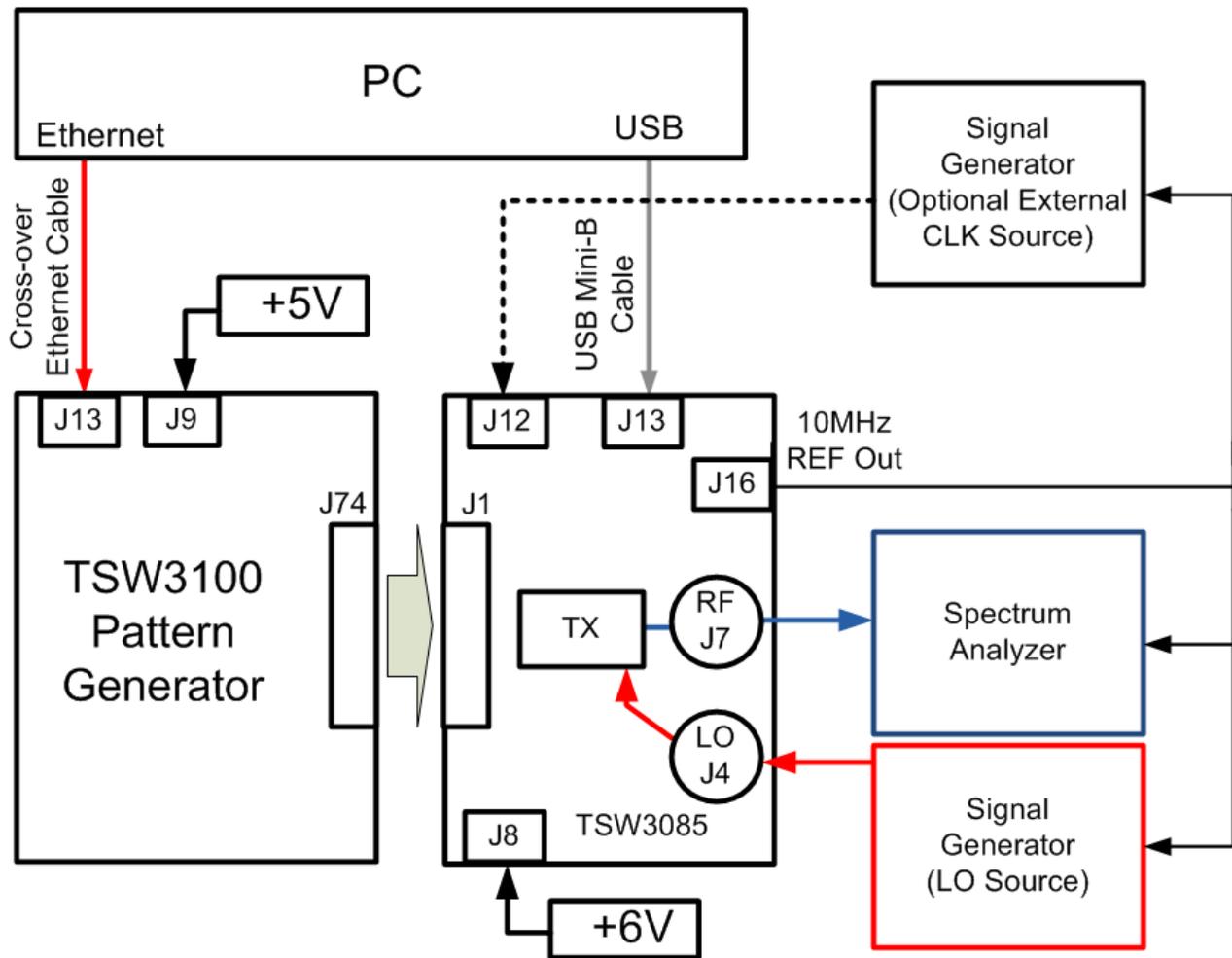


Figure 3. Testing Setup Using Onboard 10-MHz Reference Oscillator

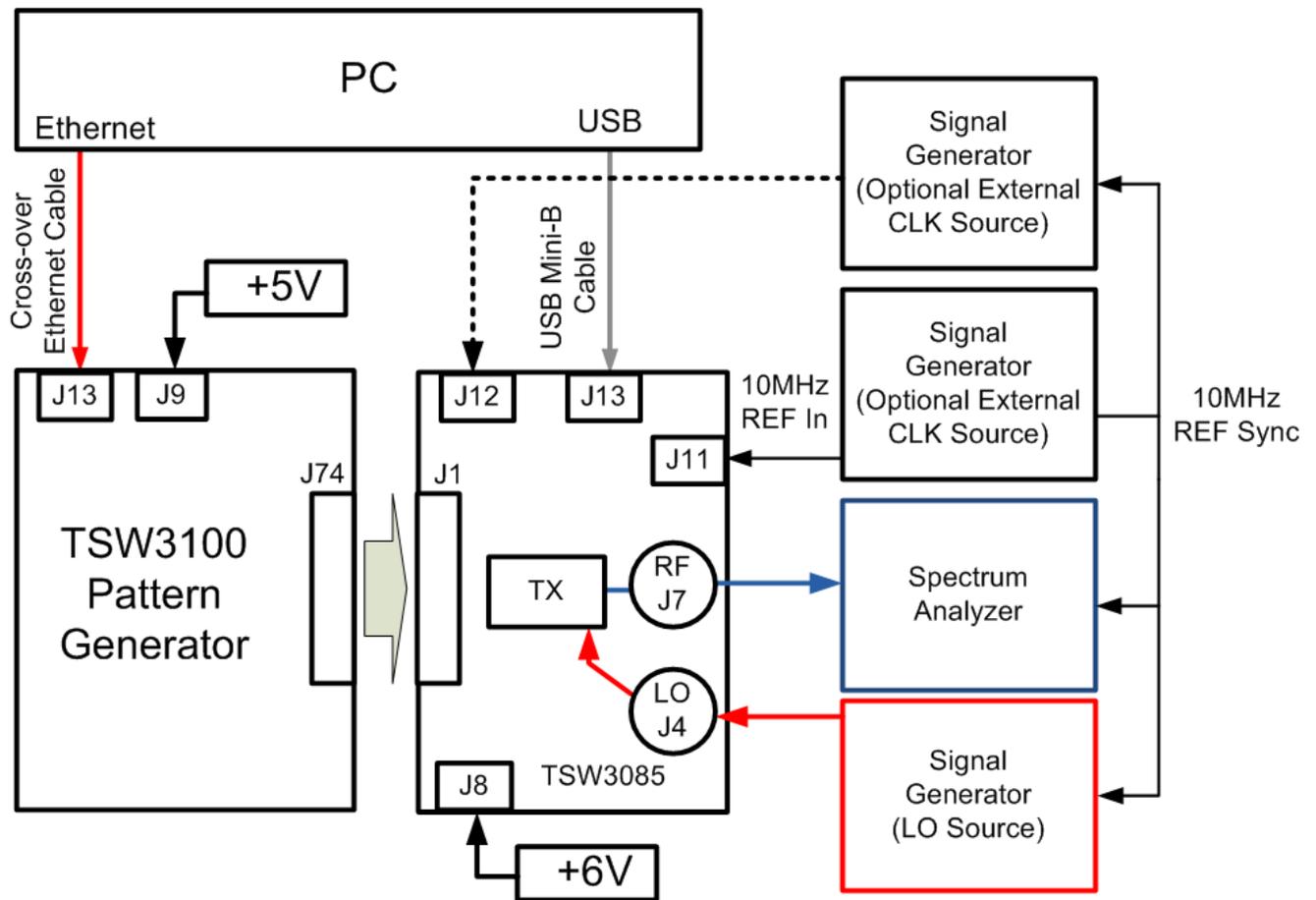


Figure 4. Testing Setup Using External 10-MHz Reference Oscillator

3 TSW3100 Configuration

The TSW3100 is used to load LTE baseband signal patterns to the TSW3085EVM. Multiple LTE bandwidths of 3, 5, 10, 15, and 20 MHz are available to test using the TSW3100 LTE GUI. Figure 5 shows the basic GUI view and the selection location for all bandwidths in the pulldown menu. Note that when using the TSW3085EVM with the TSW3100, the fractional output rate must be set to 307.2 MHz because the DAC3482 is set for 2x interpolation and receives a 614.4-MHz clock from the LMK04806B. Also, the TSW3085EVM uses LVDS signaling; therefore, ensure that the LVDS output is selected in the LTE GUI.

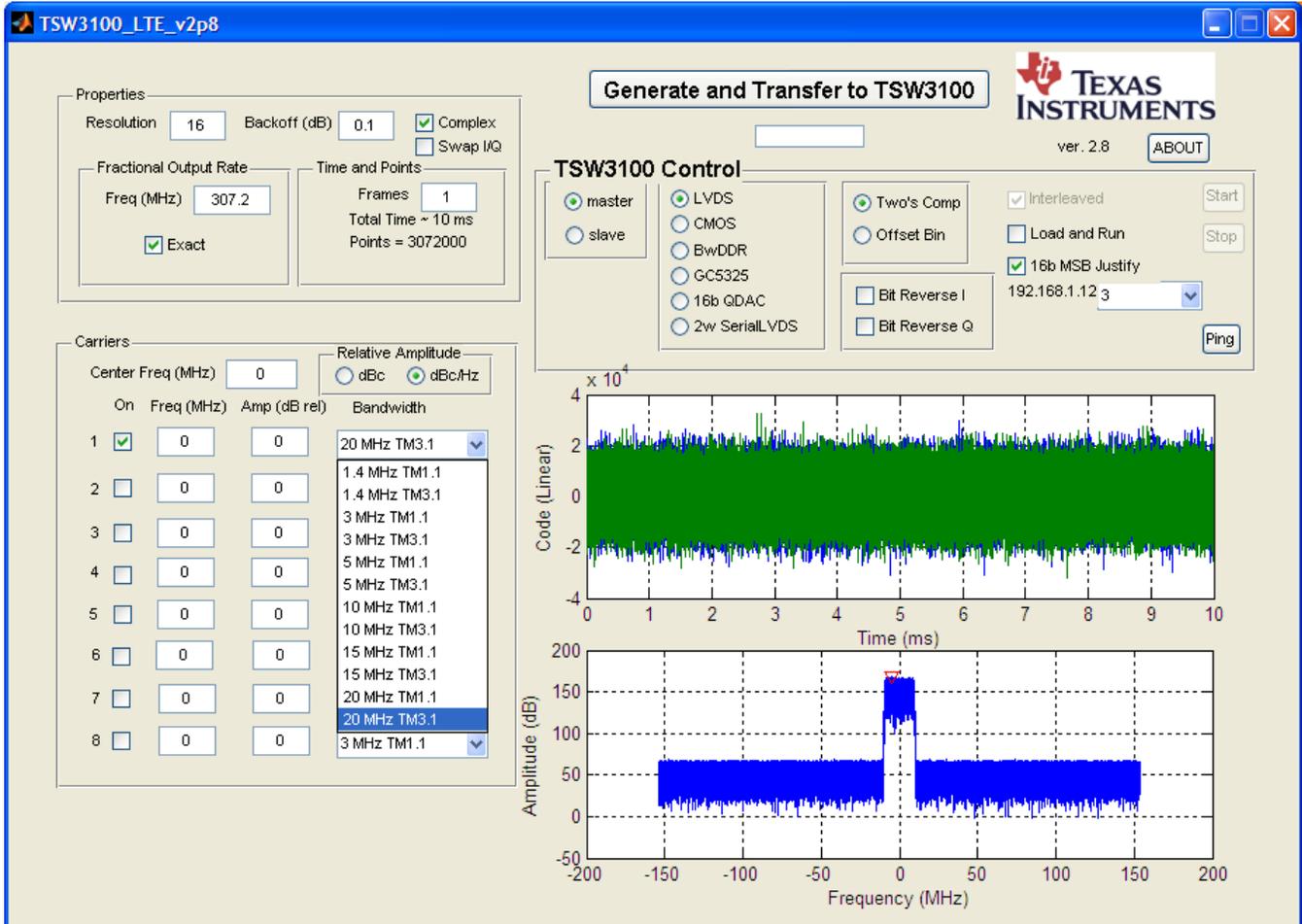


Figure 5. TSW3100 LTE GUI With TSW3085EVM Settings

4 ACPR and EVM Testing

Figure 6 through Figure 8 show ACPR measurements of the three most commonly used LTE bandwidths, 5, 10, and 20 MHz. The integrated noise power relative to the reference channel power is at least -70 dBc for all adjacent channels. The standard for ACPR measurements is required to be above 45-50 dBc, which shows that the performance of the complete signal chain is well above the minimum. All measurements for ACPR and EVM are taken at RF out, after the power amplifier, for the sake of a complete signal chain measurement.

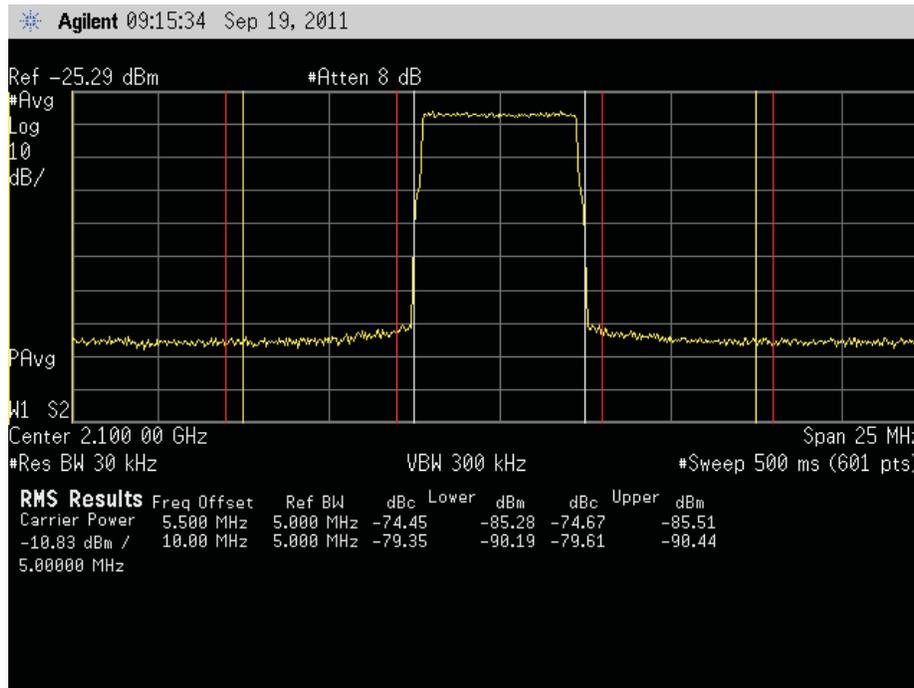


Figure 6. ACPR Measurement for 5-MHz Bandwidth

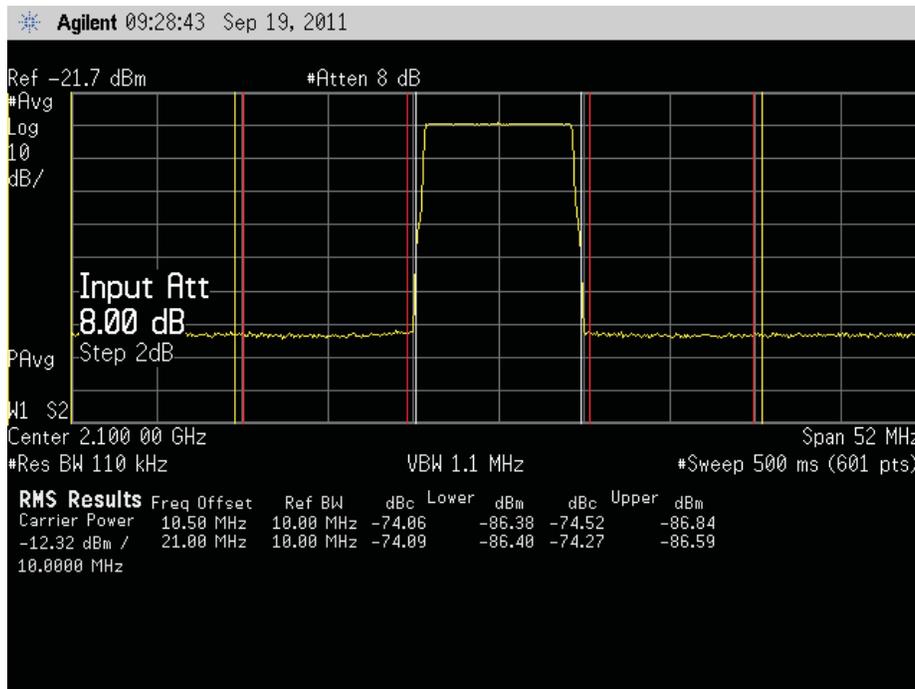


Figure 7. ACPR Measurement for 10-MHz Bandwidth

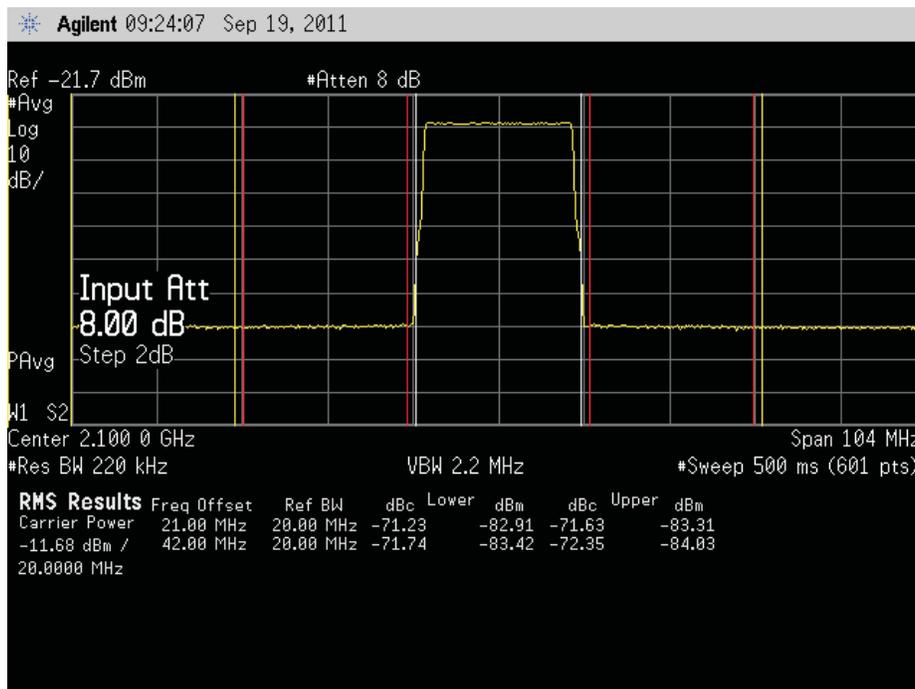


Figure 8. ACPR Measurement for 20-MHz Bandwidth

The measurements for EVM performance at specific conditions are shown in Table 1. The four test cases for testing EVM performance on the TSW3085EVM are using both the LMK04806B internal clock and external clock with 0 IF, as well as using the internal and external clock with 30-MHz IF. Testing these cases shows that the 0-IF can exhibit worse performance due to LO and sideband feedthrough versus the 30-MHz case which is not susceptible to these factors. Note that when testing EVM performance, criteria for antenna EVM is 8% to account for degradation in later signal chain manipulation with respect to gain criteria for transmission. In this case, degradation is not a factor and so to account for loss of EVM after the DAC and modulator, 1% EVM or less is the target for performance criteria. A 1% EVM translates to in-band noise deviation of -40 dB as shown by Equation 1.

$$EVM(dB) = 20 \times \log\left(\frac{1}{100}\right) = -40 \text{ dB} \tag{1}$$

For the first case with the TSW3085EVM tested with the internal clock at 0 IF, specific GUI settings must be set to account for correct measurements. Configuration files have been provided in the TSW3085 directory with default settings for the board. As shown in Figure 9, the GUI provides Load Regs and Send All buttons that allow the config file to be loaded with default DAC and TSW3100 clocking speeds. The default dividers and clock selection are preloaded as well and are outlined in Figure 9.

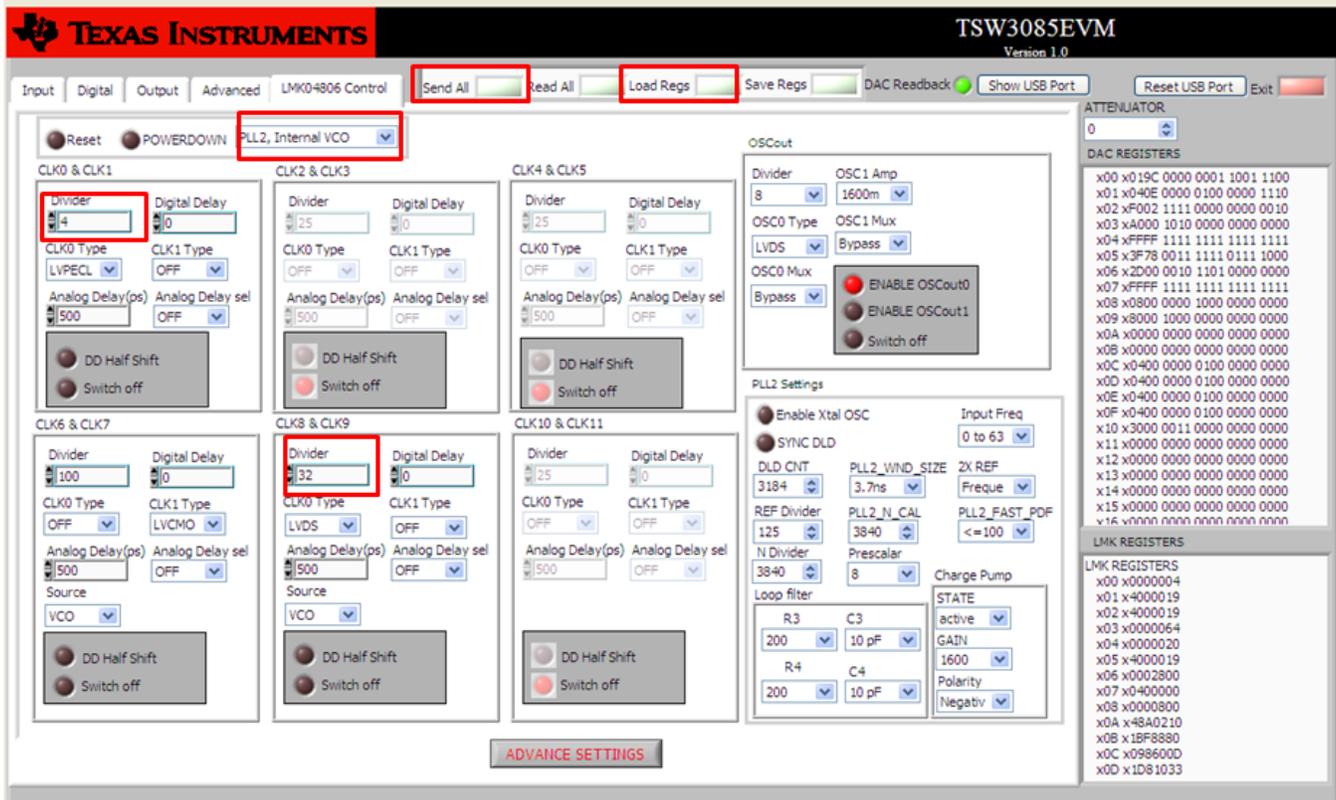


Figure 9. LMK04806B Internal Clock Configuration

When measuring EVM performance for the internal clock at 0 IF, the sideband and LO feedthrough caused degradation in EVM. This degradation is determined when QMC gain and phase as well as offset were altered, EVM performance improved to the values shown in Table 1. This reduction was approximately by 0.2% from the original values before QMC adjustments were performed. A detailed explanation for adjusting QMC and offset can be found in the TSW3085 user's guide.

Because the output of the DAC was at 0 IF, sideband and LO feedthrough possibly interfered with the carrier signal, which resulted in need for the QMC gain and phase to be changed to suppress the interference. To test the internal clock without this interference, the output of the DAC was shifted to 30-MHz IF. This resulted in slightly better EVM performance compared to 0 IF. Note that EVM results with a 30-MHz IF was tested with no alteration to QMC gain and phase because no overlap of sideband and LO feedthrough existed.

To further improve the internal clock case of 0 IF previously discussed, an external clock was used at the SMA connector CLKIN0P on the TSW3085EVM with 0 IF. In order for the TSW3085EVM to recognize the internal clock, settings in the GUI must be changed from the default settings as shown in Figure 10. Clock distribution was set to allow the TSW3085EVM to use an external clock. Because the external clock supplied is 614.4 MHz, the divide down for CLK0 must be changed from 4 to 1 as shown in Figure 8. Also, the CLK8 divider must be changed from 32 to 8, so that the speed is at 76.8 MHz for the TSW3100 pattern generator. The QMC gain and phase were also adjusted to reduce interference as was done with the internal clock. With the external clock at 0 IF, the EVM performance listed in Table 1 has only slightly improved from the internal clock EVM data. This shows that the LMK04806B is an excellent onboard clock solution.

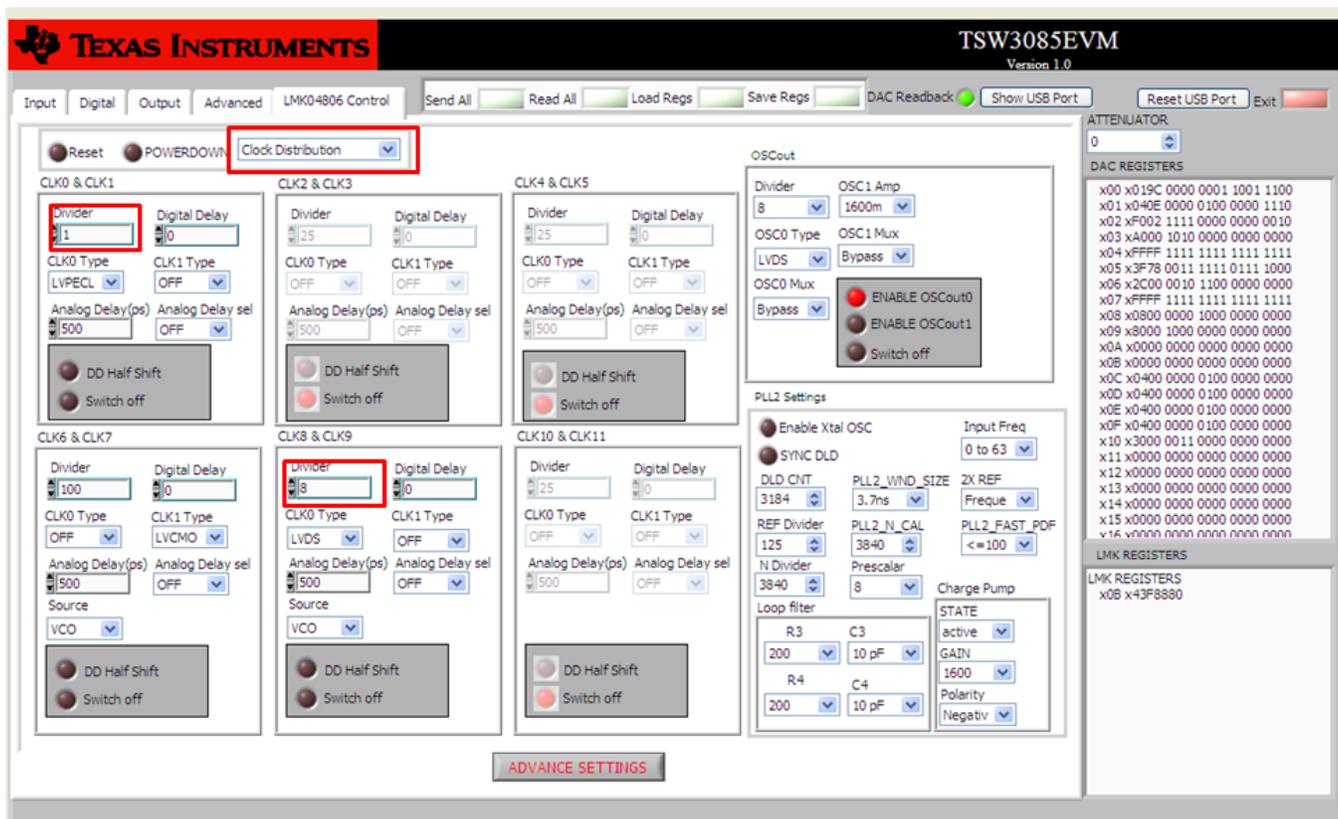


Figure 10. TSW3085 GUI Settings for External Clock

The case that improves EVM performance the most with respect to all the cases is running the setup with an external clock at 30-MHz IF. The external clock is a slightly cleaner source than the internal clock as was demonstrated, and with the 30-MHz IF, elimination of sideband interference can be achieved. As shown in Table 1, EVM percentages for this case are the lowest percentages measured from all four test setups; however, the LMK04806BEVM performance is no more than 0.2% from the external clock EVM data.

Table 1. EVM Performance Measurements

Frequency	EVM (%): External Clock With 0 IF	EVM (%): Internal Clock With 0 IF	EVM (%): External Clock With 30-MHz IF	EVM (%): Internal Clock With 30-MHz IF
3 MHz at cell ID 1	0.39	0.47	0.34	0.42
3 MHz at cell ID 2	0.40	0.48	0.36	0.44
5 MHz at cell ID 1	0.49	0.56	0.40	0.48
5 MHz at cell ID 2	0.53	0.58	0.44	0.50
10 MHz at cell ID 1	0.32	0.35	0.28	0.35
10 MHz at cell ID 2	0.35	0.41	0.30	0.40
15 MHz at cell ID 1	0.27	0.32	0.21	0.30
20 MHz at cell ID 1	0.30	0.41	0.25	0.41
20 MHz at cell ID 2	0.31	0.39	0.25	0.37

5 Summary

Testing the TSW3085EVM for ACPR and EVM performance is one of the most important tests done with DAC, clock and modulator hardware. Also important to baseband signal testing is WCDMA testing, but for sake of newer technologies, LTE is a prevalent competitor and important communication standard. As the results above show, the EVM performance of all testings met specified criteria. Notice that an IF other than zero does produce slightly better results by eliminating feedthrough from unwanted sources. This was best shown with the test data comparing a 30-MHz IF to 0 IF, where feedthrough is not directly in-band with the LTE signal. Lastly, the results obtained comparing internal and external clocks indicate that the onboard LMK04806B clock generator has great jitter performance when compared to a laboratory-quality clock source and is more than adequate for use in clocking LTE communication transmit applications.

6 References

1. TSW3100 user's guide ([SLLU101](#))
2. TSW3085EVM user's guide ([SLAU364](#))
3. *Basic RF Testing of CCxxx Devices* application report ([SWRA370](#))
4. Bhattacharya, S.; Srinivasan, G.; Cherubal, S.; Chatterjee, A.; , "Test time reduction for ACPR measurement of wireless transceivers using periodic bit-stream sequences", *Electronic Design, Test and Applications, 2004. DELTA 2004. Second IEEE International Workshop on* , vol., no., pp. 372-377, 28-30 Jan. 2004

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