ABSTRACT

This user's guide describes the operation and use of the ADS8688 evaluation module (EVM). The ADS8688 is a 16-bit, 500ksps, 8 channel multiplexed, single-supply, SAR ADC with bipolar input ranges. Operating on a single 5V the integrated analog front end can support ±10.24V input ranges with a ±20V over-voltage protection. The performance demonstration kit (PDK) eases EVM evaluation with additional hardware and software for computer connectivity through a universal serial bus (USB). The ADS8688EVM-PDK includes the ADS8688EVM as a daughter card, Precision Host Adaptor (PHI) digital controller, and a A-to-B USB cable. This user's guide covers circuit description, schematic diagram, and bill of materials for the ADS8688EVM daughter card.

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<table>
<thead>
<tr>
<th>Device</th>
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<td>ADS8688</td>
<td>SBAS582</td>
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<tr>
<td>OPA320</td>
<td>SBOS513</td>
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<td>TPS7A4700</td>
<td>SBVS204</td>
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1 Trademarks
All other trademarks are the property of their respective owners.
2 ADS8688EVM-PDK Overview

Table 1-1 lists the related documents that are available for download from Texas Instruments at

**ADS8688EVM Features**

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8688 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS8688 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft Windows™7, Windows 8, and Windows 10 operating systems
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing. Fig
- Integrated 4.096-V voltage reference.
- Bipolar (±10.24 V, ±5.12 V, ±2.56 V) or unipolar (0 V to 10.24 V, 0 V to 5.12 V) input ranges for each channel.
- Onboard, second-order, Butterworth, low-pass filters for four channels.
- Onboard regulator for generating a ±15-V bipolar supply for second-order, Butterworth, low-pass filters.
- Capable of accepting a ±100-mV signal on the negative analog inputs (AIN_xGND).

![Figure 2-1. System Connection for Evaluation](image)

**ADS8688EVM Features:**

- Eight input channels connected to external single ended signals source applied to SMA connectors or header
- Serial interface connects to the PHI controller via 60 pin connector (J3).
- Serial interface connects to the PHI controller via 60 pin connector (J2).
- All power for device from USB via PHI controller.
- Onboard ultra-low noise low-dropout (LDO) regulator generates 5.0V AVDD supply. Input to LDO from PHI controller.
- DVDD (3.3V) powered by PHI controller.
3 EVM Analog Interface

The ADS8688EVM is an evaluation module built to the TI Modular EVM system specifications. The EVM by itself has no microprocessor and cannot run software. Thus, the EVM is available as part of the ADS8688EVM-PDK kit that combines the ADS8688EVM as a daughter board with PHI controller using software as a graphical user interface (GUI).

3.1 ADC Analog Input Connections and Filter

The circuit shown in Figure 3-1 shows a typical analog input connection for the ADS8688 ADC. This circuit is repeated eight times for all eight input channels. The resistor R01 can be used for input float detection but is not populated in the default configuration. The TVS diode D01, can be used for input protection, but is not populated. Refer to Video Series on Electrical Overstress. C01, R03, and R04 form the 79.5kHz low pass input the input filter for the ADC. R05 connects the negative input to ground. R05 can be removed and the negative input can be accessed in the header J6.

Figure 3-1. ADC Analog Input Connections and Filter
3.2 Voltage Reference, Aux Input, and Supply Decoupling

The circuit shown in illustrates the decoupling on AVDD, DVDD, and the reference IO. It is possible on the ADS8688 to use an external voltage reference, but typically the integrated internal reference is sufficient. In cases where you need to use an enthral voltage reference it can be connected via the REF test point. The capacitors for decoupling match the recomendations in the ADS8688 data sheet. The layout (see Figure 8-1) uses the shortest possible connections to the decouplign capacitors and connections the ground end to the GND plane using vias. The AUX input is a standard SAR input and does not have an analog front end. Thus, this input cannot accept high voltage input signals (Vin Full Scale = VREF = 4.096V). Furthermore, this input requires an external buffer amplifier U4 to achieve good settling.

![Figure 3-2. Voltage Reference, Aux Input, and Supply Decoupling](image-url)
4 Digital Interface

As noted in Section 2, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS8688 ADC (over SPI) and the EEPROM (over I2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS8688 platform. When the hardware is initialized, the EEPROM is no longer used.

4.1 Serial Interface (SPI)

As noted in Section 2, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS8688 ADC (over SPI) and the EEPROM (over I2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS8688 platform. When the hardware is initialized, the EEPROM is no longer used.

4.2 I2C Bus for Onboard EEPROM

The circuit shown in Figure 4-1 is used with our EVM controller (PHI), for EVM identification. This circuit is not required by the ADS8688 for operation. The switch (S2) is a write protect and does not need to be changed for EVM operation.

![Figure 4-1. EEPROM for EVM ID](image-url)
5 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the USB supply of the computer. The EEPROM on the ADS8688EVM uses a 3.3-V power supply generated directly by the PHI. The EVM_REG_5V5 is a 5.5V supply from the PHI and is applied to the input of a low dropout regulator (LDO) to generate AVDD on the EVM. The analog supply of the ADC (AVDD = 5.0V) is powered by the TPS7A4700RGWR (U3). The ADC Digital supply (DVDD = 3.3V), is generated by the PHI. Two LEDs are connected to the AVDD, and DVDD supplies. These LEDs will illuminate after the software GUI loads and the PHI turns on its output power supplies.

Figure 5-1. Power Supplies, Regulators, and Indicators
6 ADS8688 Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for properly operating the ADS8688EVM.

6.1 Software Installation

Download the latest version of the EVM GUI installer from the Tools and Software folder of the ADS8688EVM and run the GUI installer to install the EVM GUI software on your computer.

**CAUTION**

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the installer. The exe file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 6-1 to complete the installation.

![Figure 6-1. ADS8688 Software Installation Prompts](image-url)
As a part of the ADS8688EVM GUI installation, a prompt with a Device Driver Installation (as shown in Figure 6-2) appears on the screen. Click Next to proceed.

![Device Driver Installation Wizard](image1)

**Figure 6-2. Device Driver Installation Wizard Prompts**

The ADS8688EVM requires the LabVIEW™ run-time engine and may prompt for the installation of this software, as shown in Figure 6-3, if not already installed.

![LabVIEW Run-Time Engine Installation](image2)

**Figure 6-3. LabVIEW Run-Time Engine Installation**
Verify that C:\Program Files (x86)\Texas Instruments\ADS8688EVM is as shown in Figure 6-4 after these installations.

![Figure 6-4. ADS8688EVM GUI Folder Post-Installation](image)
7 EVM Operation

The following instructions are a step-by-step guide to connecting the ADS8688EVM to the computer and evaluating the performance of the ADS8688:

7.1 Connecting the Hardware

After installing the software connect the EVM as shown in Figure 7-1
1. Physically connect P2 of the PHI to J2 of the ADS8688EVM. Install the screws to assure a robust connection
2. Connect USB on PHI to the computer first
   • LED D5 on the PHI lights up, indicating that the PHI is powered up
   • LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 7-1 shows the resulting LED indicators
3. Start the software GUI as shown in Figure 7-2. You will notice that the LEDs blink slowly as the FPGA firmware is loaded on the PHI. This will take a few seconds then the AVDD and DVDD power supplies will turn on.
4. Connect the signal generators to SMA inputs or headers (8 channels available). The input range is ±10.25V.

Figure 7-1. ADS8688EVM Hardware Setup and LED Indicators

Figure 7-2. Launch the EVM GUI Software
7.2 EVM GUI Global Settings for ADC Control

Section 7.2 shows that the EVM Global controls are located on the right hand side of the GUI. These controls choose the page display, SPI Mode, SCLK frequency, and sampling frequency.

- **Pages** selects the analysis display.
- **EVM GUI Global Settings for ADC Control** are on the left hand side of the GUI.
- The SCLK frequency is set here. It is limited by the "Sampling Rate" below.
- The maximum sampling rate is 500kHz for this device.
- The “Channel Range” sets the input voltage range.
- Auto mode will scan the selected channels below. Manual allows selection of one channel.

![Figure 7-3. EVM GUI Global Input Controls](image-url)
7.3 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. The user can trigger a capture of the data of the selected number of samples from the ADS8688EVM, as per the current interface mode settings indicated in Figure 7-4 by using the Capture button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

Figure 7-4. Time Domain Display Tool Options
7.4 Frequency Domain Display

The spectral analysis tool, shown in Figure 7-5, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8688 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The None option corresponds to not using a window (or using a rectangular window) and is not recommended.

Figure 7-5. Spectral Analysis Tool
7.5 Histogram Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel. As shown in Figure 7-6, the histogram corresponding to a DC input is displayed on clicking the Capture button.

![Histogram Analysis Tool](image)

**Figure 7-6. Histogram Analysis Tool**
8 Bill of Materials, Schematics, and Layout

Schematics for the ADS8688EVM are appended to this user's guide. The bill of materials is provided in Table 8-1. Section 8.2 shows the PCB layouts for the ADS8688EVM.
8.1 Bill of Materials

Note

All components are compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see www.ti.com.)

Table 8-1. ADS8688EVM Bill of Materials

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<th>Item #</th>
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<th>Value</th>
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<td>31</td>
<td>D01, D11, D21, D31, D41, D51, D61, D71</td>
<td>0</td>
<td>14V</td>
<td>SMBJ14CA</td>
<td>Littelfuse</td>
<td>Diode, TVS, Bi, 14 V, SMB</td>
<td>SMB</td>
</tr>
<tr>
<td>32</td>
<td>FID1, FID2, FID3</td>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Fiducial mark. There is nothing to buy or mount.</td>
<td>N/A</td>
</tr>
<tr>
<td>33</td>
<td>R01, R11, R21, R31, R41, R51, R61, R71</td>
<td>0</td>
<td>49.9k</td>
<td>CRCW060349K9FKEA</td>
<td>Vishay-Dale</td>
<td>RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603</td>
<td>0603</td>
</tr>
</tbody>
</table>
8.2 Board Layouts

Figure 8-1 through show the PCB layouts for the ADS8688EVM.

Note

Board layouts are not to scale. These figures are intended to show how the board is laid out; these figures are not intended to be used for manufacturing ADS8688EVM PCBs.

Figure 8-1. ADS8688EVM PCB: Top Layer (L1)

Figure 8-2. ADS8688EVM PCB: Bottom Layer
8.3 Schematic

Figure 8-3 shows the input filter, terminal block, and SMA connections.
Figure 8-3. Input Filer
Figure 8-4 shows the input filter, terminal block, and SMA connections.
Figure 8-5 shows power and EEPROM connections.

Figure 8-5. Power and EEPROM
9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2014) to Revision B (September 2020)

- Updated the numbering format for tables, figures and cross-references throughout the document........................................3
- Every section in this document has significantly changed as the hardware and software went through major revisions. ............................................................................................................................................................3
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