BURR-BROWN®

DEM-PCM3500

EVALUATION BOARD

INSTRUCTION MANUAL

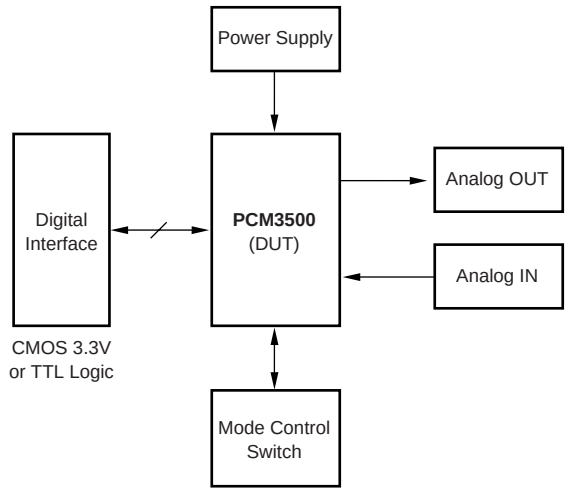
FEATURES

- **EVALUATION BOARD FOR THE PCM3500 MODEM/VOICE CODEC**
- **DIP SWITCH FOR SETTING HARDWARE MODE CONTROLS**
- **CONNECTORS FOR SERIAL INTERFACE, SYSTEM CLOCK, ANALOG INPUT/OUTPUT, AND POWER SUPPLIES**
- **PROTOTYPE AREA FOR BUILDING ANALOG FRONT END (AFE) CIRCUITS**
- **SINGLE POWER SUPPLY: +2.7V to +3.6V**

DESCRIPTION

The DEM-PCM3500 is a simple evaluation board for the PCM3500 single-channel CODEC. It is designed for quick evaluation of the PCM3500 features and performance. A prototype area allows for external analog input and output circuitry to be mounted directly on the evaluation board.

BLOCK DIAGRAM



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CONNECTORS

CN1 is the power supply connector for the DEM-PCM3500. The $+V_{CC}$ pin may be set between +2.7V and +3.6V. The GND pin should be connected to the negative (–) or ground terminal of the power supply or battery, and functions as the analog ground connection.

CN2 is the host interface connector. It includes connections for the serial interface and system clock input/output. The connector pins correspond directly to the pin names of the PCM3500. Refer to the PCM3500 data sheet for more details regarding the operation and requirements for these connections.

CN3 is the analog input connector. The V_{IN} pin is connected to the PCM3500 analog-to-digital converter input, while the GND pin is connected to analog ground. The full-scale input voltage for V_{IN} is $0.6V_{CC}$ (in Vp-p), or 1.8Vp-p for a +3V power supply.

CN4 is the analog output connector. The V_{OUT} pin is connected to the PCM3500 digital-to-analog converter output, while the GND pin is connected to analog ground. The full-scale output voltage at V_{OUT} is typically $0.6V_{CC}$ (in Vp-p), or 1.8Vp-p for a +3V power supply.

DIP SWITCH SETTINGS

Table I shows the function of each switch setting for SW1. Each switch corresponds directly to a pin of the PCM3500. Refer to the PCM3500 data sheet for more details regarding the operation and requirements for these pin functions.

SW1	DESCRIPTION
PWDN	H = Power Down Disabled (normal operation) L = Power Down Enabled
LOOP	H = ADC-to-DAC Loop Back Enabled L = ADC-to-DAC Loop Back Disabled
HPFD	H = ADC High Pass Filter Disabled L = ADC High Pass Filter Enabled
T/S	H = Time Slot Mode Enabled L = Time Slot Mode Disabled
M/S	H = Master Mode Enabled L = Slave Mode Enabled

TABLE I. DIP Switch Settings.

CRYSTAL OSCILLATOR OPERATION

The PCM3500 contains an internal crystal oscillator circuit. The oscillator can be used to generate the $512f_S$ system clock (512 times the desired sample frequency). The crystal value must be equal to $512f_S$. A fundamental mode, parallel resonant crystal is recommended. The load capacitors, C_S, should be set in the range from 10pF – 33pF, with 22pF being the typical value. When using the crystal oscillator, BCK and FS should be derived from SCKIO when using Slave mode. Alternatively, the PCM3500 may be set to Master mode so that the BCK and FS are generated by the CODEC itself.

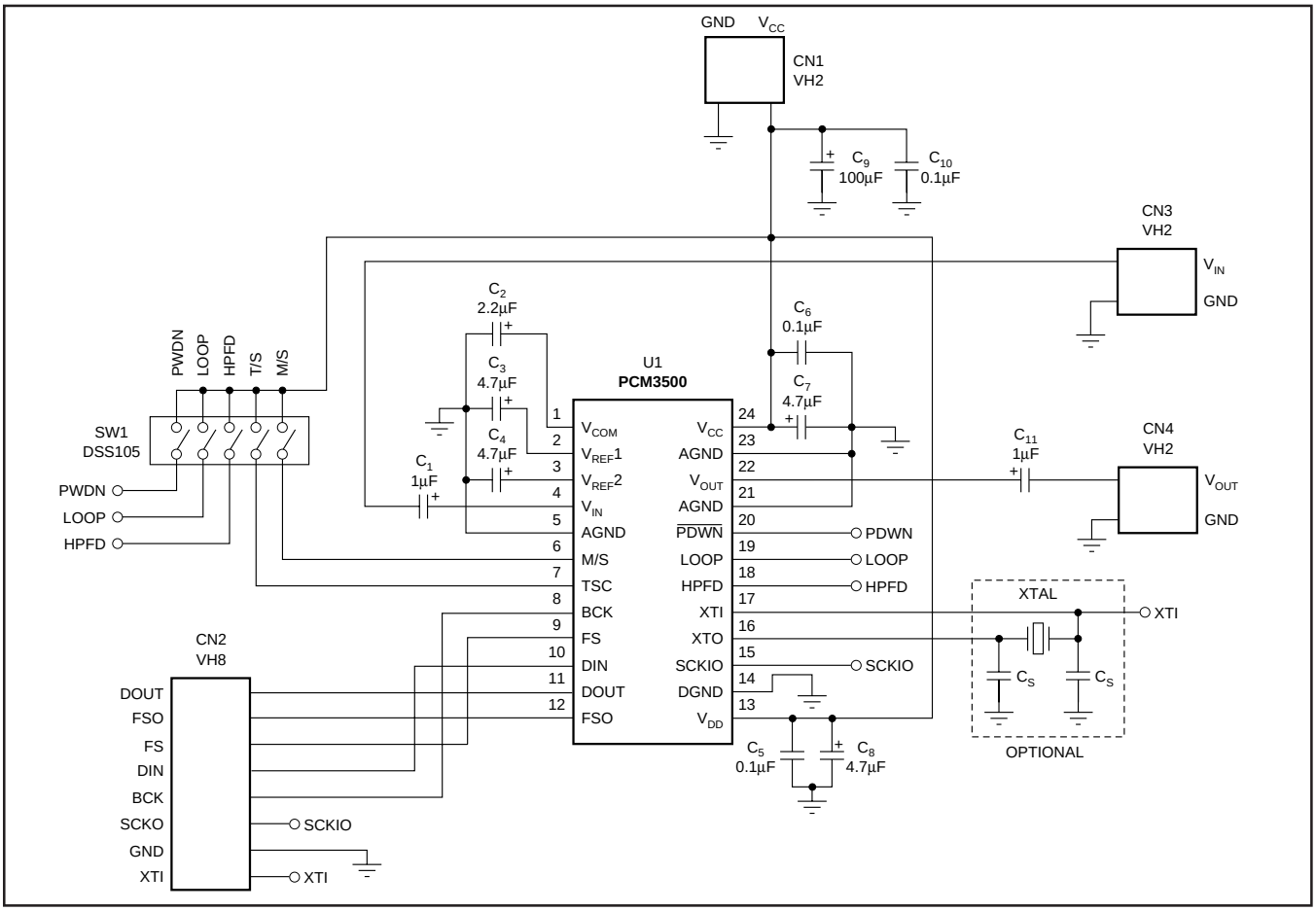
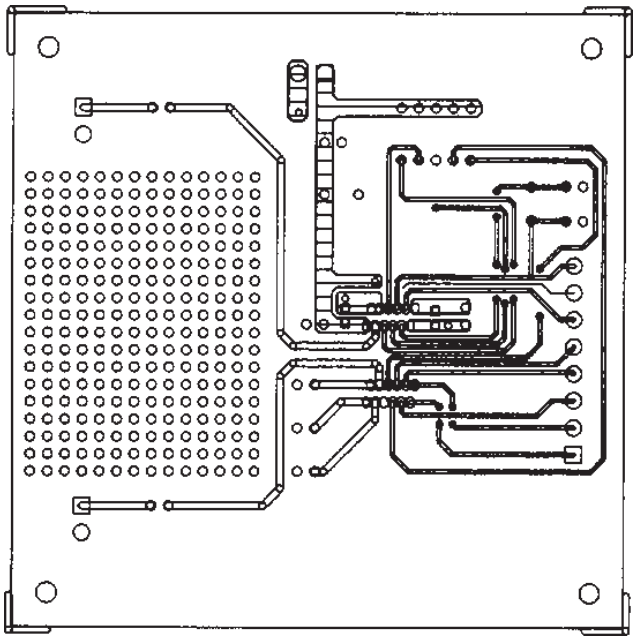


FIGURE 1. Schematic.



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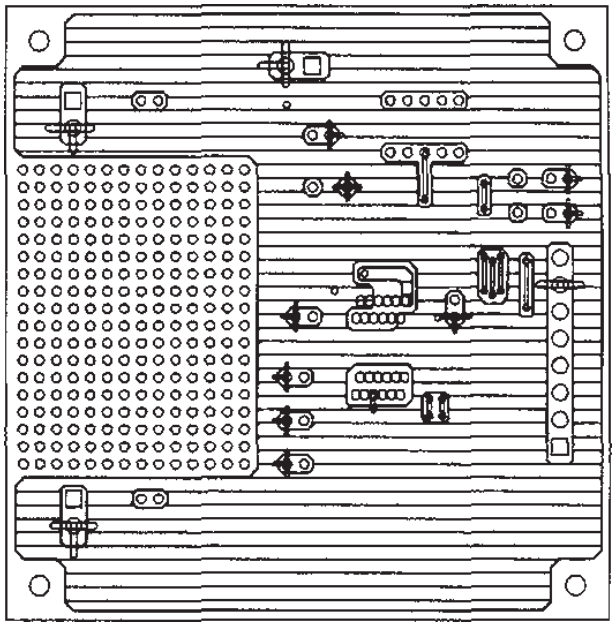

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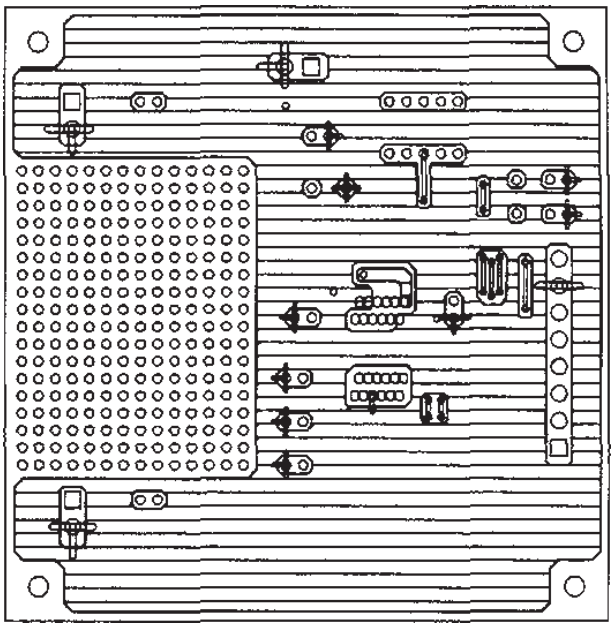

Silk Screen

FIGURE 2. Printed Circuit Board Plots.

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