DLPC4422 Software Programmer's Guide

User's Guide

Literature Number: DLPU060
July 2017

Scope

This guide details the software interface requirements for a DLPC4422 controller used in conjunction with a digital micromirror device (DMD). It defines all applicable communication protocols including I²C, initialization, default settings, timing and control register bit definitions. See Figure 1-1 and Figure 1-2.

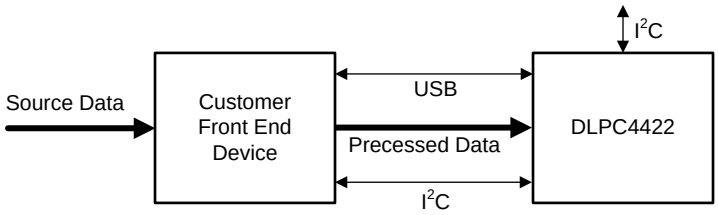

Figure 1-1. Single ASIC Data Processing Block Diagram

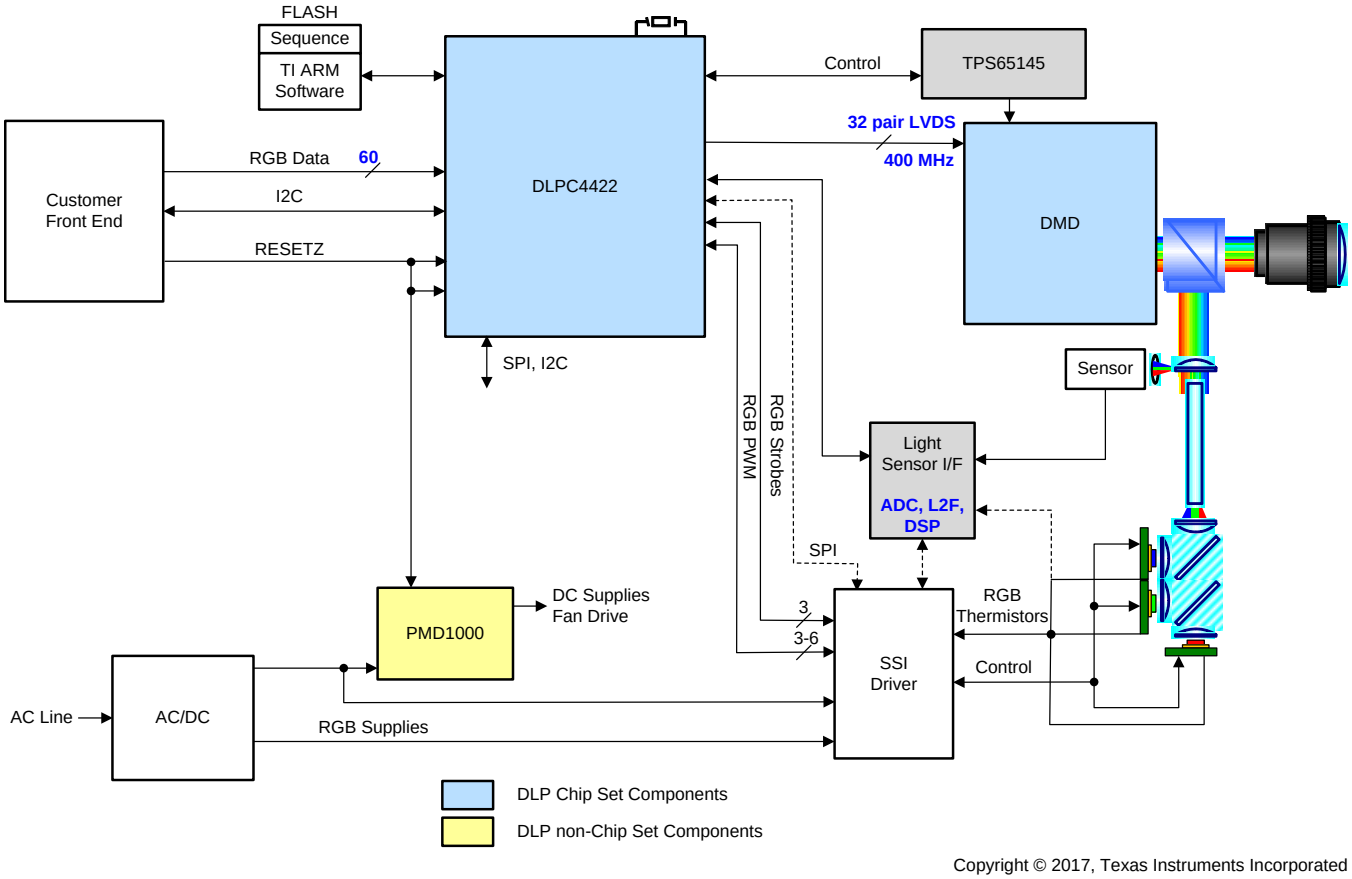

Figure 1-2. Single ASIC System Block Diagram

Applicable Documents

The following documents are for reference only.

1. DLPC4422 Datasheet
2. I^2C Bus Specification - Philips Semiconductor 1994 Desktop Video Data Handbook.

Interface Protocol

3.1 Interface Standard

The protocol used in communicating information to the DLPC4422 consists of a serial data bus conforming to the Philips I²C specification up to 400 KHz. A USB 1.1 slave interface is also supported for reprogramming the parallel flash device. Parallel flash programming is also supported over the I²C interface.

3.2 I²C Slave Receive Mode

With the DLPC4422 operating in the I²C slave-receiver configuration, the first byte following the start condition is the DLPC4422 device write address (34h). The interface consists of a number of sub-address registers each capable of accepting multiple bytes of data. Each command/sub-address expects a certain number of data bytes. The number of data bytes for each command/sub-address is described in Chapter 5. Sending the wrong number of bytes to a sub-address is not an error. If too few bytes are sent, the entire transaction is ignored. If too many bytes are sent, the correct number of bytes is used and the extra bytes are ignored. The I²C address for the command interface is 8-bit, followed by an 8-bit sub-address. The sub-address is followed by data bytes of variable lengths. The length of bytes written depends upon the sub-address.

Table 3-1. Write Command Structure

Address	Sub-Address	Data
(8-bit)	*(8-bit)*	*(n-bytes…)*
0x34	CMD	0xdd 0xdd 0xdd 0xdd 0xdd …

3.3 I²C Slave Transmit Mode

With the DLPC4422 operating in the slave-transmitter configuration, the first byte following the start condition is the DLPC4422 device read address (35h). Two bytes of system status will be returned to the host followed by the additional bytes containing system hardware values or firmware information.

Table 3-2. Read Command Structure

Address	Sub-Address	Extended- Address	Data	
(8-bit)	(8-bit)	(8-bit)	(16-bit)	(n-bytes…)
0x35	0x15	CMD	STAT	0xdd 0xdd

3.4 I²C Protocol

Figure 3-1 shows the I²C structure format and a partial I²C command table used in TI software. Only single byte commands are supported when using the I²C interface. This limits the number of commands supported over the I²C interface to 255 commands (0x01-0xFF) – command 0x00 is reserved for the USB interface. The two-byte commands are only supported when using the USB interface. This is done for the purpose of using the same I²C command table for both the I²C and USB interfaces and allows the USB interface to support up to 65535 commands.

```
/* I2C command structure */
typedef struct command_table
{
   uint08  Cmd;                    /* Command */
   uint08  BytesIn;                /* The Number of bytes for write command */
   uint08  BytesOut:               /* The number of bytes for read  command */
   int08   (*fnI2CWrite)(uint08*); /* Write handler */
   int08   (*fnI2CRead)(uint08*);  /* Read handler */
   bool    SendToSlave;            /* Send command to slave ASIC */
   uint08  SpecialFlag;            /* Special Commands indicator */
} I2C_COMMAND_TABLE;

/* I2C command table */
const I2C_COMMAND_TABLE I2CCommandTable[]=
{
/*  Cmd   BytesIn  BytesOut  fnI2CWrite          fnI2CRead           SendToSlave   SpecialFlag */
    0x00,  0x02,    0x02,    DoNothing,         USBStatus,          TRUE           0,
    0x01,  0x06,    0x06,    ImpSetBrightness,  ImpGetBrightness,  TRUE           0,
    0x02,  0x06,    0x06,    ImpSetContrast,    ImpGetContrast,    TRUE           0,
    0x15,  0x02,    0x02,    ReadCmd,           DoNothing,         FALSE          0,
};
```

Figure 3-1. I²C Structure and Command Table

Figure 3-2 shows a couple of examples of how both a write and a read are formatted, transmitted, and received over the I²C interface. All values shown are in hex format. Figure 3-2(a) shows the format for a write command. Figure 3-2(b) shows how to set the contrast using command 0x02 followed by six bytes of data. Since this command is a write, the projector executes the "fnI2CWrite" in the I²C command table, which is ImpSetContrast. The six bytes of data following the command represents the RGB values – two bytes for each color. In this example 0x0340 would be the setting for Red, 0x0340 would be the setting for Green, and 0x0340 would be the setting for Blue.

Figure 3-2(c) shows how to read the contrast settings from the projector. First note that a read command always uses a Write Address of 0x35 and is followed by command 0x15. Command 0x15 requests data from the projector and executes the "fnI2CRead" in the I²C command table. The "fnI2CRead" to execute is indicated by the command in the data portion, which in this example is 0x02, which is the ImpGetContrast. The host should then continue the I²C transaction with a Restart-Read, followed by the number of bytes associated with the command, then two bytes of status, and finally the Stop. Continuing in Figure 3-2(c), 0x0701 are the two bytes of status followed by the six bytes of RGB contrast data.

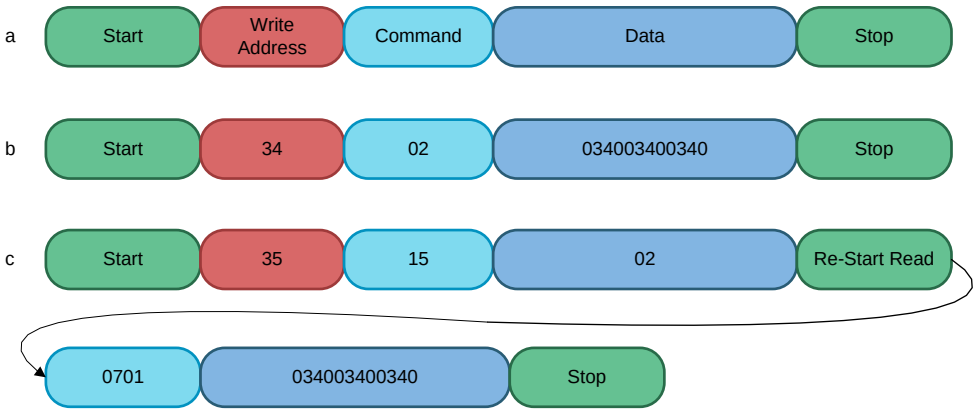

Figure 3-2. I²C Write and Read Examples

3.5 Reserved Areas

When writing to valid registers, all unused/reserved bits should be set to zero. Reserved registers should never be written to. When reading valid registers, all unused/reserved bits should be ignored.

3.6 USB

The USB port in the DLPC4422 ASIC is a full speed slave conforming to USB 1.1 specifications. The USB configuration and device descriptors used in the TI software conform to the USB HID specifications. This eliminates the need to write special host drivers to enumerate and communicate with the projector. The host should use its built-in HID drivers to enumerate the projector USB device. The projector's HID device is configured as an interrupt device with a 64-byte buffer and is preceded with a report-ID, which is set to 0x00. The report-ID is important because it identifies which device is being used on the projector.

Since the projector's HID device uses a 64-byte buffer, it is required that 65 bytes is always transmitted and received between the host and the projector's HID device regardless if the command contains less than 64 bytes. The one-byte report-ID is added to the 64-byte buffer, which is called a complete 65 byte "packet". If the command has more than 64 bytes of data, then multiple packets are transmitted or received.

Figure 3-3 shows the USB protocol packet structure format used in the reference source code and the definition of each parameter. The largest command that is supported is 576, which includes the two-byte command.

```
/* projector HID message structure. */
//Must be 4 byte aligned
typedef struct _hidmessageStruct
{
   struct _hidhead
   {
      struct _packetcontrolStruct
      {
         uint08 dest     : 3;          /* Destination, Proj = 0, RFC = 1, USB Debug MSg = 7 */
         uint08 reserved : 2;       /* Reserved */
         uint08 nack     : 1;          /* Command handler error, 1 = NACK */
         uint08 reply    : 1;          /* Host wants a reply from device, 1 = true */
         uint08 rw       : 1;          /* Write = 0, Read = 1 */
      }flags;                            /* Packet flags */

      uint08 seq;                       /* sequence number */
      uint16 length;                    /* command length */
   } head;

   union
   {
      uint16 cmd;                       /* Projector control command # */
      uint08 data[576];              /* Command Data */
   } text;
}
HID_MESSAGE_STRUCT;
```

Figure 3-3. USB Protocol Packet Structure

Figure 3-4 shows a few examples of communicating with the projector. All values shown are in hex format. Figure 3-4(a) shows the packet format description and follows the protocol packet structure. Figure 3-4(b) illustrates a write transaction. Notice the report-ID 0x00, which should always be at the start of any packet. This packet contains a command with five bytes. The command is 0x0201, and the data 0x1023AF. The sequence number is a positive non-zero number, which is 0x21 in this packet. Figure 3-4(c) illustrates a read transaction, which includes the reply bit set. After the packet has been transmitted to the projector, the projector will execute the command, and if it successfully executes the command, it will stage a reply packet similar to the one shown in Figure 3-4(d). The host must then perform an IN request on the USB bus to actually get the packet from the projector. If there were any errors in processing the command, the projector will stage a packet similar to the one shown in Figure 3-4(e), which has the NACK bit set with zero bytes as the length. The sequence number can be used to compare packets between a read packet and the reply packet from the projector, which should be the same.

The packet in Figure 3-4(f) is a debug packet, which the projector sends to the host. These types of packets are sent to the host whenever the USB debug messages are enabled. The packet data contains pure ASCII characters and the length of the string. The string is not NULL terminated so the host must add a NULL character for every packet received. The host can append the strings together into a log window or file so that it can be viewed. These debug message can be useful for debugging any issues while the projector is running. The only limitation is that debug messages are not available until the projector is enumerated with the host.

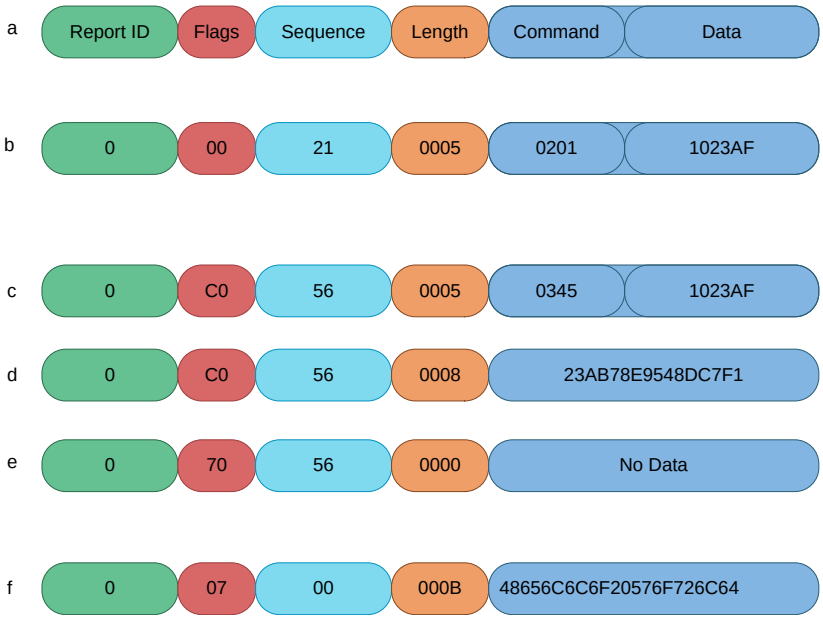

Figure 3-4. USB Write and Read Examples

Initialization (Reset Processing)

Initialization is activated by hardware control. Both DMD electronics and software are reset and initialized when POSENSE or PWRGOOD is low. Refer to the DLPC4422 Datasheet for detailed specifications of these signals.

Control Commands

Control commands, register sub-addresses and corresponding control bits are specified below. Control commands shall be accepted in any order. Each control command will be validated for sub-address and parameter error as they are received. Commands failing validation shall be ignored. Reserved bits in control commands should be set to zero, but will not set the command/parameter error bit if they are not. The OEM is not guaranteed correct operation if reserved bits are set to non-zero.

Control commands are executed once they are validated. During the execution of the command, the ASICREADY signal will be asserted (driven low) and the host can monitor this signal to determine when to send more commands. The 'ready' bit within the system status is also cleared and the host can also monitor this bit to determine when to send more commands.

Some registers (Versions) are read only.

Some bits in some registers are read only.

NOTE: When sending a 0x34 or 0x35, a negative acknowledgment (NAK) means the DLPC4422 is busy. Try the request again.

5.1 Control Commands (CMD: 0x0_H)

5.1.1 Status Read (CMD: 0x00h)

This command is issued during programming mode to determine if the function is running in normal mode. If so, programming mode will continue with its usual process.

Figure 5-1. Status Read (CMD: 0x00h) Register

7	6	5	4	3	2	1	0
Reserved							S
R-0							R-0

Table 5-1. Status Read (CMD: 0x00h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	S	R	0	Status Read 0 = Normal – used for Programming Mode All other combinations are reserved

5.1.2 Projection Mode (CMD: 0x01h)

Standby mode can be used to cool the projection system prior to power off.

Figure 5-2. Projection Mode (CMD: 0x01h) Register

7	6	5	4	3	2	1	0
Reserved				PM			
R-0				R-0			

Table 5-2. Projection Mode (CMD: 0x01h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0	
3-0	PM	R/W	0	PM(3:0) – Projection Mode Range: 0x0 = Normal - The selected source will be displayed. 0x1 = Test Pattern 0x2 = Solid Field 0x3 = Splash 0x4 = Video Curtain - A solid color Video Curtain, defined by the background color of the Background Color Select command will be displayed in place of the source image. 0x5 = Blank Curtain 0x6 = Freeze: The last source image will be kept on the screen and will not update until Projection Mode is returned to “Normal”. 0x7 = Standby: The illumination source and color wheel(s) (if applicable) will be turned off. The DMD will also be powered down and parked. 0x8 = Invalid Projection Mode. All other combinations are reserved

5.1.3 Color Wheel Index (CMD: 0x03h)

This command takes two bytes of data. Variations in the position of the color wheel sensor with respect to the color wheel can lead to performance variations from projector to projector. To facilitate calibration of this variation, this register specifies the angular distance between the stripe on the color wheel, and the color transition that indicates the start of the sequence. This is measured in degrees, and has a resolution of 0.5 degrees. Color wheel index delay time will be calculated based on the number of degrees specified, and the current color wheel speed. This will ensure that sequence start is consistent for any color wheel speed within valid operating conditions.

This value must be sent every time the projector is reset.

Figure 5-3. Color Wheel Index (CMD: 0x03h) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						DLY									
R-0						R-0									

Table 5-3. Color Wheel Index (CMD: 0x03h) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Reserved	R	0	
9-0	DLY	R/W	0	DLY 9:0 - Color wheel index delay calibration value. Delay Units: 0.5 degrees Range: 0 - 359.5 degrees

Table 5-4. Index Delay MS-Byte Bit Values

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	0	0	0	2**8	2**7

Table 5-5. Index Delay LS-Byte Bit Values

B7	B6	B5	B4	B3	B2	B1	B0
2**6	2**5	2**4	2**3	2**2	2**1	2**0	2**-1

5.1.4 Color Wheel Index Delay Fine (CMD: 0x04h)

This value must be sent every time the projector is reset.

Figure 5-4. Color Wheel Index Delay Fine (CMD: 0x04h)

23	22	21	20	19	18	17	16
CWS	Reserved					DLY	
R-0	R-0					R-0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLY								Reserved				DLYFR			
R-0								R-0				R-0			

Table 5-6. Color Wheel Index Delay Fine (CMD: 0x04h) Register Field Descriptions

Bit	Field	Type	Reset	Description
23	CWS	R./W	0	CWS – Color wheel selection. 0: Primary Color Wheel, i.e. 1st. 1: Secondary Color Wheel, i.e. 2nd.
22-18	Reserved	R./W	0	
17-8	DLY	R./W	0	DLY 9:0 – Color wheel index delay calibration value. Delay Units: 0.5 degrees Range: 0 – 359.5 degrees
7-4	Reserved	R./W	0	
3-0	DLYFR	R./W	0	DLYFR 3:0 – Color wheel index delay calibration fractional value. Delay Units: 0.1 degrees Range: 0.0 – 0.9 degrees

Table 5-7. Index Delay MS-Byte Bit Values

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	0	0	0	2**8	2**7

Table 5-8. Index Delay LS-Byte Bit Values

B7	B6	B5	B4	B3	B2	B1	B0
2**6	2**5	2**4	2**3	2**2	2**1	2**0	2**-1

5.1.5 Color Wheel Speed (CMD: 0x05h)

This command takes two bytes of data. It is used to set the desired speed of the Color Wheel for Single Segment Wheel (SSW) systems that don't require frequency or phase lock of the color wheel to VSync.

This value must be sent every time the projector is reset.

Figure 5-5. Color Wheel Speed (CMD: 0x05h) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CW	Reserved					CWS									
R-0	R-0					R-0									

Table 5-9. Color Wheel Speed (CMD: 0x05h) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CW	W	0	CW 15:15 – Color wheel selection. 0: Primary Color Wheel, i.e. 1st. 1: Secondary Color Wheel, i.e. 2nd.
14-10	Reserved	R	0	
9-0	CWS	W	0	CWS 9:0 – Color wheel desired speed. Units: 0.25 Hz (u8.2) Range: 30 - 195 Hz

Table 5-10. CW Speed MS-Byte Bit Values

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	0	0	0	2^7	2^6

Table 5-11. CW Speed LS-Byte Bit Values

B7	B6	B5	B4	B3	B2	B1	B0
2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}

5.1.6 Color Wheel Spinning (CMD: 0x06h)

This command delays the RTOS by a second to check if the color wheel is spinning. If so, the first bit will be set to true.

Figure 5-6. Color Wheel Spinning (CMD: 0x06h) Register

7	6	5	4	3	2	1	0
Reserved							CW
R-0							R-0

Table 5-12. Color Wheel Spinning (CMD: 0x06h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	CW	R	0	CW – Color Wheel Spinning

5.1.7 Color Wheel Coast (CMD: 0x07h)

This command will be set to TRUE if the color wheel is in coast mode.

Figure 5-7. Color Wheel Coast (CMD: 0x07h) Register

7	6	5	4	3	2	1	0
Reserved							CW
R-0							R-0

Table 5-13. Color Wheel Coast (CMD: 0x07h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	CW	R	0	CW – Color Wheel Coast

5.1.8 Color Wheel Debug (CMD: 0x08h)

This command will be set to TRUE if the color wheel debug is enabled.

Figure 5-8. Color Wheel Debug (CMD: 0x08h) Register

7	6	5	4	3	2	1	0
Reserved							CW
R-0							R-0

Table 5-14. Color Wheel Debug (CMD: 0x08h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	CW	R	0	Color Wheel Debug

5.1.9 Color Wheel State (CMD: 0x09h)

This command will return the state of the color wheel spinning, coast, and debug.

Figure 5-9. Color Wheel State (CMD: 0x09h) Register

23	22	21	20	19	18	17	16
Reserved							CW
R-0							R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							CW	Reserved							CW
R-0							R-0	R-0							R-0

Table 5-15. Color Wheel State (CMD: 0x09h) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-17	Reserved	R	0	
16	CW	R	0	Color Wheel Debug
15-9	Reserved	R	0	
8	CW	R	0	Color Wheel Coast
7-1	Reserved	R	0	
0	CW	R	0	Color Wheel Spinning

5.1.10 Color Wheel V Sync (CMD: 0x0ah)

This command is used to control the expected V Sync frequency. If the source has changed, this function can be called prior to enabling the input source to speed up the phase locking process.

Figure 5-10. Color Wheel V Sync (CMD: 0x0ah) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CW															
R-0															

Table 5-16. Color Wheel V Sync (CMD: 0x0ah) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CW	R/W	0	Color Wheel V Sync

5.1.11 Color Wheel Index Clock (CMD: 0x0bh)

5.1.11.1 Color Wheel Clock Index Period

This command gets the period of the color wheel index by calculating the difference between two successive timer captures of the index signal.

Figure 5-11. Color Wheel Clock Index Period Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CW															
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CW															
R/W-0															

Table 5-17. Color Wheel Clock Index Period Register Description

Bit	Field	Type	Reset	Description
31-0	CW	R	0	Color Wheel Clock Index Period

5.1.11.2 Color Wheel Clock Index Frequency

This command gets the frequency of the color wheel index by dividing the sequence clock by the period calculated above.

Figure 5-12. Color Wheel Clock Index Frequency Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CW															
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CW															
R/W-0															

Table 5-18. Color Wheel Clock Index Period Register Description

Bit	Field	Type	Reset	Description
31-0	CW	R	0	Color Wheel Clock Index Frequency

5.1.12 Hardware Test Multiplexer (CMD: 0x0Ch)

The last command received to set a HW Test Point will override any previous test point signal selection with the same Test Point Selection value.

Figure 5-13. Hardware Test Multiplexer (CMD: 0x0Ch) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MS	Reserved				TP			Reserved			HW				
R-0	R-0				R-0			R-0			R-0				

Table 5-19. Hardware Test Multiplexer (CMD: 0x0Ch) Register Description

Bit	Field	Type	Reset	Description
15	MS	R/W	0	Master or Slave ASIC 0 = Master 1 = Slave
14-11	Reserved	R	0	
10-8	TP	R/W	0	HW Test Point Selection, 0 - 7
7-5	Reserved	R	0	
4-0	HW	R/W	0	HW Test Signal Selection 0=DELAYED_CW_INDEX, 1=CW_INDEX, VSYNC, 2= SEQUENCE_INDEX, 3=SPOKE_MARKER, 4=REVOLUTION_MARKER, 5=SEQ_AUX0, 6=SEQ_AUX1, 7=SEQ_AUX2, 8=SEQ_AUX3, 9=SEQ_AUX4, 10=SEQ_AUX5, 11= SEQ_AUX6, 12=SEQ_AUX7

5.1.13 Software Test Multiplexer (CMD: 0x0Dh)

Figure 5-14. Software Test Multiplexer (CMD: 0x0Dh) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MS	Reserved				TP			Reserved			SW				
R-0	R-0				R-0			R-0			R-0				

Table 5-20. Software Test Multiplexer (CMD: 0x0Dh) Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MS	R/W	0	Master or Slave ASIC 0 = Master 1 = Slave
14-11	Reserved	R	0	
10-8	TP	R/W	0	HW Test Point Selection, 0 - 7
7-5	Reserved	R	0	

Table 5-20. Software Test Multiplexer (CMD: 0x0Dh) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	SW	R/W	0	SW Test Signal Selection 0=FRAME_TASK, 1=CW_INDEX_TASK, 2=SEQ_TASK, 3=MTR_SPIN_TASK, 4=CW_PHASE_LOCK, 5=CW_FREQ_LOCK, 6=USB_IRQ, 7=I2C_Task

5.1.14 Application Debug (CMD: 0x0Eh)

This command allows setting of the debug bytes mask to enable various debug messages to be sent to the UART/USB. To enable all debug messages, set bytes to 0xFFFFFFFF. To disable all debug messages, set four bytes to 0. The default is 0; no debug message output. The last two bytes are reserved for allocated or used string lengths for the debug messages. Enables messages on UART port.

Figure 5-15. Application Debug (CMD: 0x0Eh) Register

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reserved												I2CCMD	Reserved		
R-0												R/W-0	R-0		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EEPROM	SYSTEM	ILLUM	ENVIRO	Reserved				ALWAYS	MBOX	USB	Reserved	PERIPH	MSG	ALOCK	DPATH
R-0	R-0	R-0	R-0	R-0				R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALLOC								USED							
R-0								R-0							

Table 5-21. Application Debug (CMD: 0x0Eh) Register Field Descriptions

Bit	Field	Type	Reset	Description
47-36	Reserved	R/W	0	
36	I2CCMD	R/W	0	I^2C Handler Debug Message
34-32	Reserved	R/W	0	
31	EEPROM	R/W	0	EEPROM Debug Message
30	SYSTEM	R/W	0	System Functions Debug Message
29	ILLUM	R/W	0	Illumination: DMD, wheel, lamp Debug Message
28	ENVIRO	R/W	0	Environment Debug Message
27-24	Reserved	R/W	0	
23	ALWAYS	R/W	0	Debug messages always ON
22	MBOX	R/W	0	Mailbox message routing Debug Message
21	USB	R/W	0	USB Debug Message
20	Reserved	R/W	0	
19	PERIPH	R/W	0	Peripherals Debug Message
18	MSG	R/W	0	Projector Control/RFC Debug Message
17	ALOCK	R/W	0	Autolock Debug Message
16	DPATH	R/W	0	Datapath Debug Message

Table 5-21. Application Debug (CMD: 0x0Eh) Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	ALLOC	R/W	0	Message string size allocation
7-0	USED	R/W	0	Message string size used

5.1.15 Enable USB Debug Messages (CMD: 0x0Fh)

Enables debug messages to be sent transmitted via USB to DLP Composer™.

Figure 5-16. Enable USB Debug Messages (CMD: 0x0Fh) Register

23	22	21	20	19	18	17	16
Reserved							Enable
R-0							R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM															
R-0															

Table 5-22. Enable USB Debug Messages (CMD: 0x0Fh) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-17	Reserved	R	0	
16	Enable	W	0	Enable USB Debug messages 0 = Disable 1 = Enable
15-0	MEM	W	0	USB Message Buffer Size in bytes. Check memory pool availability before setting this value.

5.2 Control Commands (CMD: 0x1_H)

5.2.1 Image Orientation (CMD: 0x10h)

Figure 5-17. Image Orientation (CMD: 0x10h) Register

7	6	5	4	3	2	1	0
Reserved						NS	EW
R-0						R-0	R-0

Table 5-23. Image Orientation (CMD: 0x10h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0	
1	NS	R/W	0	DMD North/South (Vertical) Flip. 0: Disable – (Default) 1: Enable Vertical Flip is used to permit the design to operate in both normal and mechanically inverted applications. Vertical flip function flips the image vertically. Vertical flip function changes the position of “vertical starting line”, flipping it along a major axis, but not the meaning of the term.
0	EW	R/W	0	DMD East/West (Horizontal) Flip 0: Disable – (Default) 1: Enable East/West flip is used to permit the design to operate in both rear-projection and front-projection applications. East/West flip function flips the image horizontally. Horizontal function changes the position of “horizontal starting column”, flipping it along a major axis, but not the meaning of the term.

5.2.2 Test Pattern Generator (TPG) (CMD: 0x11h)

This command will set one of the pre-defined test patterns stored in flash. The function selects a pattern to load from flash into the test pattern generator hardware. The information retrieved from the flash includes pattern definition, color definition, and the resolution. The pre-defined patterns are included in the flash configuration data. The command will set the active display to Test Pattern, safely stop the Auto-lock algorithm (if enabled), and display the test pattern. If a pattern greater than or equal to 10 is selected this will automatically disable the TPG pattern.

Figure 5-18. Test Pattern Generator (TPG) (CMD: 0x11h) Register

7	6	5	4	3	2	1	0
Reserved				TPG			
R-0				R-0			

Table 5-24. Test Pattern Generator (TPG) (CMD: 0x11h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0	
3-0	TPG	R/W	0	Pattern : Enables patterns 0x0 - 0x9

5.2.3 TPG Frame Rate (CMD: 0x12h)

This command sets the current frame rate for the test pattern generator.

Figure 5-19. TPG Frame Rate (CMD: 0x12h) Register

23	22	21	20	19	18	17	16
TPGCR7	TPGCR6	TPGCR5	TPGCR4	TPGCR3	TPGCR2	TPGCR1	TPGCR0
R-0							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPGV B7	TPGV B6	TPGV B5	TPGV B4	TPGV B3	TPGV B2	TPGV B1	TPGV B0	TPGF R7	TPGF R6	TPGF R5	TPGF R4	TPGF R3	TPGF R2	TPGF R1	TPGF R0
R-0								R-0							

Table 5-25. TPG Frame Rate (CMD: 0x12h) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-16	TPGCR	R/W	0	Test Pattern Generator Clock Rate
15-8	TPGVB	R/W	0	Test Pattern Generator Vertical Blanking
7-0	TPGFR	R/W	0	Test Pattern Generator Frame Rate

5.2.4 Solid Field Generator (CMD: 0x13h)

This command configures the color of the solid field to be produced by the solid field generator. This command should be called before setting the display source to the solid field generator.

Table 5-26. Solid Field Generator (CMD: 0x13h) Command

Byte	Command	Register
0-1	Red	Figure 5-20
2-3	Green	Figure 5-21
4-5	Blue	Figure 5-22

Figure 5-20. Solid Field Generator (CMD: 0x13h) - Red Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED															
R/W-0															

Figure 5-21. Solid Field Generator (CMD: 0x13h) - Green Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN															
R/W-0															

Figure 5-22. Solid Field Generator (CMD: 0x13h) - Blue Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLUE															
R/W-1023															

Table 5-27. Solid Field Generator (CMD: 0x13h) - Red Register Description

Bit	Field	Type	Reset	Description
15-0	RED	R/W	0	Red Solid Field Color Value (Default: 0) Range: 0 - 1023

Table 5-28. Solid Field Generator (CMD: 0x13h) - Green Register Description

Bit	Field	Type	Reset	Description
15-0	GREEN	R/W	0	Green Solid Field Color Value (Default: 0) Range: 0 - 1023

Table 5-29. Solid Field Generator (CMD: 0x13h) - Blue Register Description

Bit	Field	Type	Reset	Description
15-0	BLUE	R/W	1023	Blue Solid Field Color Value (Default: 1023) Range: 0 - 1023

5.2.5 I²C Read (CMD: 0x15h)

By writing to this register, a subsequent read will return the two system status bytes and the data associated with the command in this register. See section Error! Reference source not found for the definition of the system status bytes.

NOTE: This register is only valid when the I²C interface is used between the host and the projector.

Figure 5-23. I²C Read (CMD: 0x15h) Register

7	6	5	4	3	2	1	0
RD							
R-0							

Table 5-30. I²C Read (CMD: 0x15h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RD	R	0	Register to be read

5.2.6 Brightness (CMD: 0x16h)

The Brightness Control provides the ability to add or subtract a fixed bias from each of the input channels. This may be used to remove any inherent offsets and/ or adjust the brightness level. The brightness coefficients are signed, 11-bit (s8.2), 2's complement values between –256 and 255.75, inclusive. Brightness Control is used after color space conversion.

All programmable coefficient values represent numbers less than 256 but greater than or equal to negative 256. The binary point is between bits 2 and 1.

Figure 5-24. Brightness (CMD: 0x16h) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B															
R-0															

Table 5-31. Brightness (CMD: 0x16h) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	B	R/W	0	Brightness coefficient data

5.2.7 Contrast Adjustment (CMD: 0x17h)

Each contrast byte controls the gain applied to the input image data for a given data channel. The contrast gain has a range from 0 to 200 (0% to 200%) with 100 (100%) being nominal (default). The desired gain is achieved by sending the percentage gain for each data channel as a number between 0h and C8h (0 and 200 decimal) in these bytes.

Note: Setting Contrast values automatically activates color space conversion.

Figure 5-25. Contrast Adjustment (CMD: 0x17h) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C															
R/W-64h															

Table 5-32. Contrast Adjustment (CMD: 0x17h) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	C	R/W	64h	Contrast percentage gain for a data channel (Default: 64h) Range: 0h – C8h

5.2.8 Source Configuration (CMD: 0x18h)

The source configuration map should match the DMD resolution and input source.

Table 5-33. Source Configuration Setup Map

Byte	Description	Range	Default
0	Total Area Pixels Per Line	0 - 2047	Per DMD resolution configuration
1	Total Area Lines Per Frame	0 - 2047	Per DMD resolution configuration
3	Active Area First Pixel	0 - 255	Per DMD resolution configuration
4	Active Area First Line	0 - 255	Per DMD resolution configuration
5	Active Area Pixels Per Line	0 - DMD Pixels	Per DMD resolution configuration
6	Active Area Lines Per Frame	0 - DMD Lines	Per DMD resolution configuration
7	Bottom Field First Line	0 - 127	Per DMD resolution configuration
8	Pixel Clock Frequency in kHz	0 to 320,000	Per DMD resolution configuration
9	Color Space Conversion Coefficients [0]	See Section 5.2.9	1023
10	Color Space Conversion Coefficients [1]		0
11	Color Space Conversion Coefficients [2]		0
12	Color Space Conversion Coefficients [3]		0
13	Color Space Conversion Coefficients [4]		1023
14	Color Space Conversion Coefficients [5]		0
15	Color Space Conversion Coefficients [6]		0
16	Color Space Conversion Coefficients [7]		0
17	Color Space Conversion Coefficients [8]		1023
18	Offset [0]	See Section 5.2.10	0
19	Offset [1]		0
20	Offset [2]		0

The Offset Control provides the ability to add or subtract a fixed bias from each of the input channels. This may be used to remove any inherent offsets and/ or adjust the black level. The offset coefficients are signed, 11-bit (s8.2), 2's complement values between –256 and 255.75, inclusive. Offset Control is used prior to color space conversion.

Table 5-34. Offset Table Command

Byte	Command	Register
0	R MSB	
1	R LSB	
2	G MSB	
3	G LSB	
4	B MSB	
5	B LSB	

Figure 5-26. Offset Table Register

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
B															
R/W-0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B															
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B															
R/W-0															

Table 5-35. Offset Table Register Description

Bit	Field	Type	Reset	Description
47-0	B	R/W	0	Offset coefficient data (Default: 0)

All programmable CSC coefficient values represent numbers less than 4 but greater than or equal to negative 4. They are 13-bit signed 2's complement numbers with the binary point between bits 9 and 10.

Figure 5-27. CSC Format Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			CSC												
R-0			R/W-0												

$$\begin{bmatrix} G \\ R \\ B \end{bmatrix} = \begin{bmatrix} C1 & C2 & C3 \\ C4 & C5 & C6 \\ C7 & C8 & C9 \end{bmatrix} \begin{bmatrix} A \\ B \\ C \end{bmatrix}$$

Figure 5-28. CSC Matrix

Table 5-36. Coefficient MS-Byte Bit Values

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	SIGN	2**1	2**0	2**-1	2**-2

Table 5-37. Coefficient LS-Byte Bit Values

B7	B6	B5	B4	B3	B2	B1	B0
2**-3	2**-4	2**-5	2**-6	2**-7	2**-8	2**-9	2**-10

5.2.9 Color Space Converter (CMD: 0x19h)

This command controls the table loaded in color space converter.

Figure 5-29. Color Space Converter (CMD: 0x19h) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					P			Reserved				CSC			

Table 5-38. Color Space Converter (CMD: 0x19h) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	Reserved			
10-8	P	R/W		Source Port Range: 0h - 3h 0h = Source Port 1 1h = Source Port 2 2h = Source Port 656 3h = Source Port IVD
7-4	Reserved			
3-0	CSC	R/W		Color Space Converter Table

5.2.10 Image Offset (CMD: 0x1bh)

This function offsets the levels of the RGB channels at a point in the datapath that is after source offset, contrast and RGB gain, brightness, and color space conversion (including hue and color adjustment). The offset addends are signed, 2's complement values with 2 fractional bits and a range of –256.00 to 255.75, boundary inclusive.

Figure 5-30. Image Offset (CMD: 0x1bh) Register

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
R															
R/W-0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G															
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B															
R/W-0															

Table 5-39. Image Offset (CMD: 0x1bh) Register Field Descriptions

Bit	Field	Type	Reset	Description
47-32	R	R/W	0	Offsets the level of the R channel
31-16	G	R/W	0	Offsets the level of the G channel
15-0	B	R/W	0	Offsets the level of the B channel

Table 5-40. Offset MSBYTE Bit Values

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	0	0	SIGN	2**7	2**6

Table 5-41. Offset LSBYTE Bit Values

B7	B6	B5	B4	B3	B2	B1	B0
2**5	2**4	2**3	2**2	2**1	2**0	2**-1	2**-2

5.2.11 Background Mode and Background Color (CMD: 0x1eh)

Sets the Background Insertion Mode to display border or full screen background color. This function also sets the background color for images that are smaller than the size of the display. By default, the background color is set to black. However, if desired, this function can be used to set primary and secondary colors along with white and black.

Note: BrightSync(tm) systems only allow black for the background border color. If this function is used to configure the image for full screen background color, then the colors described above are provided.

Figure 5-31. Background Mode and Background Color (CMD: 0x1eh) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							BGM	Reserved				BGC			
R-0							R-0	R-0				R-0			

Table 5-42. Background Mode and Background Color (CMD: 0x1eh) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	Reserved	R	0	
8	BGM	R/W	0	BGM – Background Mode 0 = full screen background color 1 = background color applies to area not covered by the active image
7-4	Reserved	R	0	
3-0	BGC	R/W	0	BGC –Background color Black color White color Green color Red color Blue color Yellow color Cyan color Magenta color

5.2.12 Display Horizontal Flip (CMD: 0x1fh)

Horizontal flip is used to permit the design to operate in both rear-projection and front-projection applications. Horizontal flip function flips the image horizontally. Horizontal function changes the position of “horizontal starting column”, flipping it along a major axis, but not the meaning of the term.

Figure 5-32. Display Horizontal Flip (CMD: 0x1fh) Register

7	6	5	4	3	2	1	0
Reserved							HF
R-0							R-0

Table 5-43. Display Horizontal Flip (CMD: 0x1fh) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved			
0	HF	R/W		Horizontal Flip 0: Disable – (Default) 1: Enable

5.3 Control Commands (CMD:0x2_H)

5.3.1 SFG Resolution (CMD: 0x21h)

This command gets the current resolution for the solid field generator (SFG).

Figure 5-33. SFG Resolution (CMD: 0x21h) Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
H															
R-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V															
R-0															

Table 5-44. SFG Resolution (CMD: 0x21h) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	H	R	0	Horizontal SFG Resolution
15-0	V	R	0	Vertical SFG Resolution

5.3.2 Splash Load (CMD: 0x22h)

Loads one or two splash images for 2D or 3D display from data stored in flash. For a standard 2D splash image, specify the proper value in byte 0 and set byte 1 to 0xFF. For 3D display, specify the image numbers in flash for both bytes. The images must be tagged with left or right eyes appropriately in Flash Builder for the images to load successfully.

Figure 5-34. Splash Load (CMD: 0x22h) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S															
R-0															

Table 5-45. Splash Load (CMD: 0x22h) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	S	W	0	S1(7:0) – Splash 1 S2(7:0) - Splash 2 Loads one or two splash images for 2D or 3D display from data stored in flash. For a standard 2D splash image, specify the proper value in byte 0 and set byte 1 to 0xFF. For 3D display, specify the image numbers in flash for both bytes. The images must be tagged with left or right eyes appropriately in Flash Builder for the images to load successfully.

5.3.3 Display (CMD: 0x23h)

This function configures the source for display on the DMD. While the source image must be the same size as the DMD size, the user may choose to start the image at a point other than the top left corner of the DMD.

Table 5-46. Display (CMD: 0x23h)

Byte	Description	Range	Default
0	Cropped Area First Pixel MSB		
1	Cropped Area First Pixel LSB		
2	Cropped Area First Line MSB		
3	Cropped Area First Line LSB		
4	Cropped Area Pixels Per Line MSB		
5	Cropped Area Pixels Per Line LSB		
6	Cropped Area Lines Per Frame MSB		
7	Cropped Area Lines Per Frame LSB		
8	Display Area First Pixel MSB		
9	Display Area First Pixel LSB		
10	Display Area First Line MSB		
11	Display Area First Line LSB		
12	Display Area Pixels Per Line MSB		
13	Display Area Pixels Per Line LSB		
14	Display Area Lines Per Frame MSB		
15	Display Area Lines Per Frame LSB		
16	Centered		

5.3.4 SRC Offset (CMD: 0x25h)

This command controls the current source configuration offset specified values. The input source can either be RGB for graphics sources or YCrCb for the video sources.

Figure 5-35. SRC Offset (CMD: 0x25h) Register

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
R7	R6	R5	R4	R3	R2	R1	R0	Reserved					R10	R9	R8
R-0								R-0						R-0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G7	G6	G5	G4	G3	G2	G1	G0	Reserved					G10	G9	G8
R-0								R-0						R-0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0	Reserved					B10	B9	B8
R-0								R-0						R-0	

Table 5-47. SRC Offset (CMD: 0x25h) Register Field Descriptions

Bit	Field	Type	Reset	Description
47-40	R	R/W	0	R(10:0) - Red Offset Range: –256 to 255.75 in signed 8.2 format
39-35	Reserved	R	0	
34-32	R	R/W	0	R(10:0) - Red Offset Range: –256 to 255.75 in signed 8.2 format
31-24	G	R/W	0	G(10:0) - Green Offset Range: –256 to 255.75 in signed 8.2 format
23-19	Reserved	R	0	
18-16	G	R/W	0	G(10:0) - Green Offset Range: –256 to 255.75 in signed 8.2 format
15-8	B	R/W	0	B(10:0) - Blue Offset Range: –256 to 255.75 in signed 8.2 format
7-3	Reserved	R	0	
2-0	B	R/W	0	B(10:0) - Blue Offset Range: –256 to 255.75 in signed 8.2 format

5.3.5 SRC Port (CMD: 0x26h)

This function configures the specified input data port. This involves configuring the mapping of its two sub-channels to the corresponding ASIC input channels and specifying the width (bits per color) of the input port. For Dual Pixel sources, call this function twice with PORT1 and PORT2 as the port to configure the ABC_Mux and PortWidth. PortWidth will be set to the width specified on the 2nd call.

Figure 5-36. SRC Port (CMD: 0x26h) Register

23	22	21	20	19	18	17	16
Reserved							P
R-0							R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							PW	Reserved						M	
R-0							R-0	R-0						R-0	

Table 5-48. SRC Port (CMD: 0x26h) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-17	Reserved	R	0	
16	P	R/W	0	Enumeration representing the following configurations 0: Port 1 1: Port 2
15-9	Reserved	R	0	
8	PW	R/W	0	PW – Enumeration representing the following configurations 0: 30 bits 1: 24 bits
7-3	Reserved	R	0	
2-0	M	R/W	0	M – Enumeration representing the following configurations SRC_ABC_STRAIGHT_THRU ABC: ABC (1-1 mapping) SRC_ABC_ROTATE_RIGHT ABC: CAB SRC_ABC_ROTATE_LEFT ABC: BCA SRC_ABC_SWAP_BC ABC: ACB SRC_ABC_SWAP_AB ABC: BAC SRC_ABC_SWAP_AC ABC: CBA

5.3.6 V Sync Period (CMD: 0x27h)

This command gets the last V Sync period measurement.

Figure 5-37. V Sync Period (CMD: 0x27h) Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VS															
R-0															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VS															
R-0															

Table 5-49. V Sync Period (CMD: 0x27h) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VS	R	0	V Sync Period

5.3.7 Primary Channel Source (CMD: 0x28h)

This command determines the current display source.

Figure 5-38. Primary Channel Source (CMD: 0x28h) Register

7	6	5	4	3	2	1	0
Reserved						PCS	
R-0						R-0	

Table 5-50. Primary Channel Source (CMD: 0x28h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0	
1-0	PCS	R	0	Primary Channel Source

5.3.8 Display Freeze (CMD: 0x29h)

Display freeze is recommended to be used when changing source or operating modes to block temporary corruption caused by reconfiguration from reaching the display. When frozen, the last display image will continue to be displayed.

Figure 5-39. Display Freeze (CMD: 0x29h) Register

7	6	5	4	3	2	1	0
Reserved							DF
R-0							R-0

Table 5-51. Display Freeze (CMD: 0x29h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	DF	R/W	0	Display Freeze. 0: Disable – (Default) 1: Enable

5.3.9 Channel Configuration (CMD: 0x2ah)

This command maps the VSync, HSync, Data Enable, Data, Field, and Clock Port signals to the ASIC main channel based on the port selection. It resets the logic in the ASIC. This is required any time there is a change to the clock source or clock polarity.

Figure 5-40. Channel Configuration (CMD: 0x2ah) Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reserved					C2	C1	C0	Reserved					Vs2	Vs1	Vs0
R-0						R-0		R-0						R-0	
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reserved					Hs2	Hs1	Hs0	Reserved					D2	D1	D0
R-0						R-0		R-0						R-0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					De2	De1	De0	Reserved					F2	F1	F0
R-0						R-0		R-0						R-0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Cp2	Cp1	Cp0	Reserved							Cpy0
R-0						R-0		R-0							R-0

Table 5-52. Channel Configuration (CMD: 0x2ah) Register Field Descriptions

Bit	Field	Type	Reset	Description
63-59	Reserved	R	0	
58-56	C	R/W	0	C(2:0) – SRC Channel
55-51	Reserved	R	0	
50-48	Vs	R/W	0	Vs(2:0) – Vsync Source
47-43	Reserved	R	0	
42-40	Hs	R/W	0	Hs(2:0) – Hsync Source
39-35	Reserved	R	0	
34-32	D	R/W	0	D(2:0) – Data Source
31-27	Reserved	R	0	
26-24	De	R/W	0	De(2:0) – Data Enable Source
23-19	Reserved	R	0	
18-16	F	R/W	0	F(2:0) – Field Source
15-11	Reserved	R	0	
10-8	Cp	R/W	0	Cp(2:0) – Clock Port
7-1	Reserved	R	0	
0	Cpy	R/W	0	Cpy0 – Clock Polarity

5.3.10 TPG Border (CMD: 0x2bh)

This command draws a border around the test pattern with a width equal to the specified number of pixels. The color for line patterns is represented by the foreground color, and for all other patterns the color will be the same as the background color. This command must be called after TPG is enabled and the border cannot exceed 20 pixels. The border command is not supported for high resolution sources.

Figure 5-41. TPG Border (CMD: 0x2bh) Register

7	6	5	4	3	2	1	0
Reserved			TPG				
R-0			R/W-0				

Table 5-53. TPG Border (CMD: 0x2bh) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0	
4-0	TPG	R/W	0	TPG Border Range: 0-20

5.3.11 TPG Resolution (CMD: 0x2ch)

This command controls the resolution of the internal test pattern generator. The TPG resolution configuration is limited to the DMD resolution.

Figure 5-42. TPG Resolution (CMD: 0x2ch) Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HR															
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VR															
R/W-0															

Table 5-54. TPG Resolution (CMD: 0x2ch) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HR	R/W	0	Horizontal TPG Resolution Range: 32 - 1200
15-0	VR	R/W	0	Vertical TPG Resolution Range: 64 - 1920

5.3.12 Gamma Curves (CMD: 0x2dh)

This command is used to specify the shifts in the gamma curve of red, green, and blue. Left shift is a positive offset and right shift is a negative offset.

Figure 5-43. Gamma Curves (CMD: 0x2dh) Register

23	22	21	20	19	18	17	16
R							
R/W-0							
15	14	13	12	11	10	9	8
G							
R/W-0							

7	6	5	4	3	2	1	0
B							
R/W-0							

Table 5-55. Gamma Curves (CMD: 0x2dh) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-16	R	R/W	0	Red Gamma Curve Range: –128 - 127
15-8	G	R/W	0	Green Gamma Curve Range: –128 - 127
7-0	B	R/W	0	Blue Gamma Curve Range: –128 - 127

5.3.13 Pixel Clock (CMD: 0x2eh)

This command determines the pixel clock frequency of the source and the total pixels per line for digital sources.

Figure 5-44. Pixel Clock (CMD: 0x2eh) Register

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Pc7	Pc6	Pc5	Pc4	Pc3	Pc2	Pc1	Pc0	Pc15	Pc14	Pc13	Pc12	Pc11	Pc710	Pc9	Pc8
R-0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Pcf7	Pcf6	Pcf5	Pcf4	Pcf3	Pcf2	Pcf1	Pcf0	Pcf15	Pcf14	Pcf13	Pcf12	Pcf11	Pcf10	Pcf9	Pcf8
R-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pcf23	Pcf22	Pcf21	Pcf20	Pcf19	Pcf18	Pcf17	Pcf16	Pcf31	Pcf30	Pcf29	Pcf28	Pcf27	Pcf26	Pcf25	Pcf24
R-0															

Table 5-56. Pixel Clock (CMD: 0x2eh) Register Field Descriptions

Bit	Field	Type	Reset	Description
47-32	R	R/W	0	Pc(15:0) – Pixel
31-0	G	R/W	0	Pcf(31:0) – Pixel Clock Frequency

5.3.14 Source Description (CMD: 0x2fh)

This command determines the source description including whether the source is active (external). It also determines the input width and height and the native height and width, the port the source is on, and the type of source that is actively displayed.

Figure 5-45. Source Description (CMD: 0x2fh) Register

127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Reserved								Sa0	Reserved						3D0
R-0								R-0	R-0						R-0
111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Fr7	Fr6	Fr5	Fr4	Fr3	Fr2	Fr1	Fr0	Fr15	Fr14	Fr13	Fr12	Fr11	Fr10	Fr9	Fr8
R-0															
95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Fr23	Fr22	Fr21	Fr20	Fr19	Fr18	Fr17	Fr16	Fr31	Fr30	Fr29	Fr28	Fr27	Fr26	Fr25	Fr24
R-0															
79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Ih7	Ih6	Ih5	Ih4	Ih3	Ih2	Ih1	Ih0	Ih15	Ih14	Ih13	Ih12	Ih11	Ih10	Ih9	Ih8
R-0															
63	62	61	60	59	58	57	56	55	54	53	52	51	49	48	47
Iw7	Iw6	Iw5	Iw4	Iw3	Iw2	Iw1	Iw0	Iw15	Iw14	Iw13	Iw12	Iw11	Iw10	Iw9	Iw8
R-0															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Nh7	Nh6	Nh5	Nh4	Nh3	Nh2	Nh1	Nh0	Nh15	Nh14	Nh13	Nh12	Nh11	Nh10	Nh9	Nh8
R-0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Nw7	Nw6	Nw5	Nw4	Nw3	Nw2	Nw1	Nw0	Nw15	Nw14	Nw13	Nw12	Nw11	Nw10	Nw9	Nw8
R-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Sp2	Sp1	Sp0	Reserved						Ad1	Ad0
R-0					R-0			R-0						R-0	

Table 5-57. Source Description (CMD: 0x2fh) Register Field Descriptions

Bit	Field	Type	Reset	Description
127-120	Reserved	R	0	
119	Sa0	R/W	0	Sa0 - Source Active Range: 0 - 1
118-113	Reserved	R	0	
112	3D0	R/W	0	3D0 - Is 3D? Range: 0 -1
111-80	Fr	R/W	0	Fr(31:0) - Input Frame Rate
79-64	Ih	R/W	0	Ih(15:0) - Input Height
63-4	Iw	R/W	0	Iw(15:0) - Input Width
47-32	Nh	R/W	0	Nh(15:0) - Native Height
31-16	Nw	R/W	0	Nw(15:0) - Native Width
15-11	Reserved	R	0	
10-8	Sp	R/W	0	Sp(2:0) - Source Port Range: 0 - 7
7-2	Reserved	R	0	
1-0	Ad	R/W	0	Ad(1:0) - Active Display Range: 0 - 3

5.4 Control Commands (CMD: 0x3_H)

5.4.1 Programming Mode (CMD: 0x30h)

Writing a 1 to this register will cause the system to go through a partial system shutdown and enter programming mode. When in programming mode, writing a 1 to this register will cause the system to reset and return to normal operating mode. System status bytes can be read to verify when programming mode is active.

Figure 5-46. Programming Mode (CMD: 0x30h) Register

7	6	5	4	3	2	1	0
Reserved							PM
R-0							R/W-0

Table 5-58. Programming Mode (CMD: 0x30h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	PM	R/W	0	Programming mode change 1: Mode change enable

5.5 Control Commands (CMD: 0x7_H)

5.5.1 DMD Spread Spectrum Enable (CMD: 0x7fh)

This function controls the Spread Spectrum value for the DMD clock output. Setting the spread value to 0.00 will disable the Spread Spectrum.

Figure 5-47. DMD Spread Spectrum Enable (CMD: 0x7fh) Register

7	6	5	4	3	2	1	0
Reserved						SS	
R-0						R/W-0	

Table 5-59. DMD Spread Spectrum Enable (CMD: 0x7fh) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0	
1-0	SS	R/W	0	SS – DMD Spread Spectrum Enumeration represents the following configurations DDP_SSC_0_00_PER : < 0.00% DDP_SSC_0_50_PER: 0.50% DDP_SSC_0_75_PER: 0.75% DDP_SSC_1_00_PER: 1.00%

5.6 Control Commands (CMD: 0x8_H)

5.6.1 DMD Resolution (CMD: 0x81h)

This command will return the physical width and height of the DMD in pixels. The first byte is reserved for the width and the second byte is reserved for the height.

Figure 5-48. DMD Resolution (CMD: 0x81h) Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
H															
R/W-00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W															
R/W-00h															

Table 5-60. DMD Resolution (CMD: 0x81h) Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	H	R	00h	DMD Width (Default: 00h) Range: 0h – FFFFh
15-0	W	R	00h	DMD Height (Default: 00h) Range: 0h – FFFFh

5.6.2 Get Application State (CMD: 0x84h)

This command returns the current power state of the application.

Figure 5-49. Get Application State (CMD: 0x84h) Register

7	6	5	4	3	2	1	0
Reserved					ST		
R-0					R-0		

Table 5-61. Get Application State (CMD: 0x84h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0	
2-0	ST	R	0	Application Power State. Enumeration represents the following configurations POWERSTATE_RESET POWERSTATE_STANDBY POWERSTATE_ACTIVE POWERSTATE_COOLING POWERSTATE_WARMING POWERSTATE_POWERUP

5.7 Control Commands (CMD: 0x9_H)

5.7.1 DDP Software Reset (CMD: 0x90h)

This function initiates a reset of the processor and all logic in the ASIC.

Figure 5-50. DDP Software Reset (CMD: 0x90h) Register

7	6	5	4	3	2	1	0
Reserved						Sr1	Sr0
R-0						R/W-0	

Table 5-62. DDP Software Reset (CMD: 0x90h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0	
1-0	Sr	W	0	Sr(1:0) – DDP Software Reset Enumeration represents the following configurations DDP_PROCESSOR_ARM7 DDP_PROCESSOR_ARM9 DDP_PROCESSOR_ARM7_AND_ARM9

5.7.2 DDP Reset Count (CMD: 0x91h)

This command returns the number of resets since the last power up. Resets occurring from a cause other than power up can be monitored for excessive failure. This value will saturate at 7.

Figure 5-51. DDP Reset Count (CMD: 0x91h) Register

7	6	5	4	3	2	1	0
Reserved					Rc2	Rc1	Rc0
R-0						R/W-0	

Table 5-63. DDP Reset Count (CMD: 0x91h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0	
2-0	Rc	R	0	Rc(2:0) - DDP Reset Count Range: 0 - 7

5.7.3 USB Clock Enable (CMD: 0x93h)

This command enables or disables the USB Clock. The USB clock runs at 48 MHz. During low power mode, this clock will NOT change frequency.

Figure 5-52. USB Clock Enable (CMD: 0x93h) Register

7	6	5	4	3	2	1	0
Reserved							USBC
R-0							R/W-0

Table 5-64. USB Clock Enable (CMD: 0x93h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	USBC	R/W	0	USB Clock Enable Range: 0 - 1 TRUE = Enable the USB Clock FALSE = Disable the USB Clock

5.7.4 Vertical Sharpness (CMD: 0x98h)

This function configures the vertical sharpness filter. A value of 0 is the sharpest while a value of 31 is the smoothest. A value of 16 disables the sharpness filter.

Both video and graphics are affected by this filter. TI recommends that the sharpness filters be disabled (sharpness = 16) for graphics sources.

Figure 5-53. Vertical Sharpness (CMD: 0x98h) Register

7	6	5	4	3	2	1	0
Reserved			VS				
R-0			R/W-0				

Table 5-65. Vertical Sharpness (CMD: 0x98h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0	
4-0	VS	R/W	0	Vertical Sharpness Range: 0 (most sharp) - 31 (most smooth)

5.7.5 Horizontal Sharpness (CMD: 0x99h)

This function configures the horizontal sharpness filter. A value of 0 is the sharpest, while a value of 31 is the smoothest. A value of 16 disables the sharpness filter.

Both video and graphics are affected by this filter. TI recommends that the sharpness filters be disabled (sharpness = 16) for graphics sources.

Figure 5-54. Horizontal Sharpness (CMD: 0x99h) Register

7	6	5	4	3	2	1	0
Reserved			HS				
R-0			R/W-0				

Table 5-66. Horizontal Sharpness (CMD: 0x99h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0	
4-0	HS	R/W	0	Horizontal Sharpness Range: 0 (most sharp) - 31 (most smooth)

5.7.6 Scalar Bypass Mode (CMD: 0x9ah)

This command enables and disables Scalar Bypass Mode. TI recommends enabling this mode for Formatter Only systems.

Figure 5-55. Scalar Bypass Mode (CMD: 0x9ah) Register

7	6	5	4	3	2	1	0
Reserved							SBM
R-0							R/W-0

Table 5-67. Scalar Bypass Mode (CMD: 0x9ah) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	SBM	R/W	0	Scalar Bypass Mode Range: 0 - 1 TRUE: Enabled - scalar is disabled (scaling bypass mode) FALSE: Disabled - scalar is performing scaling function

5.8 Control Commands (CMD: 0xA_H)

5.8.1 Fan Frequency Cycle (CMD: 0xa0h)

This function controls the switching frequency and duty cycle of the fan number specified by the 'Fan Number' field.

Figure 5-56. Fan Frequency Cycle (CMD: 0xa0h) Register

23	22	21	20	19	18	17	16
Reserved						FN	
R-0						R/W-1	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							SF	Reserved	FDC						
R-0							R/W-0	R-0	R/W-0						

Table 5-68. Fan Frequency Cycle (CMD: 0xa0h) Register Field Descriptions

Bit	Field	Type	Reset	Description
23-18	Reserved	R	0	
17-16	FN	R/W	1	FN(1:0) - Fan Number whose frequency and duty cycle are to be modified or retrieved Range: 1 - 3
15-9	Reserved	R	0	
8	SF	R/W	0	Sf0 - Switching Frequency of the Fan Range: 0 - 1 SFREQ_100KHZ: 100 kHz switching frequency SFREQ_24HZ: 24 Hz switching frequency
7	Reserved	R	0	
6-0	FDC	R/W	0	Fdc(7:0) - Duty Cycle of the Fan Range: 0 and 30 - 100 in steps of 5

5.9 Control Commands (CMD: 0xB_H)

5.9.1 Pulse Width Module Output Configuration (CMD: 0xb0h)

This command sets/retrieves the configuration data for the specified output port (PWM_OUT0 to PWM_OUT7)

Table 5-69. PWM Output Configuration Map

Byte	Bit(s)	Description	Notes
0 - 3	31:0	Frequency (in Hz) of PWM_OUT0 port	Range: 17.8 Hz - 9.33 MHz
4	7:0	Duty Cycle of PWM_OUT0 port	Range: 1 - 99 percent
5	1:0	PWM_OUT0 Port Enable	TRUE: Enable
6	1:0	PWM Output Signal Enable	TRUE: Enable
7 - 10	31:0	Frequency (in Hz) of PWM_OUT1 port	Range: 17.8 Hz - 9.33 MHz
11	7:0	Duty Cycle of PWM_OUT1 port	Range: 1 - 99 percent
12	1:0	PWM_OUT1 Port Enable	TRUE: Enable
13	1:0	PWM Output Signal Enable	TRUE: Enable
14 - 17	31:0	Frequency (in Hz) of PWM_OUT2 port	Range: 17.8 Hz - 9.33 MHz
18	7:0	Duty Cycle of PWM_OUT2 port	Range: 1 - 99 percent
19	1:0	PWM_OUT2 Port Enable	TRUE: Enable
20	1:0	PWM Output Signal Enable	TRUE: Enable
21 - 24	31:0	Frequency (in Hz) of PWM_OUT3 port	Range: 17.8 Hz - 9.33 MHz
25	7:0	Duty Cycle of PWM_OUT3 port	Range: 1 - 99 percent
26	1:0	PWM_OUT3 Port Enable	TRUE: Enable
27	1:0	PWM Output Signal Enable	TRUE: Enable
28 - 31	31:0	Frequency (in Hz) of PWM_OUT4 port	Range: 17.8 Hz - 9.33 MHz
32	7:0	Duty Cycle of PWM_OUT4 port	Range: 1 - 99 percent
33	1:0	PWM_OUT4 Port Enable	TRUE: Enable
34	1:0	PWM Output Signal Enable	TRUE: Enable
35 - 38	31:0	Frequency (in Hz) of PWM_OUT5 port	Range: 17.8 Hz - 9.33 MHz
39	7:0	Duty Cycle of PWM_OUT5 port	Range: 1 - 99 percent
40	1:0	PWM_OUT5 Port Enable	TRUE: Enable
41	1:0	PWM Output Signal Enable	TRUE: Enable
42 - 45	31:0	Frequency (in Hz) of PWM_OUT6 port	Range: 17.8 Hz - 9.33 MHz
46	7:0	Duty Cycle of PWM_OUT6 port	Range: 1 - 99 percent
47	1:0	PWM_OUT6 Port Enable	TRUE: Enable
48	1:0	PWM Output Signal Enable	TRUE: Enable
49 - 52	31:0	Frequency (in Hz) of PWM_OUT7 port	Range: 17.8 Hz - 9.33 MHz
53	7:0	Duty Cycle of PWM_OUT7 port	Range: 1 - 99 percent
54	1:0	PWM_OUT7 Port Enable	TRUE: Enable
55	1:0	PWM Output Signal Enable	TRUE: Enable

5.9.2 Pulse Width Module Input Configuration (CMD: 0xb1h)

This command reads and writes configuration data for the two PWM input counters (PWM_INCOUNT0 and PWM_INCOUNT1).

Table 5-70. PWM Output Configuration Map

Byte	Bit(s)	Description	Notes
0 - 3	31:0	Sample Rate of the Input Counter 0	Range: 284.83 Hz - 18.75 MHz
4	1:0	Input Counter Enable	TRUE: Counter is Enabled
5-6	15:0	High Pulse Width of the Input Counter 0	
7-8	15:0	Low Pulse Width of the Input Counter 0	
9	7:0	Duty Cycle of Input Counter 0	
10 - 13	31:0	Sample Rate of the Input Counter 1	Range: 284.83 Hz - 18.75 MHz
14	1:0	Input Counter Enable	TRUE: Counter is Enabled
15-16	15:0	High Pulse Width of the Input Counter 1	
17-18	15:0	Low Pulse Width of the Input Counter 1	
19	7:0	Duty Cycle of Input Counter 1	

5.9.3 Display Offset (CMD: 0xb3h)

This command sets the desired image offset on the DMD active area. 'Set' writes the desired values, while 'get' reads the previously set values.

Figure 5-57. Display Offset (CMD: 0xb3h) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						IR	IR	Reserved				OR	OR	OR	OR
R-0						R-0		R-0				R-0			

Table 5-71. Display Offset (CMD: 0xb3h) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Reserved	R	0	
9-8	IR	R/W	0	IR(1:0) – Pixels offset Range: 0 - 32
7-4	Reserved	R	0	
3-0	OR	R/W	0	OR(3:0) – Lines offset Range: 0 - 2047

5.9.4 Emergency Shutdown (CMD: 0xbfh)

This function enables or disables partial system shutdown when system faults are detected. Faults which trigger this shutdown include under voltage and thermal faults, as well as faults relating to the color wheel. Whenever such a condition occurs, the DLP subsystem always sets status bits indicating the failed condition.

If emergency shutdown is enabled, then the DLPC4422 will turn off the illumination, power down the DMD, and stop the color wheel as soon as the condition is detected.

Figure 5-58. Emergency Shutdown (CMD: 0xbfh) Register

7	6	5	4	3	2	1	0
Reserved							ES
R-0							R/W-0

Table 5-72. Emergency Shutdown (CMD: 0xbfh) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	ES	R/W	0	Emergency Shutdown Range: 0 - 1 TRUE: Enable Emergency Shutdown FALSE: Disable Emergency Shutdown

5.10 Control Commands (CMD: 0xC_H)

5.10.1 SSI Red Currents (CMD: 0xc1h)

This function reads and writes the Red illuminator current for each combination of illuminator enable strobes.

Table 5-73. SSI Red Currents (CMD: 0xc1h)

Byte	Bit(s)	Description	Notes
0	9:8	Red current during the Red strobe MSB	
1	7:0	Red current during the Red strobe LSB	
2	9:8	Red current during the Green strobe MSB	
3	7:0	Red current during the Green strobe LSB	
4	9:8	Red current during the Blue strobe MSB	
5	7:0	Red current during the Blue strobe LSB	
6	9:8	Red current during the Sample1 strobe MSB	
7	7:0	Red current during the Sample1 strobe LSB	
8	9:8	Red current during the Sample2 strobe MSB	
9	7:0	Red current during the Sample2 strobe LSB	
10	9:8	Red current during the Yellow strobe MSB	
11	7:0	Red current during the Yellow strobe LSB	
12	9:8	Red current during the Cyan strobe MSB	
13	7:0	Red current during the Cyan strobe LSB	
14	9:8	Red current during the Magenta strobe MSB	
15	7:0	Red current during the Magenta strobe LSB	
16	9:8	Red current during the White strobe MSB	
17	7:0	Red current during the White strobe LSB	
18	9:8	Red current during the Black strobe MSB	
19	7:0	Red current during the Black strobe LSB	

5.10.2 SSI Green Currents (CMD: 0xc2h)

This command reads/writes the Green illuminator current for each combination of illuminator enable strobes.

Table 5-74. SSI Green Currents (CMD: 0xc2h)

Byte	Bit(s)	Description	Notes
0	9:8	Green current during the Red strobe MSB	
1	7:0	Green current during the Red strobe LSB	
2	9:8	Green current during the Green strobe MSB	
3	7:0	Green current during the Green strobe LSB	
4	9:8	Green current during the Blue strobe MSB	
5	7:0	Green current during the Blue strobe LSB	
6	9:8	Green current during the Sample1 strobe MSB	
7	7:0	Green current during the Sample1 strobe LSB	
8	9:8	Green current during the Sample2 strobe MSB	
9	7:0	Green current during the Sample2 strobe LSB	
10	9:8	Green current during the Yellow strobe MSB	
11	7:0	Green current during the Yellow strobe LSB	
12	9:8	Green current during the Cyan strobe MSB	
13	7:0	Green current during the Cyan strobe LSB	
14	9:8	Green current during the Magenta strobe MSB	
15	7:0	Green current during the Magenta strobe LSB	
16	9:8	Green current during the White strobe MSB	
17	7:0	Green current during the White strobe LSB	
18	9:8	Green current during the Black strobe MSB	
19	7:0	Green current during the Black strobe LSB	

5.10.3 SSI Blue Currents (CMD: 0xc3h)

This command reads/writes the Blue illuminator current for each combination of illuminator enable strobes.

Table 5-75. SSI Blue Currents (CMD: 0xc3h)

Byte	Bit(s)	Description	Notes
0	9:8	Blue current during the Red strobe MSB	
1	7:0	Blue current during the Red strobe LSB	
2	9:8	Blue current during the Green strobe MSB	
3	7:0	Blue current during the Green strobe LSB	
4	9:8	Blue current during the Blue strobe MSB	
5	7:0	Blue current during the Blue strobe LSB	
6	9:8	Blue current during the Sample1 strobe MSB	
7	7:0	Blue current during the Sample1 strobe LSB	
8	9:8	Blue current during the Sample2 strobe MSB	
9	7:0	Blue current during the Sample2 strobe LSB	
10	9:8	Blue current during the Yellow strobe MSB	
11	7:0	Blue current during the Yellow strobe LSB	
12	9:8	Blue current during the Cyan strobe MSB	
13	7:0	Blue current during the Cyan strobe LSB	
14	9:8	Blue current during the Magenta strobe MSB	
15	7:0	Blue current during the Magenta strobe LSB	
16	9:8	Blue current during the White strobe MSB	
17	7:0	Blue current during the White strobe LSB	
18	9:8	Blue current during the Black strobe MSB	
19	7:0	Blue current during the Black strobe LSB	

5.10.4 SSI Driver Status (CMD: 0xc4h)

This command retrieves the SPI driver status summary byte.

Table 5-76. SSI Driver Status (CMD: 0xc4h)

Byte	Bit(s)	Description	Notes
0	7:0	Red Status Summary	See (1)
1	7:0	Green Status Summary	See (1)
2	7:0	Blue Status Summary	See (1)

(1) See TI Solid State Interface Driver Specification (Drawing #250796) for Status Summary details.

5.10.5 SSI Red Driver Timing (CMD: 0xc5h)

This function reads and writes the Red illuminator timing packet.

Table 5-77. SSI Red Driver Timing (CMD: 0xc5h)

Byte	Bit(s)	Description	Notes
0	7:0	Enable	See (1)
1	15:8	Strobe Delay MSB	See (1)
2	7:0	Strobe Delay LSB	See (1)
3	7:0	Strobe Offset	See (1)

(1) See TI Solid State Interface Driver Specification (Drawing #250796) for Timing packet details.

5.10.6 SSI Green Driver Timing (CMD: 0xc6h)

This command reads and writes the Green illuminator timing packet.

Table 5-78. SSI Green Driver Timing (CMD: 0xc6h)

Byte	Bit(s)	Description	Notes
0	7:0	Enable	See (1)
1	15:8	Strobe Delay MSB	See (1)
2	7:0	Strobe Delay LSB	See (1)
3	7:0	Strobe Offset	See (1)

(1) See TI Solid State Interface Driver Specification (Drawing #250796) for Timing packet details.

5.10.7 SSI Blue Driver Timing (CMD: 0xc7h)

This command reads and writes the Blue illuminator timing packet.

Table 5-79. SSI Blue Driver Timing (CMD: 0xc7h)

Byte	Bit(s)	Description	Notes
0	7:0	Enable	See (1)
1	15:8	Strobe Delay MSB	See (1)
2	7:0	Strobe Delay LSB	See (1)
3	7:0	Strobe Offset	See (1)

(1) See TI Solid State Interface Driver Specification (Drawing #250796) for Timing packet details.

5.10.8 SSI PWM Driver Levels (CMD: 0xceh)

This command reads and writes the current levels when using a PWM driver.

Table 5-80. SSI PWM Driver Levels (CMD: 0xceh)

Byte	Bit(s)	Description	Notes	
0	9:8	Red current MSB		
1	7:0	Red current LSB		
2	9:8	Green current MSB		
3	7:0	Green current LSB		
4	9:8	Blue current MSB		
5	7:0	Blue current LSB		
6	9:8	C1 current MSB		
7	7:0	C1 current LSB		
8	9:8	C2 current MSB		
9	7:0	C2 current LSB		
10	9:8	Sense current MSB		
11	7:0	Sense current LSB		

5.10.9 SSI PWM Driver Levels II (CMD: 0xcfh)

This function reads and writes the secondary current levels when using a PWM driver and Passive3D.

Table 5-81. SSI PWM Driver Levels II (CMD: 0xcfh)

Byte	Bit(s)	Description	Notes
0	9:8	Red current MSB	
1	7:0	Red current LSB	
2	9:8	Green current MSB	
3	7:0	Green current LSB	
4	9:8	Blue current MSB	
5	7:0	Blue current LSB	
6	9:8	C1 current MSB	
7	7:0	C1 current LSB	
8	9:8	C2 current MSB	
9	7:0	C2 current LSB	
10	9:8	Sense current MSB	
11	7:0	Sense current LSB	

5.11 Control Commands (CMD: 0xE_H)

5.11.1 Memory Dump (CMD: 0xe0h)

This command allows memory dump to terminal at the specified start address.

Figure 5-59. Memory Dump (CMD: 0xe0h) Register

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
SA															
R-0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA															
R-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NWO															
R-0															

Table 5-82. Memory Dump (CMD: 0xe0h) Register Field Descriptions

Bit	Field	Type	Reset	Description
47-16	SA	R/W	0	SA(31:0) - Start Address.
15-0	NWO	R/W	0	NWO(15:0) - Number of 32-bit Words

5.11.2 Memory Dump (CMD: 0xe1h)

This command allows memory dump at the specified start address.

Figure 5-60. Memory Dump (CMD: 0xe1h) Register

63	62	61	60	59	58	57	56	55	54	53	52	51	49	48	47
SA															
R-0															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
SA															
R-0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		LMD						Reserved							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															
R-0															

Table 5-83. Memory Dump (CMD: 0xe1h) Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	SA	R/W	0	SA(31:0) - Start Address for memory dump
31-30	Reserved	R	0	
29-24	LMD	R/W	0	LMD(5:0) - Saved Length for Memory Dump. Length is limited to 64.
23-0	Reserved	R	0	

5.11.3 UART Configuration (CMD: 0xe3h)

This function controls the UART configuration for the specified UART port (UART_PORT0, UART _PORT1 or UART_PORT2).

Note: This function may be called prior to starting the RTOS or from within an ISR.

Figure 5-61. UART Configuration (CMD: 0xe3h) Register

79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Reserved															PE
R-0															R-0
63	62	61	60	59	58	57	56	55	54	53	52	51	49	48	47
Reserved				BR				Reserved						DB	
R-0				R-0				R-0						R-0	
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reserved							SDB	Reserved						PAR	
R-0							R-0	R-0						R-0	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							FC	Reserved					RXT		
R-0							R-0	R-0					R-0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXT				Reserved							RXDP
R-0				R-0				R-0							R-0

Table 5-84. UART Configuration (CMD: 0xe3h)

Bit	Field	Type	Reset	Description
79-65	Reserved	R	0	
64	PE	R/W	0	PE0 - Port Enable: Controls the enable state of the specified UART port. Range: 0 - 1; TRUE - Port Enabled, FALSE - Port Disabled
63-60	Reserved	R	0	
59-56	BR	R/W	0	BR(3:0) - Baud Rate Enumeration represents the following configurations URT_2400, URT_4800, URT_9600, URT_14400, URT_19200, URT_38400, URT_57600, URT_115200, URT_1200, URT_923080, URT_230400
55-49	Reserved	R	0	
48-47	DB	R/W	0	DB(1:0) - Data Bits. Determines the number of bits for specified UART port. Enumeration represents the following configurations URT_5DBITS, URT_6DBITS, URT_7DBITS, URT_8DBITS
47-41	Reserved	R	0	
40	SDB	R/W	0	SDB0 - Stop Data Bits Enumeration represents the following configurations URT_1SBITS, URT_2SBITS
39-34	Reserved	R	0	
33-32	PAR	R/W	0	PAR(1:0) - Parity. Determines the data parity type for the specified UART port. Enumeration represents the following configurations URT_NONE, URT_EVEN, URT_ODD
31-25	Reserved	R	0	

Table 5-84. UART Configuration (CMD: 0xe3h) (continued)

Bit	Field	Type	Reset	Description
24	FC	R/W	0	FC0 - Type of UART Flow Control Enumeration represents the following configurations URT_OFF, URT_HW When HW flow control is enabled, data is only transmitted when UARTCTSZ for the specified Port is asserted, and data is only requested when there is space in the receive FIFO for it to be received.
23-19	Reserved	R	0	
18-16	RXT	R/W	0	RXT(2:0) - Type of Receive FIFO Interrupt Trigger Level Enumeration represents the following configurations URT_RX_ONE_EIGHTH_FULL, URT_RX_ONE_FOURTH_FULL, URT_RX_ONE_HALF_FULL, URT_RX_THREE_FOURTHS_FULL, URT_RX_SEVEN_EIGHTHS_FULL
15-11	Reserved	R	0	
10-8	TXT	R/W	0	TXT(2:0) - Type of Transmit FIFO Interrupt Trigger Level Enumeration represents the following configurations URT_TX_ONE_EIGHTH_FULL, URT_TX_ONE_FOURTH_FULL, URT_TX_ONE_HALF_FULL, URT_TX_THREE_FOURTHS_FULL, URT_TX_SEVEN_EIGHTHS_FULL
7-1	Reserved	R	0	
0	RXDP	R/W	0	RXDp0 - UART RXD Input Polarity Enumeration represents the following configurations URT_NONINV_RXDPOL - Supply non-inverted version of UART_RXD input URT_INV_RXDPOL - Supply inverted version of UART_RXD input

5.11.4 UART Port (CMD: 0xe4h)

This command gets and sets the UART port.

Figure 5-62. UART Port (CMD: 0xe4h) Register

7	6	5	4	3	2	1	0
Reserved						UP	
R-0						R/W-0	

Table 5-85. UART Port (CMD: 0xe4h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0	
1-0	UP	R/W	0	UART Port Enumeration represents the following configurations URT_PORT0 URT_PORT1 URT_PORT2

5.11.5 UART RXD Source Select (CMD: 0xe5h)

This function configures the pin driving UART RXD.

Figure 5-63. UART RXD Source Select (CMD: 0xe5h) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							UP	Reserved							RXDS
R-0							R/W-0	R-0							R/W-0

Table 5-86. UART RXD Source Select (CMD: 0xe5h) Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	Reserved	R	0	
8	UP	R/W	0	UART Port Number. Only two ports are available URT_PORT1 URT_PORT2
7-1	Reserved	R	0	
0	RXDS	R/W	0	RXD Source Select Range: 0 - 1 UART_RXD - Sourced by UART_x_RXD pin UART_LAMPSTAT - Sourced by LAMPSTAT pin

5.11.6 Auto Update Enable (CMD: 0xe6h)

This function configures port for Auto Update to DM365 when enabled.

Figure 5-64. Auto Update Enable (CMD: 0xe6h) Register

7	6	5	4	3	2	1	0
Reserved							AUE
R-0							R/W-0

Table 5-87. Auto Update Enable (CMD: 0xe6h) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0	
0	AUE	R/W	0	Auto Update Enable Range: 0 - 1 TRUE: Enable UART Auto Update Connectivity FALSE: Disable UART Auto Update Connectivity

5.11.7 Gamma Table (CMD: 0xefh)

This function loads a gamma look-up table into memory from flash or reads the table number of the gamma look-up table currently loaded in memory upon the user's request. A single load is accomplished by loading data for red, green, and blue look-up tables. DLP Composer™ can be used to create new gamma tables or modify existing gamma tables.

Figure 5-65. Gamma Table (CMD: 0xefh) Register

7	6	5	4	3	2	1	0
Reserved				GLUT			
R-0				R-0			

Table 5-88. Gamma Table (CMD: 0xefh) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0	
3-0	GLUT	R/W	0	GLUT(3:0) - Gamma Look-Up table Range: 0 - 31

I²C Command Table

```
Cmd   BytesIn     BytesOut      fnI2CWrite              fnI2CRead         SendToSlave
SpecialFlag

/********************************** Command 0x00 reserved for Status ***************************/
    0x00,   0x00,       0x01,       cmdF_Reserved,          cmdF_StatusRead,        FALSE,
  0,
    0x01,   0x01,       0x01,       cmdF_SetProjectionMode, cmdF_GetProjectionMode, TRUE,
  0,
    0x03,   0x03,       0x02,       cmdF_UtlSetCWIndex,     cmdF_UtlGetCWIndex,     TRUE,
  0,
    0x04,   0x03,       0x03,       cmdF_SetIndexDelayFine, cmdF_GetIndexDelayFine, TRUE,
  0,
    0x05,   0x02,       0x00,       cmdF_SetCWSpeed,        cmdF_Reserved,          TRUE,
  0,
    0x06,   0x02,       0x01,       cmdF_CWSpinningControl, cmdF_Reserved,          TRUE,
  0,
    0x07,   0x02,       0x01,       cmdF_CWCoastControl,    cmdF_Reserved,          TRUE,
  0,
    0x08,   0x02,       0x01,       cmdF_CWDebugControl,    cmdF_Reserved,          TRUE,
  0,
    0x0a,   0x02,       0x02,       cmdF_SetCWVSync,        cmdF_GetCWVSync,        TRUE,
  0,
    0x0b,   0x01,       0x08,       cmdF_SetGetTestMux,     cmdF_GetCWIndexClock,   FALSE,
  0,
    0x0c,   0x02,       0x02,       cmdF_SetHWTestMux,      cmdF_GetHWTestMux,      TRUE,
  0,
    0x0d,   0x02,       0x02,       cmdF_SetSWTestMux,      cmdF_GetSWTestMux,      TRUE,
  0,
    0x0e,   0x04,       0x06,       cmdF_SetAppDebug,       cmdF_GetAppDebug,       FALSE,
  0,
    0x0f,   0x03,       0x00,       cmdF_SetEnableUSBDebug, cmdF_Reserved,          FALSE,
  0,

/*****************************************************************************************
****/
    0x10,   0x01,       0x01,       cmdF_SetVerticalFlip,   cmdF_GetVerticalFlip,   TRUE,
  0,
    0x11,   0x01,       0x01,       cmdF_SetTPGPattern,     cmdF_GetTPGPattern,     TRUE,
  0,
    0x12,   0x02,       0x02,       cmdF_SetTPGCSize,       cmdF_GetTPGCSize,       TRUE,
  0,
    0x13,   0x06,       0x06,       cmdF_SetSFGColor,       cmdF_GetSFGColor,       TRUE,
  0,
    0x15,   0x01,       0x00,       I2CRead,                cmdF_Reserved,          TRUE,
  0,
    0x16,   0x02,       0x02,       cmdF_ImpSetBrightness,  cmdF_ImpGetBrightness,  TRUE,
  0,
    0x17,   0x02,       0x02,       cmdF_ImpSetContrast,    cmdF_ImpGetContrast,    TRUE,
  0,
    0x18,   0x33,       0x33,       cmdF_SetSourceConfig,   cmdF_GetSourceConfig,   TRUE,
  0,
    0x19,   0x02,       0x01,       cmdF_SetSourceCSC,      cmdF_GetSourceCSC,      TRUE,
  0,
    0x1b,   0x06,       0x06,       cmdF_SetImageOffset,    cmdF_GetImageOffset,    TRUE,
  0,
```

```
    0x1e,   0x02,       0x02,       cmdF_SetBGColorMode,    cmdF_GetBGColorMode,    TRUE,
  0,
    0x1f,   0x01,       0x01,       cmdF_SetHorizontalFlip, cmdF_GetHorizontalFlip, TRUE,
  0,

/*****************************************************************************************
****/
    0x21,   0x00,       0x04,       cmdF_Reserved,          cmdF_GetSFGResolution,  FALSE,
  0,
    0x22,   0x02,       0x00,       cmdF_SplashLoad,        cmdF_Reserved,          FALSE,
  0,
    0x23,   0x11,       0x11,       cmdF_SetDisplay,        cmdF_GetDisplay,        FALSE,
  0,
    0x25,   0x06,       0x06,       cmdF_SetSrcOffset,      cmdF_GetSrcOffset,      TRUE,
  0,
    0x26,   0x03,       0x02,       cmdF_SetSrcPort,        cmdF_GetSrcPort,        TRUE,
  0,
    0x27,   0x01,       0x04,       cmdF_SetGetSrcPort,     cmdF_GetVsyncPeriod,    FALSE,
  0,
    0x28,   0x01,       0x01,       cmdF_SetChannelSource,  cmdF_GetChannelSource,  TRUE,
  0,
    0x29,   0x01,       0x01,       cmdF_SetFreeze,         cmdF_GetFreeze,         TRUE,
  0,
    0x2a,   0x08,       0x07,       cmdF_SetChannelConfig,  cmdF_GetChannelConfig,  TRUE,
  0,
    0x2b,   0x01,       0x01,       cmdF_SetTPGBorder,      cmdF_GetTPGBorder,      TRUE,
  0,
    0x2c,   0x04,       0x04,       cmdF_SetTPGResolution,  cmdF_GetTPGResolution,  TRUE,
  0,
    0x2d,   0x03,       0x03,       cmdF_SetGammaCurves,    cmdF_GetGammaCurves,    TRUE,
  0,
    0x2e,   0x02,       0x06,       cmdF_SetGetPixelClock,  cmdF_GetCalcPixelClock, FALSE,
  0,
    0x2f,   0x11,       0x11,       cmdF_SetSRCDescription, cmdF_GetSRCDescription, FALSE,
  0,
    /********************************** Command 0x30 reserved for Programming
Mode******************/
    0x30,   0x01,       0x00,       cmdF_UtlProgramMode,    cmdF_Reserved,          TRUE,
  0,

/*****************************************************************************************
****/
    0x7f,   0x01,       0x01,       cmdF_SetDMDSSEnable,    cmdF_GetDMDSSEnable,    FALSE,
  0,

/*****************************************************************************************
****/
    0x81,   0x00,       0x04,       cmdF_Reserved,          cmdF_GetCmdDmdReso,     TRUE,
  0,
    0x84,   0x01,       0x01,       cmdF_SetPower,          cmdF_GetAppState,       TRUE,
  0,
/*****************************************************************************************
****/
    0x90,   0x01,       0x00,       cmdF_DDP_SWReset,       cmdF_Reserved,          FALSE,
  0,
    0x91,   0x00,       0x01,       cmdF_Reserved,          cmdF_DDPResetCount,     FALSE,
  0,
    0x93,   0x01,       0x01,       cmdF_SetUSBClockEnable, cmdF_GetUSBClockEnable, FALSE,
  0,
    0x98,   0x01,       0x01,       cmdF_SetVertSharpness,  cmdF_GetVertSharpness,  TRUE,
  0,
    0x99,   0x01,       0x01,       cmdF_SetHorizSharpness, cmdF_GetHorizSharpness, TRUE,
  0,
    0x9a,   0x01,       0x01,       cmdF_SetScalarBypassmode,  cmdF_GetScalarBypassmode,  TRUE,
  0,
    0x9c,   0x01,       0x01,       cmdF_TempSensorWrite,   cmdF_TempSensorRead,    FALSE,
```

```
  0,
    0x9d,   0x00,       0x01,       cmdF_Reserved,          cmdTRPDMDErrorStatusRead,
FALSE,          0,

/*****************************************************************************************************
****/
    0xa0,   0x04,       0x02,       cmdF_SetFanFreqCycle,   cmdF_GetFanFreqCycle,   TRUE,
  0,

/*****************************************************************************************************
****/
    0xb0,   0x08,       0x38,       cmdF_SetPWMOutputConfig,cmdF_GetPWMOutputConfig,FALSE,
  0,
    0xb1,   0x06,       0x14,       cmdF_SetPWMInputConfig, cmdF_GetPWMInputConfig, FALSE,
  0,
    0xb3,   0x04,       0x04,       cmdF_SetDispOffsets,    cmdF_GetDispOffsets,    TRUE,
  0,
    0xbf,   0x01,       0x01,       cmdF_SetEmergShutdown,  cmdF_GetEmergShutdown,  TRUE,
  0,

/*****************************************************************************************************
****/
    0xc1,   0x14,       0x14,       cmdF_SetSSIRedCurrents, cmdF_GetSSIRedCurrents, FALSE,
  0,
    0xc2,   0x14,       0x14,       cmdF_SetSSIGrnCurrents, cmdF_GetSSIGrnCurrents, FALSE,
  0,
    0xc3,   0x14,       0x14,       cmdF_SetSSIBluCurrents, cmdF_GetSSIBluCurrents, FALSE,
  0,
    0xc4,   0x00,       0x03,       cmdF_Reserved,          cmdF_GetSSIDriverStatus,FALSE,
  1,
    0xc5,   0x04,       0x04,       cmdF_SetSSIRedDriverTiming, cmdF_GetSSIRedDriverTiming,
 FALSE,          1,
    0xc6,   0x04,       0x04,       cmdF_SetSSIGrnDriverTiming, cmdF_GetSSIGrnDriverTiming,
  FALSE,          1,
    0xc7,   0x04,       0x04,       cmdF_SetSSIBluDriverTiming, cmdF_GetSSIBluDriverTiming,
  FALSE,          1,
    0xce,   0x0C,       0x0C,       cmdF_SetSSIPWMDriverLevels, cmdF_GetSSIPWMDriverLevels,
  FALSE,          0,
    0xcf,   0x0C,       0x0C,       cmdF_SetSSIPWMDriverLevels2,cmdF_GetSSIPWMDriverLevels2,
  FALSE,          0,

/*****************************************************************************************************
****/
    0xe0,   0x06,       0x00,       cmdF_MemoryTDump,       cmdF_Reserved,          FALSE,
  0,
    0xe1,   0x08,       0xFF,       cmdF_SetGetMemoryDump,  cmdF_MemoryDump,        FALSE,
  0,
    0xe3,   0x0a,       0x0a,       cmdF_SetUARTConfig,     cmdF_GetUARTConfig,     FALSE,
  0,
    0xe4,   0x01,       0x02,       cmdF_SetGetUARTPort,    cmdF_GetUARTStatus,     FALSE,
  0,
    0xe5,   0x02,       0x01,
cmdF_SetUARTRxdSourceSelect,cmdF_GetUARTRxdSourceSelect,FALSE,  0,
    0xe6,   0x01,       0x00,       cmdF_EnableAutoUpdate,  cmdF_Reserved,          FALSE,
  0,
    0xef,   0x01,       0x01,       cmdF_SetGammaTable,     cmdF_GetGammaTable,     TRUE,
  0,

/*****************************************************************************************************
****/
```

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