

Powering AMIC110, AMIC120, AM335x, and AM437x with TPS65216

System designs utilizing the TPS65216 Power Management IC must follow this user's guide for connectivity with the following processors:

- Sitara™ AMIC110 and AMIC120 industrial communications processors
- Sitara AM335x and AM437x Arm® application processors

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Trademarks

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1 TPS65216 Overview

The TPS65216 is an integrated Power Management IC for Sitara processors:

- Power sequencing for Sitara AMIC, AM3, and AM4 processors
- Three DC-DC step-down converters
- One LDO and one Load-Switch
- Active output discharge on all supplies
- Integrated voltage supervisor
- Power fail comparator for external or system supply

2 Connection Diagram for AMIC110

Figure 1 describes the supply mapping between AMIC110 and the TPS65216. Any ICs on the board that interface with AMIC110 should use DCDC4 for 3.3 V I/O supply and LDO1 for 1.8 V I/O supply.

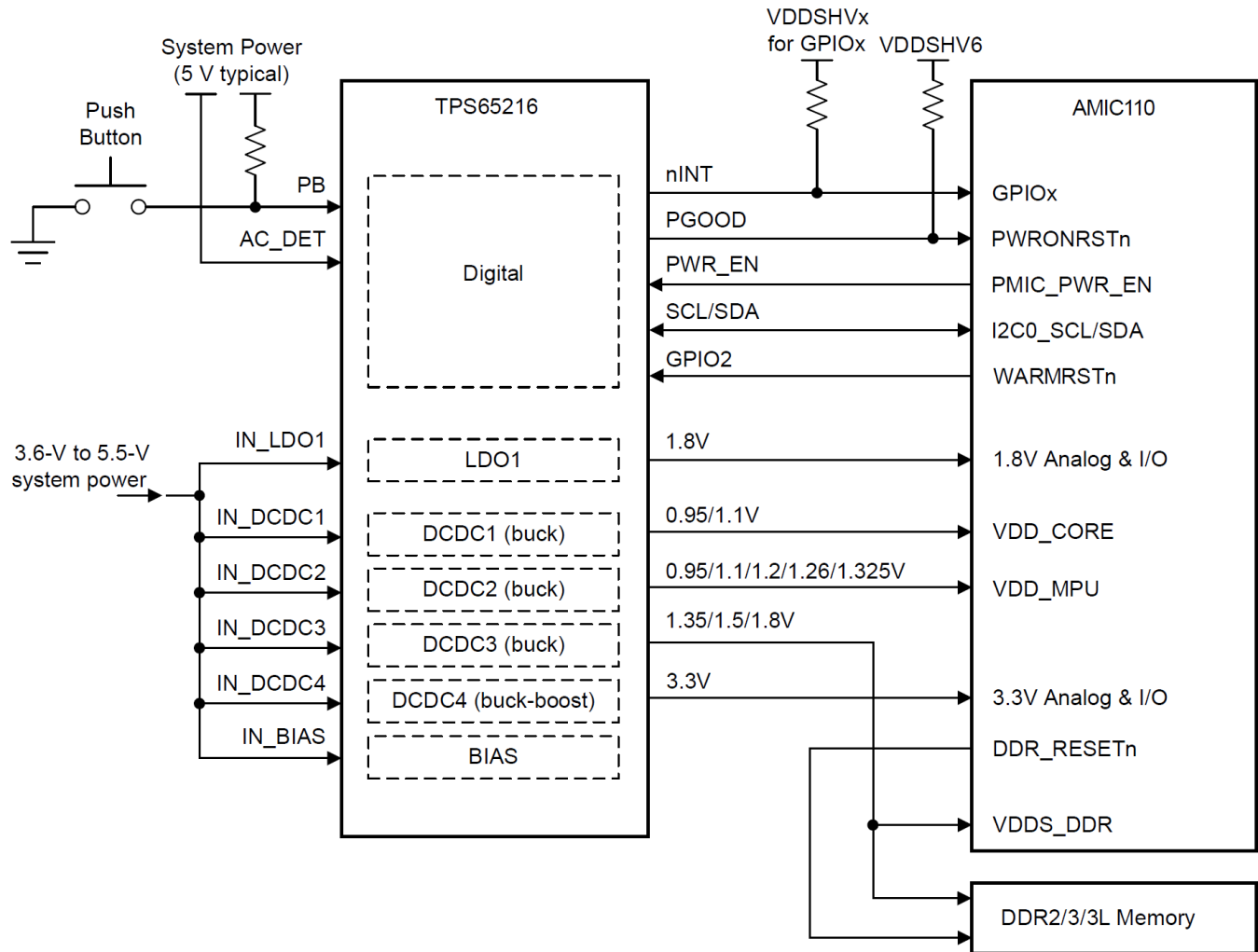


Figure 1. AMIC110 Connection Diagram

2.1 Power Rails for AMIC110

Table 1. Power Rails for AMIC110

| TPS65216 | Voltage (V) | AMIC110 |
|----------|-------------------------|------------------------|
| DCDC1 | 0.95/1.1 | VDD_CORE |
| DCDC2 | 0.95/1.1/1.2/1.26/1.325 | VDD_MPU |
| DCDC3 | 1.35/1.5 | VDDS_DDR DDR3L/DDR3 |
| DCDC4 | 3.3 | VDDSHVx (3.3 V) |
| | | VDDA3P3V_USB0/1 |
| LDO1 | 1.8 | VDDS |
| | | VDDS_RTC |
| | | VDDSHVx (1.8 V) |
| | | VDDS_SRAM_CORE_BG |
| | | VDDS_SRAM_MPU_BB |
| | | VDDS_PLL_DDR |
| | | VDDS_PLL_CORE_LCD |
| | | VDDS_OSC |
| | | VDDA1P8V_USB0/1 |
| | | VDDA_ADC |

3 Connection Diagram for AM335x

Figure 2 shows the connections between AM335x and the TPS65216. When using the ZCE package, VDD_CORE and VDD_MPU are combined on the device. The combined supply input should be connected to DCDC1 and DCDC2 can be left not-connected. Any ICs on the board that interface with AMIC110 should use DCDC4 for 3.3 V I/O supply and LDO1 for 1.8 V I/O supply.

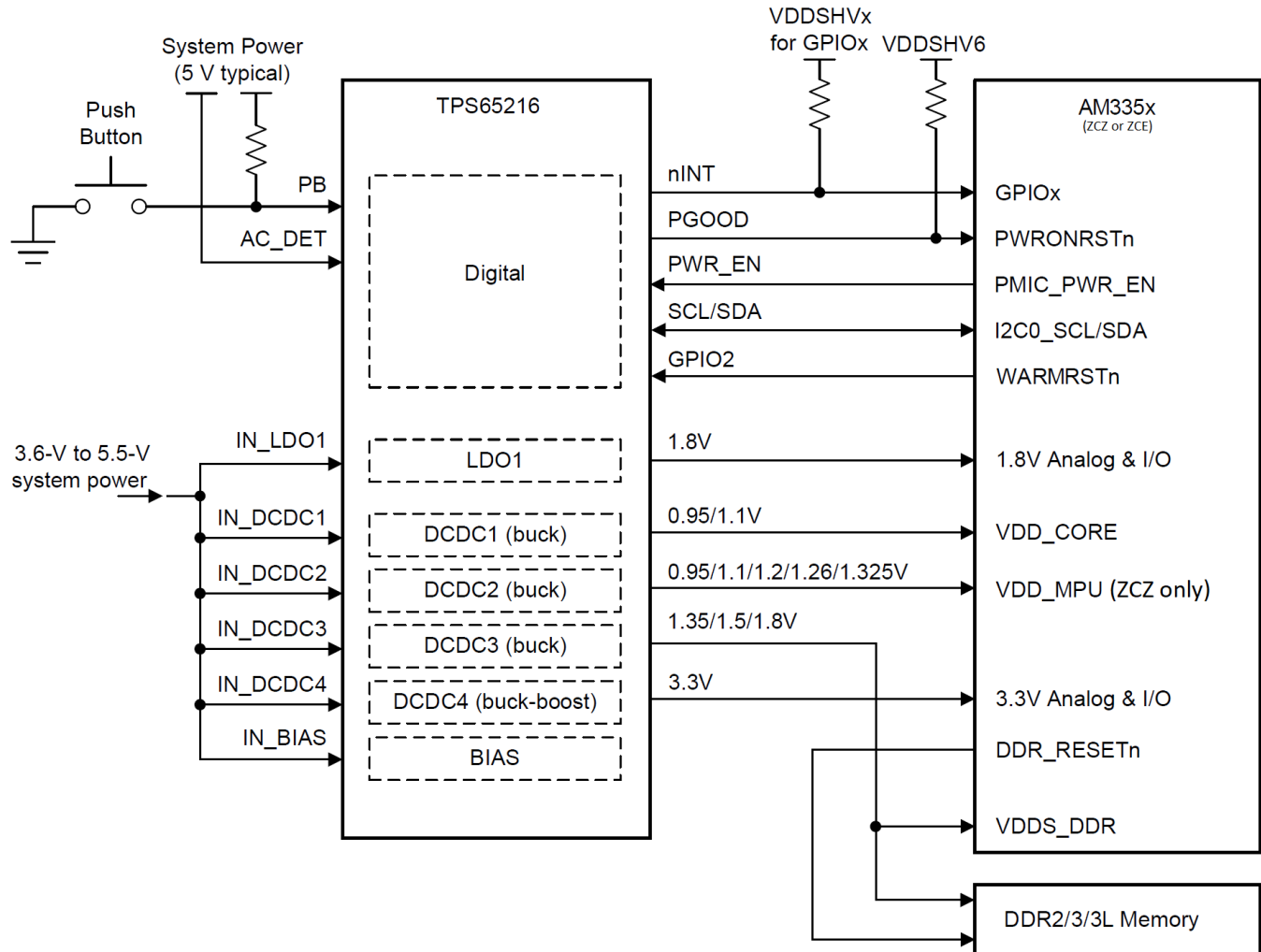


Figure 2. AM335x Connection Diagram

3.1 Power Rails for AM335x

Table 2. Power Rails for AM335x

| TPS65216 | Voltage (V) | AM335x |
|----------|-------------------------|------------------------|
| DCDC1 | 0.95/1.1 | VDD_CORE |
| DCDC2 | 0.95/1.1/1.2/1.26/1.325 | VDD_MPU |
| DCDC3 | 1.35/1.5 | VDDS_DDR DDR3L/DDR3 |
| DCDC4 | 3.3 | VDDSHVx (3.3 V) |
| | | VDDA3P3V_USB0/1 |
| LDO1 | 1.8 | VDDS |
| | | VDDS_RTC |
| | | VDDSHVx (1.8 V) |
| | | VDDS_SRAM_CORE_BG |
| | | VDDS_SRAM_MPU_BB |
| | | VDDS_PLL_DDR |
| | | VDDS_PLL_CORE_LCD |
| | | VDDS_OSC |
| | | VDDA1P8V_USB0/1 |
| | | VDDA_ADC |

4 Connection Diagram for AMIC120 and AM437x

Figure 3 shows the connections between AM437x or AMIC120 and the TPS65216. If LPDDR2 memory is used, an additional 1.8 V supply is required. GPIO1 is programmed to properly sequence the additional supply and should be tied to the external supply's enable pin as seen in Figure 4. To adjust the DCDC3 voltage for each DDR type, see Section 7.

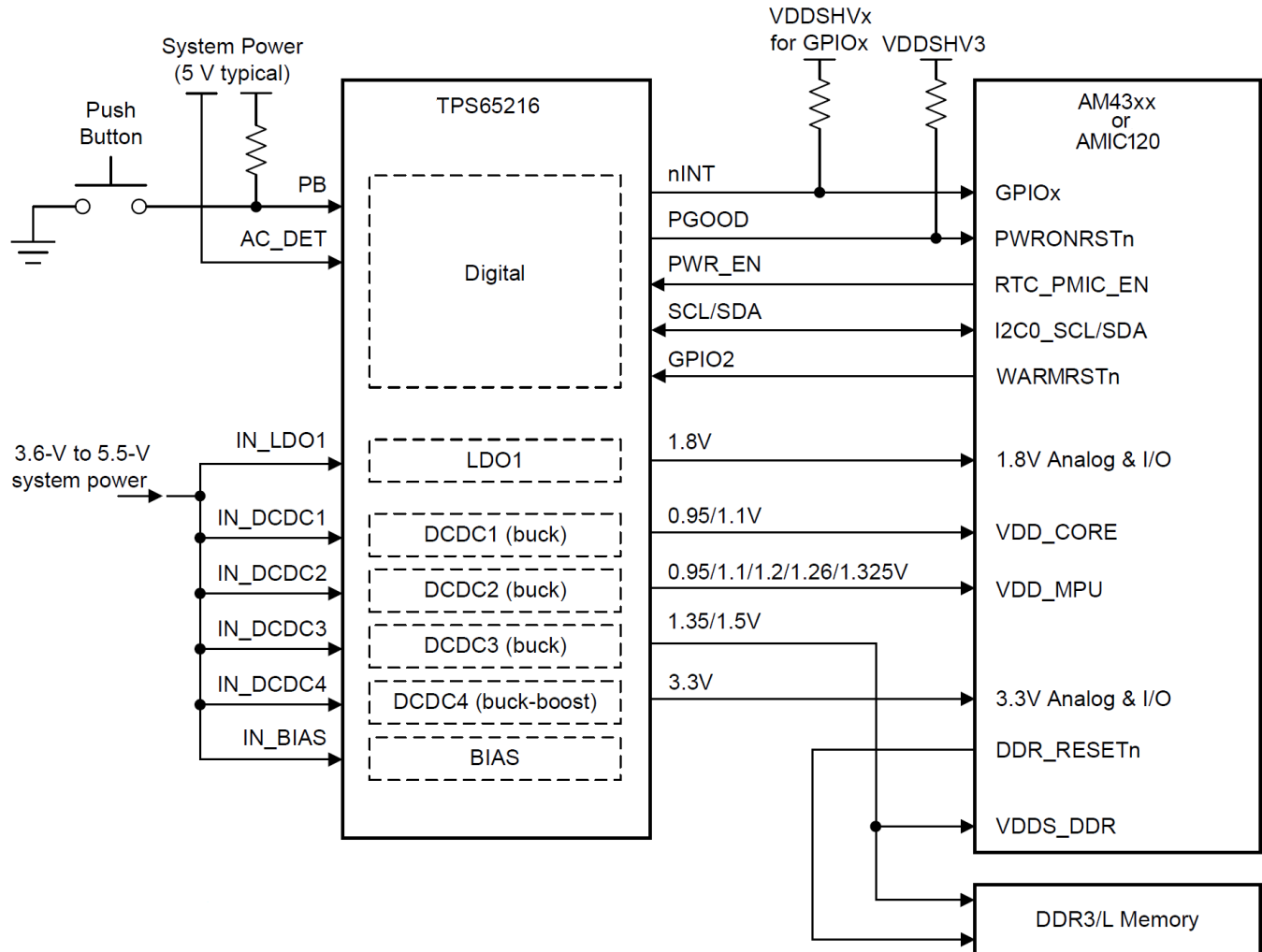


Figure 3. AMIC120 and AM437x Connection Diagram

4.1 Power Rails for AMIC120 and AM437x

Table 3 matches the AMIC120 power terminals with the appropriate power rail from the TPS65216. It also matches for AM437x.

Table 3. Power Rails for AMIC120 and AM437x

| TPS65216 | Voltage (V) | AM437x |
|----------|-------------------------|-------------------------------|
| DCDC1 | 0.95/1.1 | VDD_CORE |
| DCDC2 | 0.95/1.1/1.2/1.26/1.325 | VDD_MPU |
| DCDC3 | 1.2/1.35/1.5 | VDDS_DDR LPDDR2/DDR3L/DDR3 |
| DCDC4 | 3.3 | VDDSHVx(3.3 V) |
| | | VDDA3P3V_USB0/1 |
| | | VDDS3P3V_IOLDO |
| LDO1 | 1.8 | VDDS |
| | | VDDS_RTC |
| | | VDDSHVx(1.8 V) |
| | | VDDS_SRAM_CORE_BG |
| | | VDDS_SRAM_MPU_BB |
| | | VDDS_PLL_DDR |
| | | VDDS_PLL_CORE_LCD |
| | | VDDS_OSC |
| | | VDDA1P8V_USB0/1 |
| | | VDDA_ADC0/1 |
| | | VDDS_PLL_MPU |
| | | VDDS_CLKOUT |

5 Power Rails for RTC Domain

For normal RTC operation during the Sitara processor ACTIVE state, see [Figure 5](#). The connection diagram can stay the same if the RTC is not used; the RTC does not need to be explicitly disabled. The resistor + capacitor on RTC_PWRONRSTn is required to ensure the 1.8 V supply is stable before reset release. Connecting RTC_PWRONRSTn directly to 1.8 V causes unpredictable behavior.

This diagram does not support the RTC-only power state. RTC data is lost when LDO1 and the processor is powered off. To keep RTC data in between power states a dedicated, always-on 1.8 V supply for VDDS_RTC is required. This can be done by following the below diagram except replace LDO1 with an always-on 1.8 V supply.

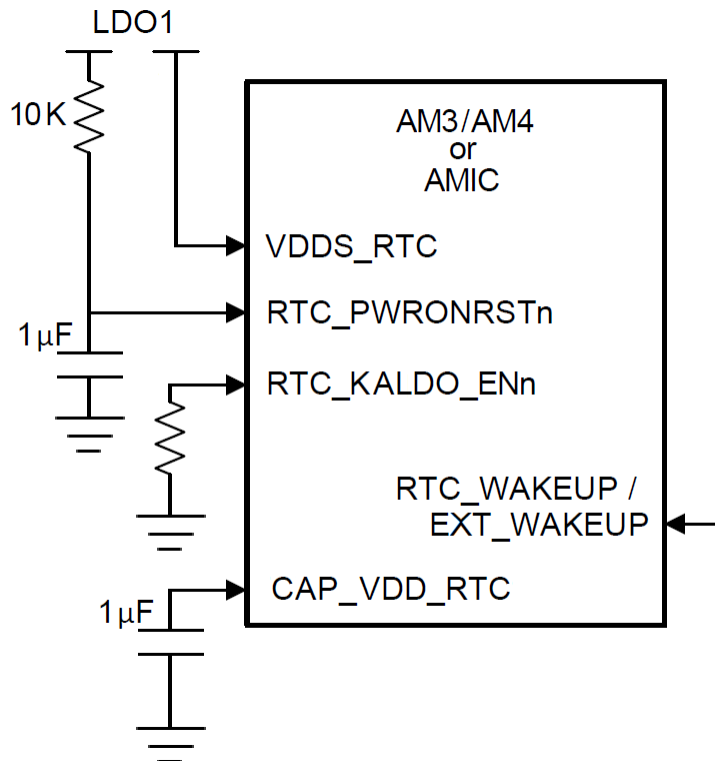


Figure 5. Power Rails for RTC Domain

6 TPS65216 Supply Sequencing

The TPS65216 supply sequencer is controlled by a series of strobes with a 2 or 4 ms delay in between. A visual reference for the power-up and power-down sequence of the TPS65216 is shown in Figure 6. For a table of the strobes and assignments, see Table 4. No changes to the defaults are required; this sequence is designed for AMIC110, AMIC120, AM335x, and AM437x.

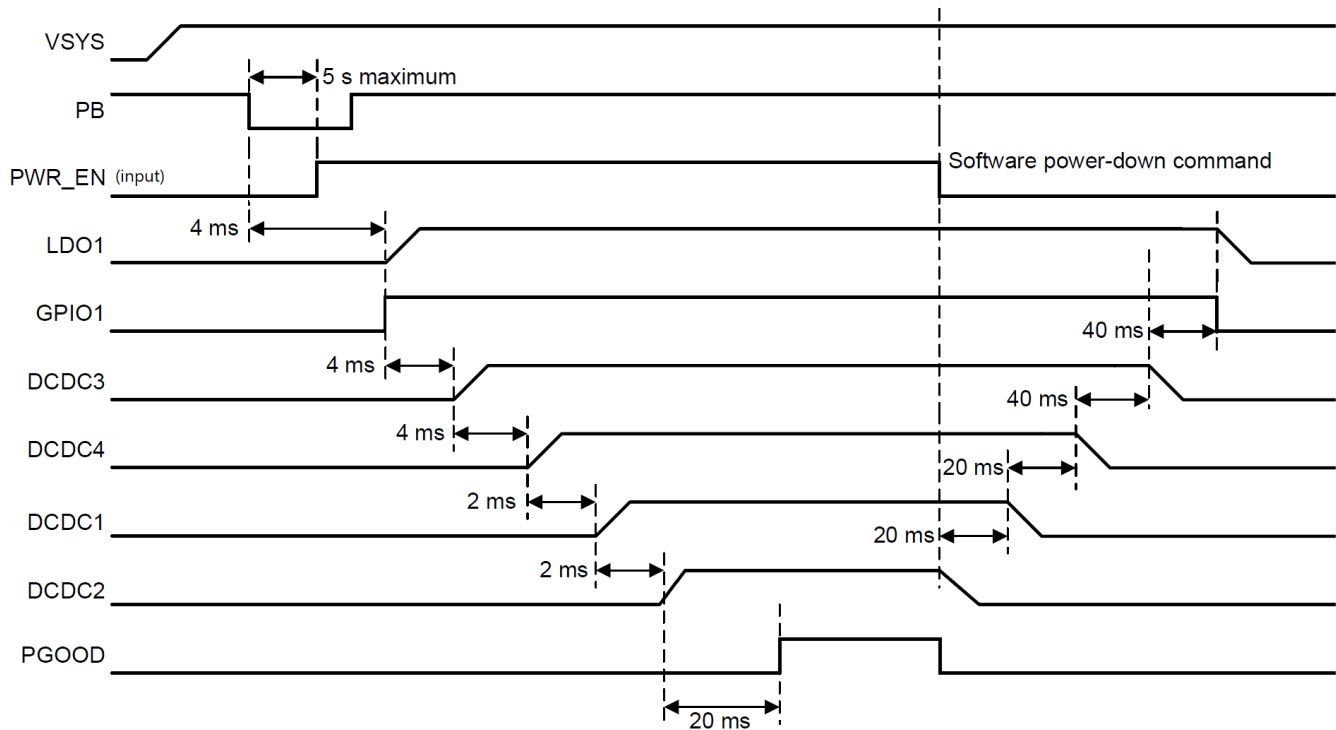


Figure 6. TPS65216 Sequencing Diagram

The power-up sequence is defined by a series of ten strobes and nine delay times. Each output rail is assigned to a strobe to determine the order in which the rails are enabled. The delay time in-between strobes is 2 ms by default. Table 4 lists the default strobe assignments for TPS65216.

The power-down sequence is the reverse of the power-up sequence. However, strobe 1 and 2 are not included in the power-down. Any supplies assigned to strobe 1 or 2 will remain powered on at the end of the power-down sequence.

Table 4. TPS65216 Strobe Sequence

| | |
|-----------|-------|
| Strobe 1 | |
| Strobe 2 | |
| Strobe 3 | LDO1 |
| | GPIO1 |
| Strobe 4 | |
| Strobe 5 | DCDC3 |
| Strobe 6 | |
| Strobe 7 | DCDC4 |
| Strobe 8 | DCDC1 |
| Strobe 9 | DCDC2 |
| Strobe 10 | |

7 Memory Voltage Selection

DCDC3 can be configured to support a variety of DDR memory voltages. The desired voltage can be selected by placing a 1% resistor to ground on the DC34_SEL pin. Table 5 lists the available memory voltages and the needed resistor for each.

Table 5. DCDC3 Voltage Selection

| Memory | DCDC3 Voltage (V) | Resistor (k Ω) |
|--------|-------------------|------------------------|
| LPDDR2 | 1.2 | 0 (tie to ground) |
| DDR3L | 1.35 | 12.1 |
| DDR3 | 1.5 | 20 |
| DDR2 | 1.8 | 31.6 |

8 Warm Reset

The TPS65216 supports warm reset functionality that is enabled by default and can be disabled through I2C. When enabled, asserting GPIO2 low causes DCDC1 and DCDC2 to slew back to their default value of 1.1 V.

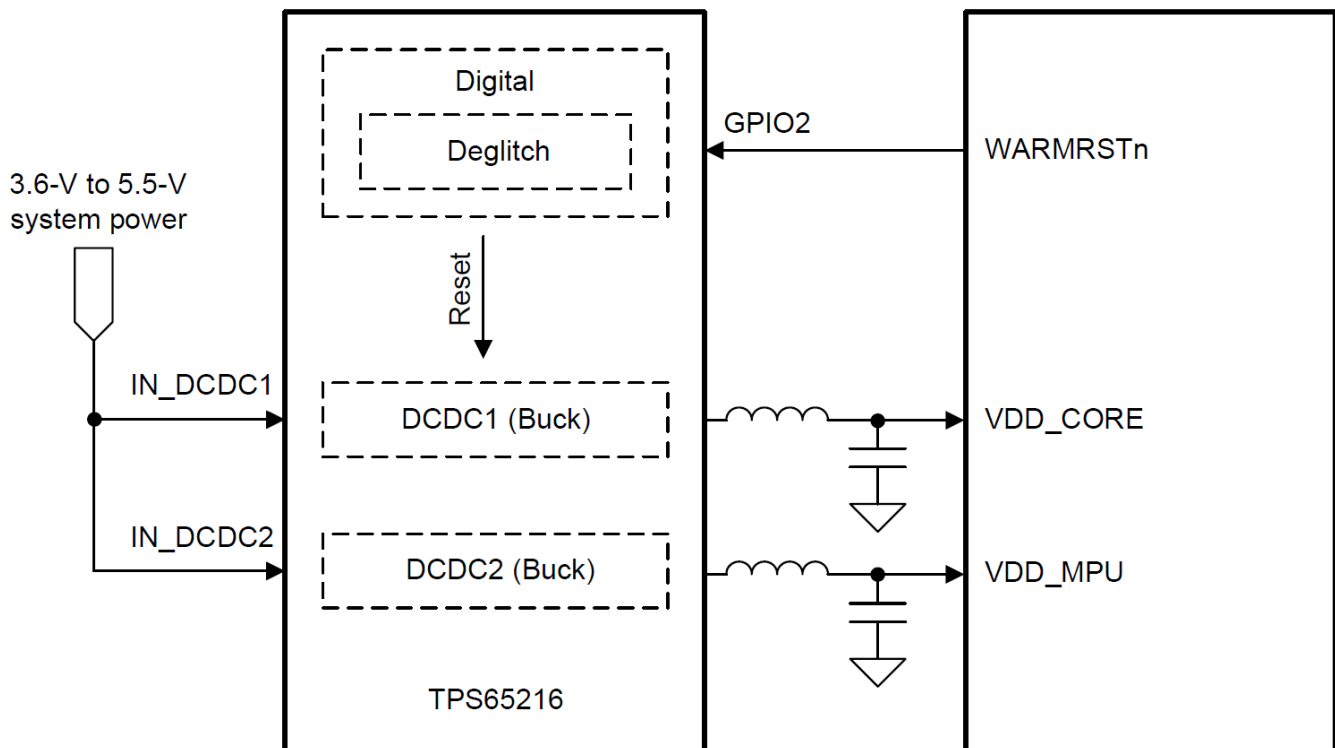


Figure 7. TPS65216 Warm Reset Functionality

9 Pullup Resistors

The TPS65216 PMIC uses open-drain outputs for nINT, PGOOD, SCL, and SDA. These signals should be pulled up using the same supply that powers VDDSHVx for each signal on the Sitara SoC. For example, I2C0 on AM335x is in the VDDSHV6 I/O domain. This VDDSHV6 is supplied by DCDC4 at 3.3 V. Therefore, I2C0 SCL and SDA should be pulled up to 3.3 V from DCDC4. If VDDSHV6 was operating at 1.8 V supplied by LDO1, then I2C0 SCL and SDA should be pulled up to 1.8 V from LDO1.

The PB input needs to operate at all times so it should be pulled up to VSYS.

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