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Texas Instruments Enhanced Plastic Products Reliability Report

(Subject To Attached Disclaimers)

Device Type/Device Family: TMS5703137CGWTMEP
Package Type: 337/GWT
Wafer Fabrication Facility: TSMC-F14
Assembly/Test Facility: TIPI
Compiled: 10/13

Biased Life Test

Test Method: JESD22-A108
Test Condition: 125°C / 1000 hours or equivalent
Sample Size: 6189
Rejects: 3
Activation Energy (eV): 0.5
Equivalent Device Hours: 1.70E+08
Failure Rate (FIT)*: 3

*Derated to +55°C with a 60% Confidence Level

Note: Data for EP product is specific to device technology and foundry. For this reason the FIT rate above may differ from Ti's external web page. This does not reflect a difference in quality but only a difference in sample size.

Package Related Tests

<u>Description</u>	<u>Condition</u>	<u>Referenced Method</u>	<u>Sample Size</u>	<u>Rejects</u>	
Biased Humidity or HAST	85°C / 85% / 1000 hours or 130°C / 85% / 96 hours	JESD22-A101 JESD22-A110	615	0	*
Autoclave or Unbiased HAST	121°C / 2 atm / 96 hours or 130°C / 85% / 96 hours	JESD22-A102	231	0	*
Temperature Cycle	-65°C to +150°C non-biased for 500 cycles or equivalent	JESD22-A104	231	0	*
High Temp Storage	150°C / 1,000 hours	JESD22-A103-A	77	0	*

* Preconditioning per JEDEC Std. 22, Method A112/A113

Initial Product Qualification

The subject Enhanced Plastic device, device family, and/or package family have passed Texas Instruments product qualification as follows:

<u>Description</u>	<u>Condition</u>	<u>Referenced Method</u>	<u>Sample Size</u>	
Electrical Characterization	TI Data Sheet	N/A	3 lot(s)/30 Units	
Electrostatic Discharge Sensitivity	HBM	EIA/JESD22-A114	N/A	
	MM	EIA/JESD22-A115	N/A	
	CDM	JESD22-C101	N/A	
Latch-up	Per Technology	EIA/JESD78	20/0	
Physical Dimensions	TI Data Sheet	EIA/JESD22- B100	30/0	
Thermal Impedance	Theta-JA on board	EIA/JESD51	Per Pin-Package	
Bias Life Test	125°C / 1000 hours or equivalent	JESD22-A108	231/0	
Biased Humidity or HAST	85°C / 85% / 1000 hours or	JESD22-A101	615/1 See Note below	*
	130°C / 85% / 96 hours	JESD22-A110		
Autoclave or Unbiased HAST	121°C @ 2 atm / 96 hours or	JESD22-A102	231/0	*
	130°C / 85% / 96 hours	JESD22-A110		
Temperature Cycle	-65°C to +150°C non-biased for 500 cycles or equivalent	JESD22-A104	231/0	*
High Temp Storage	150°C / 1,000 hours	JESD22-A103-A	45/0	*
Solderability	Condition A (steam age for 8 hours)	ANSI/J-STD-002-92	N/A	
Bond Strength	-	ASTM F-459	/	
Moisture Sensitivity	Surface Mount Only	J-STD-020-A	24/0	

* Preconditioning per JEDEC Std. 22, Method A112/A113

Note: THB fail at 500 hrs associated with improper PCC wirebond profile; 8D report available. EP device with Au wire not susceptible to this fail mode.

Supplemental Device Characteristics

Master Die: YF771529C/Q	Assembly Site: TIPI
Wafer Fab: TSMC-F14	Pin/Package Type: 337/GWT
Fab Process: 12F021.M6	Solder Ball Composition: SnPb
Fab Technology: CMOS	
Die Revision: C	Mount Compound: ABLESTIK 2000T
Passivation:	Bond: Au/0.8 MILS
Metal 1: Cu	Mold Compound: SHINETSU KMC3580LTVA
Metal 2: Cu	Packaged Die Thickness: 11 MILS/ 280 UM
Metal 3: Cu	MSL Level: LEVEL3-260CG
Metal 4: Cu	ESD Class (per MIL-PRF-38535): 2kV HBM; 500V CDM
Metal 5: Cu	
Metal 6: Cu + AICap (AICu bond pad)	

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