

TMS320TCI6618

Doubling performance for 4G wireless base stations

TMS320TCI6618

SoC



Product bulletin

The race towards 4G is on! As wireless data rates increase with high-speed 3G now, and move toward the future with even faster 4G services, the ability to efficiently handle the large number of bits flowing through base stations becomes critically important. Without the right silicon technology and design, base stations cannot handle the immense amount of network traffic that 4G demands. Operators are being forced to move to heterogeneous networks that combine macro and small cell solutions to deliver affordable bandwidth. Multiple input, multiple output (MIMO) antenna arrays and advanced receivers are key elements of the new wireless standards that increase the bandwidth capabilities of the network.

The TMS320TCI6618 is a new multistandard wireless base station system-on-chip (SoC) that delivers double the LTE performance over existing 40-nm solutions while reducing the SoC power consumption for macro and compact base stations to the industry's lowest levels – 0.075 mW/GMAC of power. The TCI6618 is ideally suited to the data-centric performance that wireless network operators are demanding today for 4G macro base stations. Its multiple TMS320C66x DSP cores provide programmable performance, while new hardware accelerators focus on bit rate processing to allow base station manufacturers to deliver up to 40 percent more spectral efficiency over conventional decoding techniques.

TI's TCI6618 is a scalable SoC based on TI's KeyStone architecture and C66x DSP core. It features the highest performance fixed- and floating-point operation, allowing base station designers to deliver the capacity and performance to meet tomorrow's demands today. The TCI6618 enables manufacturers to reduce the cost per bit on the operator's expensive air interface, as well as lower power consump-

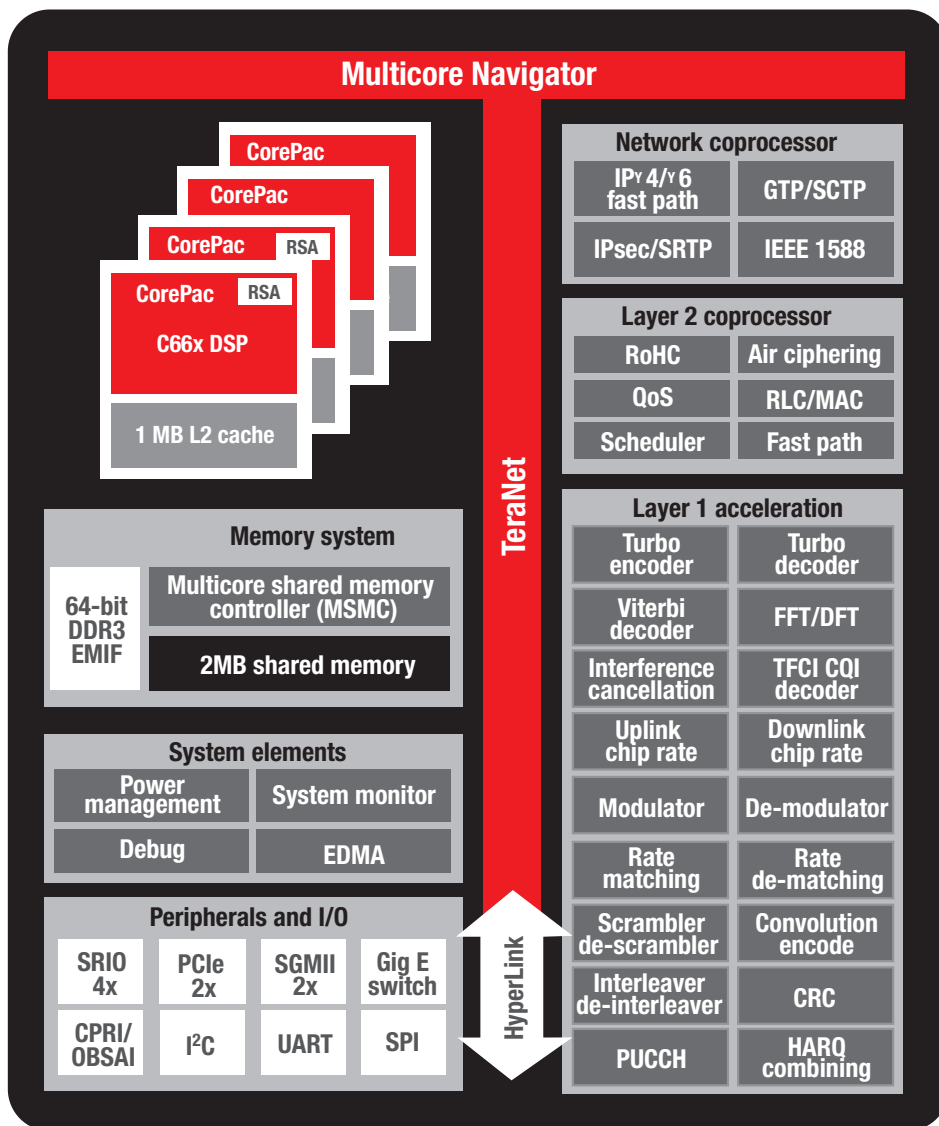
tion for new base station designs. Multicore Navigator, a queue-based packet structure, coupled with TI's Open Navigator programming interface, gives designers the ability to add differentiating, value-added features easily.

With both fixed- and floating-point processing on each DSP core, the TCI6618 enables base station designers to take advantage of rapid algorithm prototyping and quick software redesigns, reducing costs and development time. Because the C66x cores are so powerful, significantly fewer cores are needed to provide four times the processing power of previous generations of TI processors. Designers will enjoy simplified programming with fewer cores, along with increased performance. It also delivers 5.5 times cycle reduction over previous generations in MIMO decoding, and enables a software defined MIMO decoder.

In addition, designers can benefit from the TCI6618's pin and software compatibility with the previously announced TCI6616 wireless base station SoC, to design multistandard base stations that support all 2G, 3G, and 4G standards. OEMs can simplify the migration

Key features

- Newest multistandard wireless base station system-on-chip (SoC) that delivers double the LTE performance over existing solutions while reducing SoC power consumption to the industry's lowest levels at 0.075 mW/GMAC of power
- Highest performing multicore base station SoC on the market today, delivering 2X the wireless system performance of any other base station SoC for 4G, with unmatched throughput and lowest latency
- Bit rate coprocessor increases the SoC system performance and enables advanced receiver algorithms to achieve improved spectral efficiency by up to 40 percent over conventional decoding techniques
- TI's new C66x DSP combines fixed and floating point on the same core, delivering floating-point performance at fixed-point speeds for the first time
- Only solution to feature coprocessors for every standard, including WCDMA chip rate – no FPGA/ASIC required
- Network coprocessor and Multicore Navigator combine to provide Layer 2 and transport acceleration for all wireless base station standards
- Based on TI's new KeyStone architecture, enabling scalability and portability from macro to small cells reducing product development expense
- Multicore Navigator brings single core simplicity to multicore SoCs
- Best power/performance ratio, coupled with unique power-saving hibernation modes, delivers the lowest power for base stations
- Leverages high-performance 40-nm process technology



▲ TCI6618 block diagram

to 4G with this flexibility, and it allows them to develop a wider portfolio of solutions at a lower cost and in a shorter time than with competing solutions.

TCI6618 high-performance solution for 4G base stations

Designed specifically for 4G wireless infrastructure baseband applications, the TCI6618 is an ideal solution for heterogeneous network base stations. The TCI6618's coprocessor performs 95 percent of the LTE Layer 1 processing and substantially increases system capacity and performance with the lowest latency. The TCI6618 also enables SoC baseband solutions for GSM/EDGE, UMTS, TD-SCDMA, WiMAX, and LTE applications. To make the transition from C6000™ DSPs easier, the TCI6618 is backward code-compatible, allowing software reuse and maintaining value-added designs and IP. In addition, TI's TCI6618

leverages the KeyStone architecture for scalability to meet the need of all base stations, from single-sector small cells to multi-sector macro cells. With one software base driving a variety of base station products, developers will realize the highest R&D efficiency possible as well as optimized product costs

The TMS320TCI6618 is based on 40-nm process technology and delivers 4.8 GHz of raw DSP processing power, as well as performance of up to 153.6 16-bit GMACs per second, making it a cost-effective solution for high-performance DSP programming challenges. Due to its floating-point capability, the TCI6618 offers performance of up to 76.8 billion floating-point operations per second (GFLOPs), making it the industry's most powerful floating- and fixed-point SoC. Because the TCI6618 incorporates both fixed- and floating-point capabilities on the same core, it can perform up to five times faster than a

fixed-point implementation alone. In addition, the development and debugging cycle time for complex algorithms is significantly reduced from a multiple-month cycle to just a few days.

The TCI6618 integrates large on-chip memory organized as a two-level memory system that minimizes latency and increases system performance. The level-1 (L1) program and data memories on the TCI6618 device are 32 KB each per core. The level-2 (L2) memory is shared between program and data space for a total of 4,096 KB (1,024 KB per core). The TCI6618 contains 2,048 KB of multicore shared memory (MSM) that is used as a shared L2 SRAM or shared L3 SRAM. A dedicated Multicore Shared Memory Controller (MSMC) prevents memory contention between the cores and arbitrates access to the shared memory between the cores and other IP blocks.

The TCI6618 has a high-performance peripheral set with everything needed to develop robust base stations of varying coverage and capacity, including:

- I²C, SPI, and UART
- PCI Express port with two lanes supporting GEN1 and GEN2
- Sixteen 64-bit general-purpose timers (also configurable as thirty-two 32-bit timers)
- 16-pin general-purpose input/output (GPIO) port with programmable interrupt/event generation mode
- Multicore Navigator for hardware-accelerated dispatch
- Four lanes of serial RapidIO® (SRIO), compliant with RapidIO 2.1 spec for up to 5-Gbps operation per lane
- 64-bit DDR3 SDRAM interface
- 16-bit external memory interface (EMIF) for connecting to flash memory (NAND and NOR) and asynchronous SRAM
- Second-generation SERDES-based antenna interface (AIF2) capable of up to 6.25 Gbps operation per link with six high-speed serial links, compliant to OBSAI RP3 and CPRI standards

For efficient communications between the device and the network (as well as other devices), the TCI6618 includes a network coprocessor that consists of:

- Two 10/100/1000 Ethernet media access controllers (EMACs), which provide an efficient interface between the TCI6618 DSP core processor and the core network

- Management data input/output (MDIO) module (also part of the EMAC) that continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system
- Packet coprocessor that provides L2 to L4 classification functionalities and the processing power of up to 1.5 Gbps
- Security accelerator block capable of wire-speed processing on 1-Gbps Ethernet traffic on IPSec, SRTP, and 3GPP air interface security protocols
- Embedded Ethernet switch that allows multiple devices to be connected through SGMII, eliminating the need for a board level Ethernet switch

The TCI6618 has twelve high-performance embedded coprocessors to perform intensive signal processing functions common to wireless base station applications. The result is increased overall system performance, yielding 40 percent spectral efficiency over conventional decoding techniques.

Bit rate coprocessor for increased spectral efficiency

The bit rate coprocessor (BCP) is a multi-standard acceleration engine that offloads all bit rate processing in the wireless signal chain. The BCP contains the modulator, demodulator, interleaver/de-interleaver, turbo and convolution encoding, rate matcher/rate de-matcher, correlator for block code decoding, and CRC engine. The BCP enables turbo interference cancellation for MIMO equalization and enables high-performance PUCCH format 2 decoding. It offloads approximately 15 GHz of CPU MIPS with a maximum LTE downlink throughput of 2.2 Gbps and uplink throughput of 1.1 Gbps. For WCDMA, the maximum downlink throughput is 800 Mbps and uplink throughput is 400 Mbps. These techniques, coupled with the powerful MIMO processing capabilities of TI's new DSP C66x cores, yield an SoC that delivers on the promise of 4G for operators and users alike.

Faster coprocessors for optimized base station designs

Since 2001, TI has delivered radio coprocessing functions that consist of configurable IP blocks to offload processing demands as well as increase overall system performance. TI's coprocessors also reduce base station power requirements and dissipation as well as board complexity, making new products easier to design, build, and debug.

Coprocessor	Total performance (@1.2-GHz core frequency)
FFT/DFT	1,908 MSPS @ 256-FFT 1,683 MSPS @ 192-DFT
Turbo decode	LTE – 582 Mbps @ 6144 block size, 6 iterations WCDMA – 371 Mbps @ 5114 block size
Turbo encode	LTE – 2572 Mbps @ 6144 block size WCDMA – 2556 Mbps @ 5114 block size, 6 iterations
Viterbi decoder	>38 Mbps (K = 9) Mbps = 9)
Rake Search Accelerator	32-bit multiplication per cycle
WCDMA despreading	256 AMR users supported @ eight fingers
WCDMA spreading	256 users supported with two radio links and diversity
Encryption/decryption IPSec	2.8 Gbps
BCP	LTE – DL 2.2Gbps, UL 1.1Gbps WCDMA – DL: 800 Mbps, UL 400 Mbps

▲ TCI6618's coprocessors

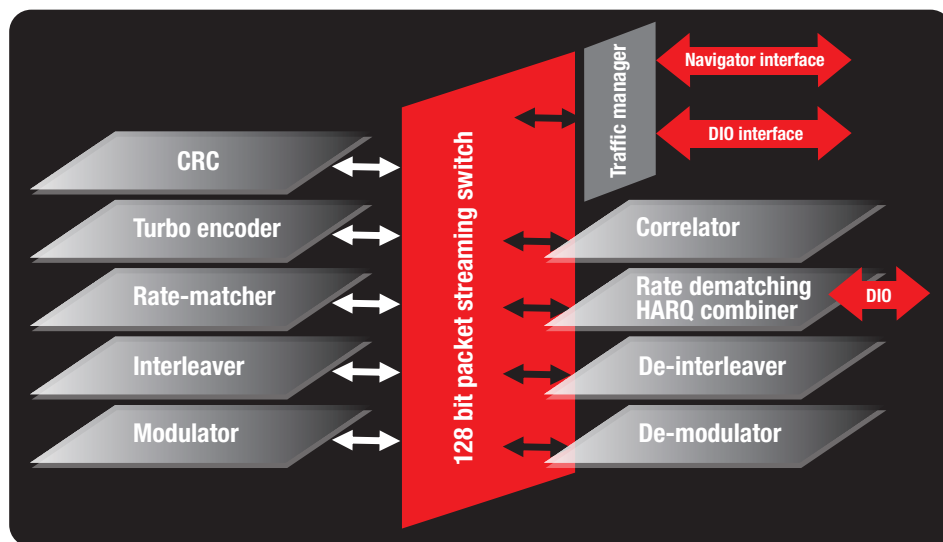
As wireless radio standards evolve and related implementations become standardized, each evolution of TI's wireless SoC devices has included more and more radio acceleration/coprocessing, and as such provides a compelling roadmap to lower power and costs while delivering higher performing base station solutions for our customers. TI's SoC strategy of integrating DSP cores with coprocessors is the simplest and most economical approach to wireless base station solutions and continues to be the market-leading solution today. TI's coprocessors eliminate external FPGAs and ASICs that were previously needed to deliver the performance needed for base stations, lowering the system cost and design complexity.

The TCI6618 has multiple, dedicated high-performance embedded coprocessors to perform intensive signal processing functions common to wireless base station applications. The coprocessors are four enhanced Viterbi

decoder coprocessors (VCP2_A, VCP2_B, VCP2_C, and VCP2_D), three third-generation turbo decoder coprocessors (TCP3d_A, TCP3d_B, and TCP3d_C), turbo encoder coprocessor (TCP3e), three fast Fourier transform coprocessors (FFTC_A, FFTC_B, and FFTC_C) and a bit rate coprocessor. Together, they significantly accelerate channel encoding/decoding operations. Also included in the TCI6618 are four tightly coupled rake/search accelerators (RSAs) for code division multiple access (CDMA) assistance with chip-rate processing.

Delivering full multicore entitlement

TI's TCI6618 is based on the KeyStone multicore SoC architecture, the first of its kind to provide full multicore entitlement. This provides non-blocking access to all processing cores, peripherals, coprocessors, and I/



▲ BCP architecture

Os. Innovations that unleash full multicore entitlement are: Multicore Navigator, TeraNet, Multicore Shared Memory Controller (MSMC), and HyperLink.

Multicore Navigator – TI's Multicore Navigator is an innovative packet-based manager that controls 8,192 queues and abstracts the connections between the various subsystems on the TCI6618. With a unified interface for communication, data transfer, and job management, Multicore Navigator enables higher system performance with fewer interrupts and reduced software complexity with a “fire and forget” paradigm.

Multicore Navigator instructs the next free DSP core to read the job and process it. Multicore Navigator simplifies the software architecture and improves performance of base stations with:

- Dynamic resource/load sharing
- Offloading CPU overhead/delay related to inter-subsystem communications
- Hardware-based task prioritization
- Dynamic load balancing
- Common communication methodology for all IP blocks (software, I/O, and accelerators)

TeraNet – TeraNet provides a hierarchical switch fabric that combines to deliver more than two terabits of bandwidth for data transfer within the SoC. This virtually guarantees that the cores or coprocessors are never starved for data and can deliver the entitled processing horsepower. Because the switch fabric is hierarchical instead of flat crossbar, overall power consumption is much lower in idle states and also delivers systems with minimal latency, which is a key requirement in next-generation base stations.

Multicore Shared Memory Controller (MSMC) – TI's TCI6618 includes a unique memory architecture for enhanced performance. TI's Multicore Shared Memory Controller (MSMC) allows the cores to directly access shared memory without having to use any TeraNet bandwidth. The MSMC arbitrates access to shared memory between the cores

and other IP blocks, eliminating memory contention. Shared memory access for code is nearly identical in latency to local L2 access, with highly effective prefetch mechanisms for code and data.

TI's TCI6618's DDR3 external memory interface (EMIF) is a 1,600-MHz, 64-bit bus with 8 GB of addressable memory space. Tied directly to the MSMC, the DDR3 EMIF reduces latency associated with external memory fetches and provides the speed increase and support needed for larger applications that operate on large amounts of data, which is essential for advanced 3G and 4G base stations.

HyperLink – HyperLink, with four lanes at up to 12.5 Gbps/lane, is a proprietary high-speed interconnect that allows low protocol and high-speed communication and connectivity to other KeyStone devices providing OEMs a seamless path to scalable solutions. The HyperLink on the TCI6618 works in conjunction with the Multicore Navigator to dispatch tasks to multiple devices transparently, so they execute as if they are running on local resources.

TCI6618 as Layer 2 and transport processing engine

TCI6618 combines the unmatched PHY processing capabilities with dedicated coprocessors for the Layer 2 and transport layer processing. This enables designers to create base stations without a separate network processor, thereby reducing board complexity and cost without compromising performance.

The network coprocessor enables fast-path processing in the transport network layer and deep into the Layer 2 of the radio network. Within the network coprocessor inside the TCI6618, the Packet Accelerator and the Security Accelerator perform fully-accelerated autonomous packet-to-packet processing. They leverage the Multicore Navigator, which uses a zero-copy approach to optimize data processing at all layers. Classification and ordering, multicore-accessible storage, memory

management, segmentations and reassembly, and delivery across multiple cores and devices are all supported by Multicore Navigator. Layer 2 data-plane and transport-plane overhead can be reduced by 10-15 times due to the fast-path and zero-copy processing enabled by the Multicore Navigator.

Lowest power consumption for performance

TI has a history of providing the lowest power wireless base station SoCs on the market. TI is able to achieve its ultimate low power through the combination of its process technology, SmartReflex™ technology, and the proactive use of power management techniques (such as adaptive voltage scaling) in every wireless base station semiconductor device to keep active power at a minimum. TI's latest technology in the TCI6618 has brought the SoC power consumption for macro and compact base stations down to the industry's lowest levels at 0.075 mW/GMAC of power.

Complete tools and support

TI provides a full suite of best-in-class Eclipse-based development and debugging tools with the TCI6618; these include a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows debugger interface for visibility into source-code execution. TI's compiler generates highly efficient code that is “first-pass efficient” so there is less need to optimize it. TI's debugging tools help developers visualize problems and resolve them quickly, so designers can get products to the field faster while saving development resources. In addition, TI will offer a TCI6618 evaluation module (EVM) to help customers prototype quickly with the TCI6618.

For more information

To learn more about the TCI6618 SoC visit www.ti.com/tci6618. Discover how the TCI6618 can add performance to your next wireless base station design.

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