

设计指南: TIDA-010058

待机功耗低于 50mW 的 5V/2A、12V/2.5A 双路输出反激式器件参考设计



说明

此参考设计是一个在 UCC28742 上进行次级侧调整的双路输出反激式转换器。5V 电压轨的精度调整范围为 $\pm 1\%$ ，12V 电压轨在 25% 至 100% 负载条件下的交叉调整范围为 -8% 至 +14%。本设计使用单层 PCB 实现成本优化。在 115V/50Hz 条件下可实现 82.82% 的峰值效率，在 230V/50Hz 条件下可实现 83.19% 的峰值效率。在 115V/50Hz 条件下可实现 31.6mW 的待机功耗，在 230V/50Hz 条件下可实现 54.2mW 的待机功耗。

资源

[TIDA-010058](#)

设计文件夹

[UCC28742](#)

产品文件夹

[TL431](#)

产品文件夹



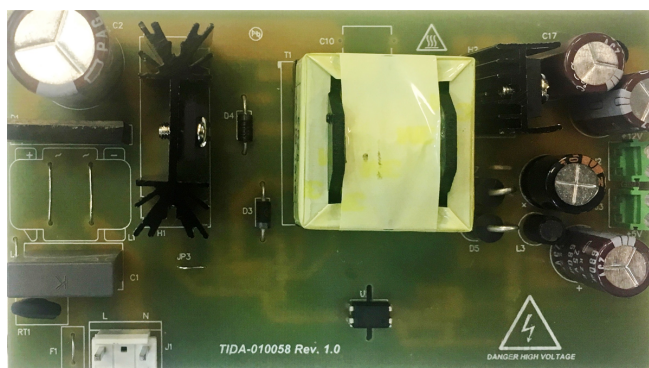
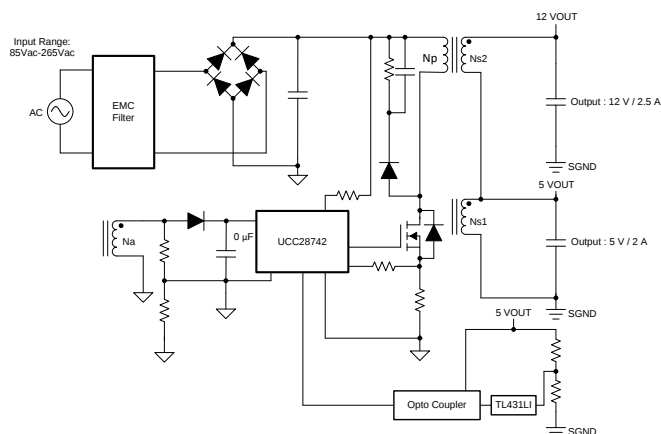
咨询我们的 E2E™ 专家

特性

- 低于 50mA 的待机功耗，适用于 50W 电源应用
- 光耦合器反馈，可提供快速瞬态响应和严格的电压调节
- 采用谷底开关的 DCM 运行模式，可提高效率并降低 EMI
- 超低启动电流和较大 VDD 迟滞，可实现低偏置电容
- 故障保护，包括输入低线路、输出过压、过流和短路保护

应用

- 炉灶面
- 洗衣机和烘干机
- 家用空调
- 咖啡机
- 空气净化器和加湿器



该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

Standby power is electricity used by appliances and equipment while switched off or not performing primary functions. Standby power is also used by circuits that are continually energized even when the device is turned off.

Under the Energy-Using Product (EuP) directive, the commission sets maximum limits for passive standby and off-mode power. The objective of the eco-design requirements for standby and off mode is to ensure the lowest possible energy use for household appliances and electronic products. The main requirement is that standby power of an appliance system without a display must not consume more than 0.5 W, and the standby power of an appliance system with an information display must not consume more than 1 W. The EU directive is expected to change from 500-mW to 300-mW standby power following the release of this design, making it difficult for new functions, such as Wi-Fi®, large displays, and drive power requirements for the active state up, to achieve the new standby power target. A solution is a lower bias power supply for cost-effective total system standby power consumption with no cost increase to the bill of materials (BOM).

1.1 Key System Specifications

表 1. TIDA-010058 Electrical Performance Specifications

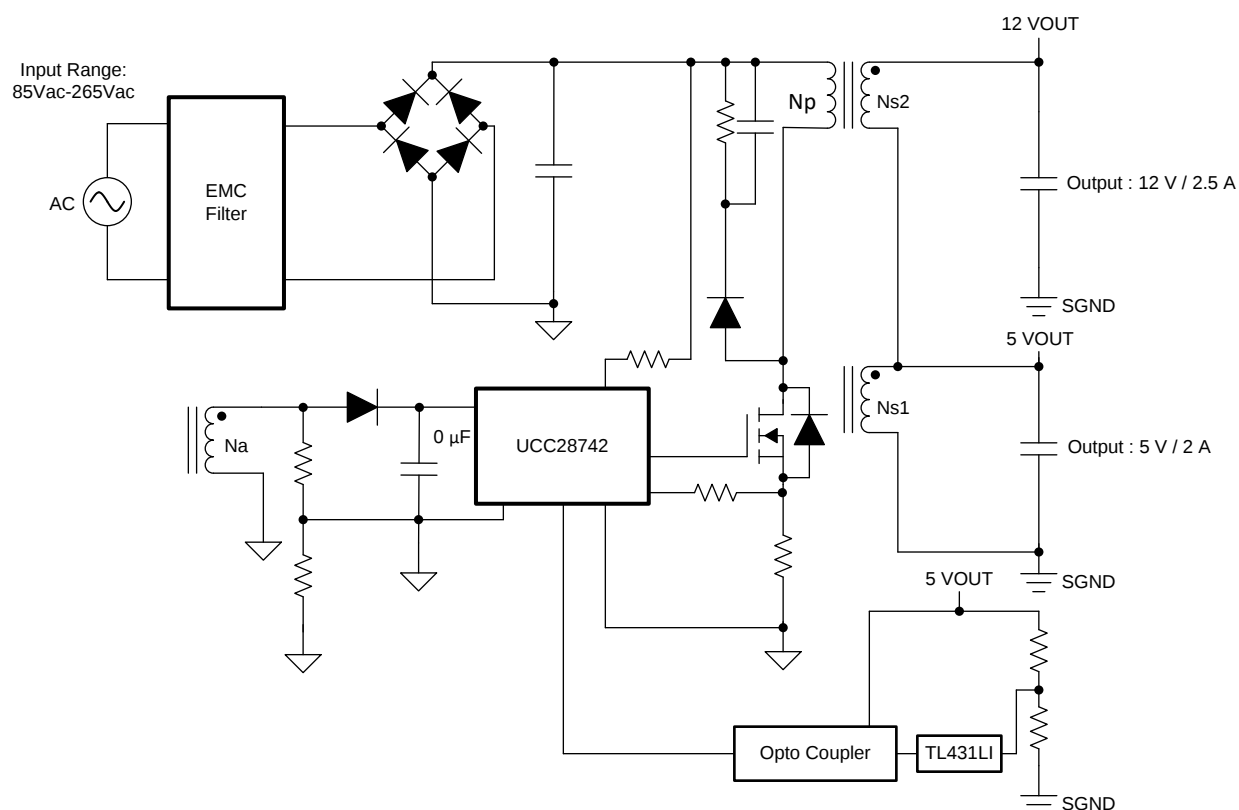
PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNIT
INPUT CHARACTERISTICS					
V_{IN}	AC-line input voltage	85	220	265	VRMS
f_{LINE}	Line frequency	47	50	63	Hz
P_{STBY}	No-load input power	$V_{IN}=typ, I_O=0A$		50	mW
OUTPUT CHARACTERISTICS					
V_{O1}	DC output voltage 1	$V_{IN} = typ, I_O = 0 \text{ to } I_{OR}$	5		V
$V_{RIPPLE1}$	Output voltage ripple 1	$V_{IN} = typ, I_O = I_{OR}$		50	mV
I_{OR1}	Output rated current 1	$V_{IN} = \text{min to max}$	2		A
V_{O2}	DC output voltage 2	$V_{IN} = typ, I_O = 0 \text{ to } I_{OR}$	12		V
$V_{RIPPLE2}$	Output voltage ripple 2	$V_{IN} = typ, I_O = I_{OR}$		100	mV
I_{OR2}	Output rated current 2	$V_{IN} = \text{min to max}$	2.5		A
η	Average efficiency	$V_{IN}=typ$, average of 25%, 50%,75%, and 100% Load		83.5	%
SYSTEMS CHARACTERISTICS					
f_{SW}	Switching frequency			100	kHz

2 System Overview

2.1 Block Diagram

图 1 shows the high-level block diagram of the circuit. The main parts of this reference design are the isolated flyback power supply controller (UCC28742) and the adjustable precision shunt regulator with optimized reference current (TL431LI).

图 1. TIDA-010058 Block Diagram



2.2 Design Considerations

Most industrial applications require a bias power supply and have at least dual power rails for the entire system: 3.3 V or 5 V for the system controller and 12 V or 15 V for the power module. This reference design provides dual isolated outputs of 5 V with 2 A and 12 V with 2.5 A that cover most industrial applications. This design also achieves very low power consumption in standby mode. The design is suited for use in isolated offline systems requiring low standby power, high efficiency, and low BOM cost.

2.3 Highlighted Products

This reference design features the following devices, which are selected based on their specifications and cost consideration. For more information on each of these devices, see their respective product folders at TI.com or click on the links for the product folders under Resources.

2.3.1 UCC28742

The UCC28742 is a flyback power-supply controller which provides high-performance voltage regulation using an optically coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous-conduction mode (DCM) with valley-switching to minimize switching losses and allow for the use of low cost output rectifiers. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which allows the power-supply designer to achieve low standby power dissipation. During low-power operating conditions, the power-management features of the controller reduce the device operating current at switching frequencies below 25 kHz. At and above this frequency, the UCC28742 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component-count solution is realized using a straight-forward design process.

2.3.2 TL431LI

This standard device has proven ubiquity and versatility across a wide range of applications, ranging from power to signal path. This is due to its key components containing an accurate voltage reference and op amp, which are very fundamental analog building blocks. TL43xLI is used in conjunction with its key components to behave as a single voltage reference, error amplifier, voltage clamp or comparator with integrated reference. TL43xLI can be operated and adjusted to cathode voltages from 2.495V to 36V, making this part optimum for a wide range of end equipments in industrial, auto, telecom and computing. In order for this device to behave as a shunt regulator or error amplifier, $>1\text{mA}$ ($I_{\text{min(max)}}$) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage. Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5%, and 1%. These reference options are denoted by B (0.5%) and A (1.0%) after the TL431LI or TL432LI. TL431LI and TL432LI are both functionally the same, but have separate pinout options. The TL43xLIXC devices are characterized for operation from 0°C to 70°C, the TL43xLIXI devices are characterized for operation from -40°C to 85°C, and the TL43xLIXQ devices are characterized for operation from -40°C to 125°C.

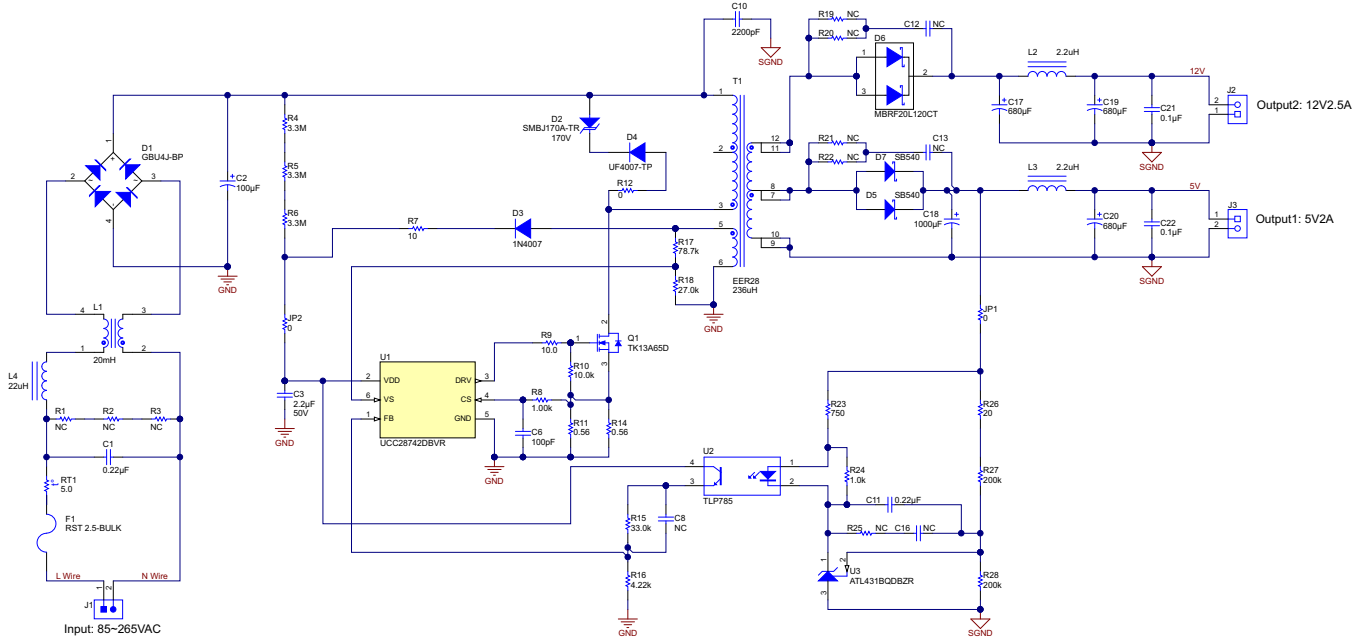
2.4 System Design Theory

During voltage regulation (CV mode), the UCC28742 operates in frequency modulation mode and peak current amplitude modulation mode.

The UCC28742 internally limits its operating frequency between $f_{\text{SW(min)}}$ and $f_{\text{SW(max)}}$, typically between 200 Hz and 105 kHz. The choice of transformer primary inductance and primary-peak current sets the maximum operating frequency of the converter, which must be equal to or lower than $f_{\text{SW(max)}}$. Conversely, the choice of maximum target operating frequency and primary-peak current determines the transformer primary-inductance value. The actual minimum switching frequency for any particular converter depends on several factors, including minimum loading level, leakage inductance losses, switch-node capacitance losses, other switching and conduction losses, and bias-supply requirements.

图 2 shows the typical application circuit for the UCC28742, in which the key components that must be calculated are current sense resistor R_{CS} (R11 and R14), VDD capacitance C_{DD} (C3), VDD start-up resistance R_{STR} (R4, R5 and R6), VS resistor divider (R17 and R18), and the transformer.

图 2. Typical Application Circuit for the UCC28742



2.4.1 Current Sense Resistor

The current sense pin is connected through a series resistor to the current-sense resistor (R_{CS}). The controller varies the internal current sense threshold between 190 mV and 770 mV. The values of R_{CS} can be determined by 公式 1. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer core and copper losses, bias power, and primary leakage inductance losses.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (1)$$

Where,

- V_{CCR} is a current regulation constant with a typical value of 363 mV
- N_{PS} is the transformer primary-to-secondary turns ratio
- I_{OCC} is the target output current in constant-current limit
- η_{XFMR} is the transformer efficiency

2.4.2 VDD Capacitance, C_{DD}

The capacitance on VDD must supply the device operating current until the output of the converter reaches the target minimum operating voltage. At this time, the auxiliary winding can sustain the voltage to the UCC28742. The total output current available to the load and to charge the output capacitors is the constant current regulation target. 公式 2 assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved to maintain VDD above its $V_{VDD(on)}$. The gate drive current depends on a particular MOSFET to be used. With an estimated average of 1.0 mA of gate-drive current, C_{DD} is determined using 公式 2.

$$C_{DD} = \frac{(I_{RUN} + 1\text{mA}) \times \frac{C_{OUT} \times V_{OCV}}{I_{OCC}}}{(V_{DD(on).min} - V_{DD(off).max})} \quad (2)$$

2.4.3 VDD Start-Up Resistance R_{STR}

Once the VDD capacitance is known, the start-up resistance from V_{BULK} to achieve the power-on delay time (t_{STR}) target can be determined using 公式 3.

$$R_{STR} = \frac{\sqrt{2} \times V_{IN(min)}}{I_{START} + \frac{V_{DD(on)} \times C_{DD}}{t_{STR}}} \quad (3)$$

2.4.4 VS Resistor Divider

The VS divider resistors determine the output voltage regulation point of the flyback converter. The high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on the transformer auxiliary to primary turns-ratio and the desired input voltage operating threshold. R_{S1} can be calculated using 公式 4.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (4)$$

$I_{VSL(run)}$ is VS pin run current with a typical value of 210 μA for a design. The low-side VS pin resistor is selected based on desired output over voltage V_{OV} and can be calculated using 公式 5.

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} + V_F) - V_{OVP}} \quad (5)$$

2.4.5 Transformer Turns Ratio N_{PS} , Inductance L_P , Primary-Peak Current $I_{PP(MAX)}$

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM resonant time.

Determine the maximum available total duty cycle of the on time and secondary conduction time based on the target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if an estimate is not available from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is $\frac{1}{2}$ of the DCM resonant period, or 1 μs assuming 500-kHz resonant frequency. D_{MAX} can be determined using 公式 6.

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{MAX} \right) - D_{MAGCC} \quad (6)$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined using 公式 7. D_{MAGCC} is defined as the secondary diode conduction duty cycle when load current reaches a specified limit operation. It is set internally by the UCC28742 at 0.475. The total voltage on the secondary winding needs to be determined, which is the sum of V_{OCV} , and the secondary rectifier, V_F . N_{PS} can be determined using 公式 7.

$$N_{PS} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F)} \quad (7)$$

N_{PS} is determined also with other design factors such as voltage and current ratings of the primary MOSFET, secondary rectifier diode, as well as the secondary MOSFET if the synchronous rectifier is used. Once an optimum turns ratio is determined from a detailed transformer design, use this ratio for the other parameters.

The primary transformer inductance and primary-peak current, $I_{PP(MAX)}$, can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, and output and transformer efficiency are included in 公式 8 and 公式 9.

The transformer primary current should be determined. Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \quad (8)$$

$$L_P = \frac{2 \times (V_{OCV} + V_F) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \quad (9)$$

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Test Equipment Needed

- Chroma AC source MODEL 61603
- Chroma DC E-load MODEL 6314A
- Single-phase power meter WT210
- Tektronix DPO 3054
- Multimeter (current): Fluke 287C
- Multimeter (voltage): Fluke 287C
- Electrical thermography: Fluke TiS55
- EMI test receiver: KH3939

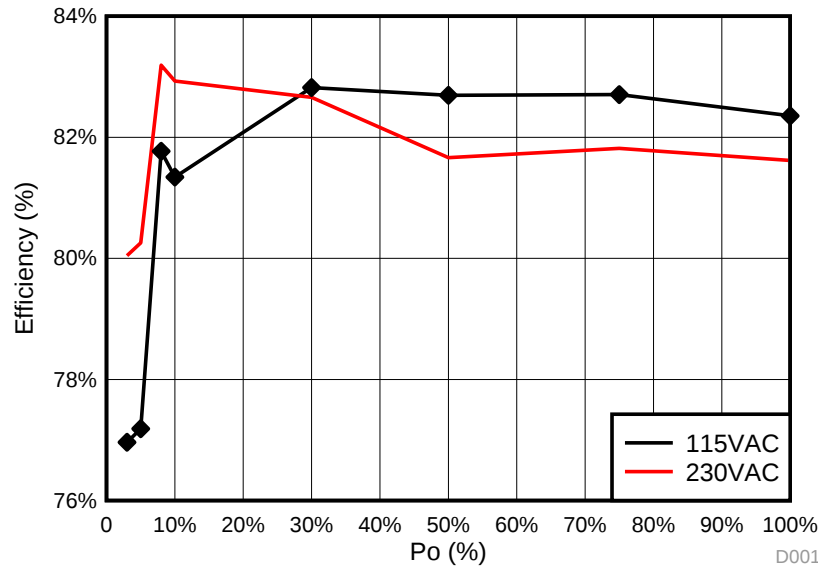
3.1.2 Test Setup

- Connect the line of the AC source on the design input (pin 1 of connector J1), and connect the neutral of the AC source on the TIDA-010058 input (pin 2 of connector J1) through the current sensing module of the power meter.
- Connect the voltage sensing module to the design input (connector J1).
- Connect an electronic load to the 12-V output terminal (connector J2) with the load set to draw 30 W through the multimeter.
- Connect another electronic load to the 5-V output terminal (connector J3) with the load set to draw 10 W.
- Turn on the AC source connected to the design input with a universal input voltage (85-V to 264-V AC).
- Once the design activates, monitor the input power consumption and dual output performance.
- Turn off the AC source and disconnect the AC source from the board when the test is complete.

3.2 Testing and Results

3.2.1 Efficiency With Load Variation

图 3. Efficiency With Load Variation



3.2.1.1 115-V AC/50-Hz Efficiency Measurement

表 2. 115-V AC/50-Hz Efficiency Measurement

Vin (Vac)	LOAD (%)	PIN (W)	Vout1 (V)	Iout1 (A)	Vout2 (V)	Iout2 (A)	Pout (V)	η (%)
115 V	3%	1.61	4.99	0.05	12.37	0.08	1.24	76.96%
	5%	2.74	4.99	0.1	12.43	0.13	2.11	77.19%
	8%	4.10	4.99	0.15	12.4	0.21	3.35	81.77%
	10%	5.20	4.99	0.2	12.43	0.26	4.23	81.34%
	30%	15.00	4.99	0.57	12.44	0.77	12.42	82.82%
	50%	24.60	4.98	0.92	12.41	1.27	20.34	82.69%
	75%	36.30	4.98	1.33	12.38	1.89	30.02	82.70%
	100%	47.60	4.97	1.7	12.35	2.49	39.20	82.35%

3.2.1.2 230-V AC/50-Hz Efficiency Measurement

表 3. 230-V AC/50-Hz Efficiency Measurement

Vin (Vac)	LOAD (%)	PIN (W)	Vout1 (V)	Iout1 (A)	Vout2 (V)	Iout2 (A)	Pout (V)	η (%)
230 V	3%	1.55	4.99	0.05	12.39	0.08	1.24	80.05%
	5%	2.64	4.99	0.1	12.46	0.13	2.12	80.26%
	8%	4.04	4.99	0.15	12.44	0.21	3.36	83.19%
	10%	5.11	4.99	0.2	12.46	0.26	4.24	82.93%
	30%	15.02	4.99	0.57	12.43	0.77	12.42	82.66%
	50%	24.91	4.98	0.92	12.41	1.27	20.34	81.66%
	75%	36.67	4.98	1.33	12.37	1.89	30.00	81.82%
	100%	48.00	4.97	1.7	12.34	2.49	39.18	81.62%

3.2.2 Cross Regulation

3.2.2.1 Cross Regulation Under 115-V AC/50 Hz

表 4. Vin = 115 V, Vout1

LOAD 2 / LOAD 1	3%	5%	8%	10%	30%	50%	75%	100%
1%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
3%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
5%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
8%	4.99	0.99	4.99	4.99	4.99	4.99	4.99	4.99
10%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
30%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
50%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
75%	4.99	5	4.99	4.99	4.99	4.99	4.99	4.99
100%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99

表 5. Vin = 115 V, Vout2

LOAD 2 / LOAD 1	3%	5%	8%	10%	30%	50%	75%	100%
1%	13.08	13.85	14.48	15.03	-	-	-	-
3%	12.39	12.74	13.06	13.35	15.21	-	-	-
5%	12.16	12.46	12.69	12.89	14.28	15.32	-	-
8%	11.9	12.26	12.44	12.58	13.61	14.38	-	-
10%	11.75	12.15	12.34	12.46	13.35	14.01	14.71	-
30%	-	11.29	11.63	11.83	12.49	12.8	13.14	13.43
50%	-	10.67	11.11	11.3	12.19	12.46	12.68	12.88
75%	-	10.07	10.58	10.9	11.91	12.21	12.41	12.55
100%	-	-	-	-	-	12.04	12.24	12.37

3.2.2.2 Cross Regulation Under 230-V AC/50 Hz

表 6. Vin = 230 V, Vout1

LOAD 2 / LOAD 1	3%	5%	8%	10%	30%	50%	75%	100%
1%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
3%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
5%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
8%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
10%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
30%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
50%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99
75%	4.99	5	4.99	4.99	4.99	4.99	4.99	4.99
100%	4.99	4.99	4.99	4.99	4.99	4.99	4.99	4.99

表 7. Vin = 230 V, Vout2

LOAD 2 / LOAD 1	3%	5%	8%	10%	30%	50%	75%	100%
1%	13.08	13.87	14.54	15.1	-	-	-	-
3%	12.39	12.78	13.1	13.38	15.26	-	-	-
5%	12.15	12.48	12.7	12.9	14.26	-	-	-
8%	11.87	12.26	12.45	12.6	13.59	14.38	-	-
10%	11.71	12.14	12.35	12.48	13.34	14.02	14.72	-
30%	-	11.34	11.68	11.87	12.49	12.8	13.14	13.44
50%	-	-	11.17	11.43	12.19	12.45	12.69	12.9
75%	-	-	-	10.98	11.92	12.21	12.41	12.57
100%	-	-	-	-	11.7	12.03	12.24	12.38

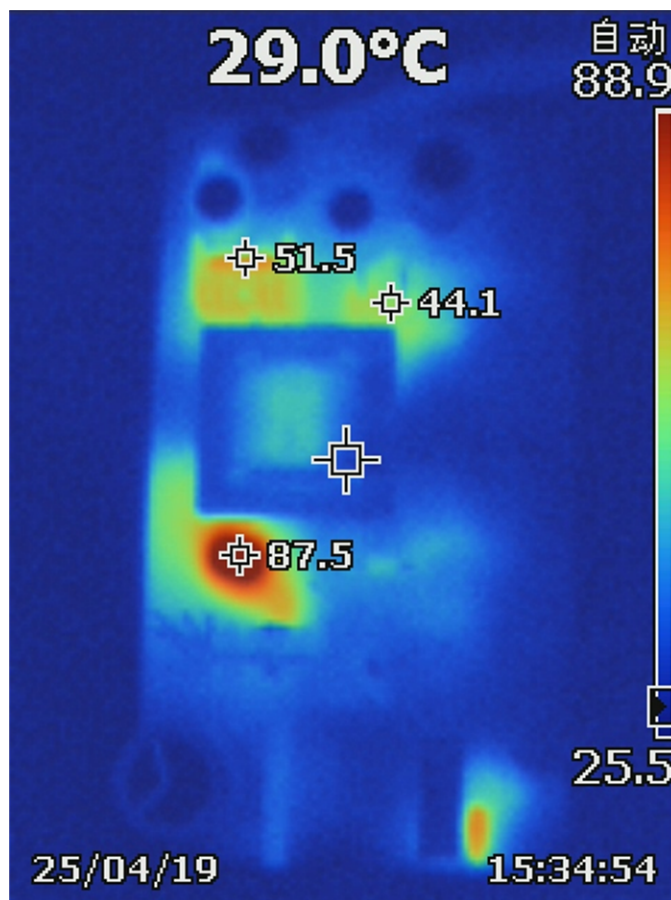
3.2.3 No-Load Power Consumption

表 8. No-Load Power Consumption

Vin (V)	85	115	130	150	180	200	230	265
Pin (mW)	27	36.7	43.12	35.02	40.47	39.33	48.2	59.1

3.2.4 Thermal Test

图 4. Thermal Test Under 230-V AC and Full Load



The thermal test shows a top view of the board because all of the power components are on the top layer. The output load is 5 V-2 A and 12 V-2.5 A and runs for 30 minutes. The ambient temperature was 22.5°C, open frame.

3.3 Waveforms on Key Components

3.3.1 V_{DS} Waveform of Primary MOSFET

图 5 shows the test under 85-V AC input and full load.

图 5. V_{DS} Under 85-V AC Input and Full Load

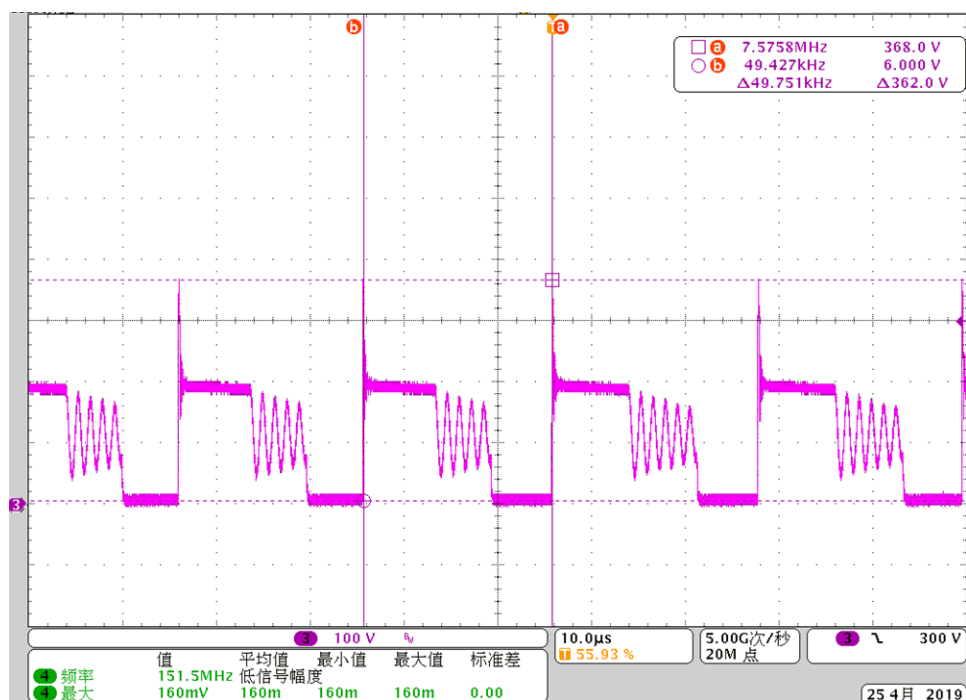


图 6 shows the test under 115-V AC input and full load.

图 6. V_{DS} Under 115-V AC Input and Full Load

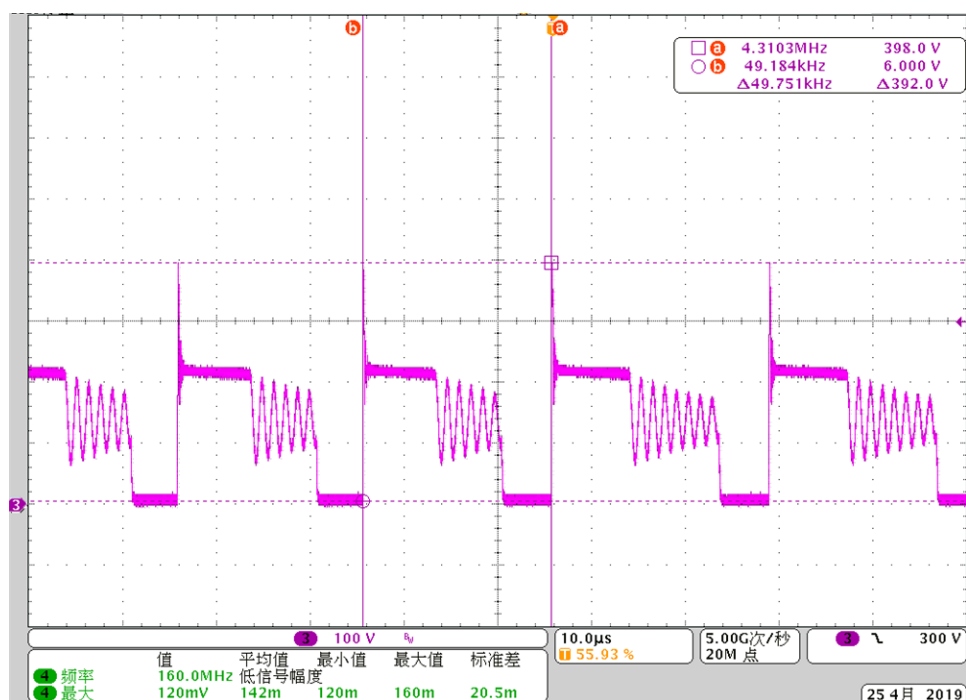


图 7 shows the test under 230-V AC input and full load.

图 7. V_{DS} Under 230-V AC Input and Full Load

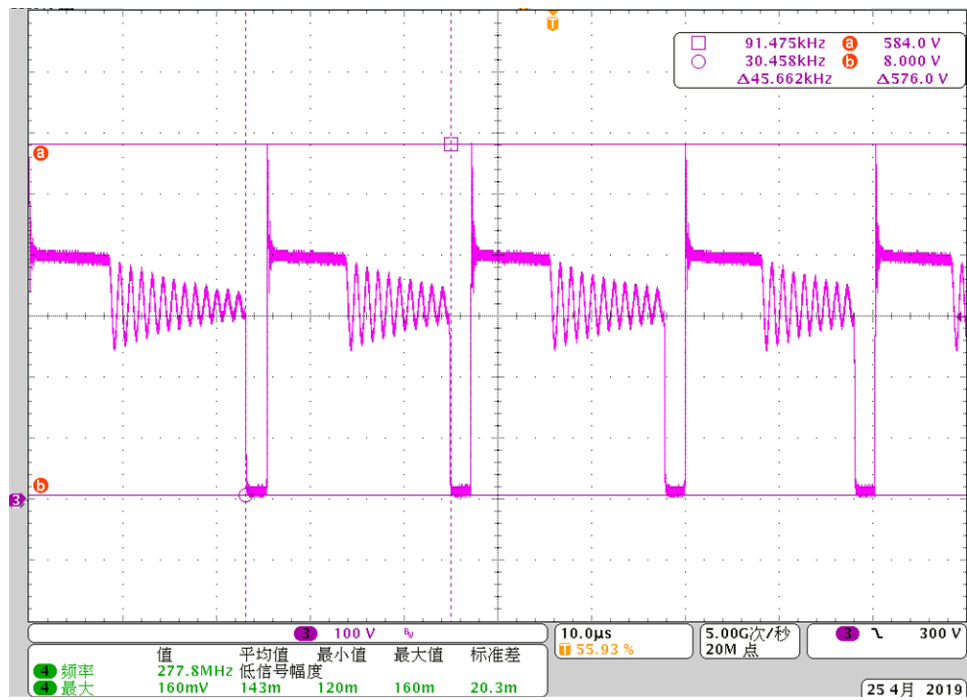
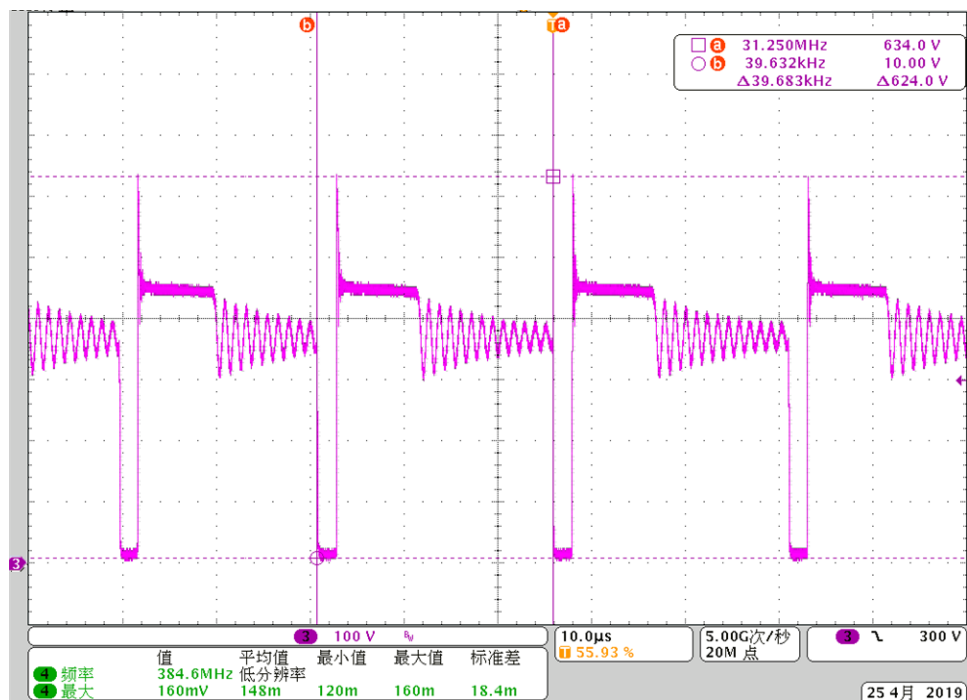


图 8 shows the test under 265-V AC input and full load.

图 8. V_{DS} Under 265-V AC Input and Full Load



3.3.2 Secondary Rectifier Diode Stress V_{DD}

图 9 shows the test under 265-V AC input and full load.

图 9. V_{DD} of 5 V Under 265-V AC Input and Full Load

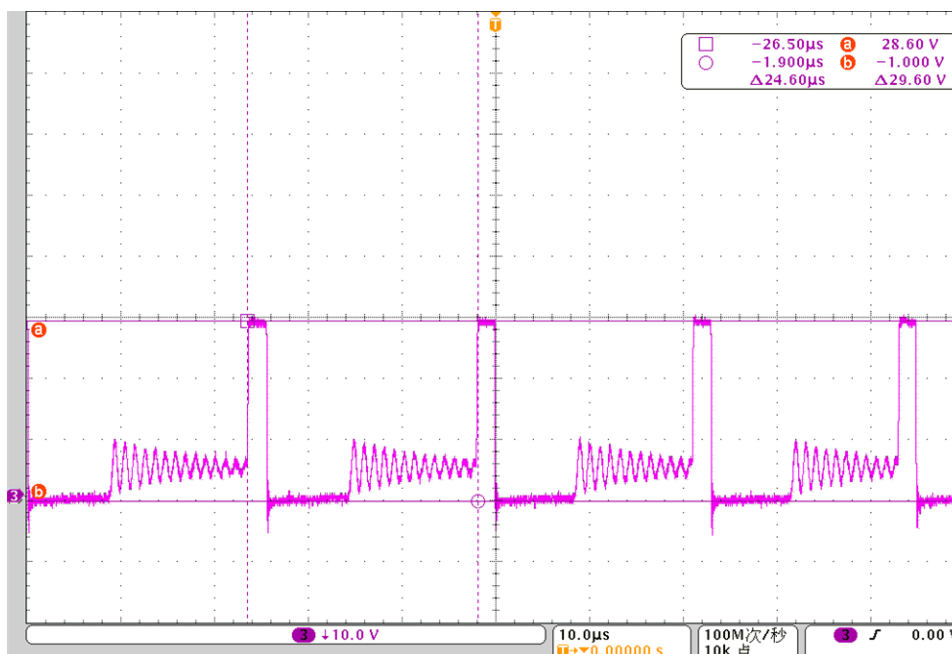
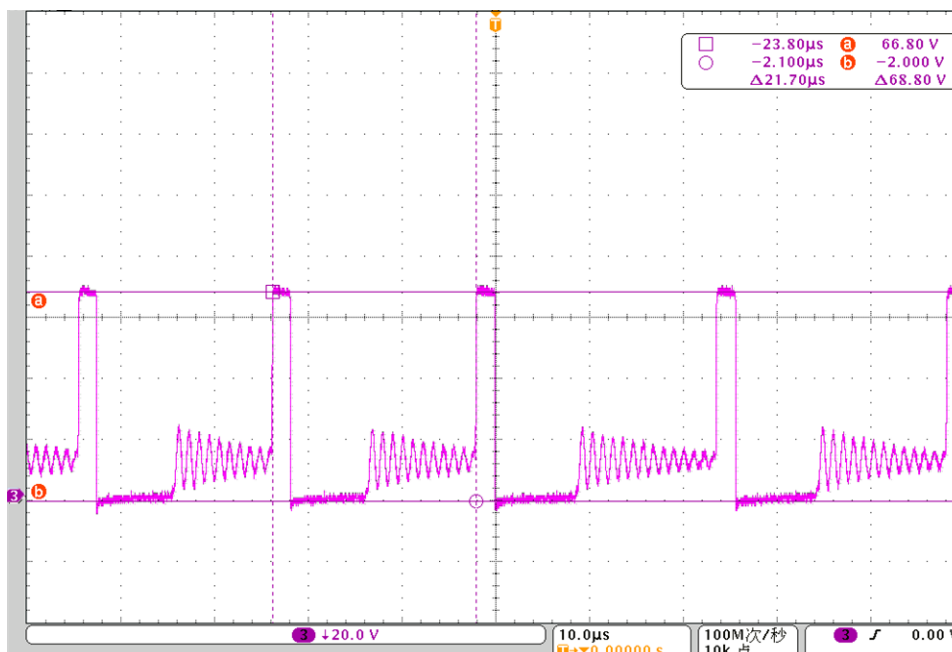


图 10. V_{DD} of 12 V Under 265-V AC Input and Full Load



3.3.3 Output Voltage Ripple

图 11. Output Voltage Ripple Under 85-V AC Input and Full Load

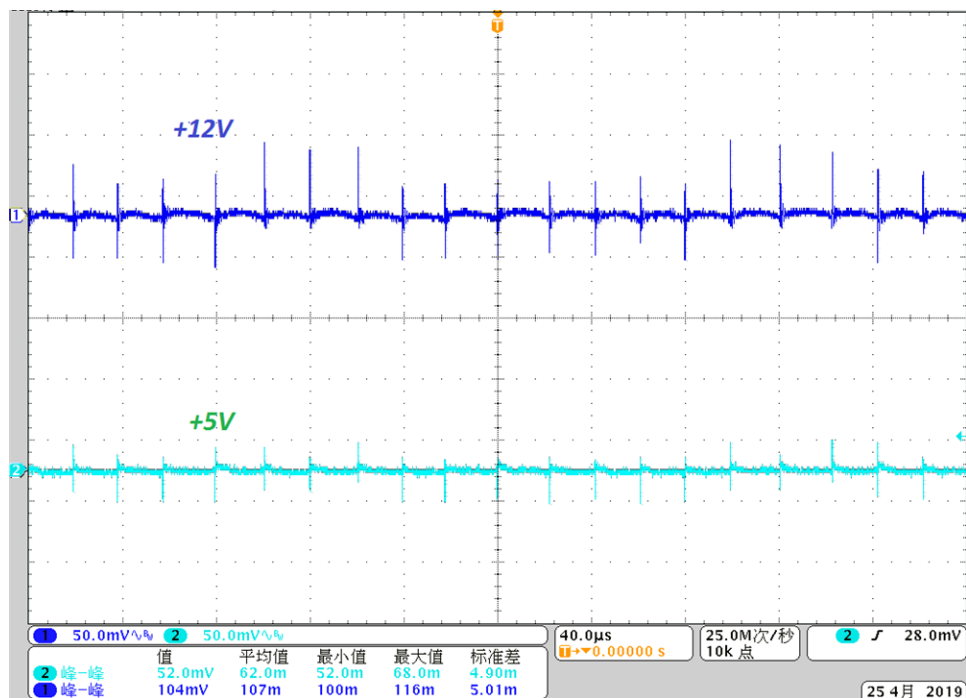


图 12. Output Voltage Ripple Under 115-V AC Input and Full Load

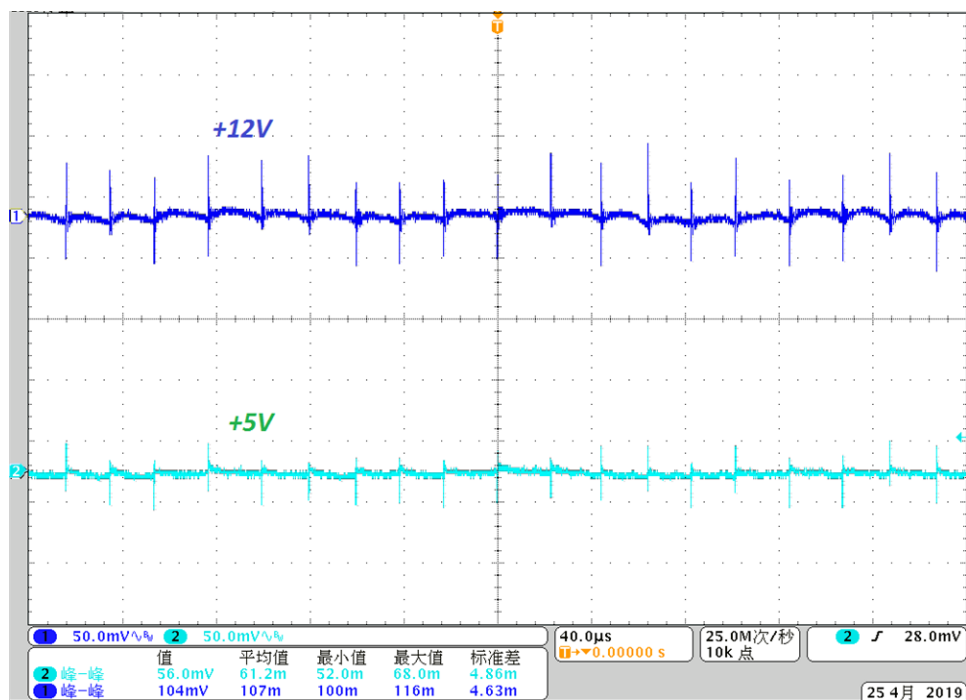


图 13. Output Voltage Ripple Under 230-V AC Input and Full Load

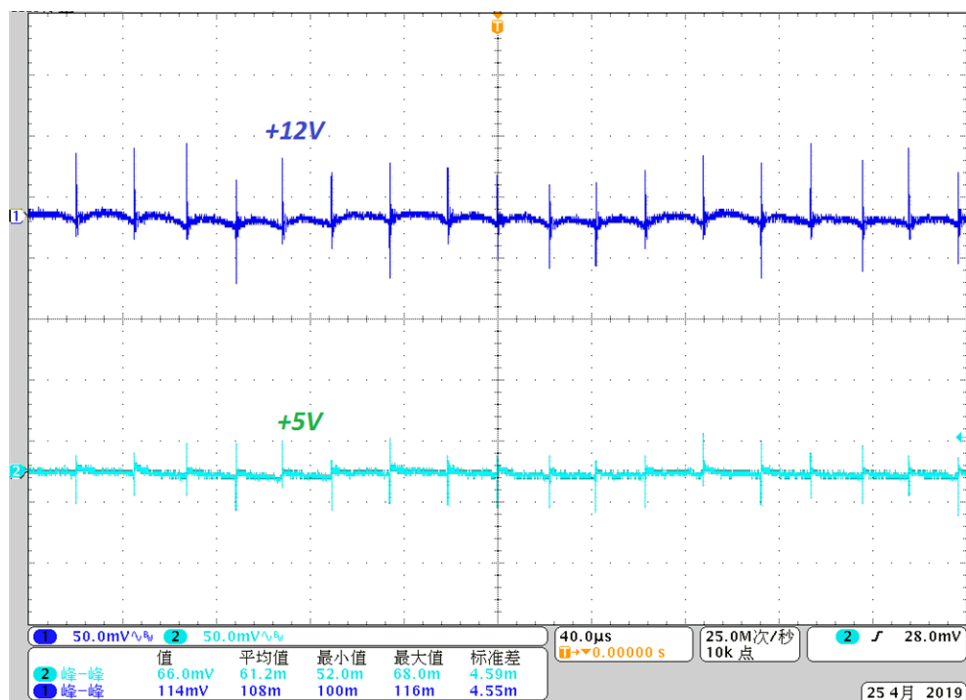
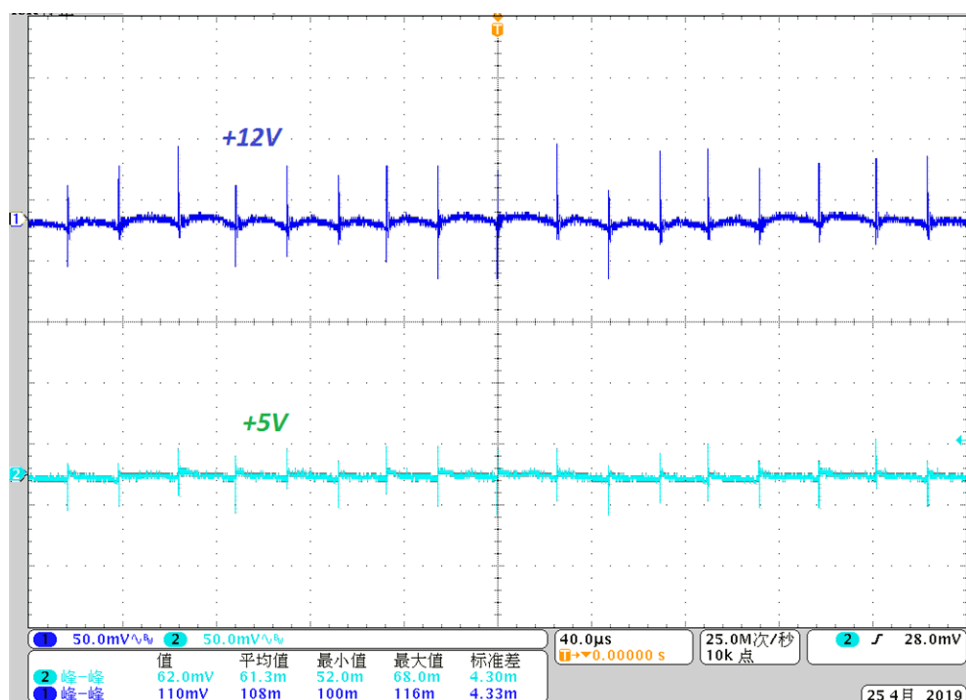


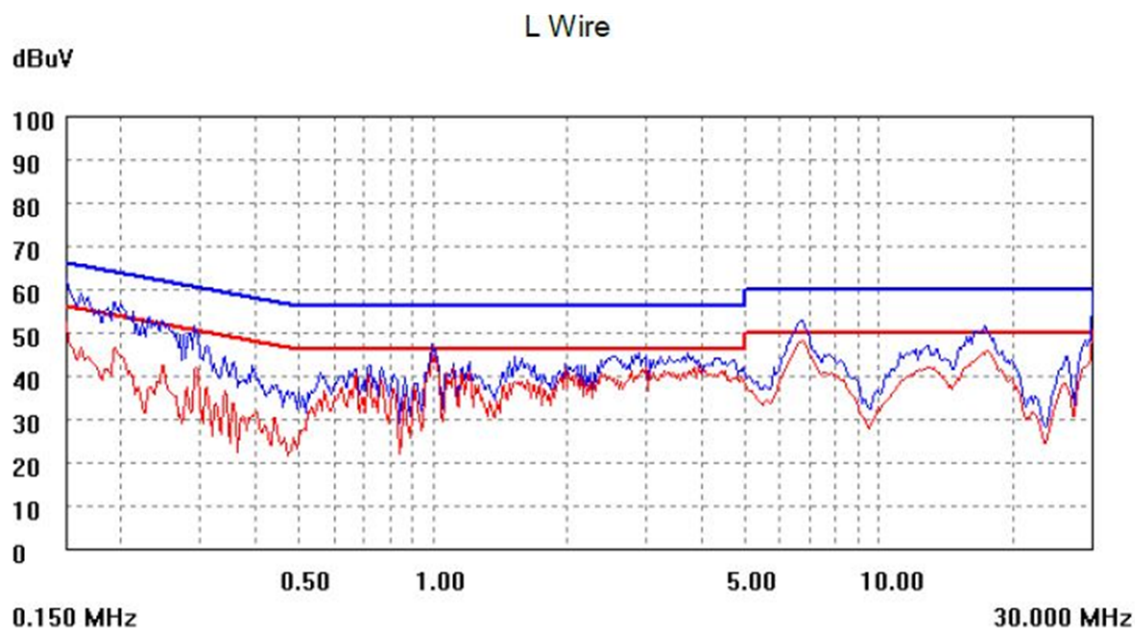
图 14. Output Voltage Ripple Under 265-V AC Input and Full Load



3.3.4 Conducted Emission (EN55022 Class B)

图 15 shows the test under 230-V AC/50 Hz and full load.

图 15. Conducted Emission Test Under 230-V AC/50-Hz Input and Full Load



4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-010058](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-010058](#).

4.3 PCB Layout Recommendations

To increase the reliability and feasibility of the project, use the following guidelines:

- Minimize stray capacitance on the VS node.
- Place the voltage sense resistors R17 and R18 close to the VS pin.
- Connect the high-voltage input to a non-switching source of high voltage — not to the MOSFET drain — to avoid injecting high-frequency capacitive current pulses into the device.
- Connect the main power loop ground and the UCC28742 ground through a single point connection at the C2 ground pin.
- Arrange the components to minimize the loop areas of the switching currents as much as possible.

4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-010058](#).

4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-010058](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-010058](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-010058](#).

5 Related Documentation

1. Texas Instruments, [UCC28742 High-Efficiency Flyback Controller With Optocoupler Feedback Data Sheet](#)

5.1 商标

E2E is a trademark of Texas Instruments.

Altium Designer is a registered trademark of Altium LLC or its affiliated companies.

Wi-Fi is a registered trademark of Wi-Fi Alliance.

All other trademarks are the property of their respective owners.

6 About the Author

YUAN (JASON) TAO is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Yuan brings to this role his extensive experience in power electronics, high-frequency DC/DC, AC/DC converters, and analog circuit design. Yuan earned his master of IC design and manufacture from Shanghai Jiao Tong University in 2007.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司