TI Designs：TIDA-010005
软件可配置的心脏起搏器检测模块参考设计

说明

此参考设计采用了一款基于硬件、结构紧凑的电路，用于检测 ECG 测量期间出现的起搏器脉冲。它通过标志和板载 LED 指示有效起搏信号。借助此设计，用户可以通过板载 DAC 用软件来配置起搏信号（振幅、上升时间、脉冲持续时间、极性）的各种参数。可通过板载 ADC 读取测量值。从电路板上的噪声 ECG 信号中提取*起搏*信号，并进行放大与调节。与 TI 的 ADS129X 系列器件配合使用时，增加了*起搏*检测功能。

资源

TIDA-010005	设计文件夹
INA317	产品文件夹
TLV9062	产品文件夹
DAC5578	产品文件夹
ADS7142	产品文件夹
TLV1702	产品文件夹
SN74LV4040A	产品文件夹
SN74AUP3G14	产品文件夹

TI E2E™ Community

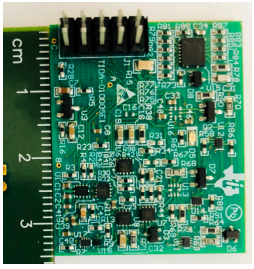
咨询我们的 E2E™ 专家

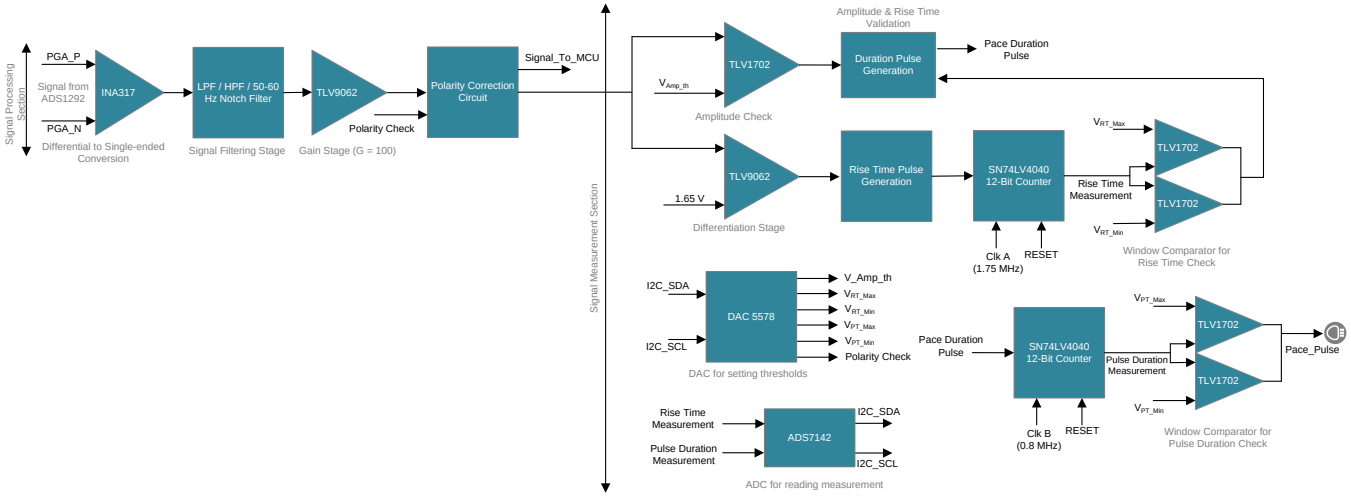
特性

- 针对以下检测的可编程阈值：起搏脉冲的上升时间、振幅、持续时间和极性。
  - 上升时间（30µs 至 200µs）
  - 振幅（8mV 至 700mV）
  - 持续时间（100µs 至 2000µs）
- 提供测量参数和 I^2C 总线上经过调节的起搏信号，以便进行进一步分析和处理
- 可连接 TI 的 ADS129X ECG 前端器件系列
- 可识别各种类型的起搏器信号
- 通过软件命令实现极性更正
- 紧凑的尺寸（29mm × 35mm）

应用

- 多参数患者监视器
- 无线患者监控仪
- 心电图 (ECG)





1 System Description

The TI Design TIDA-010005 implements a modular, standalone monitoring system which detects the presence of a *Pace* signal originated from a pacemaker implanted in humans to improve heart functionality. This characteristic signal is present in the ECG waveform of the patient which comes from the ECG front end. The pace signal has certain characteristics from which it can be distinguished from the other signals. This TI design implements a hardware-based approach to look for these special characteristics in the signal and detects the presence of the pace signal. The attributes of the pace signal are its amplitude, rise time (T_R), and the pulse duration (T_D) for which the pulse lasted. This is described in detail in 图 3. The system is designed to be configurable means that the thresholds for pace attributes can be programmed through the onboard DAC which enables the system to look for different types of the *Pace* pulses. The filtering in the system provides a fine signal for the processing. This design also detects the negative pace pulses as well. This negative pace signal detection can be enabled by the software command which programs the DAC. The real-time monitoring of the ECG is done and the measured attributes can be taken back to the external MCU for diagnostic purposes.

The design acts as a support to the ADS129X family of TI's patient monitoring devices and provides an additional feature of pace detection making a complete patient monitoring solution.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS	DETAILS
Input Voltage	3.3 V	Supply voltage to the system
PGAP	Analog non-inverting ECG input to system	Analog output of ADS129X PGA non-inverting pin which serves as input to the TIDA-010005
PGAN	Analog inverting ECG input to system	Analog output of ADS129X PGA inverting pin which serves as input to the TIDA-010005
Rise-time (T_R) measurement range	30–200 µs	The measurement range of the rise time of the pace pulse
Pace pulse duration (T_D) measurement range	0.1–2 ms	The measurement range of the duration of the pace pulse
Input *Pace* signal amplitude range	8 mV – 700 mV	The range of amplitude of the pace signal tested with the TIDA-010005
Average steady-state current consumption	8 mA	Current consumption of the system
Clock A frequency	1.75 MHz	Onboard clock to the counter for T_R measurement
Clock B frequency	806 kHz	Onboard clock to the counter for T_D measurement
ADC resolution	12 bits (2 channel)	ADS7142 ADC to capture the rise time and duration
DAC resolution and channels	8 bits (8 channel)	DAC5578 sets the various threshold for pace pulse. I^2C enabled

2 System Overview

The pacemaker is an electronic device that is implanted surgically inside the body, typically just under the collarbone. The pacemaker is used to treat the heart arrhythmias - broadly tachycardia and bradycardia. which are abnormal beating of the heart instead of normal sinus rhythm. It sends out electrical impulses to stimulate the heart muscles and regulate its contractions to produce a heartbeat. 图 1 shows the image of a typical pacemaker. It is a small electrically charged device and it typically contains two parts, one is the *Pulse Generator*, which is comprised of the battery and other electrical circuits to generate electrical pulses while the other part is the leads or electrodes which connects the pacemaker to the right ventricle in the heart. The pacemaker generates electric impulses which travel from the top to the bottom of the heart which controls muscle contractions. It can also store the heart beats so a diagnostician can better understand the activity inside the heart.

图 **1. Electronic Heart Pacemaker**

图 2 illustrates the pacemaker inserted inside the human body. As 图 2 shows, it is a fairly complex device which performs all these functions inside the body and aids the heart to beat in a regular fashion.

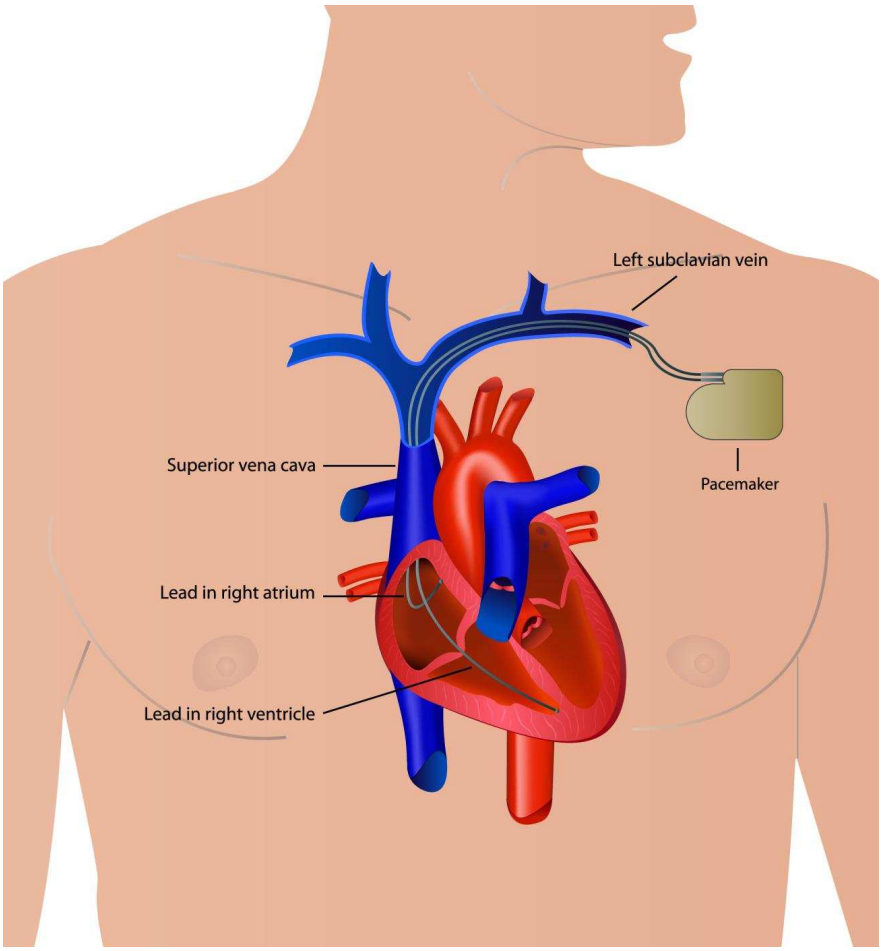


图 2. Illustration of Pacemaker Inserted Inside Human Body

When a heart patient undergos ECG testing or any medical diagnosis, it is important that the cardiologist can detect the presence of a pacemaker. The electrical signature of the pace signal looks like a small narrow pulse which, when added to the noise and the signal of the heart, becomes very difficult to identify. The pace pulse is a very fast signal (order of kHz) as compared to the normal ECG signal which is typically very slow (a few Hz) and hence it is difficult to see in the normal ECG trace. The TIDA-010005 solves this issue of identification by looking for the pace artifacts present in the mixed signal and generates a binary signal whenever it encounters a valid pace pulse which can be used to mark a stamp on the ECG signal indicating the presence of the pacemaker inside the body.

The major difficulty in identifying the pace artifact comes due to the small amplitude, narrow-width, and varying slope of the pulse accompanied with the background electrical noise. Moreover, due to the huge advancement in pacing therapy, there are dozens of different modes of pace signals available; for example, single-chamber pacing, three-chamber pacing, and so forth. This means that there are a variety of pacemakers with different types available in the market. Also there are various medical standards which require certain conditions for the pacemaker detection and are required to display the pacing artifacts.

The polarity of the signal can also vary depending upon the location of the electrodes in the heart. 图 3 shows the illustration of a typical ideal pace artifact. The pacing artifacts generally have a fast rising edge of the pacemaker signal. The heart generates the pulse with a rise time of the order of 100 ns but due to the inductance and the capacitance of the human body and the pacing leads or electrodes, the rise time at the external electrodes becomes slower and is in of the order of 10 µs - 100 µs. We denote this duration as rise time (T_R). The pulse then reaches its maximum amplitude followed by a capacitive droop as 图 3 shows, and the time for which the signal stays before falling down steeply is the duration of the pace artifact which is denoted as *Pulse Duration* (T_D). The signal then falls back and goes slightly negative (reverses polarity) to produce a *Recharge Pulse* which make sure that the heart tissue is left with a net zero charge. The TIDA-010005 is designed to measure the *Rise Time* (T_R) of the artifact in the range 30 µs to 200 µs and *Pulse Duration* (T_D) in the range 0.1 ms to 2 ms. The minimum amplitude which can be measured is 8 mV (see 节 2.3.7.1 for more details on the amplitude settings). The design returns a flag PACE_DETECT that indicates a presence of pace pulse along with the measured values of T_R and T_D which can be read over from the TI's ADC ADS7142 over I^2C.

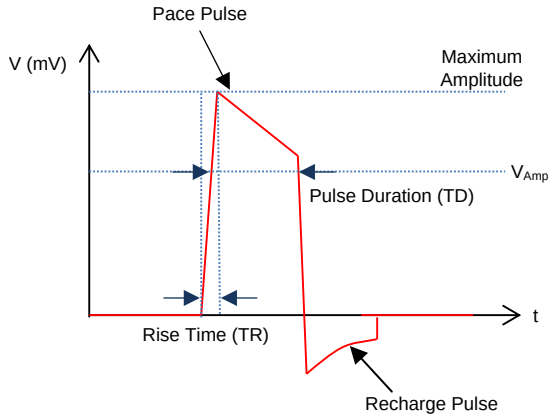


图 3. Illustration of Ideal Pace Artifact

2.1 Block Diagram

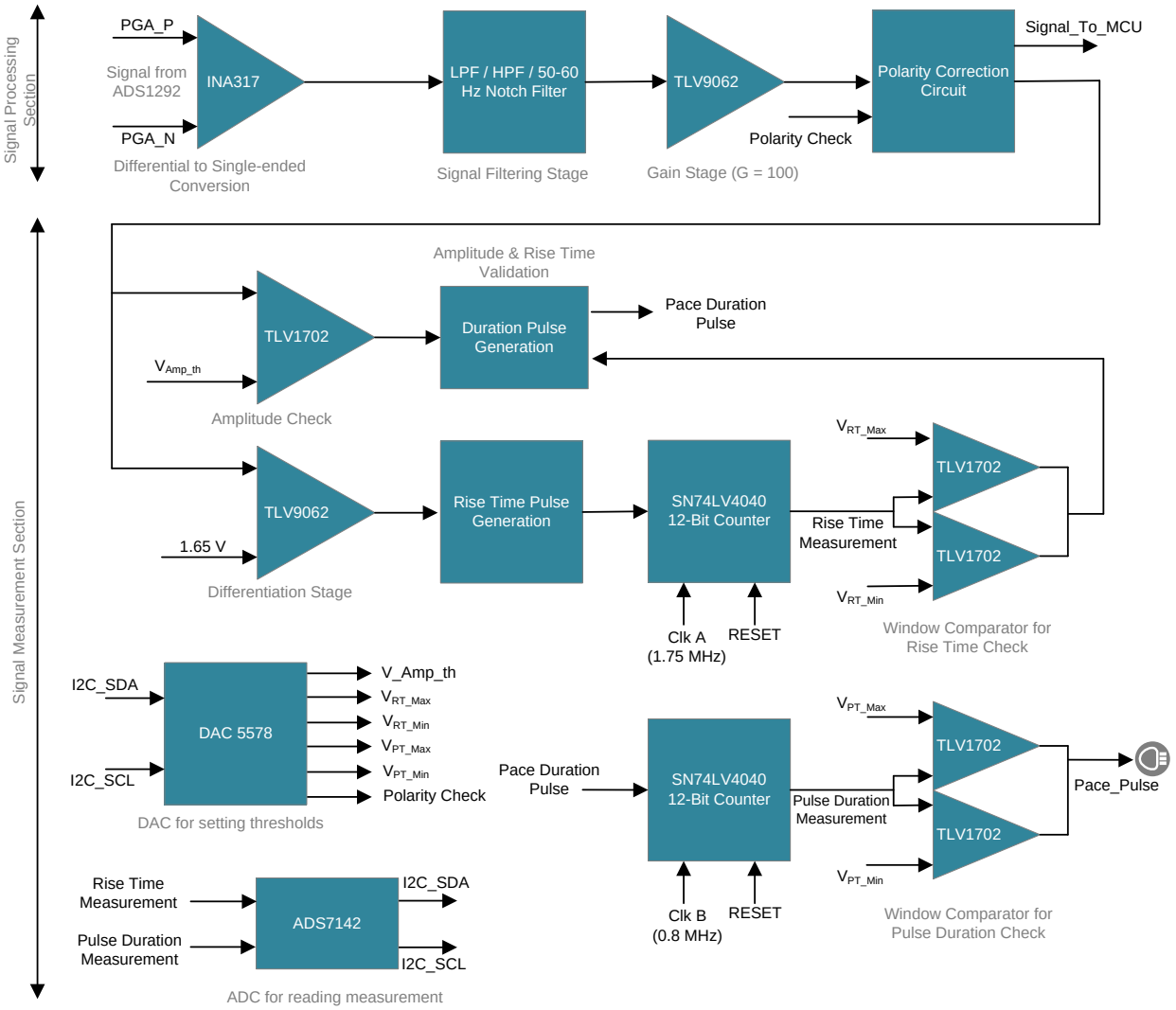


图 4. TIDA-010005 System-Level Block Diagram

The design implements a fully-configurable solution to detect the presence different types of pacemaker pulse. 图 4 shows the system-level block diagram of the TIDA-010005 design. The entire implementation is divided into two sections – *Signal Processing* and *Signal Measurement*. The system takes its input, a differential signal from the ECG front-end ADS129X channel, PGAP and PGAN which goes to the signal processing section. The differential signal from the ADS129X device is converted into a single-ended output through a precision instrumentation amplifier (INA317) and is passed through the filtering stage. A second-order filter is implemented using one op amp which can be configured either in low-pass configuration or a 50- or 60-Hz notch filter based on the application and quality of the signal received after the single-ended conversion.

The signal is then amplified in the *Gain Stage* and then it is processed in the *Polarity Correction Stage*. The polarity correction stage is like a full-wave rectifier which allows the positive-going signal to pass through exactly the same but inverts the negative-going signals to positive ones which is activated by the signal *Polarity Check* which comes from the DAC. The main advantage of this circuit is that it provides the system the capability to detect even the negative-going pace pulse. The signal obtained till this point is sent back to the MCU for diagnostics. The processed signal is now ready to be sent to the signal measurement section which analyzes the characteristics of the signal and detects the pace pulse.

The *Signal Measurement Section* tracks the signal characteristics – amplitude, rise time, and duration and based on the user's supplied thresholds, classifies the signal as a valid pace pulse or not. The circuit implemented does two things in parallel, looks at the amplitude and measures the rise time. For the rise-time calculations, the signal is differentiated and a TTL pulse corresponding to the rise time is generated by the *Rise Time Pulse Generator*. This pulse is then fed to an asynchronous binary counter with a high-frequency Clock A, and ANDed together with the signal so that the counter counts only till the signal is high. The final count on the counter is then converted into an equivalent analog voltage which is further sent to the window comparator to determine whether it lies between the set thresholds for rise time. V_{RT_Max} and V_{RT_Min} are the thresholds for the rise time which is programmed by the user using the onboard DAC5578 through the I^2C interface. DAC programming details are described in 节 2.3.9. 图 5 demonstrates the conceptual waveforms to get the rise time. The detailed explanation of the principle involved is discussed in 节 2.3.7. The *Rise Time Measure* is the equivalent analog voltage corresponding to the final count. The threshold for the amplitude V_{Amp_Th} also comes from the DAC. If and only if, both the amplitude and the rise time criteria is satisfied, the signal is allowed to pass further for pulse duration measurements, else it is blocked by the circuit. For the duration measurements, a similar circuitry is implemented. The pace duration pulse is generated after the earlier operations are sent to the counter for counting with another Clock B, which is slightly slower than Clock A since the range of measurements for the two times, rise time and pulse duration, are different.

The final count of the second counter is converted to equivalent analog voltage and is sent to the window comparator to check if it lies within the bounds specified by the user. V_{PT_Max} and V_{PT_Min} are similar thresholds for the pulse duration which is specified by the user through the DAC. 图 6 shows the conceptual waveforms for the measurement of the pulse duration. The detailed explanation of the principle involved is similar to the rise-time measurement and is discussed in 节 2.3.7. If all three conditions are satisfied, the signal is a valid pace pulse and a flag PACE_DETECT shows a low-to-high transition after the detection of the *valid* pace signal. The onboard ADC ADS7142 measures the values obtained for the rise and duration which can be read by the MCU through the I^2C interface.

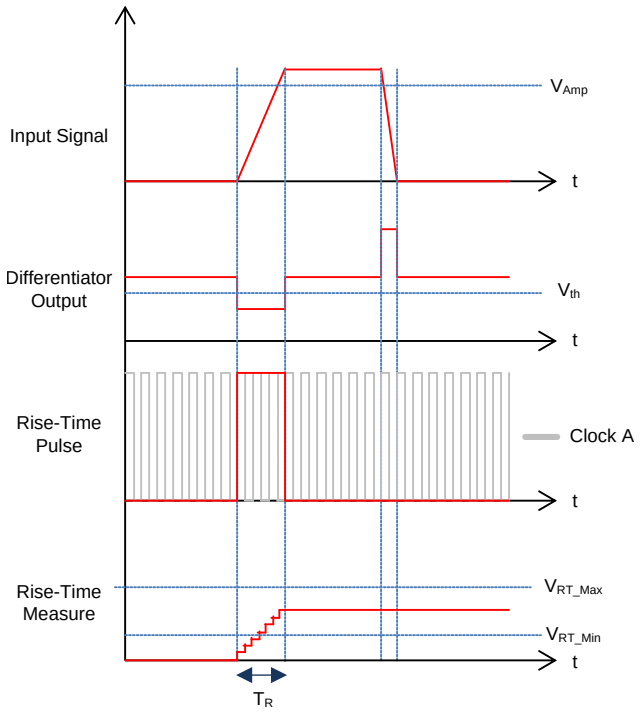


图 5. Rise Time Pulse Generation and Measurement

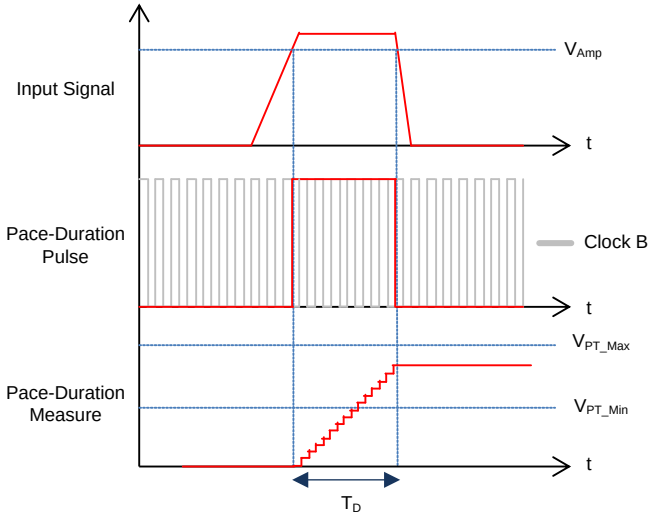


图 6. Pace Duration Pulse Generation and Measurement

2.2 Highlighted Products

2.2.1 INA317 Micro-Power (50 μA), Zero-Drift, Rail-to-Rail-Out Instrumentation Amplifier

The INA317 device is a low-power, precision instrumentation amplifier offering excellent accuracy. The versatile 3-operational amplifier design, small size, and low power make the INA317 usable in a wide range of portable applications. A single external resistor sets any gain from 1 to 1000, as defined by the industry-standard gain equation:

$$G = 1 + \left(\frac{100\ k\Omega}{R_G} \right)$$

where

- R_G is the external resistor, 100 kΩ is used in the design (1)

The instrumentation amplifier provides low offset voltage (75 µV, G ≥ 100), excellent offset voltage drift (0.3 µV/°C, G ≥ 100), and high common-mode rejection (100 dB at G ≥ 10). The INA317 operates with power supplies as low as 1.8 V (±0.9 V) and a quiescent current of 50 µA, making the device usable in battery-operated systems.

2.2.2 TLV9062 10-MHz, Low-Noise, CMOS Operational Amplifier for Cost-Sensitive Systems

The TLV9062 device is a low-voltage (1.8 V to 5.5 V) op amp with rail-to-rail input- and output-swing capability. The unity-gain bandwidth of TLV9062 is 10-MHz. These devices are highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the TLV906x is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. This op amp is designed specifically for low-voltage operation with high-performance specifications.

The TLV906xS devices include a shutdown mode that allow the amplifiers to switch off into standby mode with typical current consumption less than 1 µA. The TLV906xS family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter, and provides no phase reversal in overdrive condition.

2.2.3 TLV1702 Dual, 2.2-V to 36-V, Micro-Power Comparator

The TLV170x family of devices offers a wide supply range, rail-to-rail inputs, low quiescent current (50 µA per comparator), and low propagation delay (560 ns). All these features come in industry-standard, extremely-small packages, making these devices the best general-purpose comparators available. The open collector output offers the advantage of allowing the output to be pulled to any voltage rail up to +36 V above the negative power supply, regardless of the TLV170x supply voltage.

These devices are available in single (TLV1701), dual (TLV1702), and quad (TLV1704) channel versions. Low input offset voltage (300 µV), low input bias currents, low supply current, and open-collector configuration make the TLV170x family flexible enough to handle almost any application, from simple voltage detection to driving a single relay.

2.2.4 SN74LV4040A 12-Bit Asynchronous Binary Counter

The SN74LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits. These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

2.2.5 ADS7142 Nanopower, Dual-Channel, Programmable Sensor Monitor

The ADS7142 autonomously monitors signals while optimizing system power, reliability, and performance. It implements event-triggered interrupts per channel using a digital windowed comparator with programmable high and low thresholds, hysteresis, and event counter. The device includes a dual channel analog multiplexer in front of a successive approximation register analog-to-digital converter (SAR ADC) followed by an internal data buffer for converting and capturing data from sensors.

The ADS7142 consumes only 900 nW of power. The small form-factor and low power consumption make this device suitable for space-constrained, or battery-powered applications, or both. The features of the ADS7142 are efficient host sleep and wake up, false-trigger prevention, an I^2C interface for communication, and a wide operating range. The resolution of the device is 12-bit in normal mode and 16-bit in high-precision mode.

2.2.6 REF2930 3.0 V 100 ppm/Degrees C, 50 µA in SOT23-3 Series (Bandgap) Voltage Reference

The REF29xx is a precision, low-power, low-voltage dropout voltage reference family available in a tiny 3-pin SOT-23 package.

The small size and low power consumption (50-µA maximum) of the REF29xx make it ideal for portable and battery-powered applications. The REF29xx does not require a load capacitor, but it is stable with any capacitive load.

Unloaded, the REF29xx can be operated with supplies within 1 mV of output voltage. All models are specified for the wide temperature range, –40°C to 125°C.

2.2.7 DAC5578 8-Bit, Octal Channel, Ultra-Low Glitch, Voltage Output, 2-Wire Interface DAC

The DAC5578 (8 bit), DAC6578 (10 bit), and DAC7578 (12 bit) devices are low-power, voltage-output, octal-channel, digital-to-analog converters (DACs). The devices are monolithic, provide good linearity, and minimize undesired code-to-code transient voltages (glitch).

The devices use a versatile, 2-wire serial interface that is I^2C-compatible and operates at clock rates of up to 3.4 MHz. Multiple devices can share the same bus. The devices incorporate a power-on-reset (POR) circuit that ensures the DAC output powers up to zero-scale or midscale until a valid code is written to the device. These devices also contain a power-down feature, accessed through the serial interface, that reduces the current consumption of the devices to typically 0.42 µA at 5 V. Power consumption is typically 2.32 mW at 3 V, reducing to 0.68 µW in power-down mode. The low power consumption and small footprint make these devices ideal for portable, battery-operated equipment. For details of the DAC programming, see 节 2.3.9.

2.2.8 SN74AUP2G08 Low-Power Dual 2-Input Positive-AND Gate

The AUP family is TI's premier solution to the low-power needs of the industry in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity with very low undershoot and overshoot characteristics.

This dual 2-input positive-AND gate performs the Boolean function given by 公式 2 and 公式 3 in positive logic.

$$Y = A.B \quad (2)$$

$$Y = \overline{\overline{A} + \overline{B}} \quad (3)$$

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

2.2.9 SN74AUP3G14 Low Power Triple Schmitt-Trigger Inverter

The AUP family is TI's premier solution to the low-power needs of the industry in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity.

The SN74AUP3G14 contains three inverters and performs the Boolean function Y=Ã. The device functions as three independent inverters but, because of Schmitt action, it may have different input threshold levels for positive-going (VT+) and negative-going (VT–) signals. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

2.2.10 SN74LVC1G3157 1-Channel, 2:1 Analog Switch

This single-channel, single-pole, double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V VCC operation. The SN74LVC1G3157 device can handle both analog and digital signals. The SN74LVC1G3157 device permits signals with amplitudes of up to VCC (peak) to be transmitted in either direction. Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

2.3 System Design Theory

This section gives a detailed description of the architecture of the system. The intricate design details and the theory of operation of various circuit sections is discussed. Simulation results from TINA-TI™ are also provided to help understand the system better. The TIDA-010005 design is a configurable design not only in terms of software but also in terms of hardware. The subsequent subsections shed more light on this aspect. For example, the low-pass filter (LPF), or 50- or 60-Hz notch filter is optional in terms of need or application.

2.3.1 System Flow Diagram

图 7 shows the system flow diagram of the design. The input signal is a very small differential signal coming from the ADS129X family of medical analog front-ends from TI , which is then processed in the signal processing block. Signal processing essentially means the small signal is filtered to remove unwanted components and is amplified and polarity correction is done so that the subsequent parts of the system do not have to care about the polarity and cleanliness of the signal. In other words, the signal processing block essentially prepares the input incoming signal for the pace measurements.

The processed signal then goes to amplitude validation part where the amplitude of the signal is compared to a set threshold value. If the amplitude is greater than the set threshold V_{Amp_Th}, then it is passed further for more calculations; otherwise, the system waits for the next pulse. Simultaneously, the rise-time measurements are performed and the measured rise time is compared through a window comparator to two thresholds V_{RT_Min} and V_{RT_Max}. If the rise time lies between these values, then only the system enables the pace pulse duration measurement circuit, else it waits for the next pulse. Note that if and only if both the amplitude and rise-time criteria are satisfied, then only the duration measurement circuit activates.

Once the rise time and amplitude are done then the system measures the duration of the incoming pulse. The measured duration is then passed through the window comparator where it is compared with the two thresholds for the pulse duration V_{PT_Max} and V_{PT_Min}. If the measured value of duration lies between the specified thresholds, then the system generates a flag indicating the presence of the pace signal and the system is then reset by the external MCU or internal reset (whichever is used) and the system then looks for the next pulse and the sequence repeats. If the pace duration does not lie between these thresholds, the system then again waits for the next pulse which satisfies the earlier two criteria that is the amplitude and valid rise time.

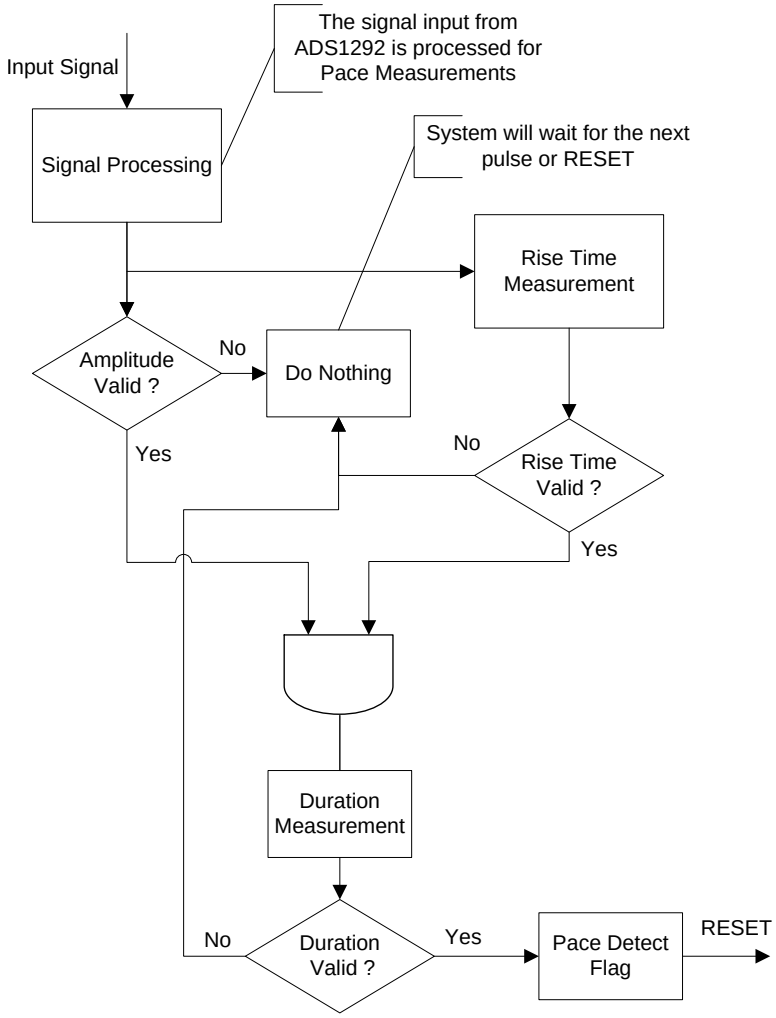


图 **7. TIDA-010005 System Flow Diagram**

2.3.2 Input Section

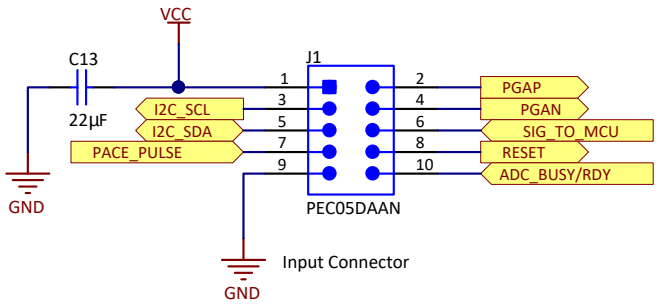


图 8. Input Connector to TIDA-010005

The TIDA-010005 design interfaces with other patient monitoring boards through the input connector as 图 8 shows. The design is powered through a 3.3-V source and has I^2C lines to communicate with the master device. 表 2 describes the function of each pin in the input connector.

表 2. Input Connector Pin Description

PIN NUMBER	PIN NAME	DESCRIPTION
1	VCC	3.3-V input supply
2	PGAP	Non-Inverting differential ECG Signal from ADS129X Channel-1/2
3	I2C_SCL	Clock line for I^2C interface (pulled up to supply)
4	PGAN	Inverting differential ECG Signal from ADS129X Channel-1/2
5	I2C_SDA	Data line for I^2C interface (pulled up to supply)
6	SIG_TO_MCU	Processed single ended signal before Pace measurements sent to the MCU for diagnostic purpose
7	PACE_PULSE	Digital Signal indicating presence of pace pulse
8	RESET	Reset pin to reset the system externally
9	GND	System Ground
10	ADC_BUSY/RDY	The device pulls this pin high when it is scanning through channels in a sequence and brings this pin low when sequence is completed or aborted in TI device ADC ADS7142. (Not used in the design)

2.3.3 Input Signal Filtering for Pace Detection

The TIDA-010005 design takes the source ECG signal from TI's ADS129X family of analog front-end for bio-potential measurements. 图 9 shows the functional block diagram of the device. The device has two channels for the analog output before the signal gets digitized namely PGA1P - PGA1N and PGA2P - PGA2N as highlighted in red boxes in 图 9. The analog output is available on PGA1P-PGA1N or PGA2P-PGA2N channels depending on the mode of operation of the device. As the signal at the output is very small and is susceptible to a lot of noise, filtering techniques used in the design play a critical role to get the clean signal for pace detection.

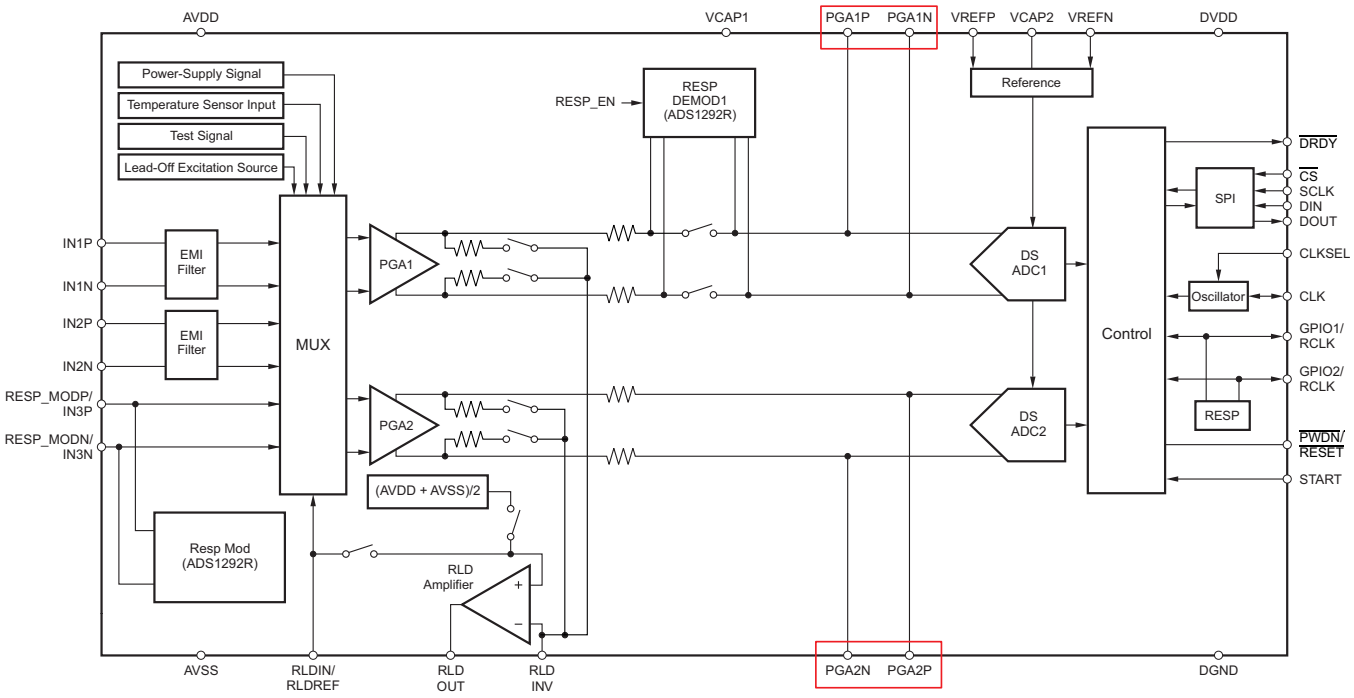


图 9. ADS129X Functional Block Diagram

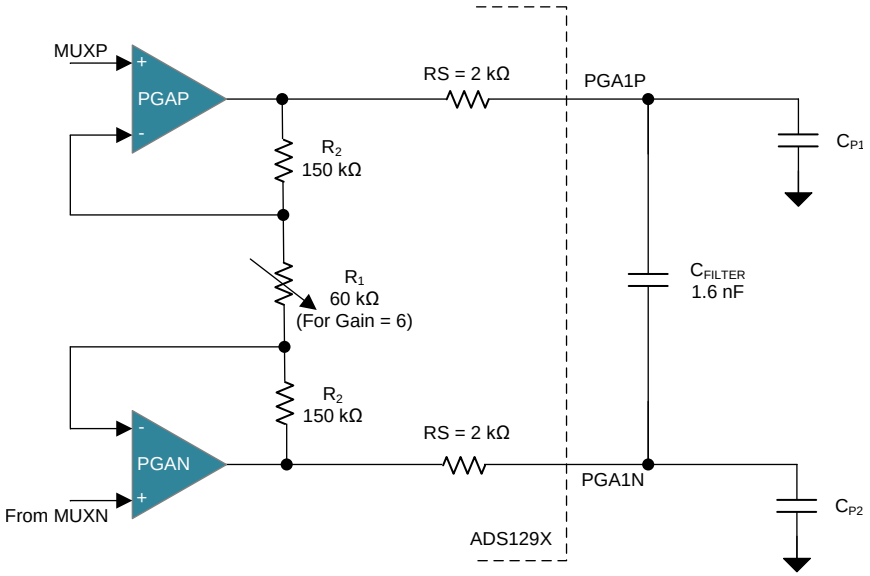


图 10. PGA Implementation in ADS129X Device

图 10 shows the PGA implementation inside the ADS129X device. The PGA is a differential input & differential output amplifier. It has seven gain settings (1, 2, 3, 4, 6, 8, and 12) that are set by writing to the CHnSET register (see *Low-Power, 2-Channel, 24-Bit Analog Front-End for Biopotential Measurements Data Sheet*).

The PGA output is filtered by an RC filter before it goes to the ADC. The filter is formed by an internal resistor R_S = 2 kΩ and an external capacitor C_{FILTER}. This RC filter also suppresses the glitch at the PGA output caused by ADC sampling. The PGA are chopped internally at either 8, 32, or 64 kSPS, as determined by the CHOP bits (see *Low-Power, 2-Channel, 24-Bit Analog Front-End for Biopotential Measurements Data Sheet*).

If PGA output is used for hardware pacemaker detection, the chopping ripple must be filtered. First-order filtering is provided by the RC filter at the PGA output. If the PGA output is routed to other circuitry, a 20-kΩ series resistance must be added in the path near the C_{FILTER} capacitor.

This filter is designed to act as an anti-aliasing filter with the –3-dB bandwidth of 25 kHz.

Hence,

$$C_{FILTER} = \frac{1}{2\pi(2R_S)f_S} = 1.6\ nF \quad (4)$$

注: To get better signal quality, TI recommends putting a 1.6-nF capacitor between the PGAP and PGAN outputs in the ADS129X device. Set the PGA chop frequency of the device at 64 kSPS.

2.3.4 Differential to Single-Ended Conversion

As discussed in 节 2.3.3, a 20-kΩ series resistance is placed in the input path, which with the 330-pF capacitor makes another stage of low-pass filter with cutoff frequency given by 公式 5:

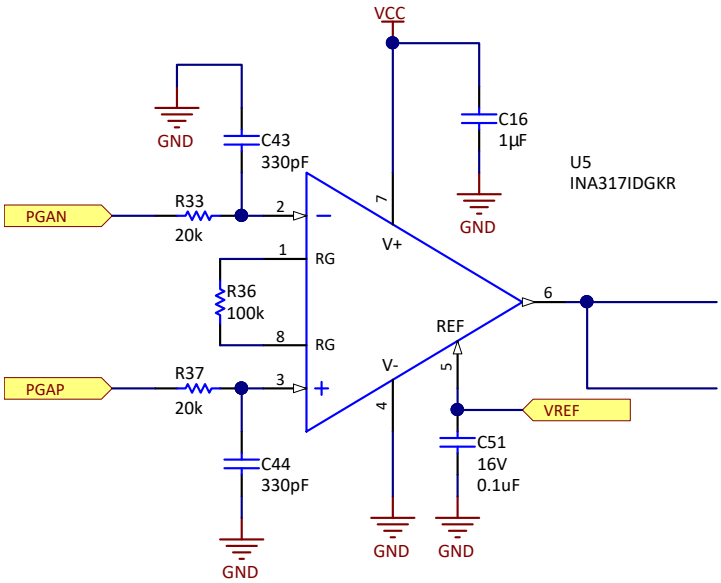


图 **11. Differential to Single-Ended Conversion Circuit**

$$f_{lpf} = \frac{1}{2\pi RC} = 25\ kHz \quad (5)$$

The instrumentation amplifier INA317, converts the differential signal to a single ended output. The amplifier also gives a gain of 2 which makes the value of R_G (R36) to be 100 kΩ as given by 公式 1. The VREF is the reference voltage to bias the amplifier at the mid-supply, the value of VREF is 1.65 V.

2.3.5 Low-Pass Filter, High-Pass Filter, 50- 60-Hz Notch Filter Design

The TIDA-010005 design is configurable in hardware as well. A provision is made to place a LPF, HPF, 50- or 60-Hz Notch Filter for applications in which additional filtering is required. The pace signal from the pacemaker is generally a high-frequency signal as compared to the ECG is which is much slower typically in order of a few Hertz. On the other hand, the signal coming out from ADS1292 has significant high-frequency content from the PGA chopping as described in 节 2.3.3. Hence, the second-order LPF stage is implemented with the 3-dB frequency of 25 kHz.

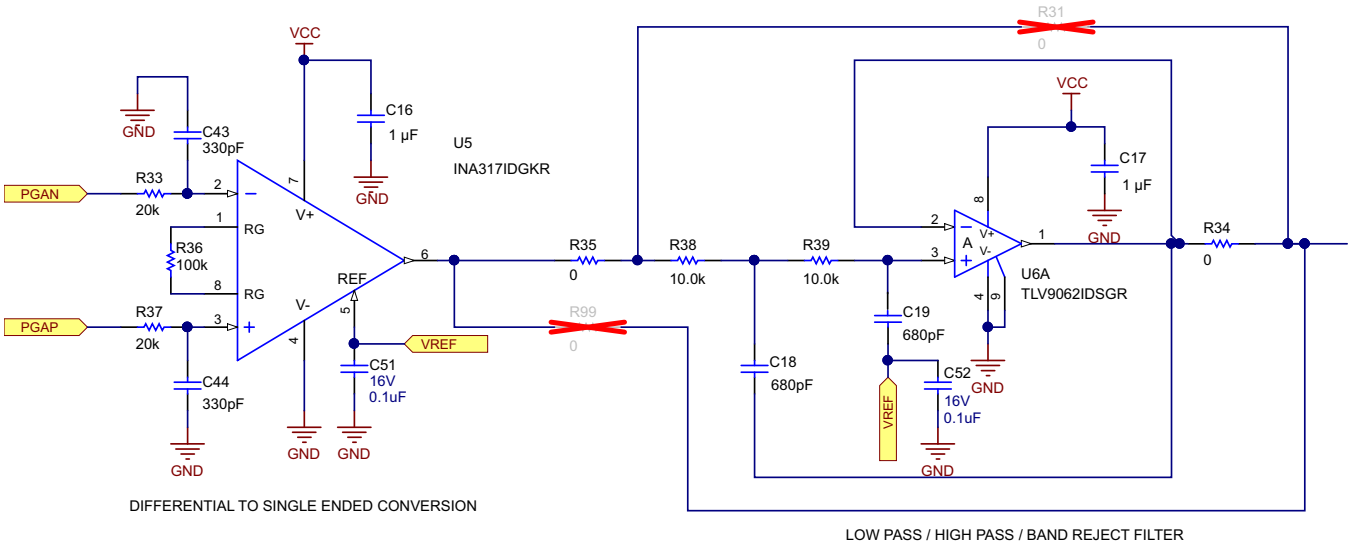


图 12. Low-Pass Filter Schematics for Filter Implementation

图 12 shows the LPF configuration settings for the filter implementation. A second-order LPF is made through two sets of RC and TI's TLV9062 device. The 3-dB frequency is set at 25 kHz. It is important to note that the amplifier has a positive feedback coming back to the filter resistor which essentially provides the boost of gain at low frequencies. 图 13 shows the TINA-TI™ simulation diagram of the filter with the instrumentation amplifier INA333 at the single-ended conversion stage. 图 14 shows the frequency and phase response of the circuit from 10-Hz to 2-MHz. It can be verified from the frequency response that the filter has almost constant gain at low frequencies. The VREF is generated through a resistor divider network followed by a voltage follower (TLV9062) to have sufficient drive strength.

The same circuit can also be configured as a high-pass filter (HPF) by interchanging the positions of the resistor and capacitor of the two RC pairs, R38-C18 and R39-C19, with a provides a suitable cutoff frequency.表 3 shows all the connections for the possible configurations.

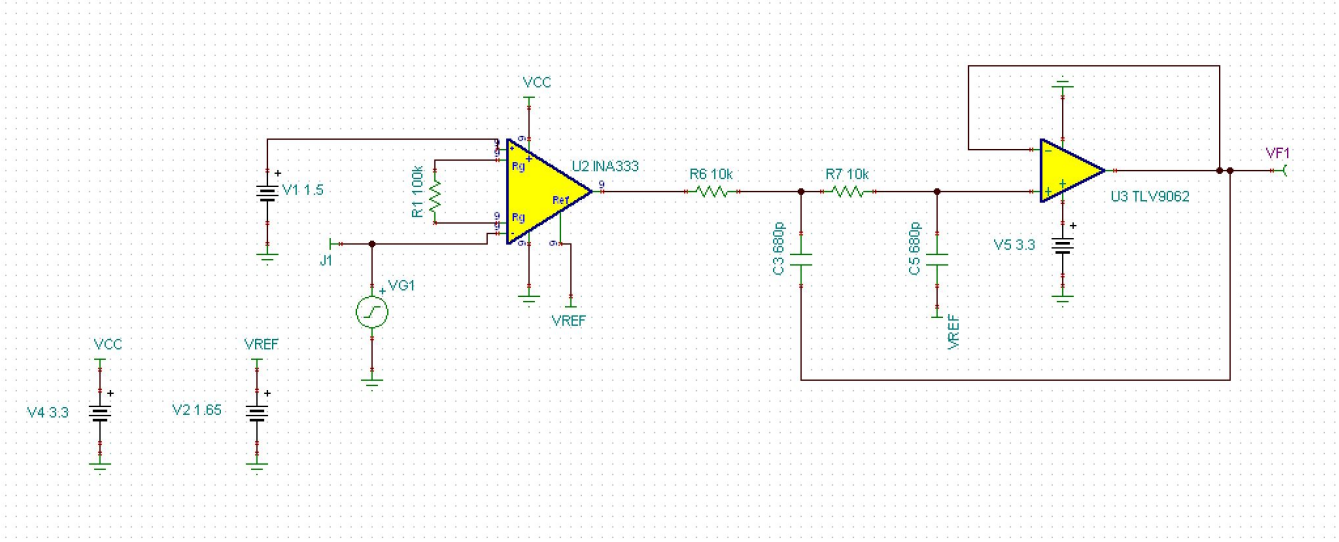


图 **13. TINA-TI™ Simulation Circuit of the Low-Pass Filter**

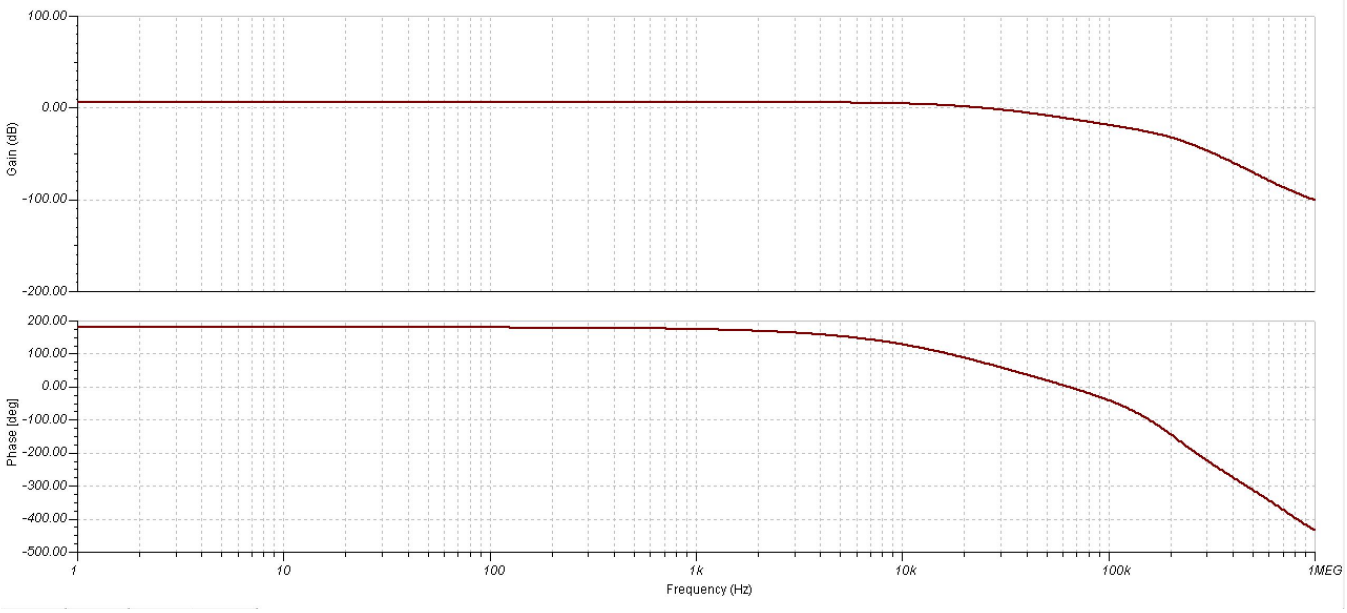


图 **14. Frequency and Phase Response of the High-Pass Filter From 1 Hz to 1 MHz**

Reconfigure the same hardware to use as a 50- or 60-Hz notch filter. The notch filter is implemented through the same op amp (TLV9062) as an inductor and made an LC-based notch filter. Note the value of the components is changed in the implementation as compared to HPF and the output of the filter is taken from the other end of R35. Use R35 to be 10-kΩ, C18 and C19 to be 1-µF, R39 to be 15-kΩ and R38 to be 500-Ω for a 60-Hz notch filter. 图 15 and 图 16 show the TINA-TI™ schematic and simulation results of the frequency response of the filter. As the plot in 图 17 shows, at 60-Hz the gain is close to –15 dB.

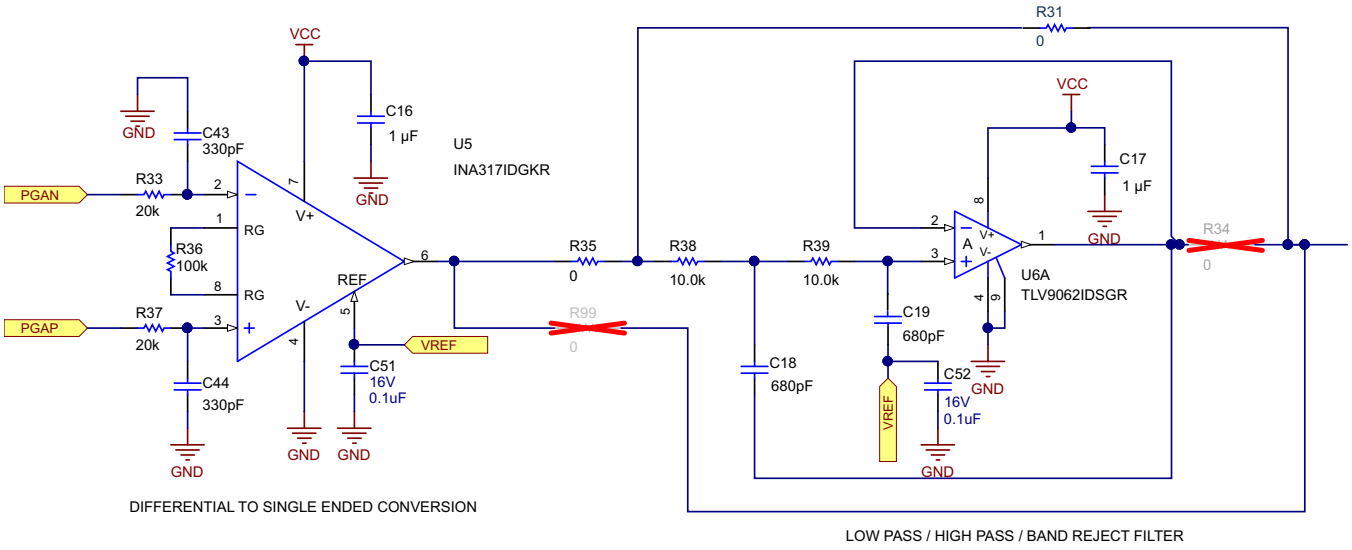


图 **15. 50, 60 Hz Notch Filter Schematics for the Filter Implementation**

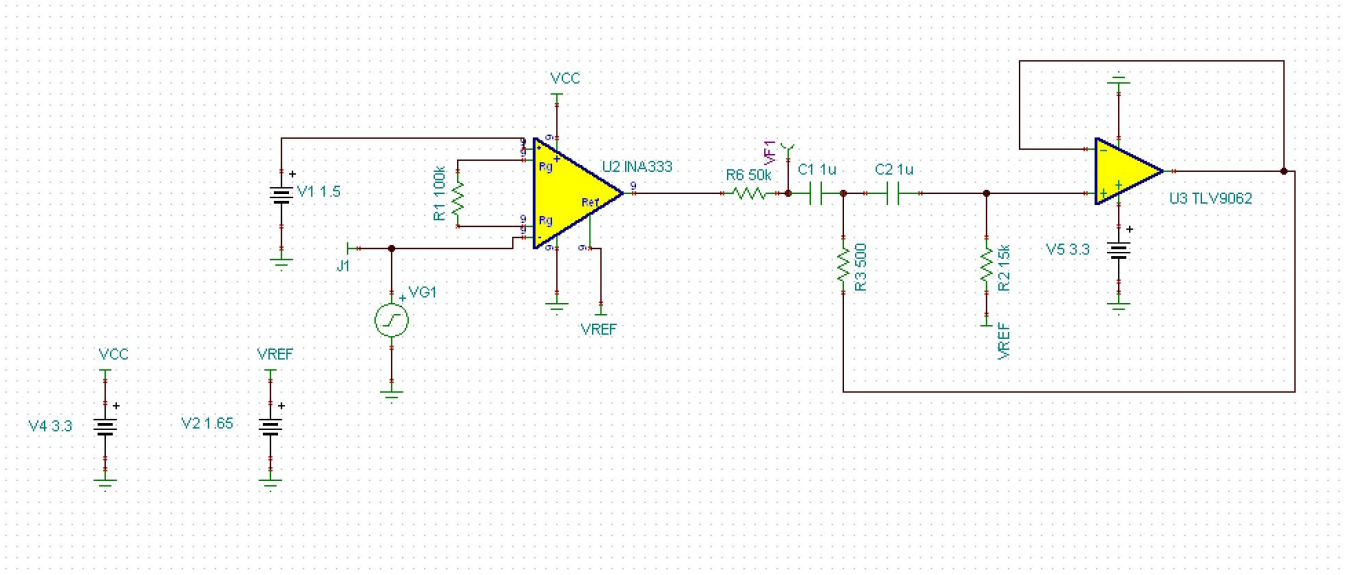


图 **16. TINA-TI™ Simulation Circuit of the 60-Hz Notch Filter**

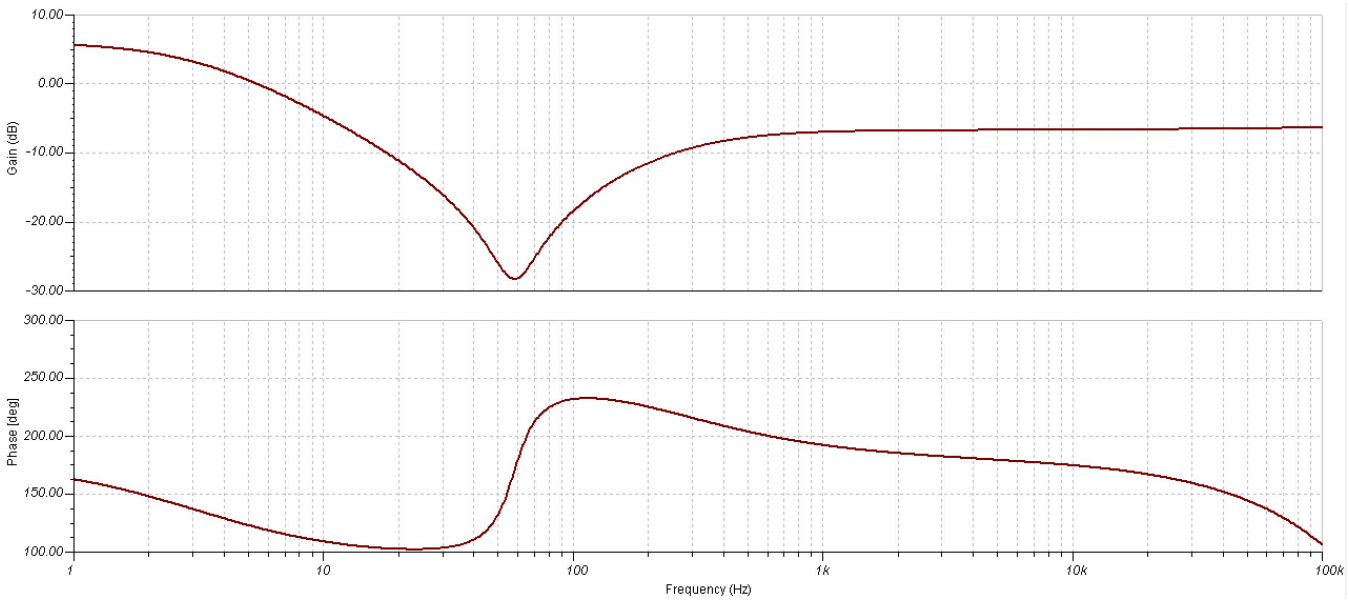


图 **17. Frequency and Phase Response of the 60-Hz Notch Filter From 1 Hz to 100 kHz**

The same 60-Hz notch can also be modified for a 50-Hz notch filter by changing the resistor R38 from 500-Ω to 720-Ω. Use R35 to be 10-kΩ, C18 and C19 to be 1-µF, R39 to be 15-kΩ and R38 to be 720-Ω for 50-Hz notch filter. 图 18 and 图 19 show the TINA-TI™ schematic and simulation results of the frequency response of the filter. As the plot in 图 19 shows, at 50-Hz the gain is close to –12 dB.

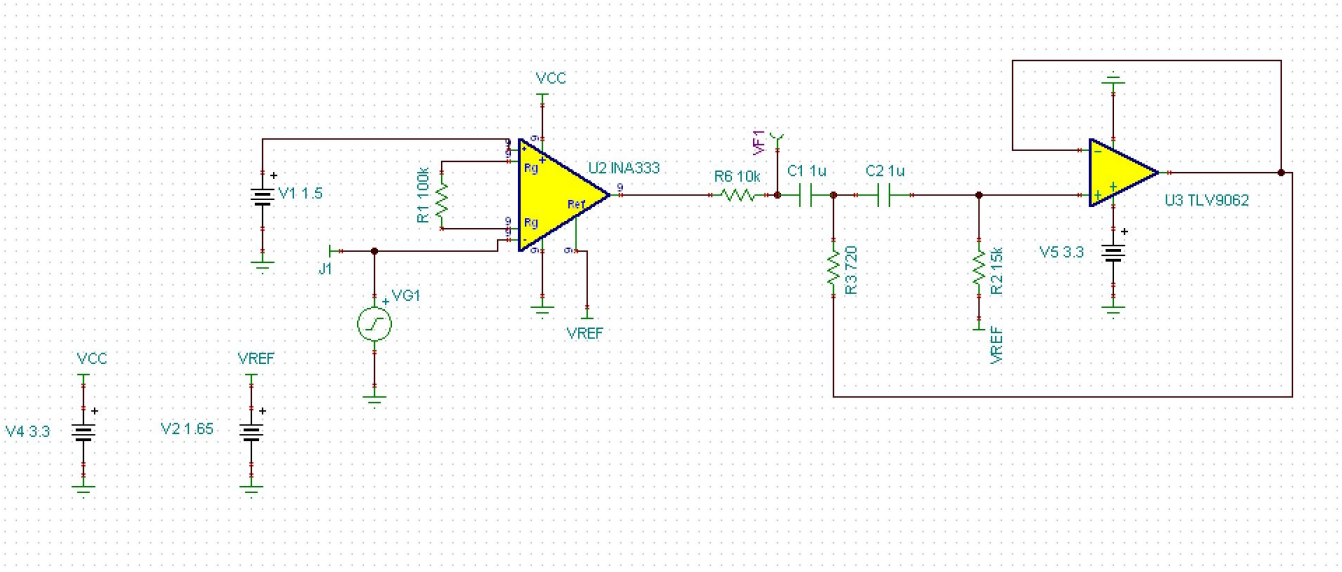


图 **18. TINA-TI™ Simulation Circuit of the 50-Hz Notch Filter**

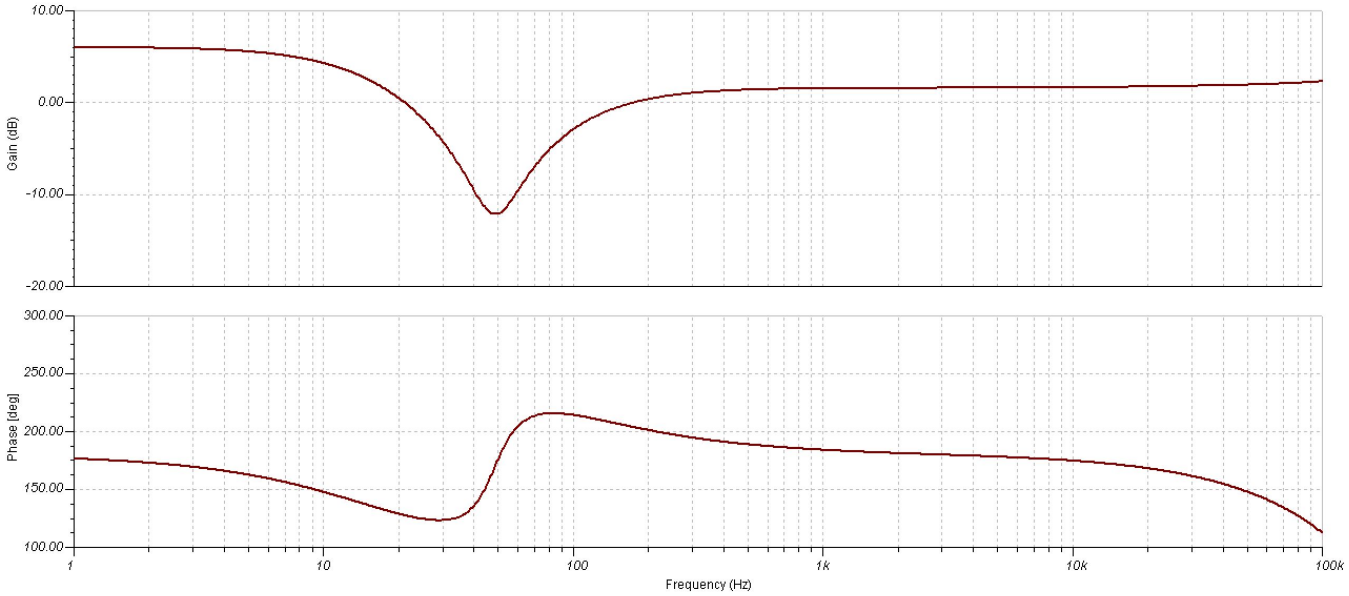


图 19. Frequency and Phase Response of the 50-Hz Notch Filter From 1 Hz to 100 kHz

Note the resistor configuration required to change the configuration of the system. Make sure the DNP (Do Not Populate) components for a particular configuration are not mounted or mounted accordingly. 表 3 shows the component values for the different configurations of the filtering stage. For interchanging position, see the schematics provided in 图 15, 图 16 and 图 18 for the required configuration.

表 3. Component Values for Different Filtering Stage Configurations

COMPONENT	LPF (25 kHz)	HPF (85 Hz)	50 Hz NOTCH	60 Hz NOTCH	BYPASS FILTER
R35	0 Ω	0 Ω	10 kΩ	50 kΩ	DNP
R99	DNP	DNP	DNP	DNP	0 Ω
R38	10 kΩ	124 kΩ (interchange position with C18)	720 Ω (interchange position with C18)	500 Ω (interchange position with C18)	Don't Care
C18	680 pF	15 nF (interchange position with R38)	1 µF (interchange position with R38)	1 µF (interchange position with R38)	Don't Care
R39	10 kΩ	124 kΩ (interchange position with C19)	15 kΩ (interchange position with C19)	15 kΩ (interchange position with C19)	Don't Care
C19	680 pF	15 nF (interchange position with R39)	1 µF (interchange position with R39)	1 µF (interchange position with R39)	Don't Care
R31	DNP	DNP	0 Ω	0 Ω	Don't Care
R34	0 Ω	0 Ω	DNP	DNP	DNP

2.3.6 Gain & Polarity Correction Circuit Design

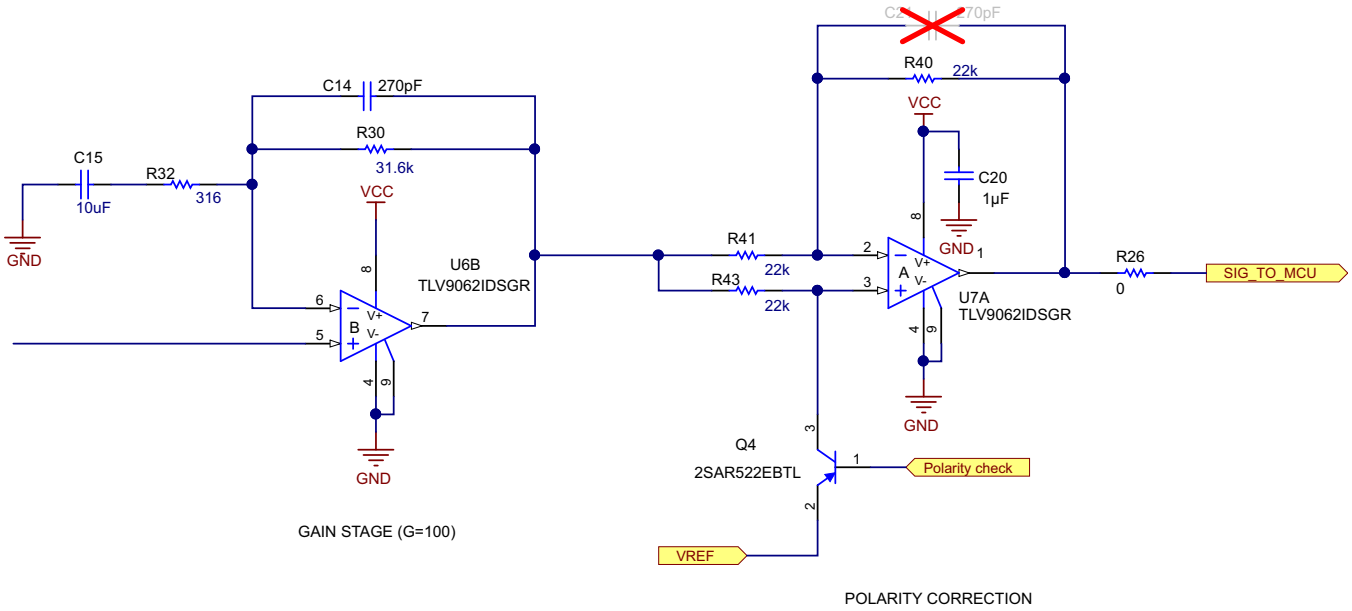


图 20. Gain and Polarity Correction Circuitry Schematic

图 20 shows the schematic of the Gain and Polarity Correction circuitry implemented in the design. As shown in the schematic the gain to the input signal is provided by the TLV9062 device in non-inverting amplifier configuration. The gain is given by 公式 6:

$$G = \frac{V_O}{V_{IN}} = 1 + \frac{R_{30}}{R_{32}} = 101 \quad (6)$$

Another LPF is placed at the inverting terminal of the op amp TLV9062. The cutoff frequency is given by 公式 7

The polarity correction is implemented as shown in 图 20. The function of this block is to invert the negative-going pace pulse and convert it into positive so that it's characteristics could be measured by the Pace Measurement Section as shown in 图 4. This is done by providing a control signal to the operational amplifier through the DAC output Polarity check.

图 21 depicts the idea behind the implementation of the polarity correction circuit. The output V_{out} of the circuit depends on the input $V_{control}$ of them N-MOS.

When $V_{control}$ is HIGH, the positive non-inverting terminal of TLV9062 becomes GND. Then the whole circuit is just a inverting amplifier with a gain of -1.

However, when $V_{control}$ is LOW, then we have

$$f_{lpf} = \frac{1}{2\pi R_{30} C_{14}} = 18.7 \text{ kHz} \quad (7)$$

$$V_+ = V_{IN} = V_- \text{ since } i_+ = 0 \quad (8)$$

$$V_{OUT} = V_{IN} \quad (9)$$

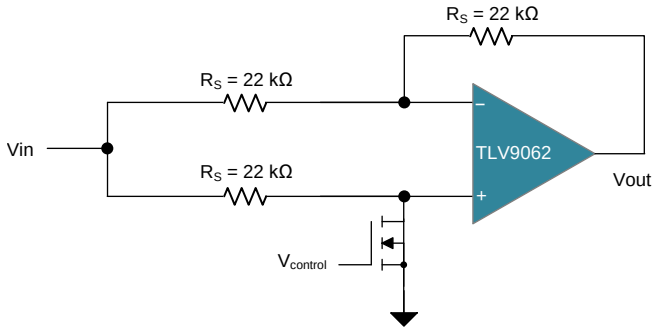


图 21. Polarity Reversal Circuit Explanation

Hence the circuit in 图 21 acts as a full bridge rectifier which passes the signal as inverted or same depending on the $V_{control}$ input. The schematic shown in 图 20 replaces the N-MOS shown in 图 21 with a pnp transistor at the non-inverting input of the TLV9062 device and acts as the switch which makes the circuit function as polarity correction circuit. Whenever the input signal is greater than the VREF that is the mid-supply (1.65 V), the transistor is OFF of the circuit exactly follows the input. However, when the input signal goes lower than the VREF - V_{th} that is approximately 1 V, the output becomes inverted with a gain of -1. 图 22 and 图 23 depict the schematic and output characteristics of the polarity correction stage. A 10-mV, 4.5-kHz sine wave (VG1) is input at the gain stage and the corresponding output at each stage is shown. A control signal Polarity check is sent to the base of the pnp transistor which essentially activates the negative polarity check and inverts the waveform. As shown 图 23, the Polarity check is 3 V for 500 µs and then 0 V for the remaining 500 µs, and the output polarity correction gets inverted once the control signal changes.

Note that to enable negative pace signal detection, Polarity check signal which comes from DAC (ch 6 Polarity check) should be set LOW (0 V). By default, it is set HIGH (3 V) to monitor positive pace signal detection.

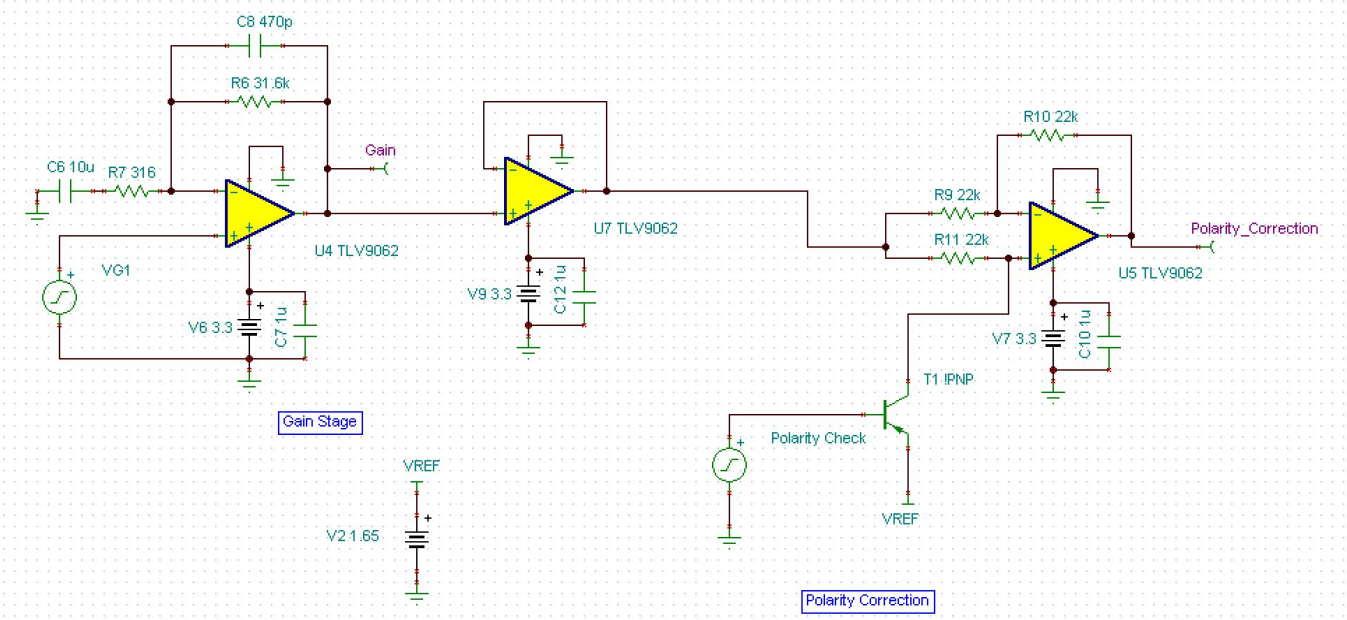


图 **22. TINA-TI™ Simulation Schematic Gain and Polarity Correction Circuit**

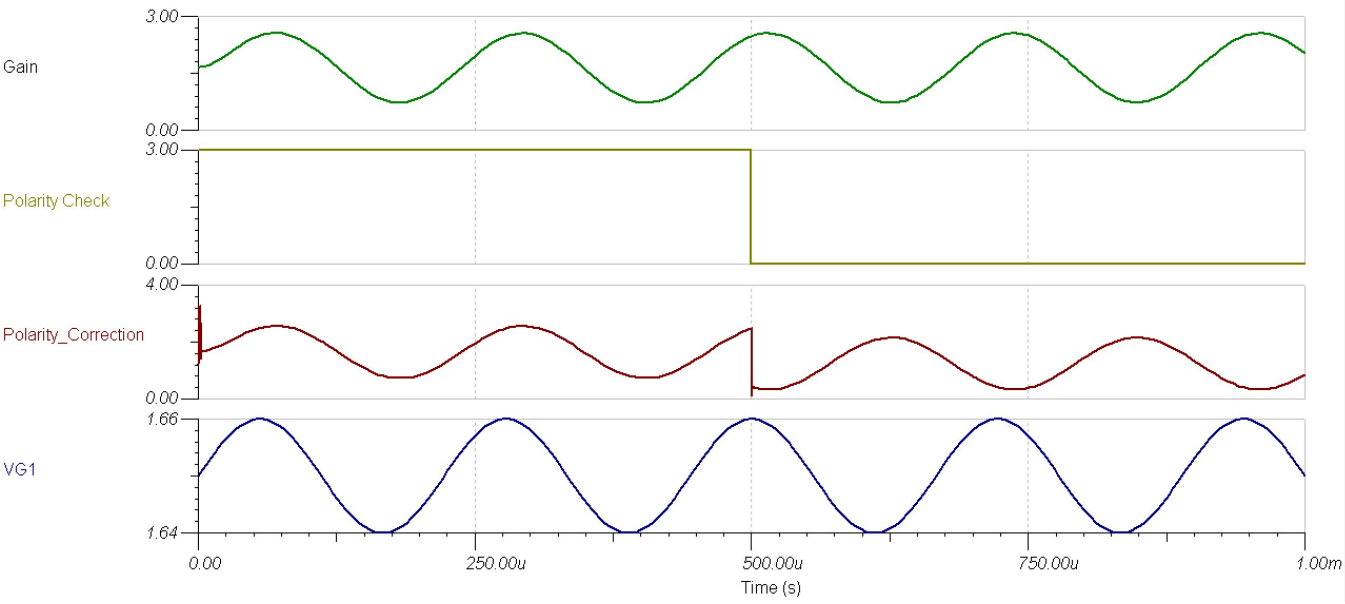


图 **23. TINA-TI™ Simulation Output Characteristics of Gain and Polarity Correction Circuit**

图 24 shows the TINA-TI™ schematic of the full Signal Processing Section implemented till the polarity correction. A 5-mV, 4.5-kHz sine wave is the input to the INA333 and the output at each stage is shown in 图 25. 图 26 shows the magnitude and phase response at each stage. The color coding is consistent with the name of the stage.

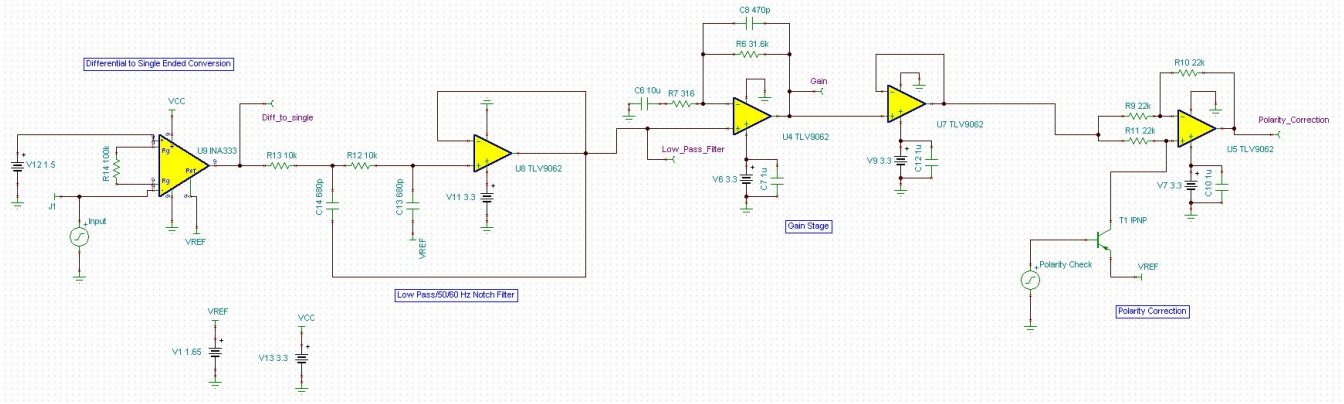


图 24. TINA-TI™ Schematic of the Entire Signal Processing Section

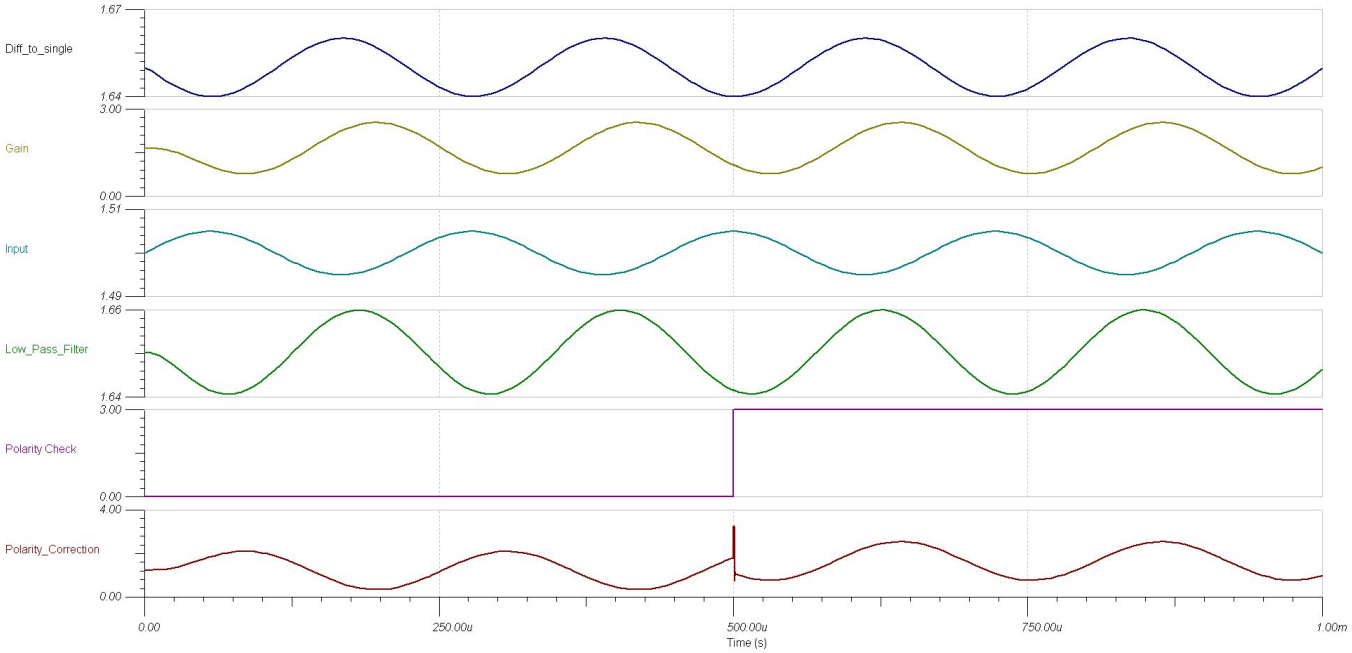


图 25. TINA-TI™ Simulation Output Characteristics of Entire Signal Processing Section

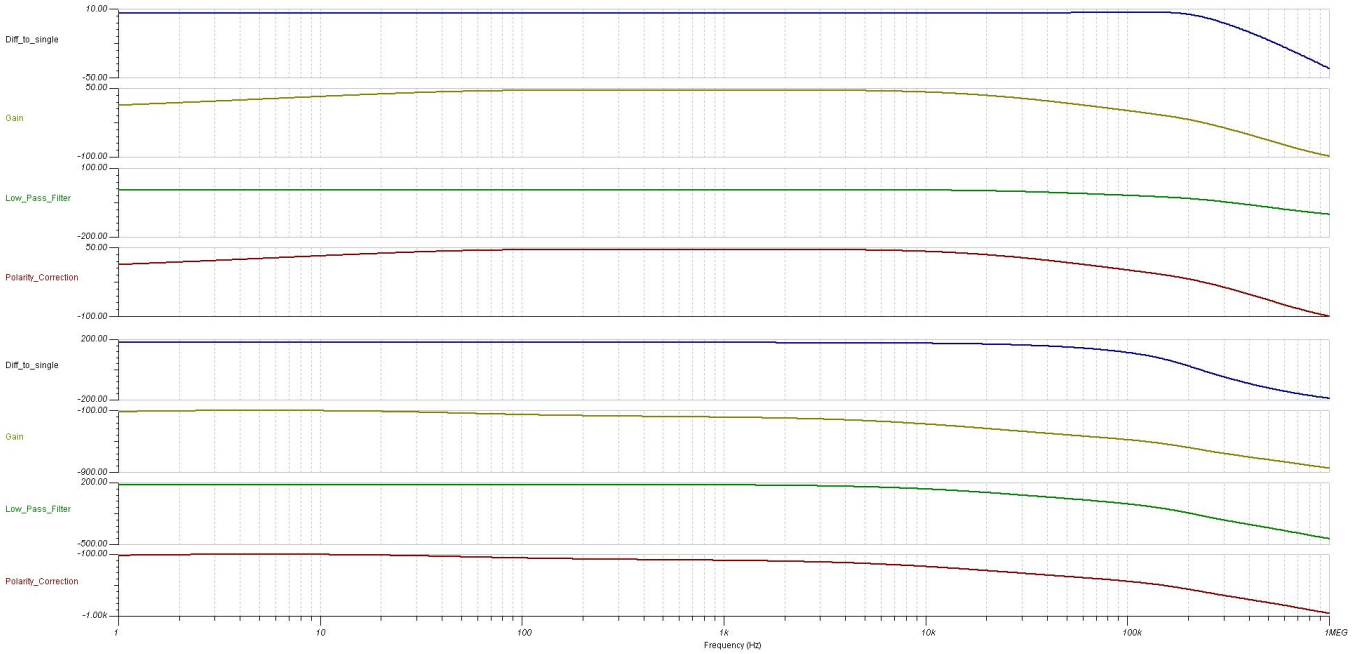


图 26. Magnitude and Phase Response of the Entire Signal Processing Section From 1 Hz to 1 MHz

2.3.7 Signal Measurement Section

This section discuss the implementation of the measurement part of the system where we will measure individual characteristic of the pace pulse, its amplitude, rise time and the duration. We will discuss the theory behind the implementation in detail in the following subsections.

2.3.7.1 Rise Time and Amplitude Measurement

As discussed earlier in 2 节, the pace pulse is identified by its three characteristics: Amplitude (V_{Amp}), Rise Time (T_R) and Pulse Duration (T_D). From the block diagram shown in 图 4, we generate TTL pulses corresponding to the rise time and the duration, the explanation for the same is provided in 2.1 节. From the flowchart in 图 7, we see that the sequence of events is very important in measurement of the pulse.

图 27 shows the schematic implemented for the signal measurement. The comparator TLV1702 (U13A) checks the amplitude of the incoming signal. The threshold for the same, V_{Amp_th}, comes from the DAC which is programmed by the user.

On the other hand, the signal is differentiated by the differentiator implemented using TLV9062 (U8B), the output of the differentiator is proportional to the following parameters given by 公式 10.

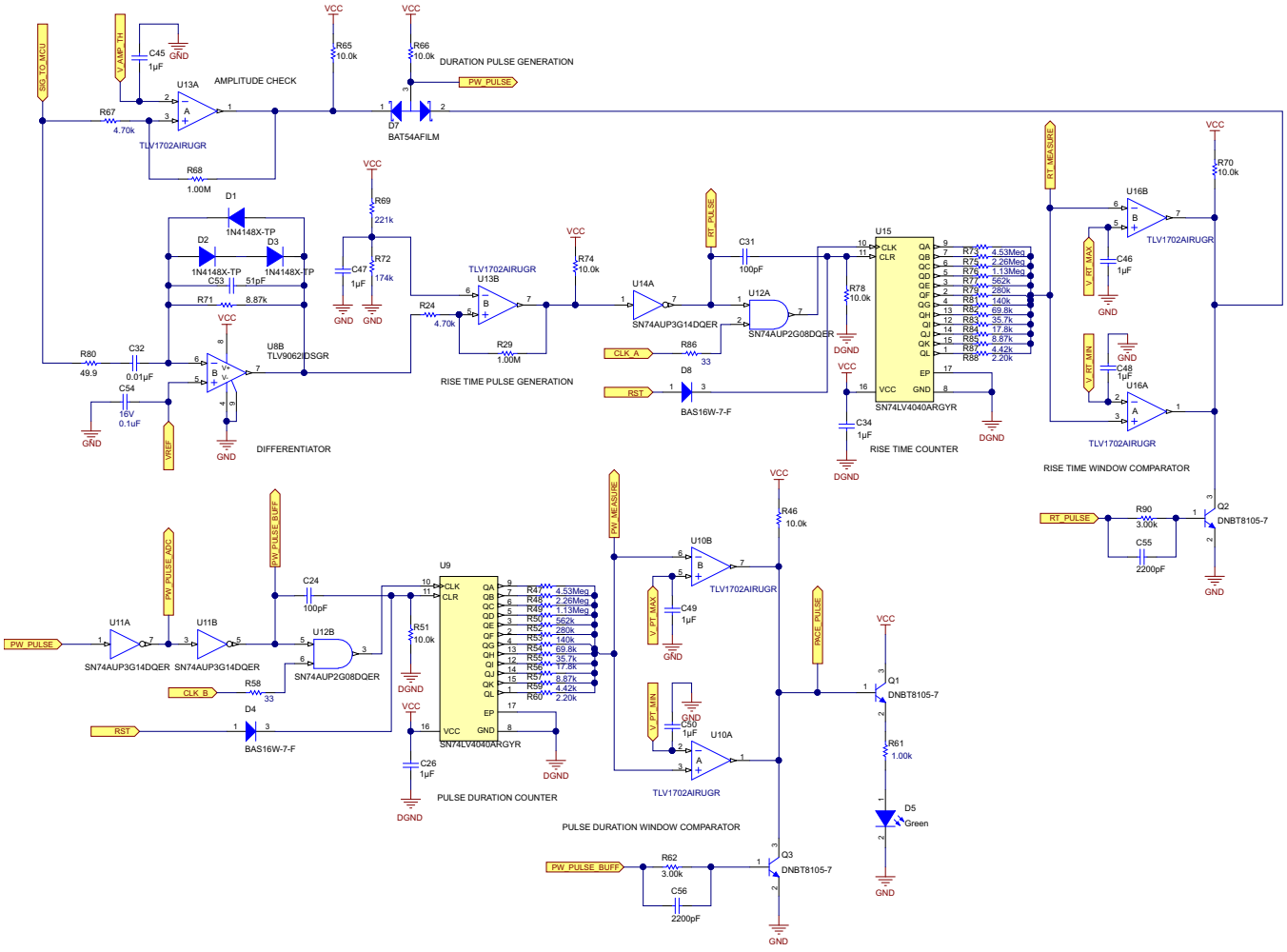


图 **27. Signal Measurement Section Schematic**

The output of the differentiator is a signal whose amplitude depends on the rise time and the amplitude of the input signal and also on the RC time of the differentiator. For practical pace pulses the rise time typically lies in the interval 10 µs – 150 µs, the RC time constant is taken to be 88.7 µs. The resistor R80 (49.9 Ω) removes the ringing at the output of the differentiator and limits the gain at very high frequencies. The anti-parallel diodes across the output and the inverting terminal limits the range of operation of the differentiator so that the output does not saturates to the supply. This is essential for the fast recovery of the signal when the rise time is very small. The range of the output in the positive direction is 1.65+V_{th} and in the negative direction is 1.65 - 2 V_{th}, where V_{th} is the cuttin voltage of the diode which is 0.72 V for diode 1N4148.

The output of the differentiator is converted to the TTL pulse using the comparator TLV1702 (U13B). The threshold at the inverting terminal is set according to the largest rise time so than any pulse whose rise time is lesser will always get recognized.

The TTL pulse corresponding to the rise time is ANDed together with the clock CLK A and is fed to the counter SN74LV4040 which basically measures the time for which the TTL pulse lasts. The counter output is connected to the R2R ladder which translates it to an equivalent voltage. As the count increments the analog voltage rises in a staircase form, which if fed further to the window comparator.

An important aspect of the design to be noted here is that the window comparator gets the threshold for minimum and maximum rise time and is activated by the npn transistor Q2. It pulls down the output of the window comparator to ground till the pulse last. Once the counting is done then only the comparator's output is released.

If the counted analog voltage lies between the two thresholds: V_{RT_min} and V_{RT_max} and the Amplitude condition is satisfied that is $V_{Amp} > V_{Amp\_th}$, then and only then is the next pulse to measure pulse duration is generated.

The diode D7 takes care of both the conditions that is the amplitude check and the validity of the rise time. If both the things are right, we will see a TTL pulse corresponding to the duration of the pace pulse at the other end of R66. This is also explained in 2.1 节.

图 28 and 图 29 show the TINA-TI™ simulation of the measurement section till the generation of both the TTL pulse that is the Rise Time Pulse and the Pace Duration pulse. The input signal is a waveform whose rise time is st at 50 µs and its duration is 1 ms. From the simulation output we can see the Rise Time Pulse of approximately 50 µs and the Pace Duration pulse is approximately 1 ms which verifies the theory implemented.

$$V_o \alpha \frac{dV_{IN}}{dt} \times (R_{71}C_{32}) \quad (10)$$

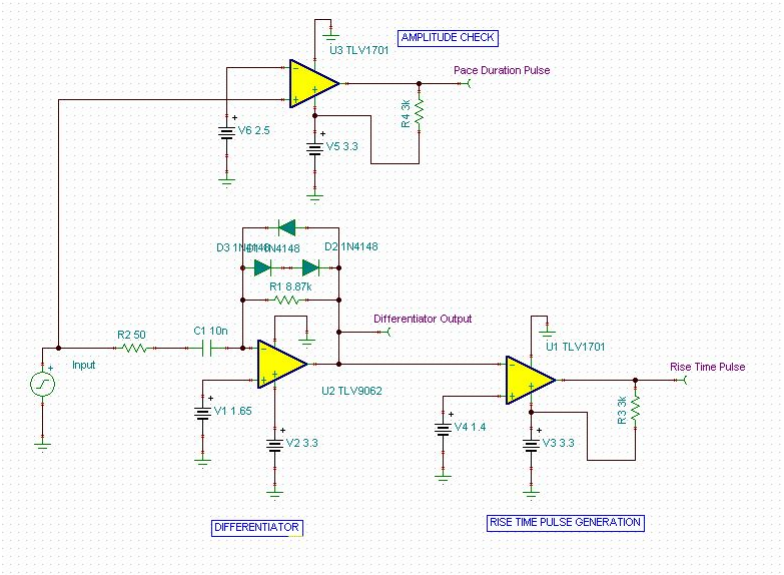


图 28. TINA-TI™ Simulation Schematic of the Signal Measurement Section Till Pulse Generation

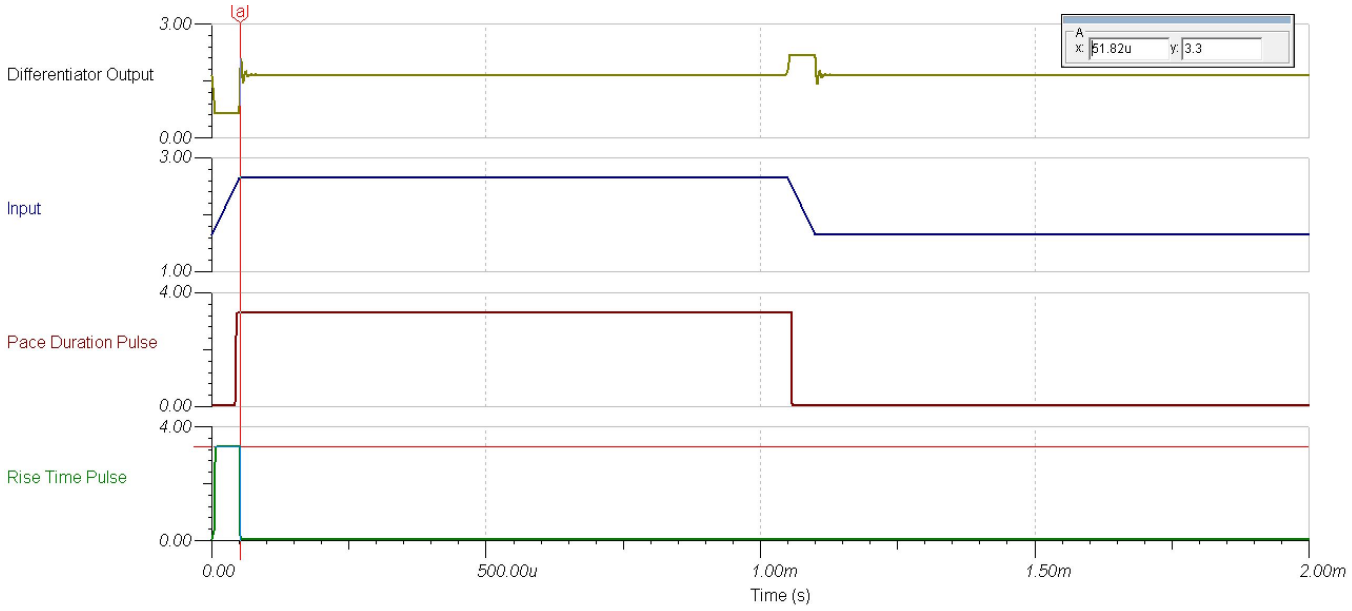


图 **29. Simulation Output of the Signal Measurement Section Till TTL Pulse Generation**

2.3.7.2 Pulse Duration Measurement

The pulse duration is measured using the identical hardware system as the rise time measurement. The TTL pulse generated for the duration of the pulse as discussed in 2.1 节and 节 2.3.7.1 is ANDed together with CLK_B and is fed to a counter SN74LV4040 (U9). The duration is measured and a similar window comparator is used to check the bounds of the duration. If the signal satisfies all the three criteria : Amplitude, Rise Time and the Pulse Duration. The output of the window comparator gives a rising edge pulse called PACE_PULSE, which is sent back to the MCU as a flag for the pace pulse detection. An onboard LED also blinks indicating the presence of pace signal real time.

2.3.8 Clock Generation

The TIDA-010005 performs the measurement of the pulse characteristics using the counter. The counter increments its value at each falling edge of the clock. Hence the clocks required for the measurement must be faster than the signal. Since we have different ranges for the rise time (30-200 µs) and pace duration (0.1-2 ms), it makes sense to employ two different clocks with different frequency to be able to measure both the ranges without losing the resolution. The TIDA-010005 employs two on-board clocks CLK_A and CLK_B of frequency 1.75 MHz and 0.806 MHz, respectively. 图 30 shows the circuitry implemented to generate the onboard clock. This uses a Schmitt Trigger based inverter which is configured in an oscillator configuration to generate the clock signal whose time period is proportional to the RC time constant of the placed resistor and capacitor.

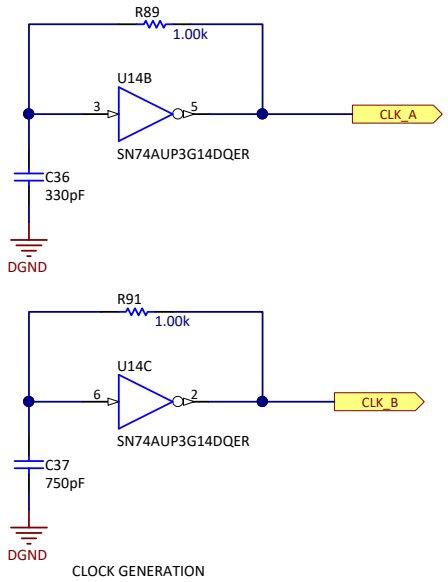


图 **30. Circuitry Implemented to Generate Onboard Counter Clocks**

2.3.9 DAC5578 & ADS7142 ADC Implementation – 2 Wire I²C Compatible Interface

The two-wire serial interface used by the DAC5578 used in TIDA-010005 is I²C-compatible. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up resistors as shown in the input connector in 图 8. 图 31 shows the schematics of the DAC and the ADC implementation in the design. The Slave Address (SA) of the DAC5578 device is 1001000 which is selected by making the ADDR0 pin to GND (R19 as DNP). The reference voltage to the DAC is taken from the TI Device REF2930 (R16-DNP) which can be bypassed (optional) by using the supply voltage VCC directly (place R16 and DNP - R25). When the I²C bus is idle, both SDA and SCL lines are pulled high. The master device generates the SCL signal and the special timing conditions to indicate the start or stop of a data transfer. The Device addressing is also performed by the master controller.

The design uses 6 channels of the DAC5578 to generate the various thresholds and the control signal Polarity check to activate the negative pace detection which is active low signal as shown in the schematics in 图 31

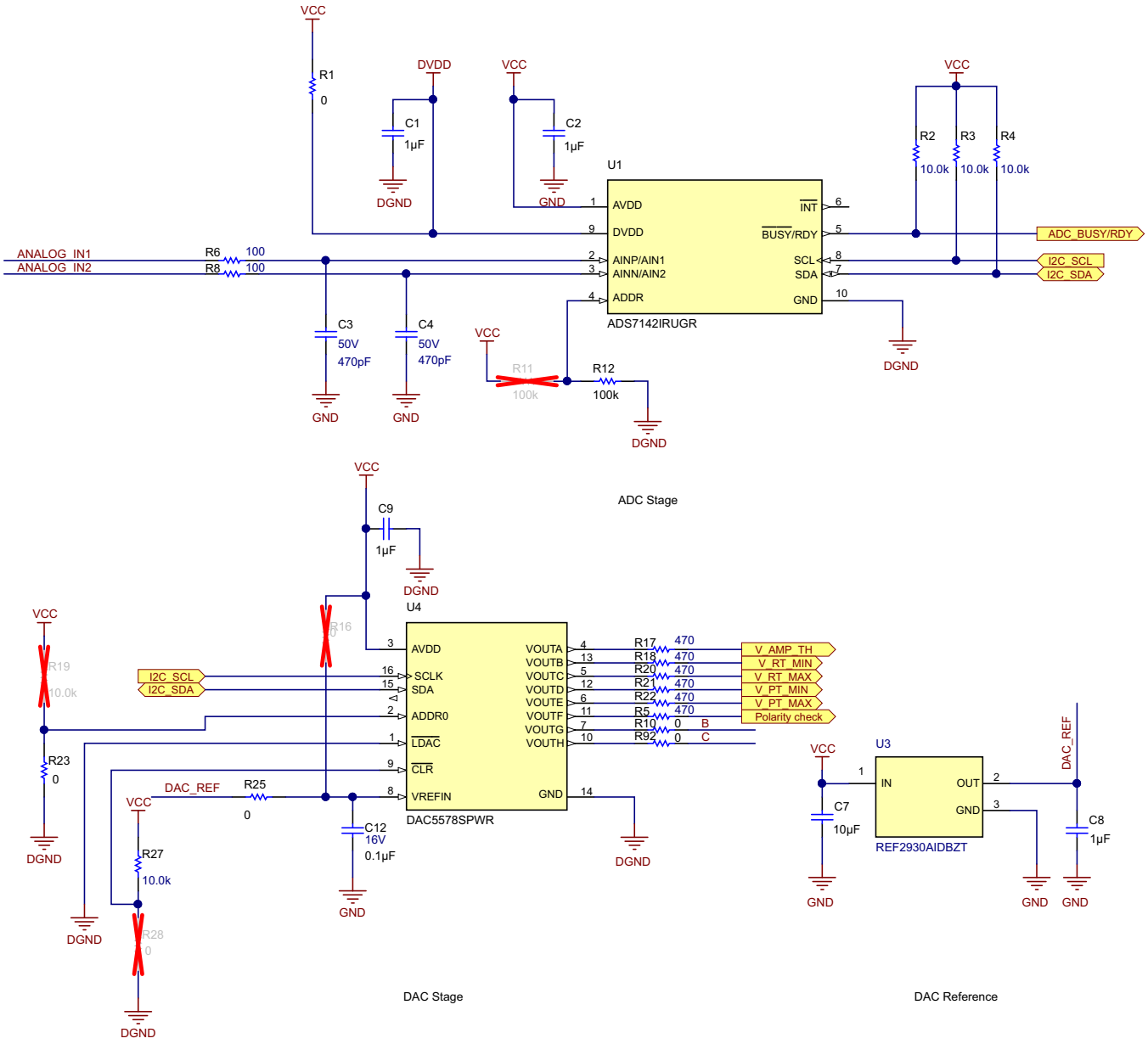


图 31. ADC & DAC Implementation in the Reference Design

The DAC5578 in TIDA-010005 operates as a slave device on the I^{2}C bus. A slave device acknowledges the master commands, and upon the direction of the master, either receives or transmits data. For a single update, the DAC requires a start condition, a valid I^{2}C address (SA), a command and access byte (CA), a two data bytes : the most significant data byte (MSDB) and least significant data byte (LSDB). For more information of the DAC protocol, see *8-/10-/12-Bit, Octal-Channel, Ultra-Low Glitch, Voltage Output, Two-Wire Interface Digital-to-Analog Converters*.

When using an external reference the ideal output voltage V_{OUT} of the DAC is given by 公式 11:

$$V_{OUT} = \frac{D_{IN}}{2^n} \times (V_{REFIN})$$

where

- D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. The code can range

from 0 to 255 for the 8-bit DAC5578.

- V_{REFIN} = external reference voltage of 0 V to 5 V (3 V used in the design), supplied at the V_{REFIN} pin.
- n = resolution on bits; 8 for DAC5578 (11)

Upon power up, the controller sends the DAC all the thresholds sequentially. Once all the thresholds are set on the board, the system starts to detect the pace signal if they are present in the input ECG system and satisfy the criteria set by the user. The coding for the DAC can be easily set up by interfacing the DAC through any I^2C enabled controller. Please use the datasheet of the TI Device DAC5578 for the specific commands and addresses of the registers to configure it.

The value of the parameters can be stored and read using the sample and hold circuit implemented in the design which can then be read over through ADS7142 over I^2C. The sample and hold circuit uses a SPDT analog mux with some logic elements to store the analog value of rise time and the duration. Please see the schematics of the design TIDA-010005 to further understand the implementation.

The ADS7142 device used in the design is a nano power device optimizing system power, reliability, and performance to read the data. The device also uses the same SCL and SDA lines (I^2C protocol) to communicate with the host controller. 图 31 shows the schematic of the ADC section implemented in the design. The slave address of the device is taken as 0011011 (1Bh) which can be set using an external resistor to pin ADDR of the device. The device has various modes of operation and we have used manual mode with two single-ended channel reading with auto-sequencing enabled to read the corresponding durations on the channel. The ADC programming is explained very well in the literature provided in the product folderr of the device ADS7142. The firmware for all the different modes are also available online in the tools and software section of the device's product folder. The user can easily port the codes and modify it based on the requirements.

注: While programming the ADC in Manual mode with Auto-sequencing enabled, please make sure to set SEQ_ABORT bit before the start of conversion. Its a good practice to do this while working with ADS7142 device to get precise measurements.

2.3.10 System Reset

The reset to the system basically means resetting the counter output to zero so that new measurements could be taken and to refresh the system. The reset signal can either come from external MCU through pin 8 of the input connector as shown in 图 8 or from the onboard oscillator (see schematics). The onboard oscillator uses the same SN74AUP3G14 Schmitt-Trigger Inverter similar to the clock generation but the only difference is that it generates a small pulse after a specified time period (which is proportional to R63xC28). The diode D8 and resistor R64 creates a fast discharge path which essentially creates a repetitive reset signal for the system.

When using onboard reset functionality, make sure to DNP R96 so that RESET signal is blocked and RST is allowed. On the other hand, if using MCU then make sure to DNP R97 so that RST gets blocked and RESET is allowed through.

2.4 Design Considerations and Limitations

The design TIDA-010005 is a hardware based solution which provides efficient signal processing and measurements for the pace signal. The various considerations while designing such patient monitoring solutions are described below which directly relates to the selection of the right parts and devices in order to obtain optimum performance. While designing a pace detection solution the effective challenges that one needs to address are:

- Extraction of raw pace signal from the composite 50 Hz, ECG signal with PGA chopping etc without disturbing the pace waveform shape appreciably
- Accurate measurement of amplitude, rise time and width of each and every pulse presented to the unit.

Hence the signal chain requires certain specifications which should be met in order to get good performance:

- Differential to single ended convertor should have a good CMRR with low noise, 3.3 V operation with high bandwidth. TI device INA317 is selected to achieve the desired specs.
- The operational amplifiers should have High Gain Bandwidth Product (10 MHz for TLV9062), 3.3 V operation with Rail to Rail output and low noise. The offset for the device is not critical here since the signal is AC coupled.
- The comparator should have 3.3 V operation with open collector output and small package.

The reference design has certain limitations as well which are listed below:

- The rise time of the signal is larger because of the delay introduced in the signal path due to extensive filtering which limits the bandwidth of the system. Hence very small rise time waveforms can be found longer than expected.
- For very high amplitude of the inserted pace signal, the output becomes saturated (since high gain is there) so the rise time is much smaller. The detection of such signals can be done by properly selecting the DAC thresholds for the rise time. See test results for pace amplitude higher than 20 mV.
- For very small pace signal, typically 2-4 mV the PGA gain can be increased from 1 to some higher value and then the pace detection can be activated. However the performance of the system is subject to the quality of the PGA output of the device ADS129X.

3 Hardware, Software, Testing Requirements, and Test Results

This section describes the details of the evaluation of the design in terms of its performance in detecting the pace signal accurately. The essential system requirements in terms of the hardware and the software are provided in this section.

3.1 Required Hardware and Software

The design TIDA-010005 has been evaluated in two different test conditions based on the input signal:

- Pace Pulse generated from function generator with variable rise time, duration and amplitude
- Pace Pulse generated from a patient simulator interface with TI's ADS129X EVM

The required hardware and software setup for both the cases have been described in the subsequent section

3.1.1 Hardware

The hardware used for evaluation of the design in both test conditions are included in the following list:

- TIDA-010005 board
- 3.3-V power supply
- MSP430FR2311 Launchpad to set the DAC thresholds through I^2C
- A function generator to make square wave with adjustable rise-time and duration
- ADS1292 Performance Demonstration Kit (ADS1292ECG-FE)

图 32 and 图 33 show the image of the top view and the bottom view of the TIDA-010005 PCB board, respectively. The dimension of the board is 35 mm X 29 mm.

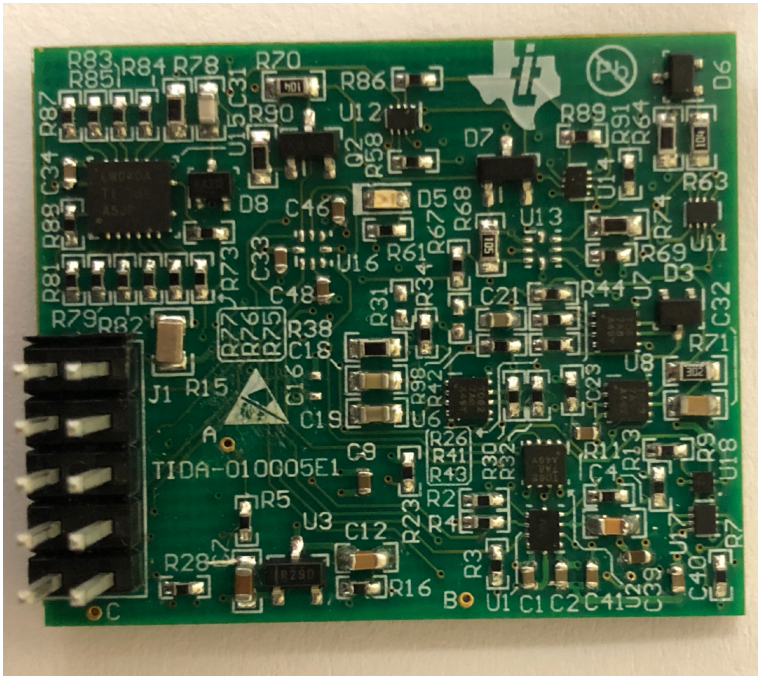


图 **32. Reference Design PCB (Top View)**

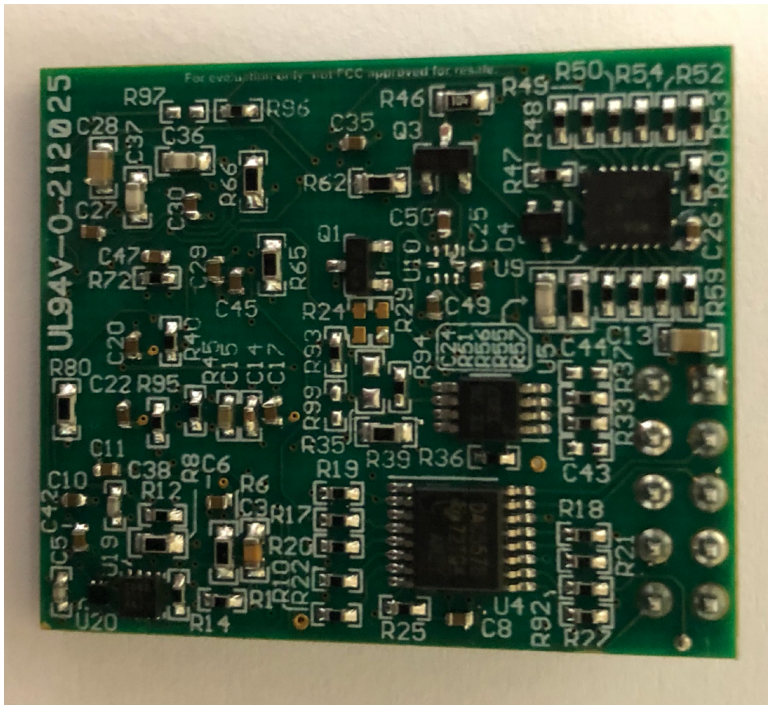


图 **33. Reference Design PCB (Bottom View)**

3.1.2 Software

The design TIDA-010005 has been designed keeping in mind that the software involvement should be minimal and at the same time it should provide maximal flexibility to the user to configure the system to be able to detect variety of pace pulse. The software to evaluate the design can be made very easily just by programming the DAC and ADC. The product folder for both the devices has extensive literature and firmware to enable the user to program the devices. We have evaluated the design on the MSP430FR2311 processor and it communicates with the onboard DAC to set the required thresholds over I^2C interface. The user can just put the thresholds and test for basic functionality. The other features of the design such as the DC and the Reset and pace-pulse output can be taken back to the processor from the input connector and the user can run his own algorithm to detect and measure pulses synchronously.

3.2 Testing and Results

3.2.1 Test Setup

图 34 shows the test setup and connections to evaluate the design with the function generator. The function generator generates the square wave having a small amplitude (order of mV) with adjustable rise-time and duration which is fed to the PGA input of the board. The gain stage amplifies the signal and the thresholds for the DAC comes from the launchpad over I^2C. The onboard circuitry measures the characteristics of the input signal and stores the corresponding data onto a sample and hold circuit which is then read by the ADC and the data can be taken back to the controller over I^2C. The pace-pulse flag signal also goes to the launchpad indicating the presence of pace pulse and the system can be reset from the RESET pin.

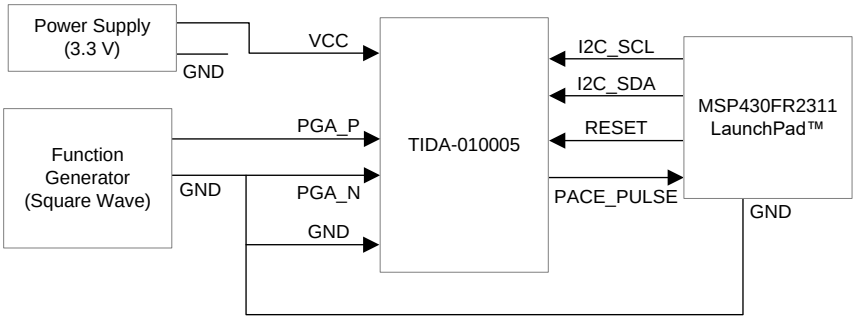


图 34. Test Setup to Evaluate the TIDA-010005 Using Function Generator

图 35 shows the test setup used to evaluate the design by interfacing the ADS1292 device. A patient simulator from Datrend is used to generate the pacemaker pulses with various characteristics. The rest of the circuitry and the functions remain the same as previously described.

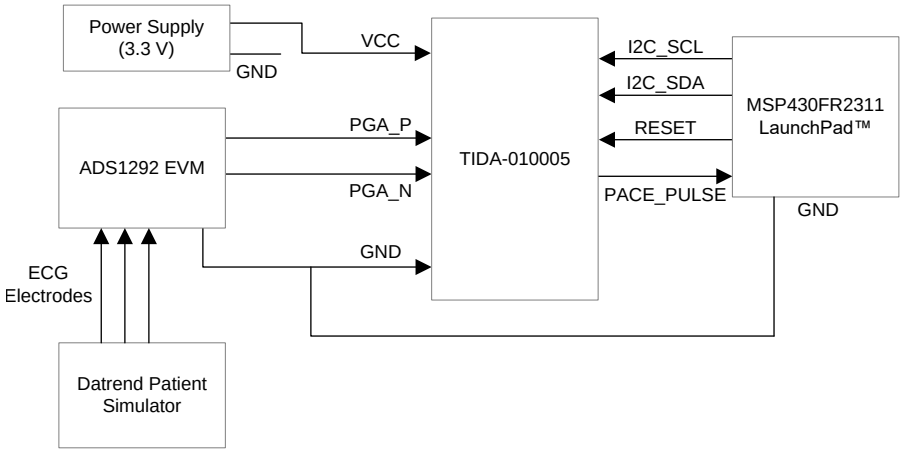


图 35. Test Setup to Evaluate the TIDA-010005 Using ADS1292 EVM and Patient Simulator

3.2.2 Test Results

3.2.2.1 Signal Processing Circuit Characterization

The signal processing section which consists of differential to single ended conversion, the filter and the gain stage has been tested with small amplitude sine wave. 图 36 shows the output of the differential to single ended conversion circuit that is output of INA317 device. The input signal is 2 kHz, 425 mV sine wave shown in green at the PGA_P pin of the input connector. The PGA_N pin is grounded. The output, shown in yellow, is the amplified version of the input with a gain approximately 2.

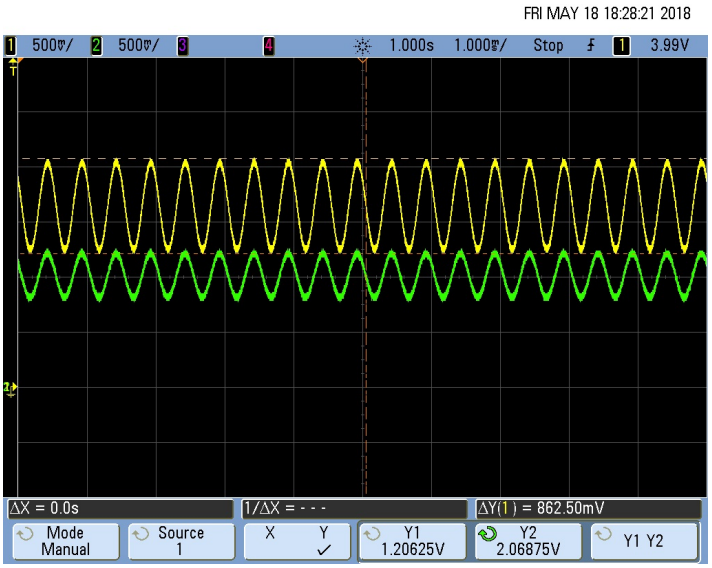


图 **36. Output Characteristics of Differential to Single-Ended Converter (INA317)**

图 37 shows the output of the gain stage (G = 101). The input signal is a 2 kHz, 40 mV sine wave shown in green at the PGAP pin of the input connector. The output (yellow waveform) is taken at the output pin of TLV9062 device at the gain stage as shown in 图 20.

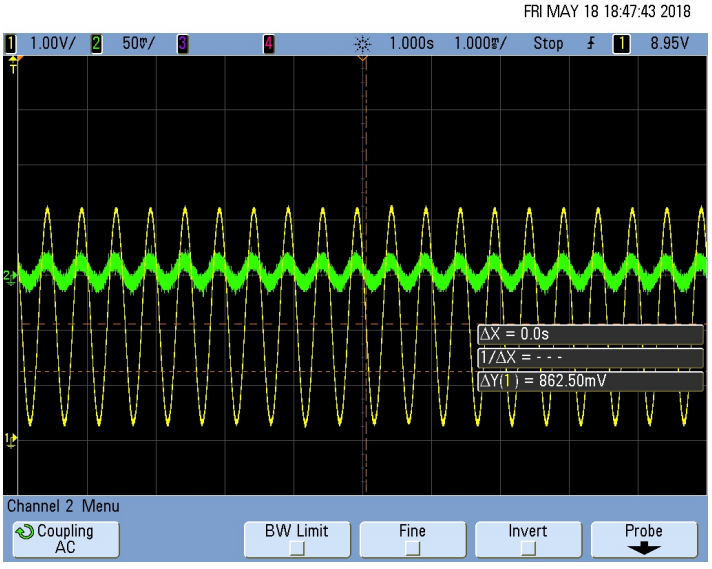


图 **37. Output Characteristics of the Gain Stage**

3.2.2.2 Interfacing ADS1292 With TIDA-010005

The design has been evaluated with ADS1292 device's EVM as a front-end for the ECG signal. 图 35 shows the test setup for the interface between the reference design and the ADS1292. The source signal is taken from a patient simulator and 图 38 shows the 5 mV ECG output at the gain stage.

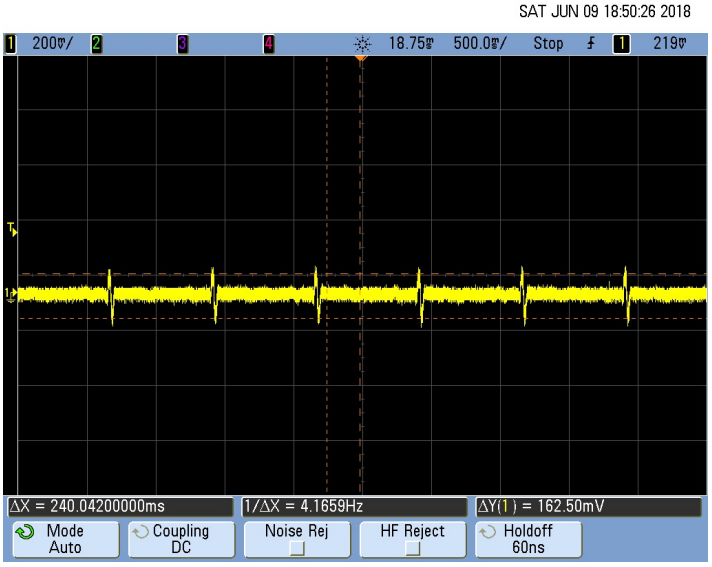


图 38. 5 mV ECG Signal at the Output of the Gain Stage Interfaced With ADS1292

图 39 and 图 40 show the images of the 16 mV pace signal at 70 bpm from the patient simulator after being processed by the signal processing section at the output of the gain stage.图 41 shows the negative pace signal with the same attributes as previously described.

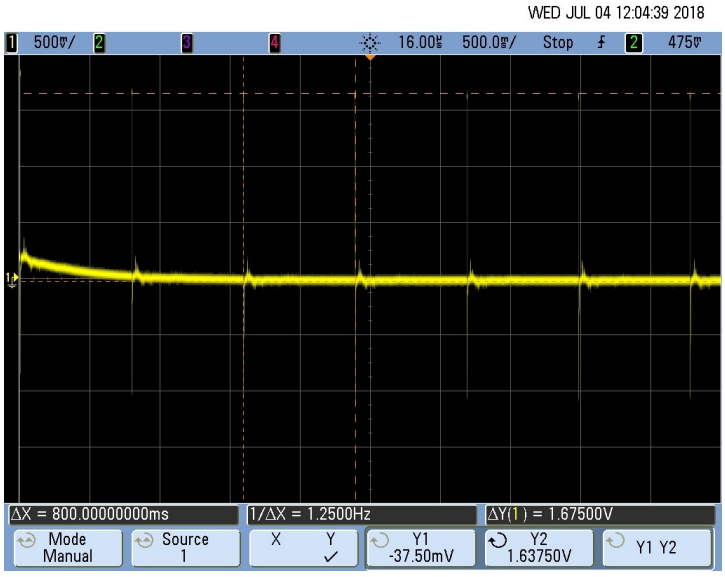


图 39. 16-mV Pace Signal 5 at the Output of the Gain Stage Interface With ADS1292

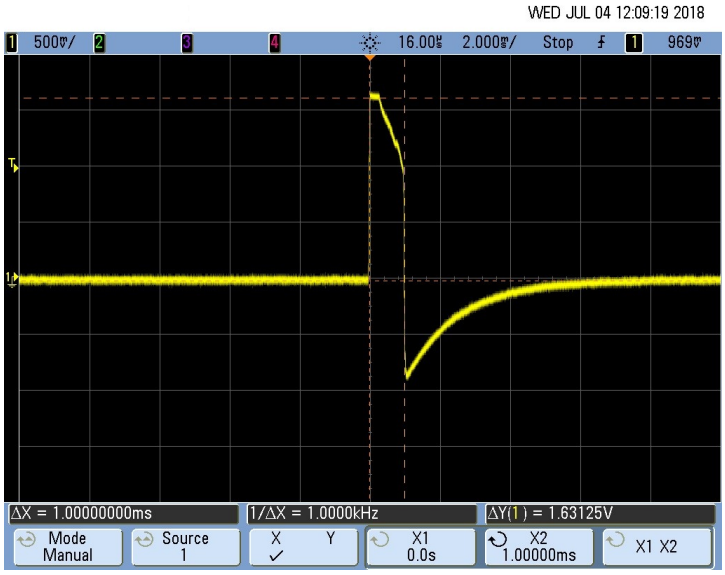


图 **40. Zoomed in Image of the Pace Signal**

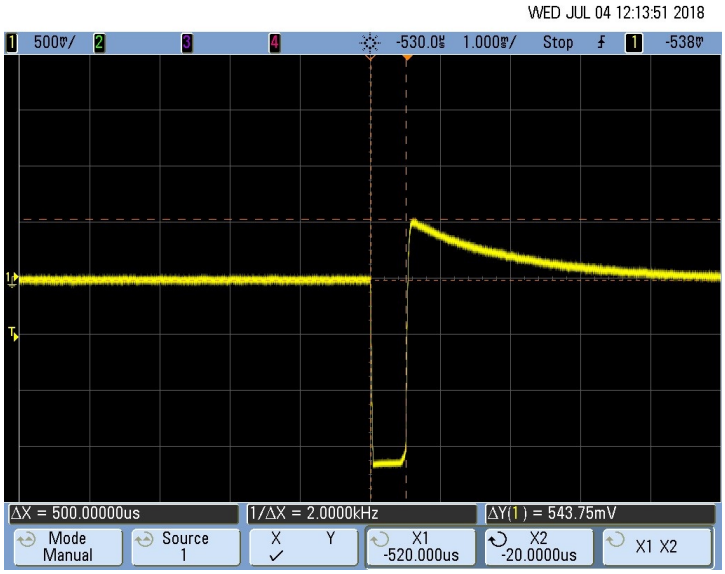


图 **41. Negative Pace Signal From the Patient Simulator Interfaced With ADS1292**

3.2.2.3 Test Results With Signal Generator

图 42 shows the waveform obtained from the evaluation of the reference design using the simulated pace signal generated from a signal generator. The waveform in yellow is the amplified signal at the gain stage output. The waveform in purple is the corresponding rise time measurement counter's analog output (staircase waveform) at the junction of the summing resistors shown in 图 27. As shown in 图 42, the system measures the rise time of the waveform which is 150 µs in this case and the equivalent analog voltage is 860 mV which is further sent to the window comparator.

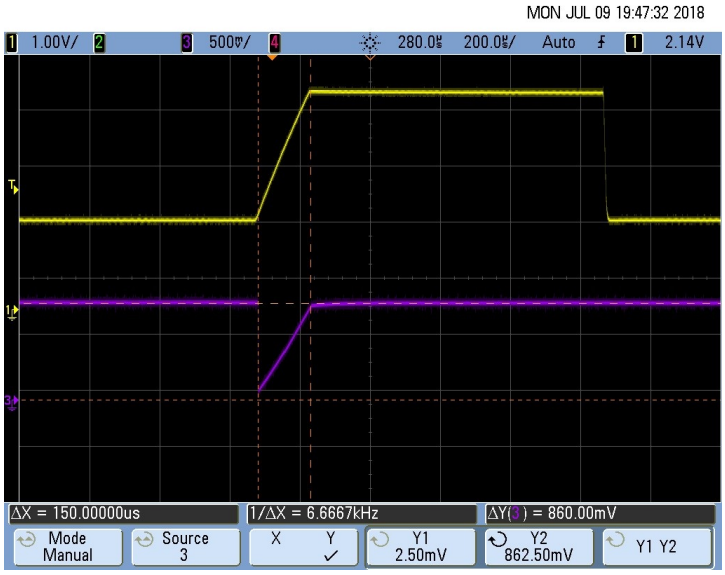


图 **42. Rise Time Measurement of the Pace Signal (T_R = 150 µs)**

图 43 to 图 46 show the similar measurements for different rise times (T_R) that is 100 us, 40 us, 20 us and 10 us respectively. The corresponding analog voltage for the same are 570 mV, 285 mV, 122.5 mV and 60 mV respectively. The waveforms in green and pink are duration counter's output and pace-pulse flag which can be ignored for the purpose of this section. The graph in 图 47 shows the tabulated output equivalent analog voltage of the counter vs the rise time.

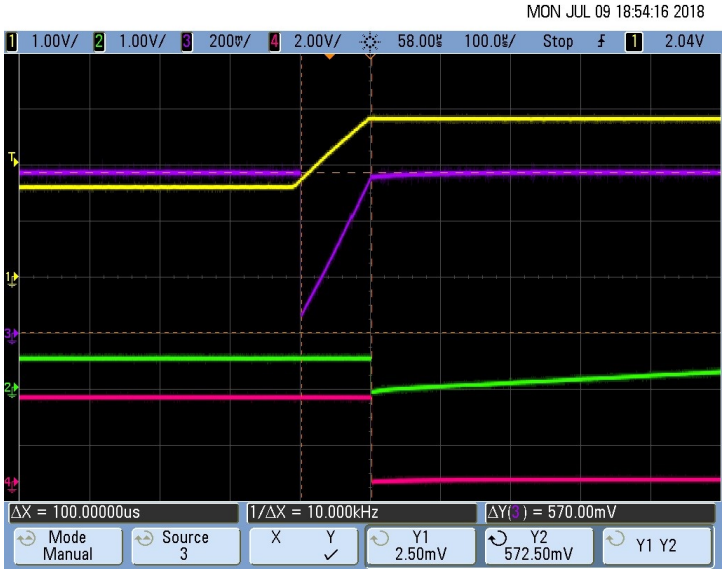


图 **43. Rise Time Measurement of the Pace Signal (T_R = 100 µs)**

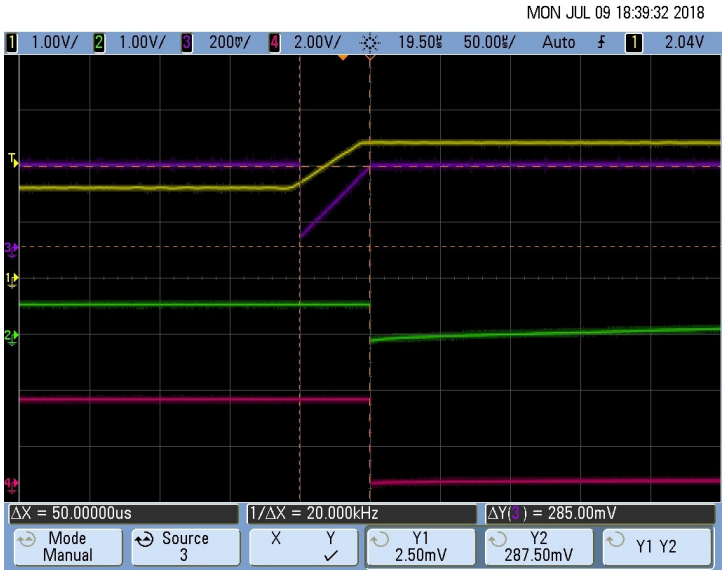


图 44. Rise Time Measurement of the Pace Signal (T_R = 50 µs)

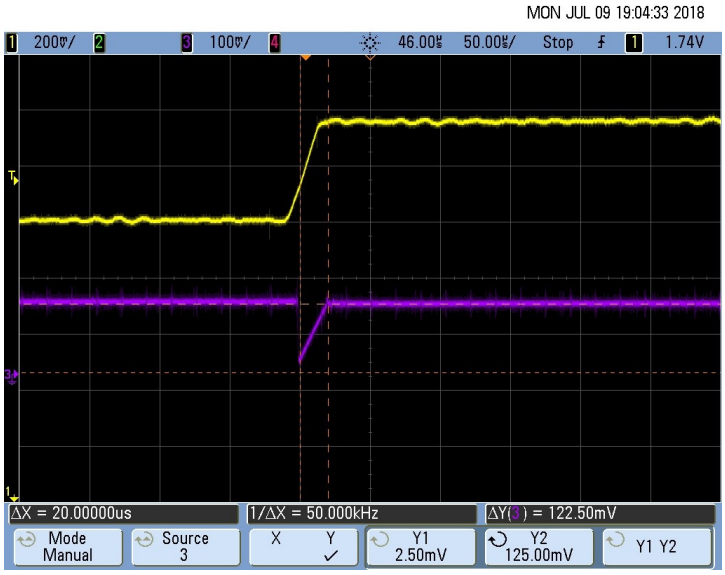


图 45. Rise Time Measurement of the Pace Signal (T_R = 20 µs)

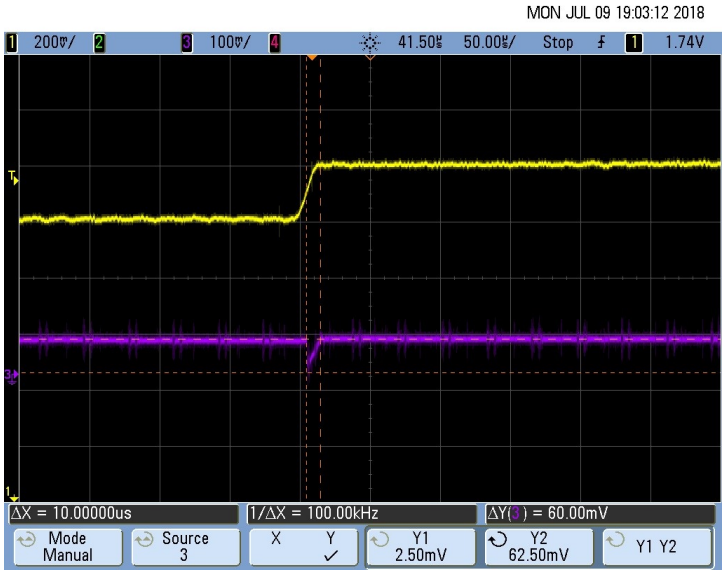


图 **46. Rise Time Measurement of the Pace Signal (T_R = 10 µs)**

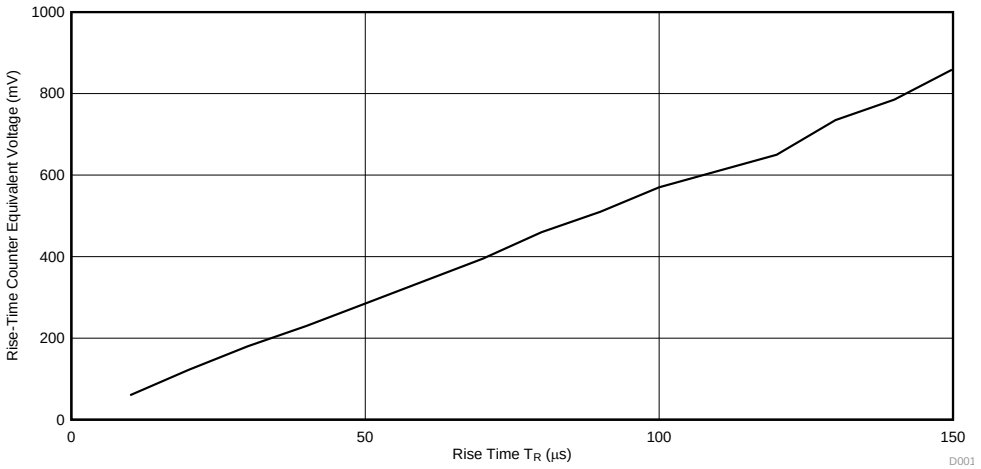


图 **47. Equivalent Analog Voltage of the Rise Time Counter (mV) vs the Rise Time T_R (µs)**

图 48 to 图 51 show the similar measurement performed to measure the duration of the pace pulse. The waveform in yellow is the input pace pulse, the purple waveform shows the rise time measurement, and the green waveform is the output of the pace duration counter's summing resistors as shown in schematics in 图 27. The waveform in pink is the pace detect flag. Note that the DAC thresholds in these measurements are chosen such that the individual counter's output lies between them. Essentially implying the presence of a valid pace pulse.

图 48 to 图 51 show the measurement performed to measure the duration of the pulse which is 0.5 ms, 1 ms, 2 ms and 2.5 ms respectively. The equivalent analog voltage at the input of the duration window comparator are 340 mV, 631.25 mV, 1.29 V and 1.64 V respectively. The graph in 图 52 shows the tabulated output equivalent analog voltage of the pulse duration counter vs the pulse duration.

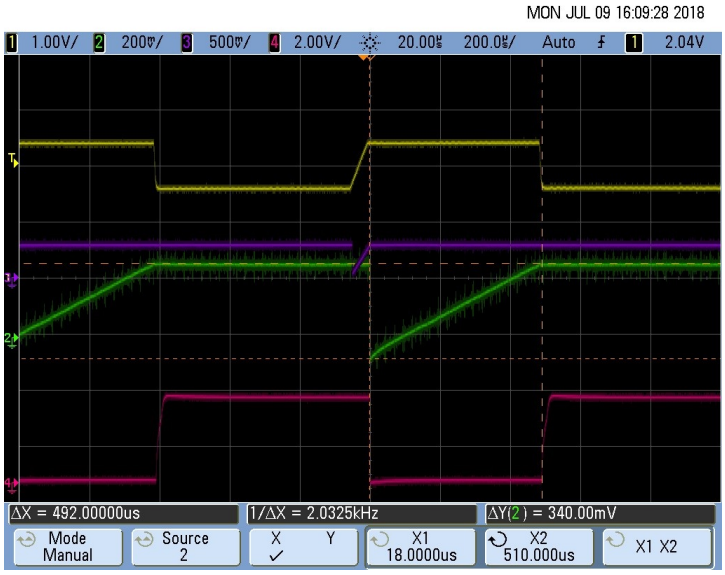


图 **48. Pulse Duration Measurement of the Pace Pulse (T_D = 0.5 ms)**

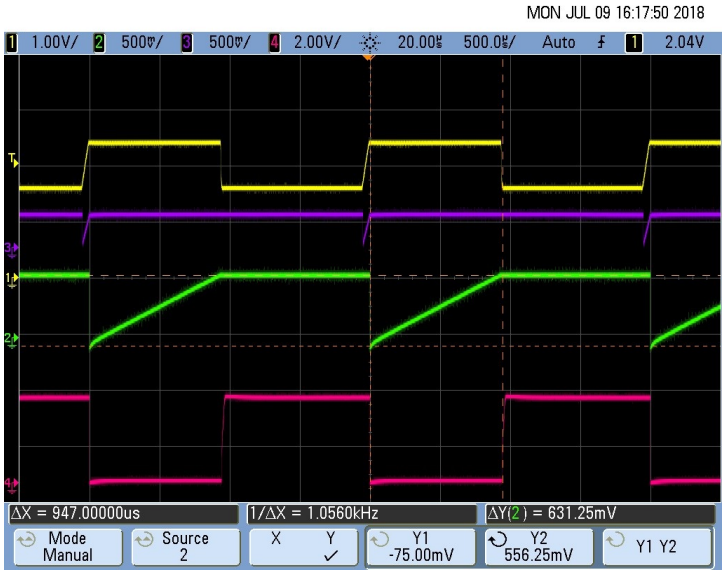


图 **49. Pulse Duration Measurement of the Pace Pulse (T_D = 1 ms)**

图 **50. Pulse Duration Measurement of the Pace Pulse (T_D = 2 ms)**

图 **51. Pulse Duration Measurement of the Pace Pulse (T_D = 2.5 ms)**

图 52. Equivalent Analog Voltage of the Pulse Duration Counter (mV) vs the Pulse Duration T_D (ms)

3.2.2.4 Clocking and DAC Communication Results

图 53 and 图 54 show the output of the Schmitt Trigger Inverter implemented as a clock input to the system as described in 节 2.3.8. The measured time period of CLK A is 570 ns and the measured time period of CLK B is 1.24 us. Hence the clock frequencies are 1.75 MHz and 806 kHz for CLK A and CLK B respectively.

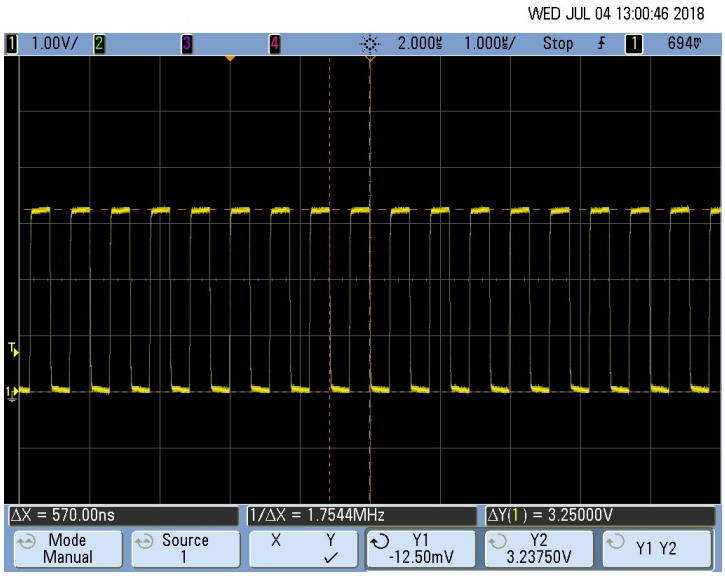


图 53. Clock (CLK A) Input to Rise Time Counter

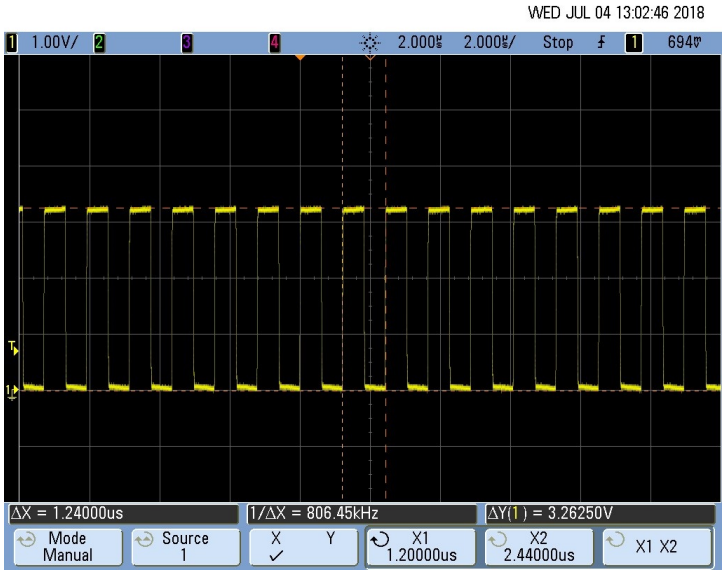


图 **54. Clock (CLK B) Input to the Pulse Duration Counter**

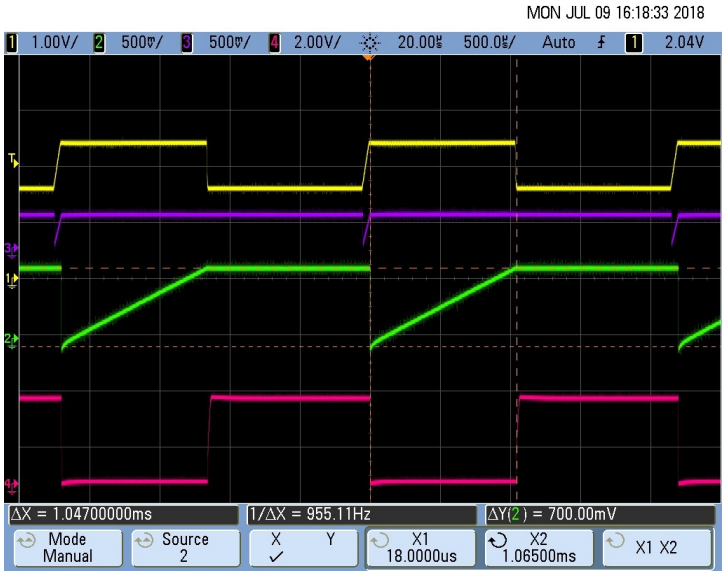


图 **55. Pacemaker Detection Output for 8-mV, 100-µs Pace Pulse**

3.2.2.5 Test Results With ADS1292

The reference design has been evaluated with a patient simulator simulating the pace pulses which has been sent to the pacemaker detection board through the TI ADS1292 EVM, which is an analog front-end for ECG applications. 节 3.2.2.2 and 图 35 describes the interfacing in detail. The pace signal which is getting measured by the circuitry has a fixed rise time of approximately 38 µs (it includes the delay due to various filtering stages implemented in the design). The design has been evaluated for the amplitude and duration variations from 8 mV to 700 mV and 100 us to 2 ms respectively. The following subsections depict the measurement waveforms for various amplitudes of the input pace pulse.

3.2.2.5.1 Test Results for Pulse Amplitude of 8 mV

图 56 to 图 63 show the output waveform for a pace amplitude of 8 mV for various durations. The waveform in yellow is the amplified pace signal, green waveform depicts the rise time counter's equivalent analog voltage, purple waveform shows the pulse duration counter's analog voltage and pink waveform shows the pace detect flag. Note that the DAC thresholds are set such that the incoming pace pulse is a valid pace pulse.

图 56 and 图 57 show the output waveforms for 8 mV, 100 µs pace pulse with measured rise time of 58 µs (equivalent voltage 412.5 mV) and pulse duration of 76 µs (equivalent voltage 62.5 mV). Note that duration is less than 100 µs simply because the rise time is not added to it. In this case the rise time is comparable to the duration.

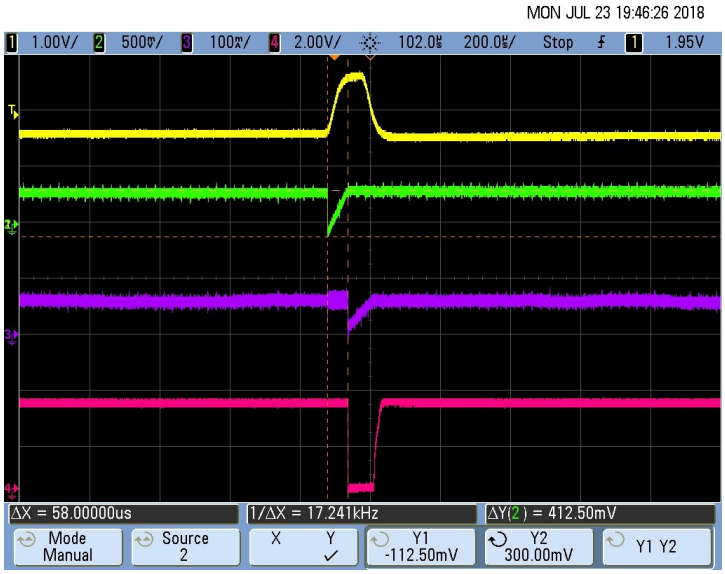


图 56. Pacemaker Detection Output (Rise Time T_R) for 8-mV, 100-µs Pace Pulse

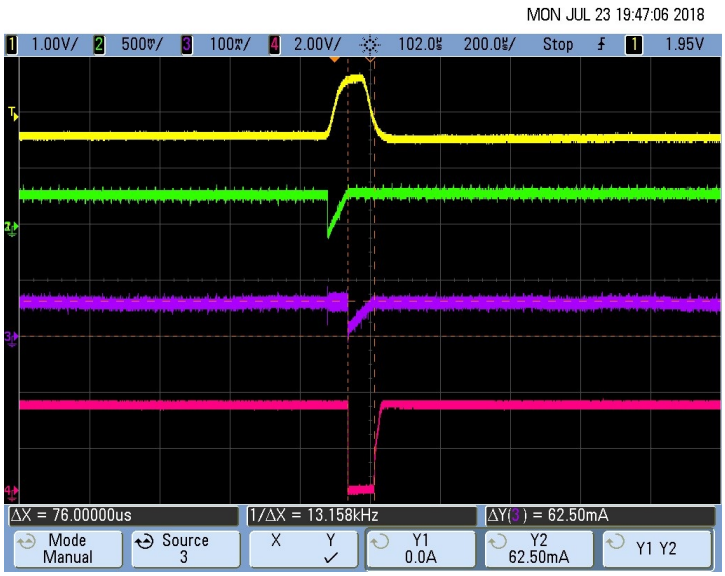


图 57. Pacemaker Detection Output (Pulse Duration T_D) for 8-mV, 100-µs Pace Pulse

图 58 and 图 59 show the output waveforms for 8-mV, 200-µs pace pulse with measured rise time of 56 µs (equivalent voltage 418.75 mV) and pulse duration of 172 µs (equivalent voltage 127.5 mV). Note that duration is less than 200 µs simply because the rise time is not added to it

图 58. Pacemaker Detection Output (Rise Time T_R) for 8-mV, 200-µs Pace Pulse

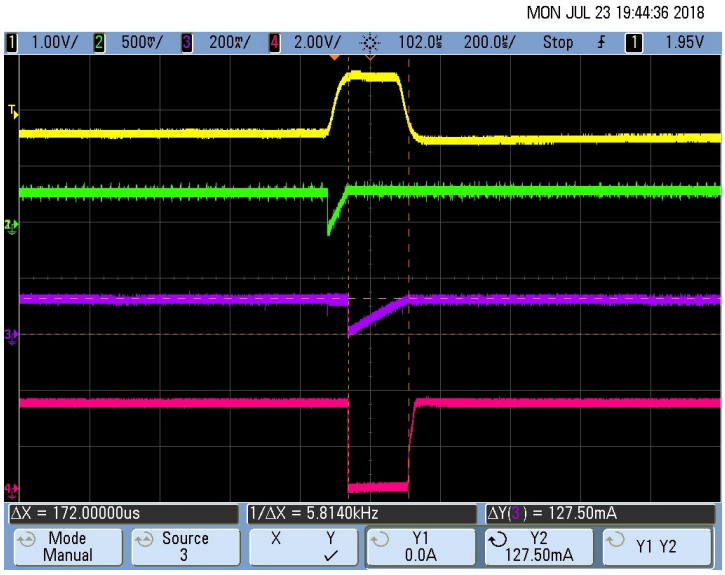


图 59. Pacemaker Detection Output (Pulse Duration T_D) for 8-mV, 200-µs Pace Pulse

图 60 and 图 61 show the output waveforms for 8-mV, 500-µs pace pulse with measured rise time of 55 µs (equivalent voltage 375 mV) and pulse duration of 465 µs (equivalent voltage 318.75 mV). Note that duration is less than 500 µs simply because the rise time is not added to it

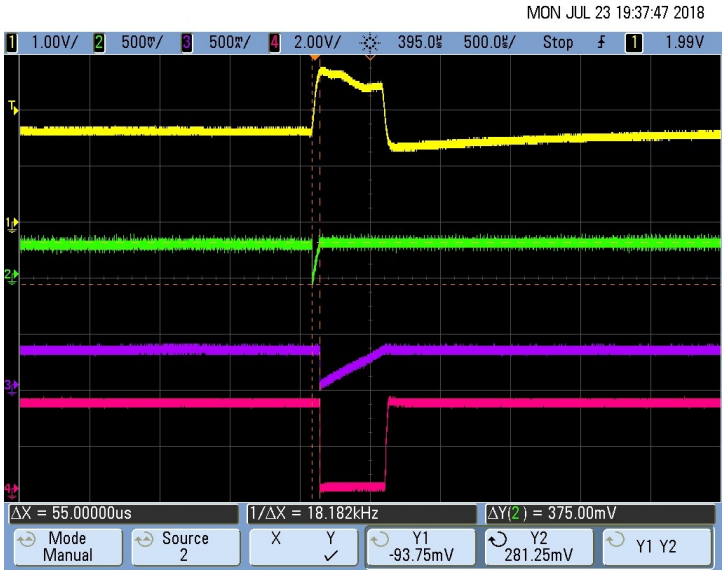


图 **60. Pacemaker Detection Output (Rise Time T_R) for 8-mV, 500-µs Pace Pulse**

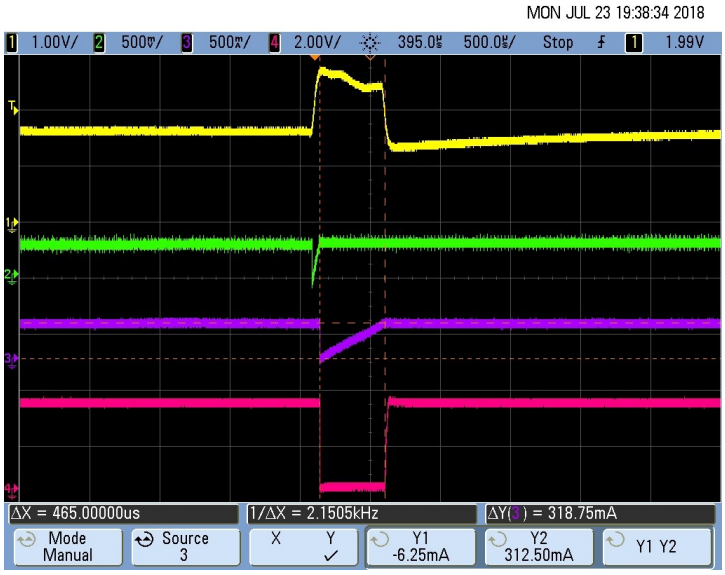


图 **61. Pacemaker Detection Output (Pulse Duration T_D) for 8-mV, 500-µs Pace Pulse**

图 62 and 图 63 show the output waveforms for 8-mV, 1-ms pace pulse with measured rise time of 54 µs (equivalent voltage 381.25 mV) and pulse duration of 960 µs (equivalent voltage 643.75 mV). Note that duration is less than 1000 µs simply because the rise time is not added to it

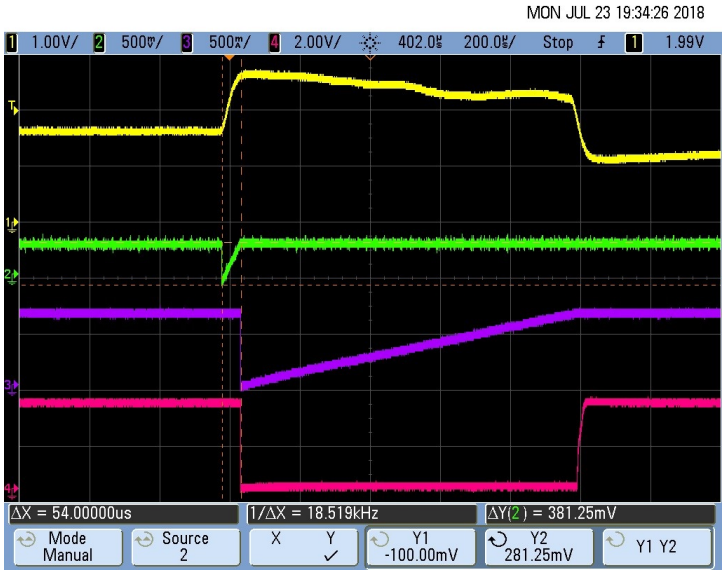


图 62. Pacemaker Detection Output (Rise Time T_R) for 8-mV, 1-ms Pace Pulse

图 63. Pacemaker Detection Output (Pulse Duration T_D) for 8-mV, 1-ms Pace Pulse

3.2.2.5.2 Test Results for Pulse Amplitude of 16 mV

图 64 to 图 73 show the output waveform for a pace amplitude of 16 mV for various durations.

图 64 and 图 65 show the output waveforms for 16-mV, 100-µs pace pulse with measured rise time of 38 µs (equivalent voltage 281.25 mV) and pulse duration of 107 µs (equivalent voltage 85 mV).

图 **64. Pacemaker Detection Output (Rise Time T_R) for 16-mV, 100-µs Pace Pulse**

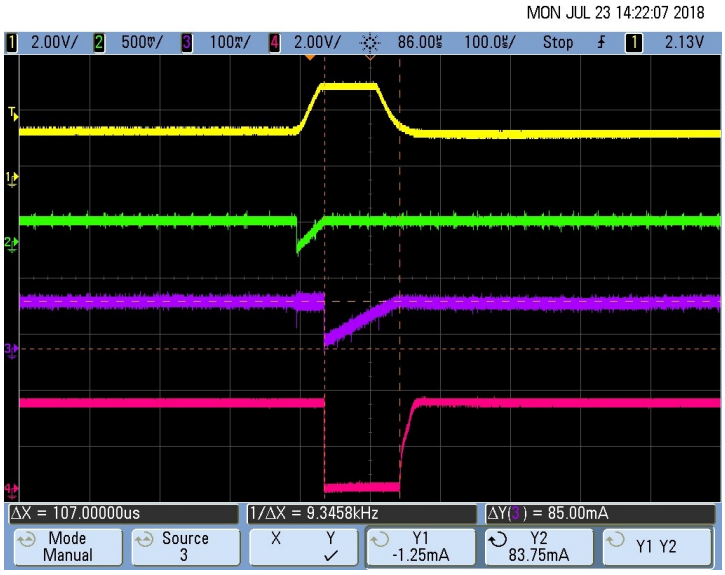


图 **65. Pacemaker Detection Output (Pulse Duration T_D) for 16-mV, 100-µs Pace Pulse**

图 66 and 图 67 show the output waveforms for 16-mV, 200-µs pace pulse with measured rise time of 40 µs (equivalent voltage 275 mV) and pulse duration of 200 µs (equivalent voltage 175 mV).

图 **66. Pacemaker Detection Output (Rise Time T_R) for 16-mV, 200-µs Pace Pulse**

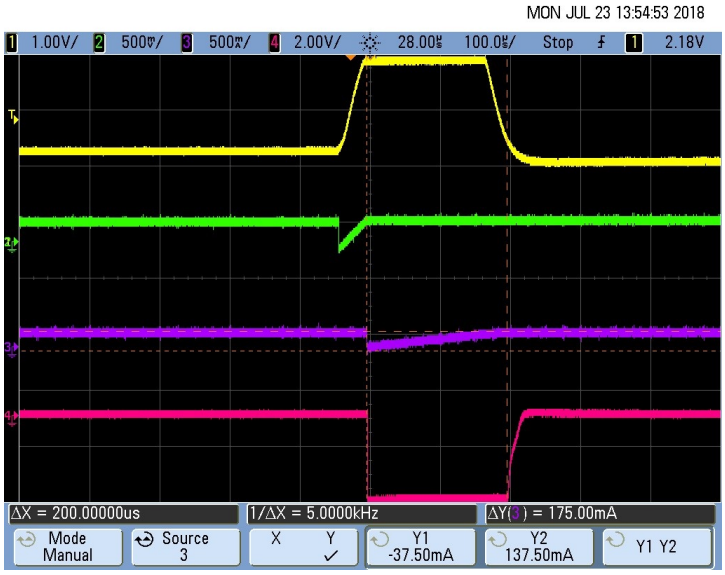


图 **67. Pacemaker Detection Output (Pulse Duration T_D) for 16-mV, 200-µs Pace Pulse**

图 68 and 图 69 show the output waveforms for 16-mV, 500-µs pace pulse with measured rise time of 38 µs (equivalent voltage 287.5 mV) and pulse duration of 500 µs (equivalent voltage 381.25 mV).

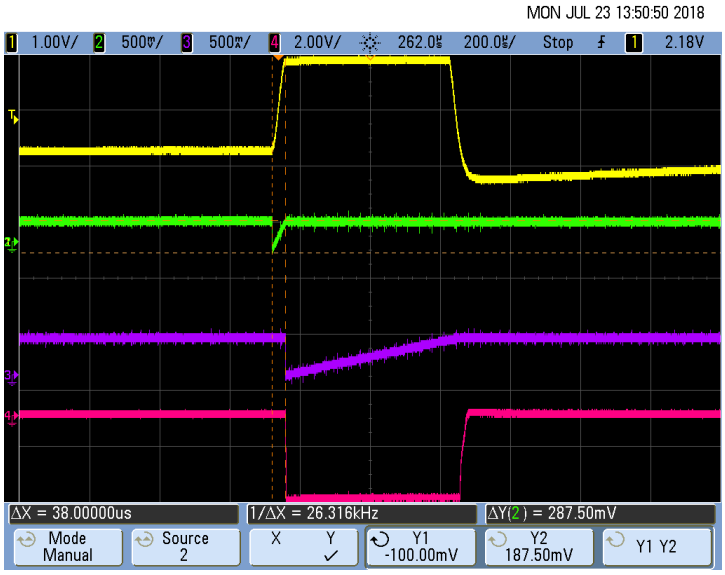


图 **68. Pacemaker Detection Output (Rise Time T_R) for 16-mV, 500-µs Pace Pulse**

图 **69. Pacemaker Detection Output (Pulse Duration T_D) for 16-mV, 500-µs Pace Pulse**

图 70 and 图 71 show the output waveforms for 16 mV, 1 ms pace pulse with measured rise time of 38 µs (equivalent voltage 287.5 mV) and pulse duration of 990 µs (equivalent voltage 687.5 mV).

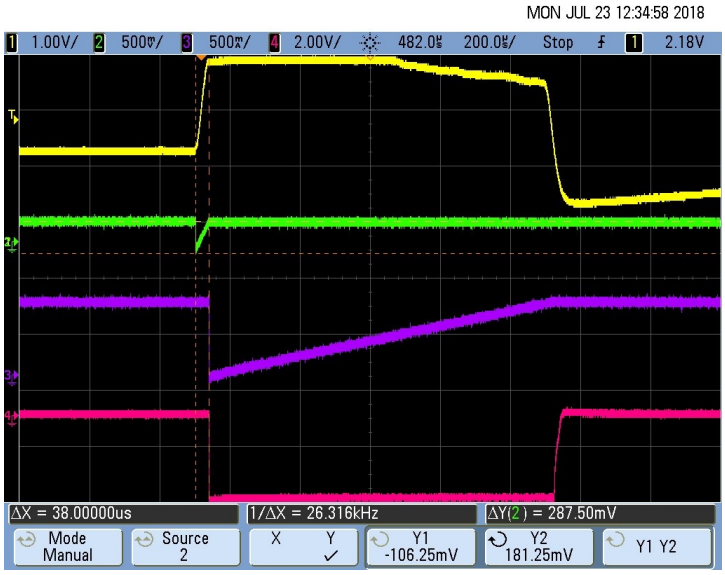


图 **70. Pacemaker Detection Output (Rise Time T_R) for 16-mV, 1-ms Pace Pulse**

图 **71. Pacemaker Detection Output (Pulse Duration T_D) for 16-mV, 1-ms Pace Pulse**

图 72 and 图 73 show the output waveforms for 16-mV, 2-ms pace pulse with measured rise time of 35 µs (equivalent voltage 281.5 mV) and pulse duration of 1.98 ms (equivalent voltage 1.35 V).

图 **72. Pacemaker Detection Output (Rise Time T_R) for 16 mV, 2 ms Pace Pulse**

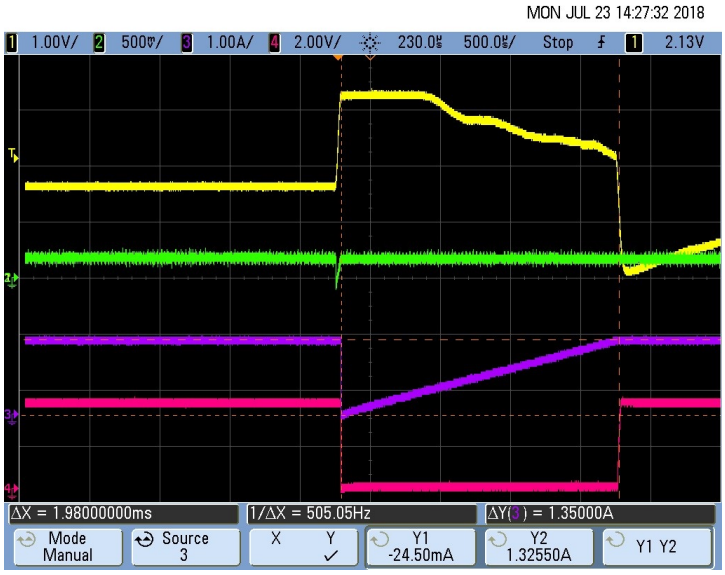


图 **73. Pacemaker Detection Output (Pulse Duration T_D) for 16 mV, 2 ms Pace Pulse**

3.2.2.5.3 Test Results for Pulse Amplitude of 50 mV, 500 mV and 700 mV

图 74 to 图 76 show the output waveform for a pace amplitude of 50 mV with pulse duration of 1 ms and 2 ms. The measured Rise Time is 18 µs (equivalent voltage 110 mV) and pulse duration 1.035 ms (equivalent voltage 725 mV) in 图 75 and 2.03 ms (equivalent voltage 1.3625 V) in 图 76

It is important to note that for pace amplitude greater than 16 mV, due to the 100 × gain in the system the output of the gain stage will saturate to the supply as the following images show. This will considerably reduce the rise time of the pace pulse since the voltage cannot go beyond the supply. The system still detects the pace pulse provided appropriate DAC thresholds for the Rise Time is applied.

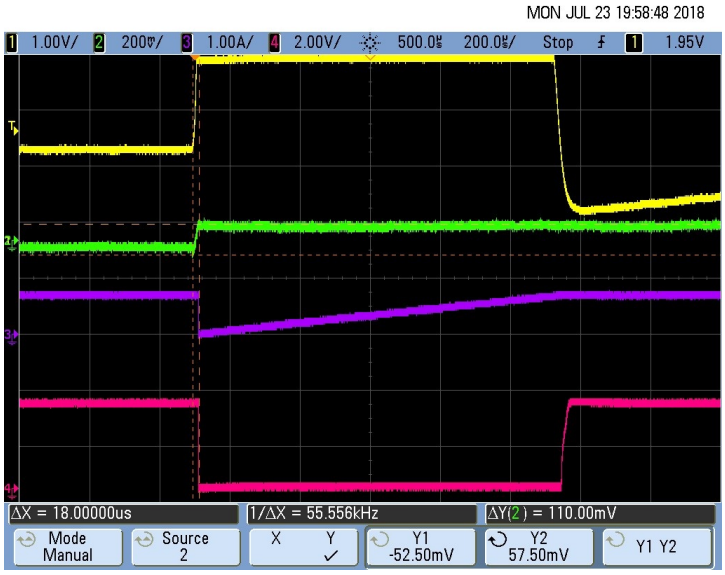


图 74. Pacemaker Detection Output (Rise Time T_R) for 50-mV, 1-ms Pace Pulse

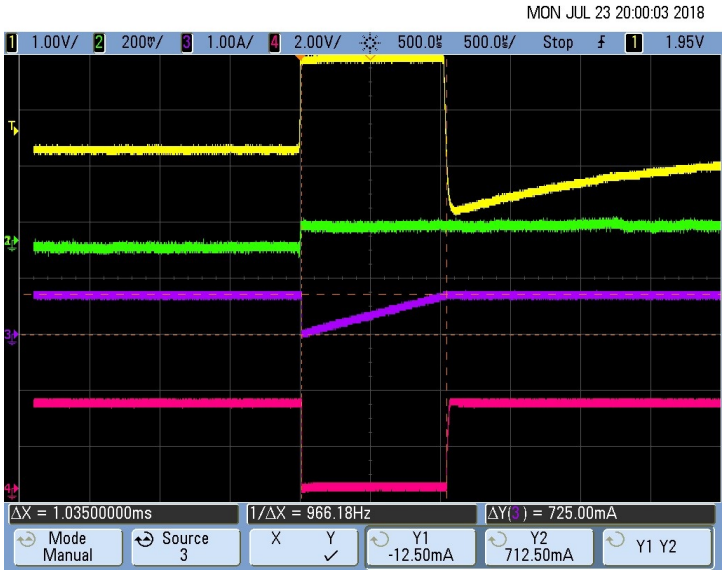


图 75. Pacemaker Detection Output (Pulse Duration T_D) for 50-mV, 1-ms Pace Pulse

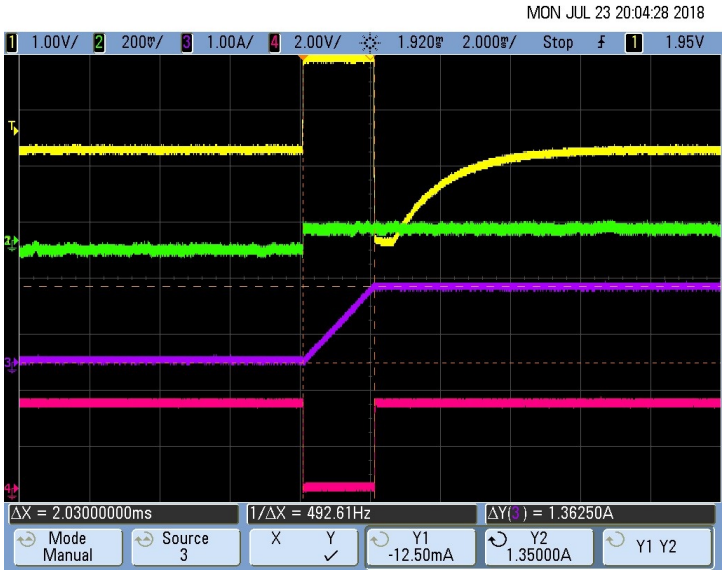


图 **76. Pacemaker Detection Output (Pulse Duration T_D) for 50-mV, 2-ms Pace Pulse**

图 77 and 图 78 show the output waveforms for a pace amplitude of 500 mV with pulse duration of 1 ms and 2 ms. The measured pulse duration is 1.035 ms (equivalent voltage 750 mV) and 2.03 ms (equivalent voltage 1.4125 V) respectively.

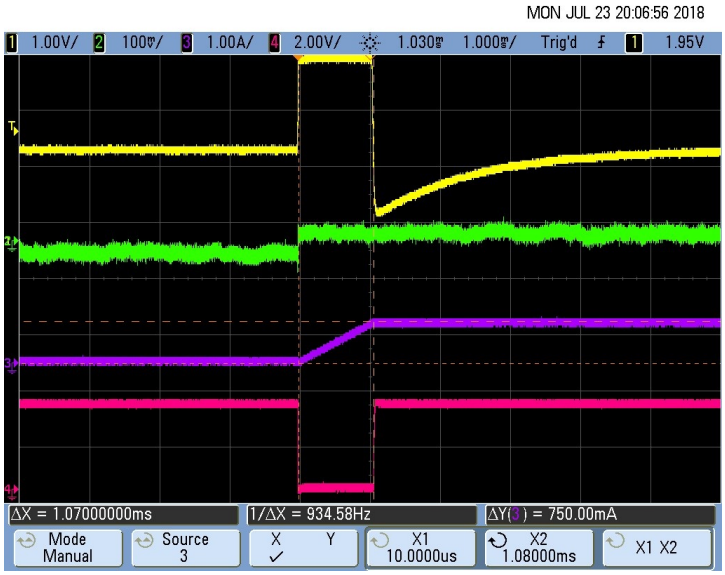


图 **77. Pacemaker Detection Output (Pulse Duration T_D) for 500-mV, 1-ms Pace Pulse**

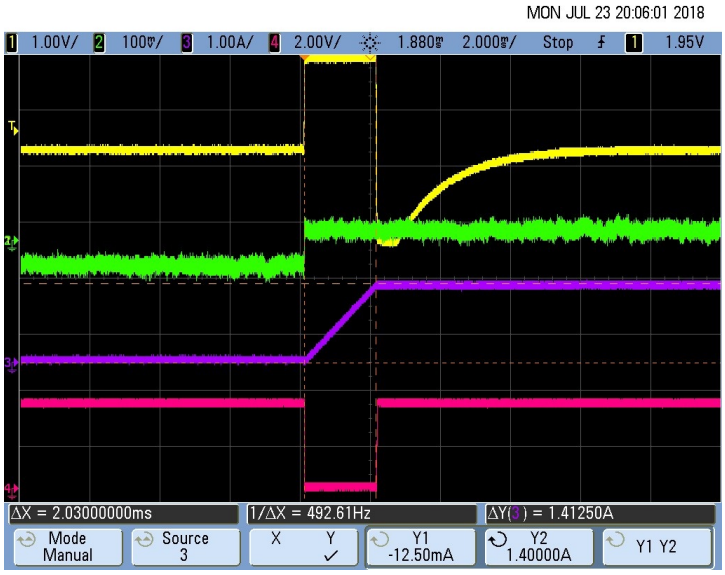


图 **78. Pacemaker Detection Output (Pulse Duration T_D) for 500-mV, 2-ms Pace Pulse**

图 79 and 图 80 show the output waveforms for a pace amplitude of 700 mV with pulse duration of 1 ms and 2 ms. The measured pulse duration is 1.07 ms (equivalent voltage 750 mV) and 2.05 ms (equivalent voltage 1.4 V) respectively.

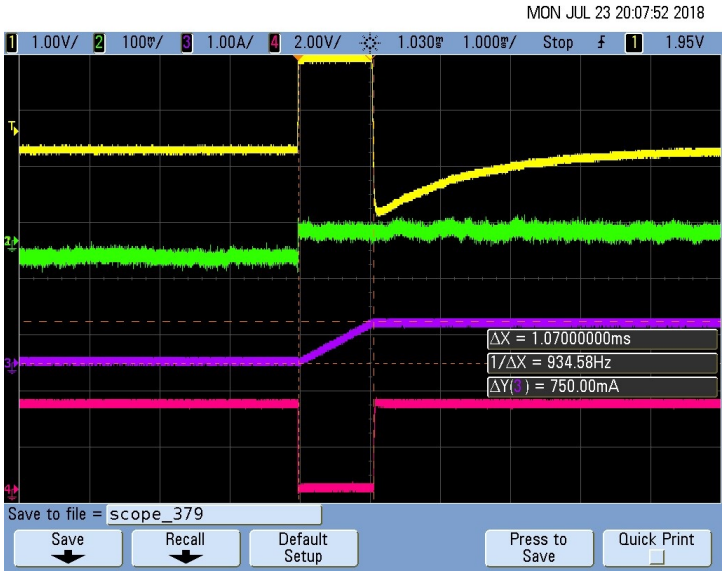


图 **79. Pacemaker Detection Output (Pulse Duration T_D) for 700-mV, 1-ms Pace Pulse**

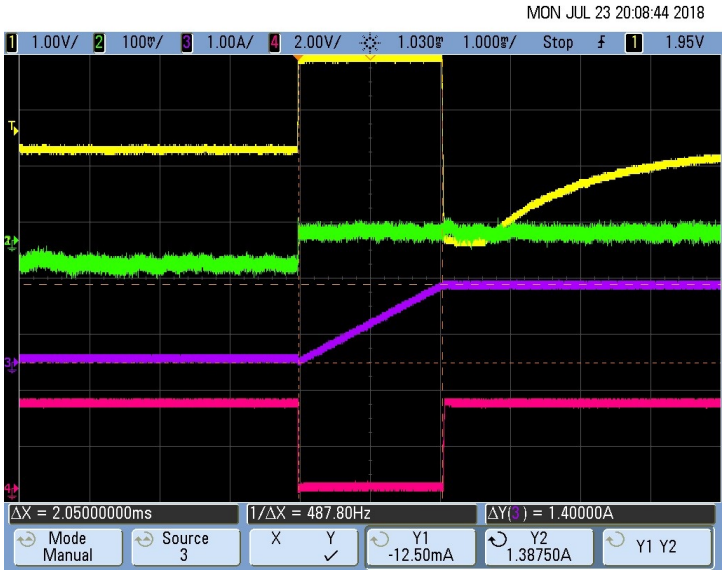


图 **80. Pacemaker Detection Output (Pulse Duration T_D) for 700-mV, 2-ms Pace Pulse**

3.2.2.5.4 Test Result for Negative Pace Pulse

The design TIDA-010005 provides user the flexibility to detect negative-going pace signal just by setting the DAC's Polarity Check output High. As discussed in 节 2.3.6, the polarity check operation is provided in the design by programming the DAC's channel 6 (Polarity Check Output) High. This will essentially convert the negative pace signal into positive one in the hardware and the further measurements are performed using the processed inverted (positive) signal. Thus the thresholds will always be positive and the same thresholds will work which were there if the signal were positive.

图 81 shows the negative pace signal (yellow) as the input to the system and the polarity check is not activated. Thus the rise time counter counts the falling edge of the signal (green) and pulse counter (purple) measure the signal according to the amplitude threshold as shown in the diagram. However, since the other thresholds and negative polarity check is not there the output of the polarity flag does not recognize it as a valid pace signal (pink).

图 82 shows the same signal sent to the system, but the polarity check is activated and the system recognizes the Pace Signal and the Pace Pulse Flag shows the rising edge indicating the presence of a valid pace signal.

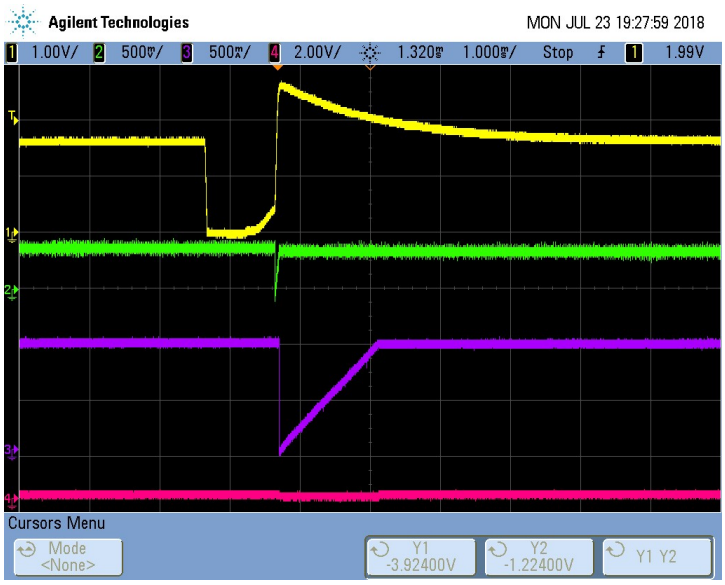


图 **81. Negative Pace Signal Detection - Negative Pace Pulse Undetected**

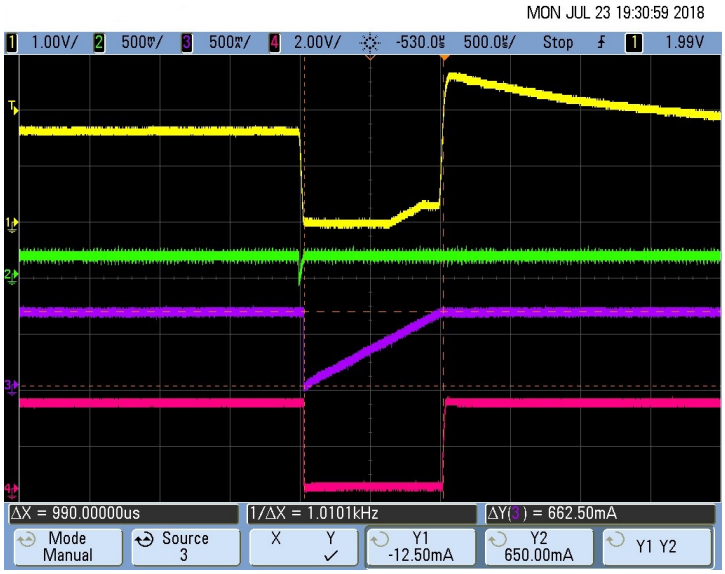


图 **82. Negative Pace Signal Detection - Negative Pace Pulse Detected by setting the Polarity Check (CH-6) Output of the DAC Low`**

3.2.2.6 Thermal Images of the Board

图 83 and 图 84 show the thermal images of the top and bottom sections of the board TIDA-010005 respectively.

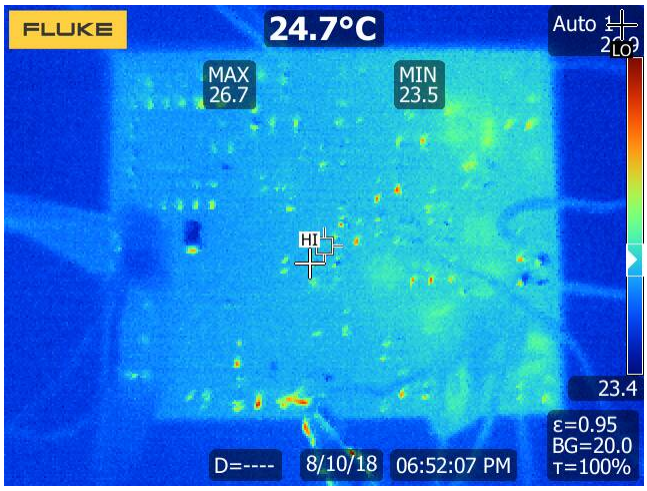


图 **83. Thermal Image of the Top Section of TIDA-010005**

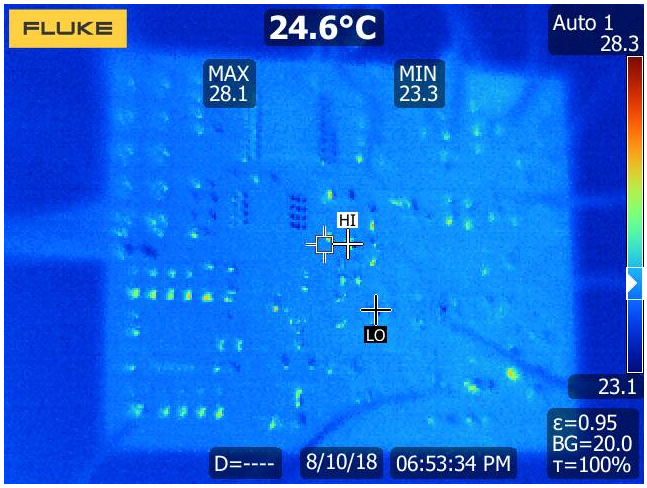


图 **84. Thermal Image of the Bottom Section of TIDA-010005**

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010005.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010005.

4.3 PCB Layout Recommendations

Find device-specific layout guidelines for each individual TI device used in this reference design in the corresponding data sheets.图 32 and 图 33 show the top and the bottom views of the reference design PCB, respectively.

4.3.1 Ground and Power Planes

图 85 shows the ground plane on the middle layer 1 (referred to as the GND layer) and 图 86 shows the power plane on the middle layer 2 (referred to as the PWR layer) on the reference design board.

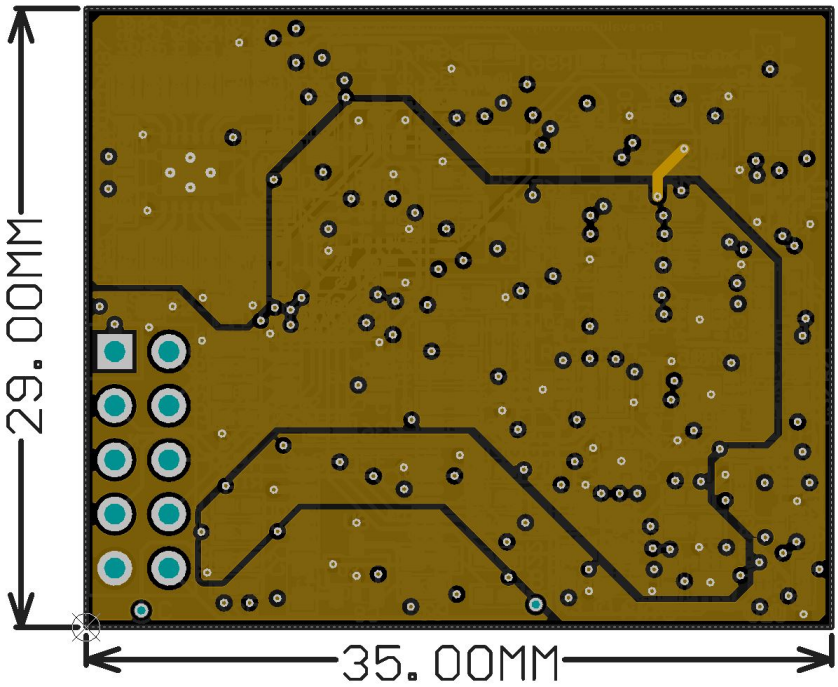


图 **85. Ground Planes of the Reference Design Board**

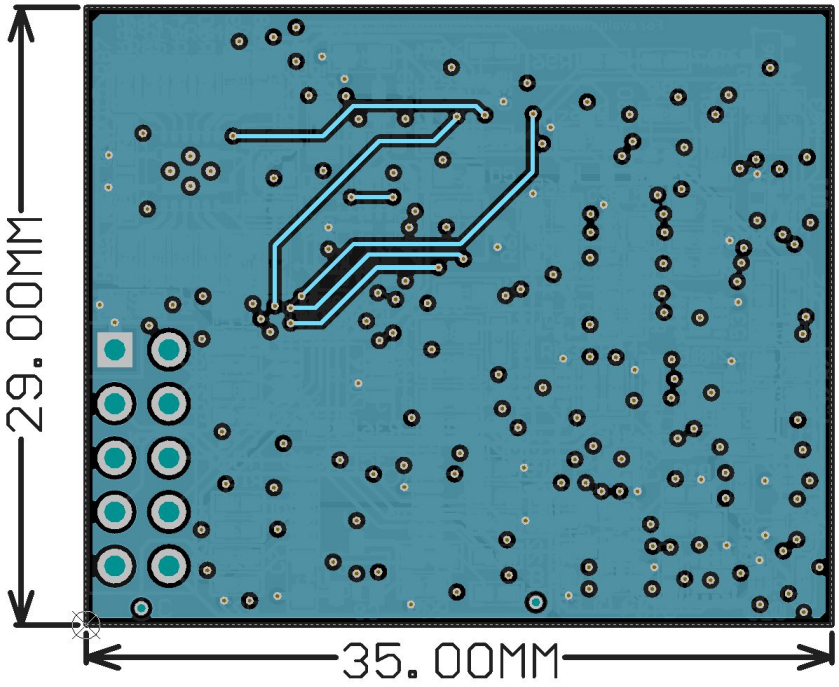


图 **86. Power Plane of the Reference Design Board**

4.3.2 Top and Bottom Layers

图 85 shows the top layer of the reference design board and 图 86 shows the bottom layer of the reference design board.

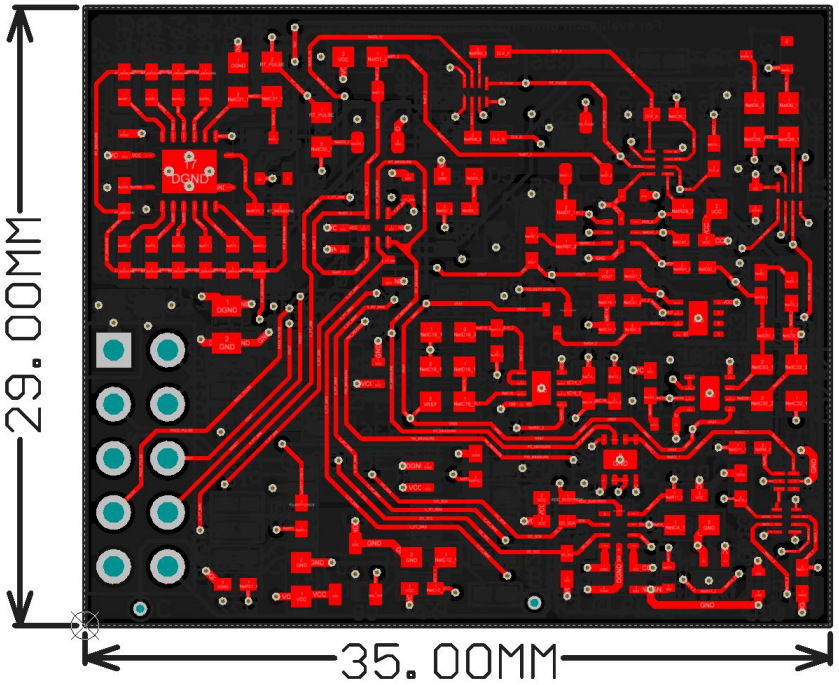


图 **87. Top Layer of the Reference Board**

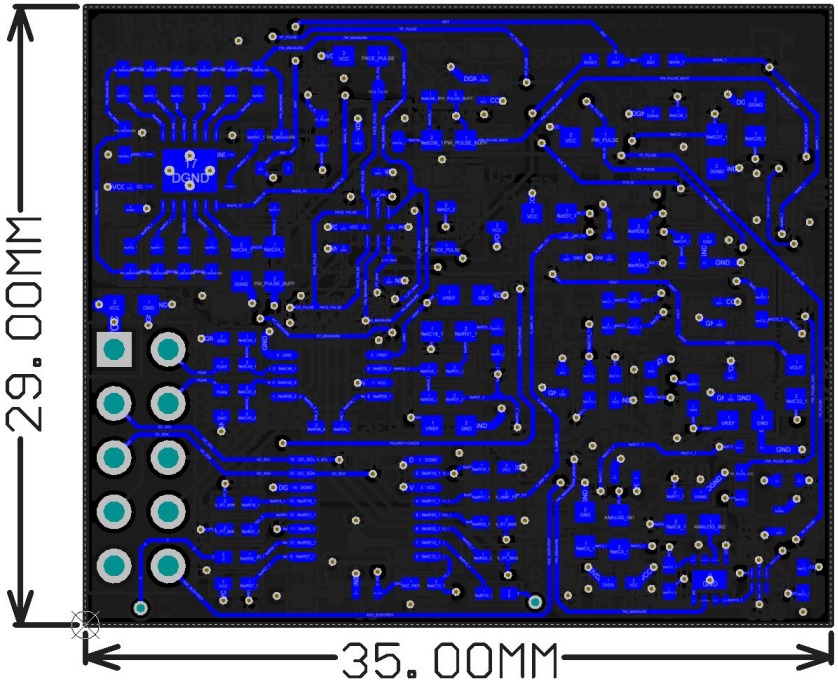


图 **88. Bottom Layer of the Reference Board**

4.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-010005.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010005.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010005.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010005.

5 Software Files

To download the software files, see the design files at TIDA-010005.

6 Related Documentation

1. Texas Instruments, *Hardware Pace using Slope Detection*
2. Texas Instruments, *Software Pacemaker Detection Reference Design*

6.1 Trademarks

6.1.1 商标

7 About the Author

ABHISHEK VISHWA is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Medical Healthcare and Fitness sector. Abhishek joined TI in July 2017. Abhishek brings to this role his experience in analog design, mixed signal design, industrial interfaces, and power supplies. Abhishek completed his B. Tech in Electrical Engineering and M. Tech in Microelectronics from IIT Bombay.

SANJAY DIXIT is a system architect in the Industrial Systems-Medical Healthcare and Fitness Sector at Texas Instruments where he is responsible for specifying reference designs

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