TI Designs：TIDA-01392
具有高达 100MHz PCLK 的 12 位原始视频输出的汽车 130 万像素摄像头模块参考设计

说明

此参考设计展示了一款适用于 130 万像素汽车摄像头的极小型解决方案。仅需单个同轴电缆连接即可提供数字视频、电源、摄像头控制和诊断。输出视频格式为 10 位或 12 位（高达 100MHz）。

资源

TIDA-01392	设计文件夹
DS90UB933-Q1	产品文件夹
TPS62172-Q1	产品文件夹
TPS79915-Q1	产品文件夹
TLV70018-Q1	产品文件夹

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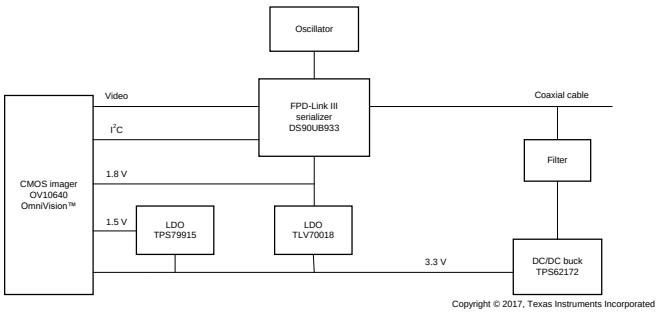
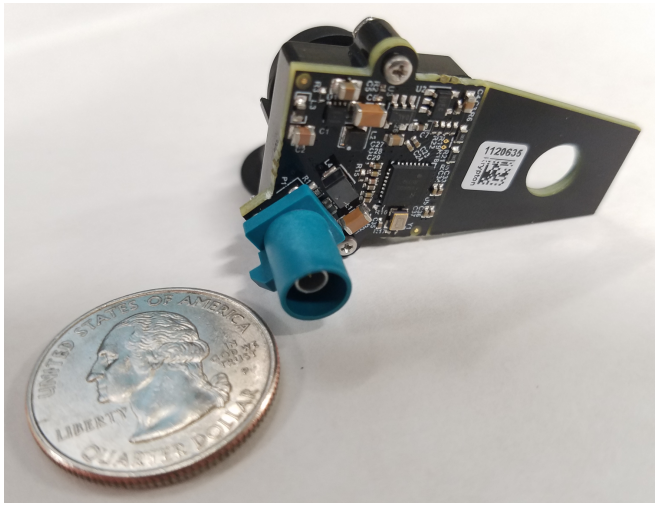
特性

- 电源解决方案经过优化，可将空间降到低至 20mm × 20mm
- 电源开关频率高于 AM 频段
- 来自 OmniVision™的 130 万像素 HDR 图像传感器，可提供 12 位原始图像数据
- 配备适用于数字视频、电源、控制和诊断的单个 Rosenberger Fakra 同轴电缆连接器
- 适用于 ASIL B 应用的诊断和内置 自检 (BIST)
- 所有器件均符合 AEC Q100 (-Q1) 标准

应用

- 高级驾驶员辅助系统 (ADAS) 视觉系统
- 环视系统
- 后置摄像头





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1 System Description

For many automotive safety systems, small cameras are required. This reference design addresses these requirements by combining a 1.3-MP imager with a 1.9-Gbit/s serializer and providing the necessary power supply for both devices. All of this functionality is contained on a 20-mm × 20-mm circuit card. The only connection required by the system is a single 50-Ω coaxial cable.

A combined signal containing the DC power and the FPD-Link front and back channels enters the board through the FAKRA-mini coax connector. 图 1 shows the filter that blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass.

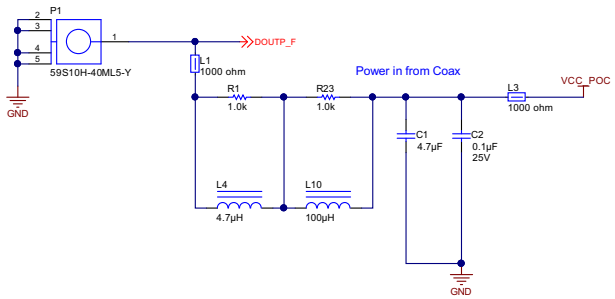


图 **1. FPD-Link III Signal Path**

The DC portion is connected to the input of the 3.3-V buck converter. The two other rails required by the serializer and the imager are then created with low dropout (LDO) regulators.

The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control backchannel will take between the serializer and deserializer.

The output of the CMOS imager is connected through digital video port (DVP) to the serializer. This 10-bit or 12-bit video data (with two sync signals) is converted to a single, high-speed serial stream that is transmitted over a single LVDS pair to the deserializer located on the other end of the coax cable.

On the same coax cable, there is separate low-latency, bidirectional control channel that transmits control information from an I^2C port. This control channel is independent of video blanking period. The channel is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax (POC)	4	12	17	V
P_{TOTAL}	Total power consumption	V_{POC} = 12 V		0.6	1	W
F_{PCLK}	Pixel clock frequency		37.5		100	MHz

2 System Overview

2.1 Block Diagram

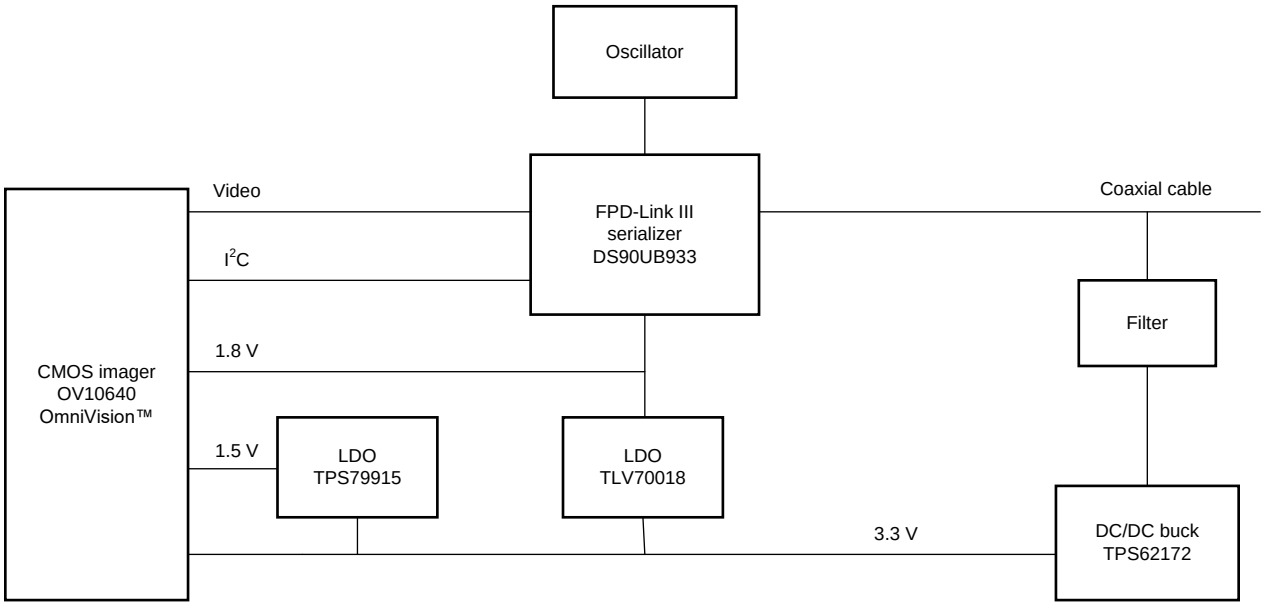


图 **2. Block Diagram of Camera**

2.2 Design Considerations

The following subsections discuss the considerations behind the design of each section of the system.

2.2.1 PCB and Form Factor

This reference design is not intended to fit any particular form factor. The only goal of the design—with regards to the PCB—is to make as compact a solution as possible. The square portion of the board is 20 mm × 20 mm. The area near the board edge in the second image is reserved for attaching the optics housing that holds the lens.

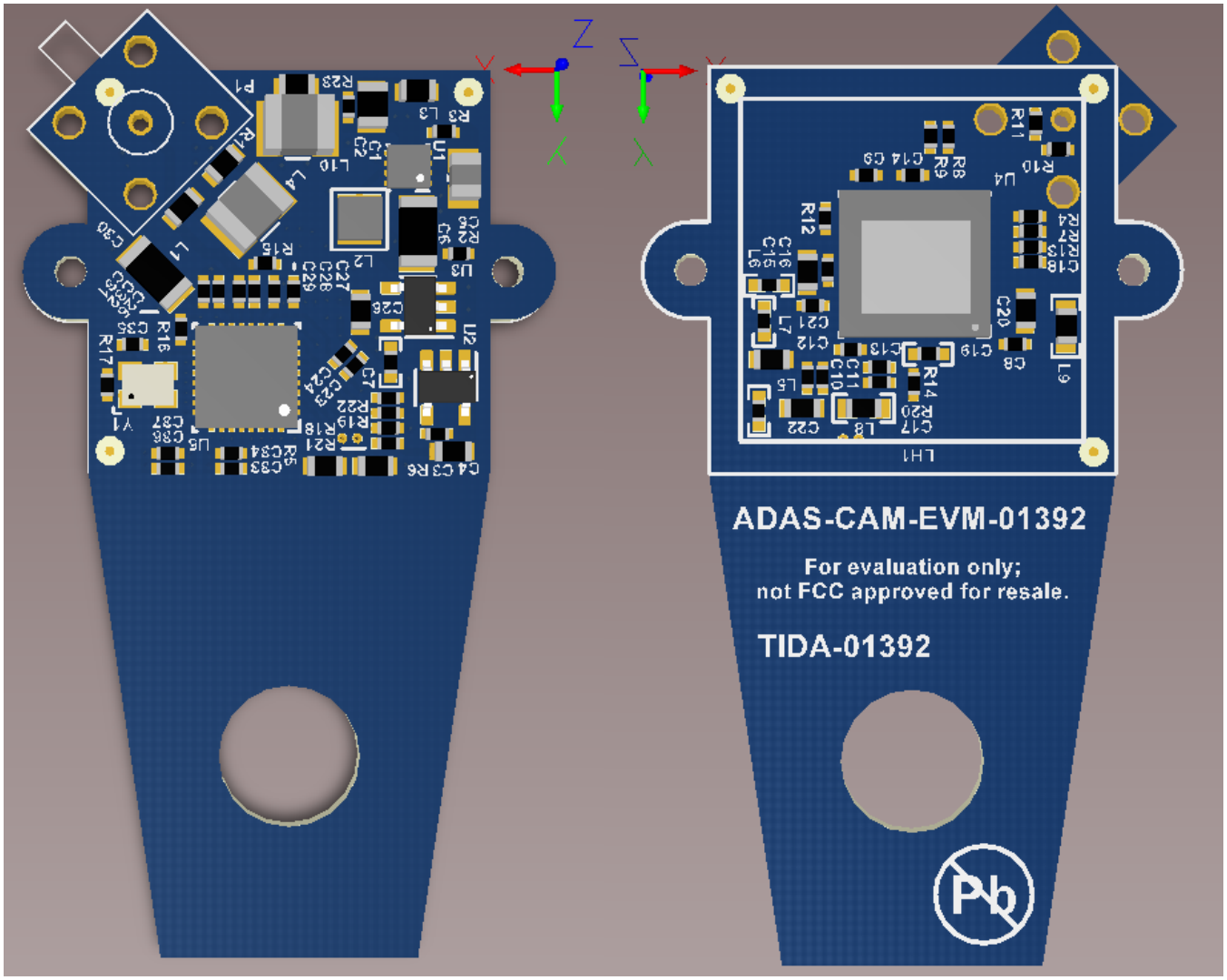


图 **3. PCB Top and Bottom Views**

2.2.2 Power Supply Design

2.2.2.1 POC Filter

One of the most critical portions of a design, which uses POC, is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators.
2. Protect the FPD-Link communication channels from noise coupled backwards from the rest of the system.

The DS90UB933/DS90UB934 SerDes devices used in this system communicate over two carrier frequencies, 1 GHz at full speed ("forward channel") and 2.5 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC. Luckily, by filtering the backchannel frequency, this reference design also filters the frequencies from the switching power supplies on the board.

The nominal backchannel speed is 2.5 MHz, but can vary from 1 MHz to 4 MHz when taking into account process variation, temperature, and power supply. To achieve the 1-kΩ impedance for the POC network across the full frequency range of 1 MHz to 1 GHz, it is recommended to use two inductors: a 4.7-µH inductor for high-frequency forward channel filtering, and a 100-µH inductor for low-frequency backchannel filtering. For more details, see the application report *Sending Power Over Coax in DS90UB913A Designs*. In addition, a 1-kΩ resistor is placed in parallel with both of these inductors. A 1-kΩ ferrite bead is also placed in series for extra filtering at the forward channel data rate.

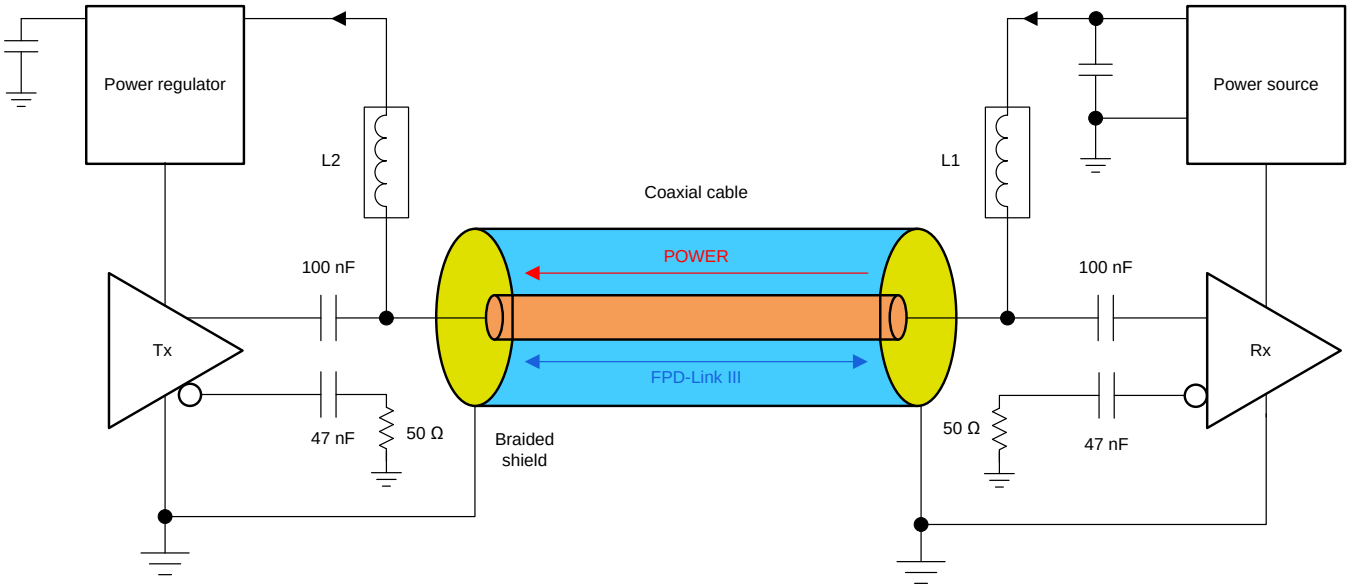


图 **4. Power Over Coax**

2.2.2.2 Power Supply Considerations

Because this reference design is targeted at automotive applications, there are few considerations that constrict design choices. In addition, there are few systems-level specifications that shaped the overall design:

- The total solution size must be minimized to meet the size requirement, which is less than 20 mm × 20 mm. This means choosing parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate external circuitry.
- To avoid interference with the AM radio band, all switching frequencies must be greater than 1700 kHz or lower than 540 kHz. Lower-switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason, this reference design focuses on higher-frequency switchers.
- All devices must be AEC Q100 (-Q1) rated.

Before choosing parts, know the input voltage range, rails required, and current required by each rail. In this case, the input voltage is a preregulated 9-V supply coming in over coax. The range is discussed later, but this is the nominal value. This system has only two main devices that consume the majority of the power. 表 2 shows the requirements for each supply on these devices.

表 2. Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (TYP) (A)	CURRENT (MAX) (A)	POWER (TYP) (W)	POWER (MAX) (W)
DS90UB933-Q1					
VDDT	1.8	0.076	0.095	0.1368	0.1710
VDDIO	1.8	0.0015	0.003	0.0027	0.0054
OV10640					
MTXAVDD, SVDD, PLL_AVDD	3.3	0.015	0.025	0.0495	0.0825
DOVDD	1.8	0.030	0.040	0.054	0.072
DVDD, PLL DVDD, MTXDVDD, AVDD_LO	1.5	0.080	0.120	0.12	0.18
RAIL TOTAL					
3.3-V rail	3.3	0.015	0.025	0.0495	0.0825
1.8-V rail	1.8	0.1075	0.138	0.1935	0.2484
1.5-V rail	1.5	0.080	0.120	0.12	0.18
OVERALL TOTAL					
		0.2025	0.283	0.363	0.5109

Summing these values, the 3.3-V rail requires 15 mA, 1.8-V rail requires 107.5 mA , and 1.5-V rail requires 80 mA. If choosing to cascade these power supplies, the 3.3-V regulator actually requires to source the current for the 1.8-V and 1.5-V rails as well. This neglects the consumption of passive components, oscillator, IC quiescent currents, and so on, but this is a good general number.

Because the input and output voltages, output current requirements, and total wattage consumption are known, calculate what the input currents will look like with 公式 1.

$$P_{OUT} = P_{IN} = I_{IN} \times V_{IN} \rightarrow 510.9\ mW = I_{IN} = 56.77\ mA\ (max) \quad (1)$$

These numbers give a good starting point for selecting the parts and topology for the regulators as well as inductor selections later on. However, this calculation does not take into account the efficiencies of the power supplies.

As previously mentioned, the parts in the power supply must be Q100-rated, switch outside the AM band, and satisfy the voltage and current requirements as listed. Because the input voltage is a regulated voltage that will always be greater than any of the power rail needs, only choose from step-down converters and LDOs.

The key feature of the system is the small size, so integration of external circuitry is a high priority. Integrating FETs, compensation networks, and sometimes feedback can significantly reduce total solution size. Many buck regulators integrate everything but the input-output caps and the inductor into very small packages. High integration also loses a lot of efficiency across different operating points. However, this reference design sacrifices some efficiency for size and simplicity reasons.

Ultimately, three device families are good candidates: the TPS62172 for the 3.3-V rail (TPS6217x), the TLV70018 for the 1.8-V rail, and the TPS79915 for the 1.5-V rail. Clearly the largest trade-off with using LDOs is that the efficiency drops significantly. In this reference design, the efficiency hit is required to avoid the inherent noise and EMI issues associated with switching-power supplies for the sensitive OV10640 imager rails.

图 5 shows a typical application circuit.

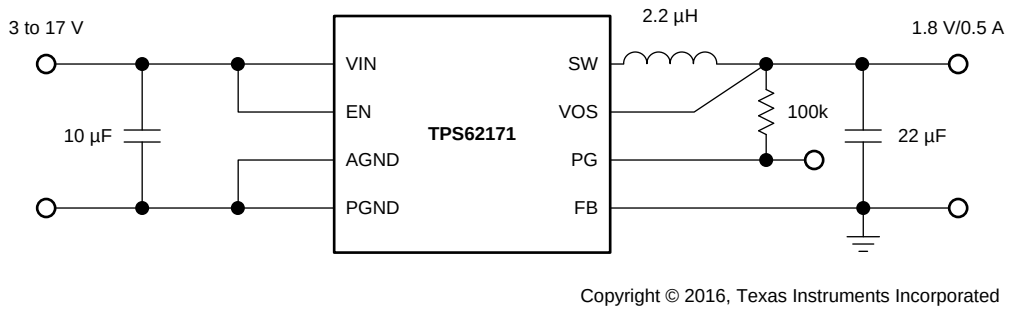


图 5. Typical Application Circuit

Much of the component selection and design theory can be found in the *Application Information* section of *TPS6217x-Q1 3-V to 17-V 0.5-A Step-Down Converters with DCS-Control™*.

2.2.2.2.1 Choosing the Output Inductor

As mentioned in 节 2.2.2.2, the switching frequency of the converter must remain above 2.1 MHz. This requirement means that the converter must always operate in continuous mode. Because input voltage and output voltage are fixed and the output current is almost constant and can be predicted easily, the minimum inductance, L, for the converter to operate with continuous inductor current can be calculated using 公式 2.

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2 \times V_{IN} \times I_{OUT} \times f} = \frac{3.3\ V\left(14\ V - 3.3\ V\right)}{2 \times 14\ V \times 0.2025\ A \times 2.1\,MHz} = 2.96\ \mu H \quad (2)$$

Because 2.96 µH is not a standard inductor values, the next higher value of 3.3 µH is chosen.

With the inductance value chosen, the design now requires an inductor with a proper saturation current. This is going to be the combination of the steady state supply current as well as the inductor ripple current. The current rating must be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current (from *TPS6217x-Q1 3-V to 17-V 0.5-A Step-Down Converters with DCS-Control™*) using 公式 3.

$$\Delta I_L = V_{OUT} \times \left(\frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{SW}} \right) \quad (3)$$

The following are the parameters for this design using the TPS62172:

- V_{OUT} = 3.3 V
- V_{IN} = 14 V
- L = 3.3 µH
- f_{SW} = 2.25 MHz

which yields an inductor current of ΔI_L = 340 mA. The maximum current draw of the system through this regulator is 283 mA. Finally, 公式 4 gives the minimum saturation.

$$L_{sat} \geq \left(I_{max} + \frac{I_{ripple}}{2} \right) \times 1.2 = \left(283\ mA + \frac{340\ mA}{2} \right) \times 453\ mA \quad (4)$$

For this inductor to be capable of the 453-mA maximum current, select an inductor that has a higher saturation rating than maximum load current. A good rule is to rate the inductor with a 20% higher saturation current rating, which requires a minimum of 543 mA. The Coilcraft® XPL2010-332MLB was initially the choice for a 3.3-µH inductor because of its saturation current rating; however, the inductance has a 20% tolerance, which means, worst case, the inductor would be below the 2.96-µH minimum inductance requirement. With that in mind, this reference design uses a XPL2010-472MLB, which has a saturation current of 580 mA, and with the 20% inductance tolerance on 4.7 µH, the inductor's minimum is 3.76 µH. This part comes in a very small, 2.0-mm × 1.9-mm package.

2.2.2.2.2 Choosing the Output Capacitor

Because the device is internally compensated, the device is only stable for certain component values in the LC output filter. The application report *Optimizing the TPS62130/40/50/60/70 Output Filter* provides the chart of stable values shown in 表 3. For a 4.7-µH inductor, an output capacitance from 4.7 µF to 47 µF can be used. This reference design uses a 22-µF output capacitor and remain in the stable region of effective corner frequencies.

表 3. Stability versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL)								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
	EFFECTIVE CORNER FREQUENCIES (kHz)								
0.47 µH	151.4	103.8	70.0	47.9	32.8	23.2	16.4	11.6	8.2
1.00 µH	103.8	71.2	48.0	32.8	22.5	15.9	11.3	8.0	5.6
2.2 µH	70.0	48.0	32.4	22.1	15.2	10.7	7.6	5.4	3.8
3.3 µH	57.2	39.2	26.4	18.1	12.4	8.8	6.2	4.4	3.1
4.7 µH	47.9	32.8	22.1	15.1	10.4	7.3	5.2	3.7	2.6
10.0 µH	32.8	22.5	15.2	10.4	7.1	5.0	3.6	2.5	1.8

	Recommended for TPS6213x, TPS6214x, TPS6215x, TPS6216x, TPS6217x
	Recommended for TPS6213x, TPS6214x,TPS6215x only
	Stable without Cff (within recommended LC corner frequency range)
	Stable without Cff (outside recommended LC corner frequency range)
	Unstable

2.2.2.3 TPS79915-Q1 LDO

The TPS79915-Q1 is very easy to design in. As the data sheet *Automotive 200mA, Low Iq, Low-Dropout Regulator* recommends, add a ceramic capacitor of > 2 µF to the output of the device. In addition, the device has a couple of optional capacitors at the input and NR pin for better noise immunity. For this reference design, the NR pin is bypassed with a 0.1-µF capacitor for better noise performance.

2.2.2.4 TLV70018-Q1 LDO

The TLV70018-Q1 is also very easy to design in. As the data sheet *Automotive 300mA, Low Iq, Low-Dropout Regulator* recommends, add a ceramic capacitor of 1 µF to the output of the device.

For ADAS applications, it is recommended that all ceramic capacitors use X7R dielectric material, which ensures minimum capacitance variation over the full temperature range. The voltage rating of the capacitors should be greater than the maximum voltage they could detect and two times the typical voltage they detect to avoid DC bias effects.

2.3 Highlighted Products

This reference design uses the following TI products:

- DS90UB933-Q1 is the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer-deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU)
- TPS62172-Q1 is an automotive-qualified, 3.3-V fixed output, step-down DC converter optimized for applications with high-power density. A high-switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response
- TPS79915-Q1 is an automotive-qualified 200-mA, low-IQ, LDO regulator with a fixed output voltage of 1.5 V.
- TLV70018-Q1 is an automotive-qualified 300-mA, low-IQ, LDO Regulator with a fixed output voltage of 1.8 V.

2.3.1 OV10640 Imager

Available from OmniVision Technologies Inc., this imager is a color, 1.3-MP, CMOS imager with high dynamic range (HDR). This device is suitable for automotive systems and can provide a 12-bit raw DVP output. Some additional features of the imager are:

- Supports image sizes: 1280 × 1080, VGA, QVGA, and any cropped size
- Low-power consumption
- Requires three voltage rails (1.5 V, 1.8 V, and 3.3 V)
- Can be configured using an I^2C-compatible, two-wire serial interface

2.3.2 DS90UB933-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The parallel video input of the DS90UB933-Q1 mates well with the 12-bit parallel video output of the OV10640 imager. Once combined with the filters for the POC, video, I^2C, diagnostics, and power can all be transmitted up to 15 m on a single, inexpensive coax cable.

For more information on the cable itself, see the application report *Cable Requirements for the DS90UB913A and DS90UB914A*.

2.3.3 TPS62172-Q1

To keep the camera small, the power supply must be small. The supply must also be power efficient while not adding measurable noise to the video from the imager. Often, these two requirements stand in opposition. A switching-power supply is more efficient than a linear regulator, but this supply can add noise to the system.

Camera sensor circuits usually are sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications. This means that the TPS62172-Q1-switching regulator operating at 2.25 MHz meet both requirements. This high-switching frequency also helps to reduce the size of the discrete components in the circuit.

2.3.4 TPS79915-Q1

The TPS79915-Q1 LDO linear regulator is a low-quiescent current device with excellent line and load transient performance. This automotive-qualified LDO is small, which allows the 1.5-V rail to be created in a very small space. A precision band gap and an error amplifier provide overall 2% accuracy. Low-output noise, high power-supply rejection ratio (PSRR) make these LDOs ideal for this application.

2.3.5 TLV70018-Q1

The TLV70018-Q1 LDO linear regulator is a low-quiescent current device. This automotive-qualified LDO is small, which allows the 1.8-V rail to be created in a very small space. A precision band gap and an error amplifier provide overall 2% accuracy. Low-output noise, high power-supply rejection ratio (PSRR) make these LDOs ideal for this application.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

This reference design requires only one connection to a system with a compatible deserializer. Simply connect the FAKRA connector on the coax cable between the serializer and deserializer.

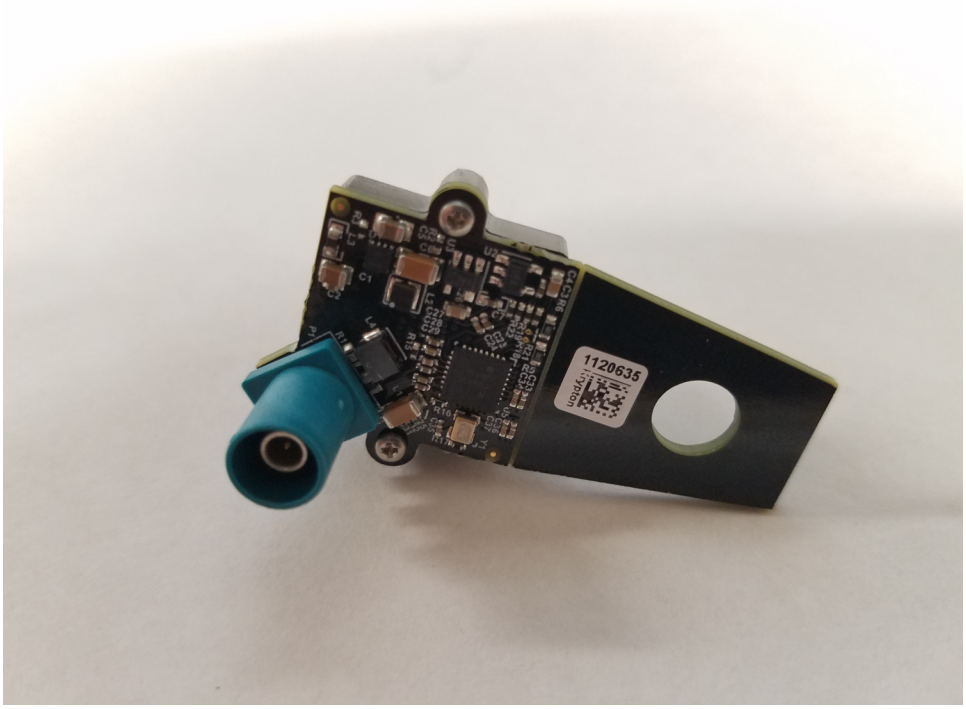


图 6. Getting Started With Board

3.1.1 Video Hardware Setup

The setup for testing video output on the camera module of this reference design is displayed in 图 7. The design includes an OV10640 device that connects to the DS90UB933 serializer over parallel DVP interface and I^2C interfaces. The DS90UB953 serializer then connects through POC to a DS90UB964 quad deserializer on the TIDA-01005 design.

注: For test setup, only one channel was used from the DS90UB964.

To enable video output from the TIDA-01005 design, the TIDA-01005 CSI-2 Samtec connector is connected to a TDA3x EVM. The TDA3x EVM enables video output by writing all the backchannel I^2C setting configurations for the OV10640, DS90UB933, and DS90UB964 devices. When these writes are completed, VisionSDK software enables video output to an HDMI-connected monitor.

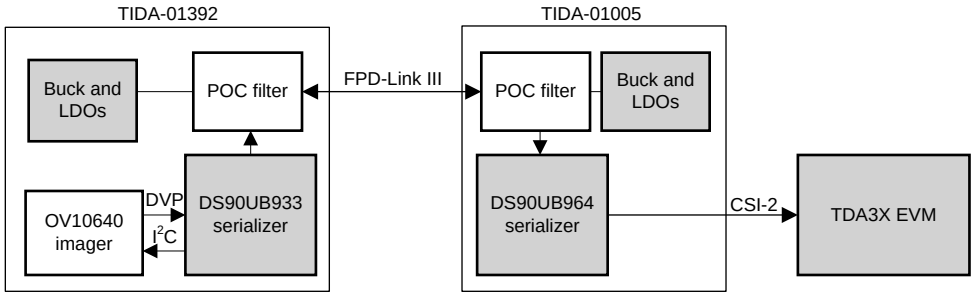


图 **7. Video Output Setup Block Diagram**

3.1.2 FPD-Link III Initialization

With the setup in 图 7 in place, the TIDA-01005 design uses a main 12-V supply, delivers POC supply for this reference design's camera power and steps down to 1.8 V and 1.1 V for the DS90UB964 supplies. The OV10640, DS90UB933, and DS90UB964 devices now have power. Lastly, by connecting the TDA3x EVM to the TIDA-01005 design, the I^2C writes for initialization can begin. The writes to initialize the deserializer and serializer are as follows:

- Deserializer slave I^2C address 0x7A (8-bit) or 0x3D (7-bit):
  - Register 0x4C with 0x01: Enables write enable for Port 0
  - Register 0x58 with 0x58: I^2C passthrough enabled and backchannel frequency select
  - Register 0x5C with 0xB0: Sets serializer alias to B0
  - Register 0x5D with 0x60: Sets slave ID for imager to 60
  - Register 0x65 with 0x60: Sets slave alias for imager to 60
  - Register 0x6D with 0x7E: Configures port to coax mode and FPD III to CSI mode
  - Register 0x0F with 0x03: Changes GPIO0 and GPIO1 to output mode for driving GPIOs over backchannel
  - Register 0x6E with 0x9A: Sets Backchannel control of GPIO0 and GPIO1 for framesync on GPIO0 and GPIO1 toggle high for pulling DS90UB933 out of reset

3.1.3 OV10640 Initialization

Once the FPD-Link III setup for the DS90UB933 and DS90UB964 is complete, the I^2C initialization on the OV10640 can now be completed. For these writes, see the OV10640 data sheet for register settings. There are many register settings listed, but as long as the 933 and 964 FPD-Link III parts are configured, the I^2C backchannel allows for the OV10640 to be accessed at address 0x60 in 8-bit addressing or 0x30 in 7-bit addressing.

3.2 Testing and Results

3.2.1 Test Setup

For the following tests, the camera is connected to a multiple-camera surround view system.

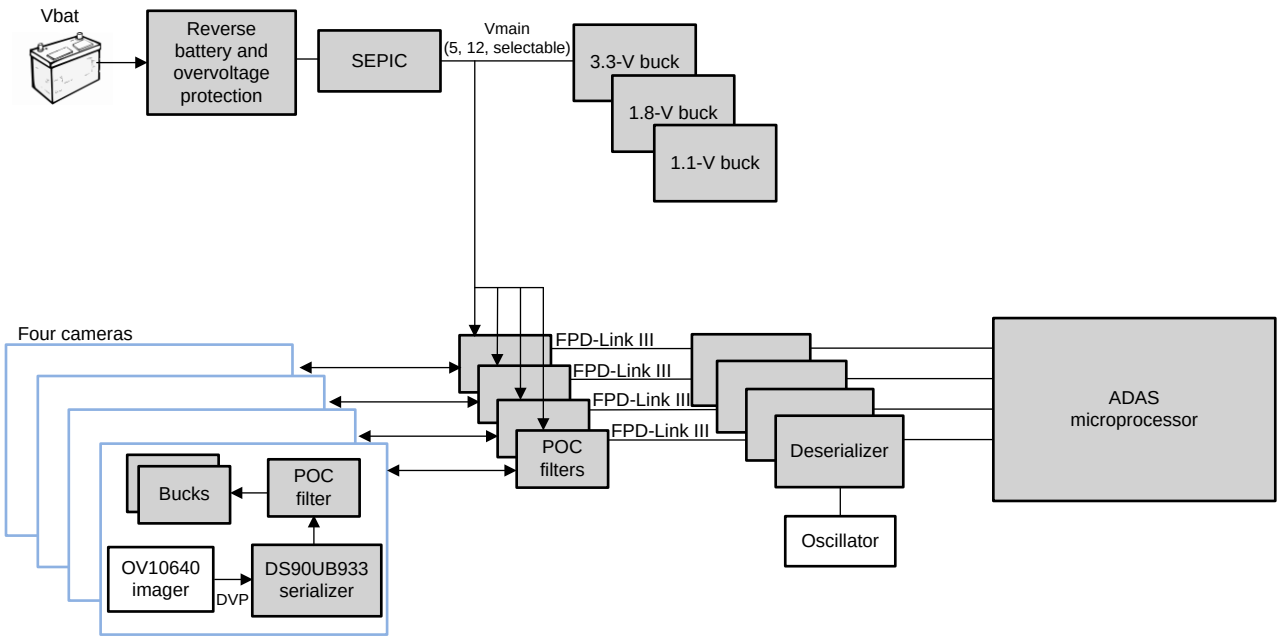


图 8. Block Diagram of Simplified Surround View

3.2.1.1 Setup for Verifying Power Supply Start-up

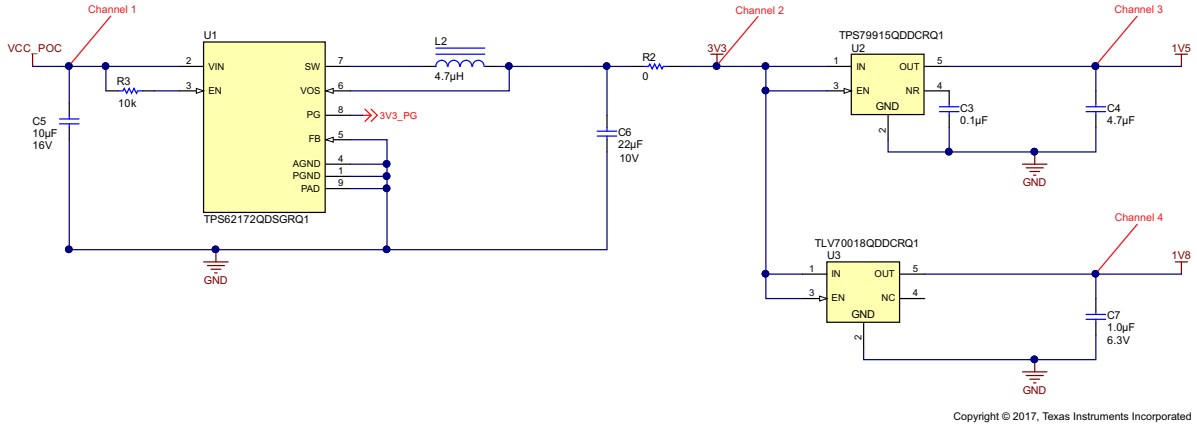


图 9. Setup for Measuring All Power Rails

3.2.1.2 Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two busses of interest are:

1. I²C connection from serializer to imager (shown as I2C_camera)
2. I²C connection from microprocessor to deserializer (shown as I2C_uC)

Make connections to both the clock and data lines of each bus.

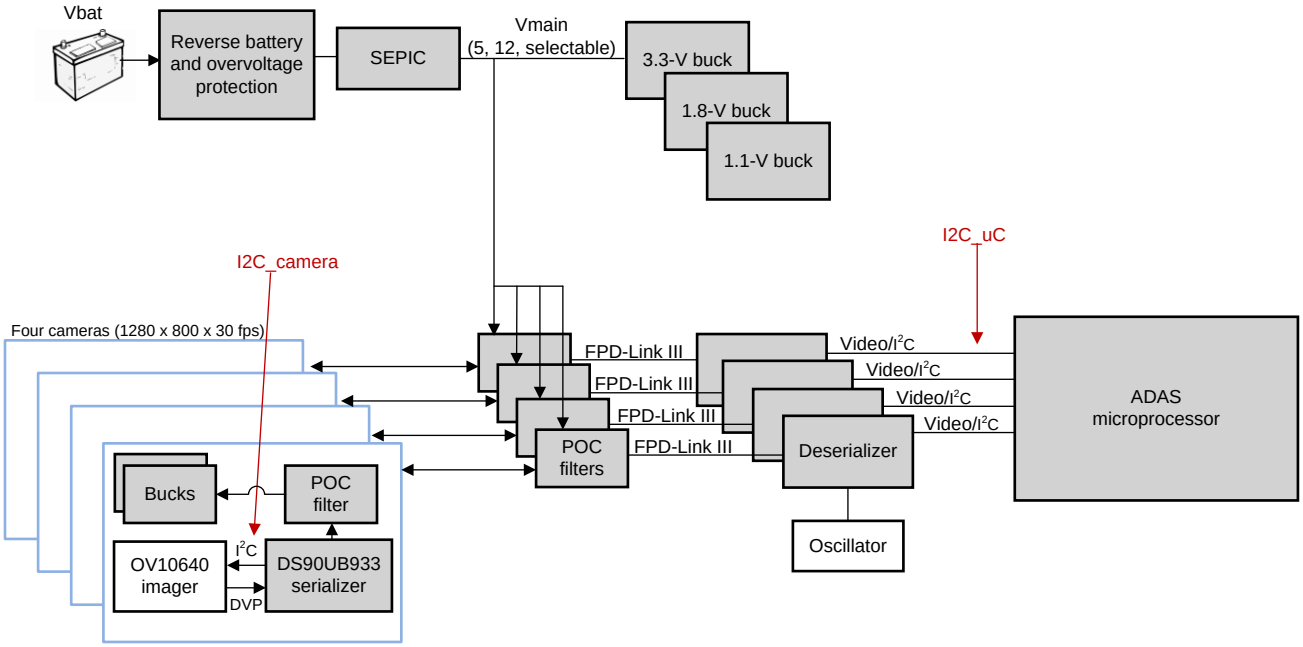


图 10. Setup for Monitoring I²C Transactions

3.2.2 Test Results

The following sections show the test data from verifying the functionality of the camera design.

3.2.2.1 Power Supply Startup: V_{IN}, 3.3-V, 1.8-V, and 1.5-V Rails

For 图 11:

- Channel one (blue) 12-V, POC in
- Channel two (turquoise) 3.3-V switcher output
- Channel three (pink) 1.5-V LDO output
- Channel four (green) 1.8-V LDO output

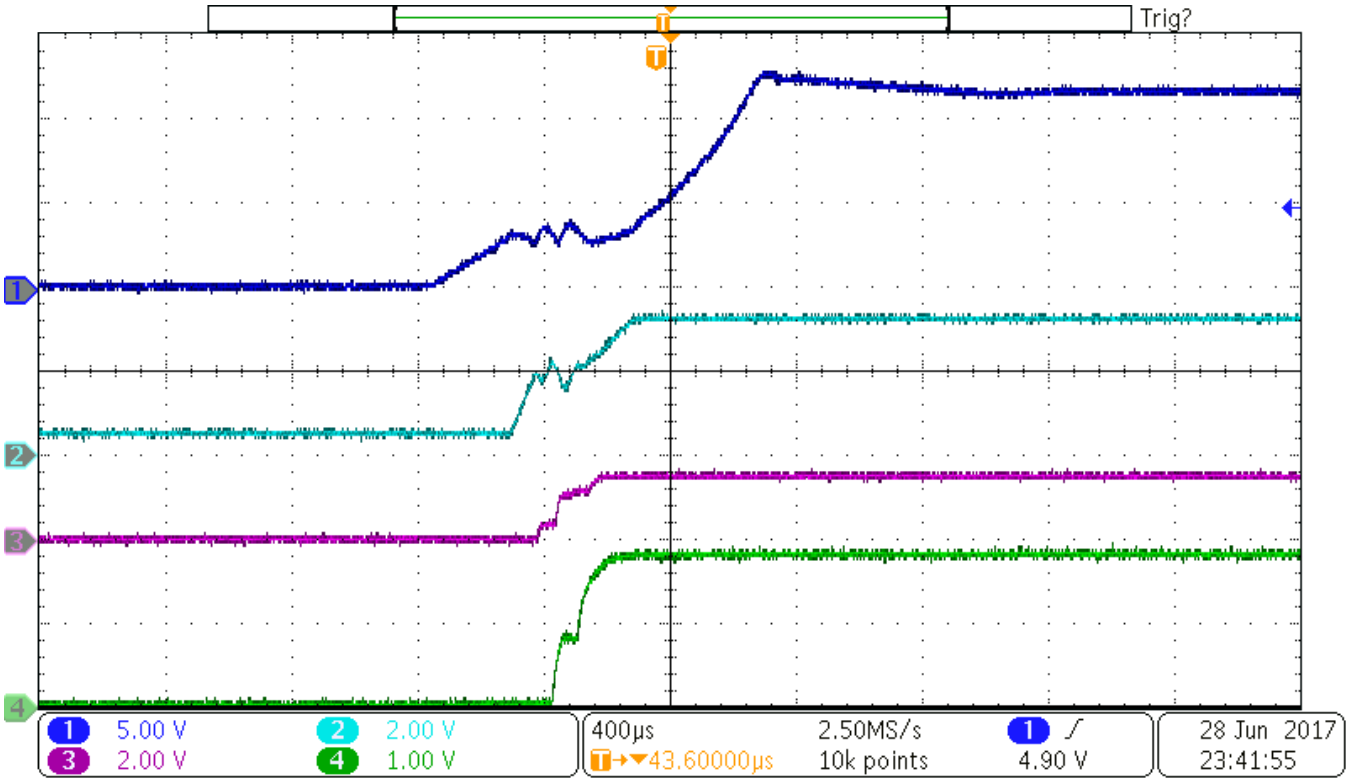


图 11. Power Supply Start-up

3.2.2.2 I²C Addressing

Some applications require multiple camera devices with the same fixed address to be accessed on the same I²C bus. The DS90UB933 provides slave ID matching and aliasing to generate different target slave addresses when connecting more than two identical devices together on the same bus. This application allows the slave devices to be independently addressed. Each device connected to the bus is addressable through a unique ID by programming the slave alias register on deserializer. This programming remaps the slave alias address to the target SLAVE_ID address.

In this reference design, the OV10640 imager default address is 0x30 (0110000x). For a system using more than one imager, GPIO 2/1 can be used to select different addresses for each imager. However, this process requires that each camera in the system be built differently. Each system would have to be built with one of each unique camera. In a production environment, this process is not desirable.

Instead, the aliasing feature of the DS90UB933 can be used. In the deserializer, unique addresses are assigned to each imager. These aliases are used to refer to the imagers that are all addressed at 0x30 (0110000x). The host microprocessor can now communicate with each imager by using its alias even though the imagers in each camera are physically addressed identically.

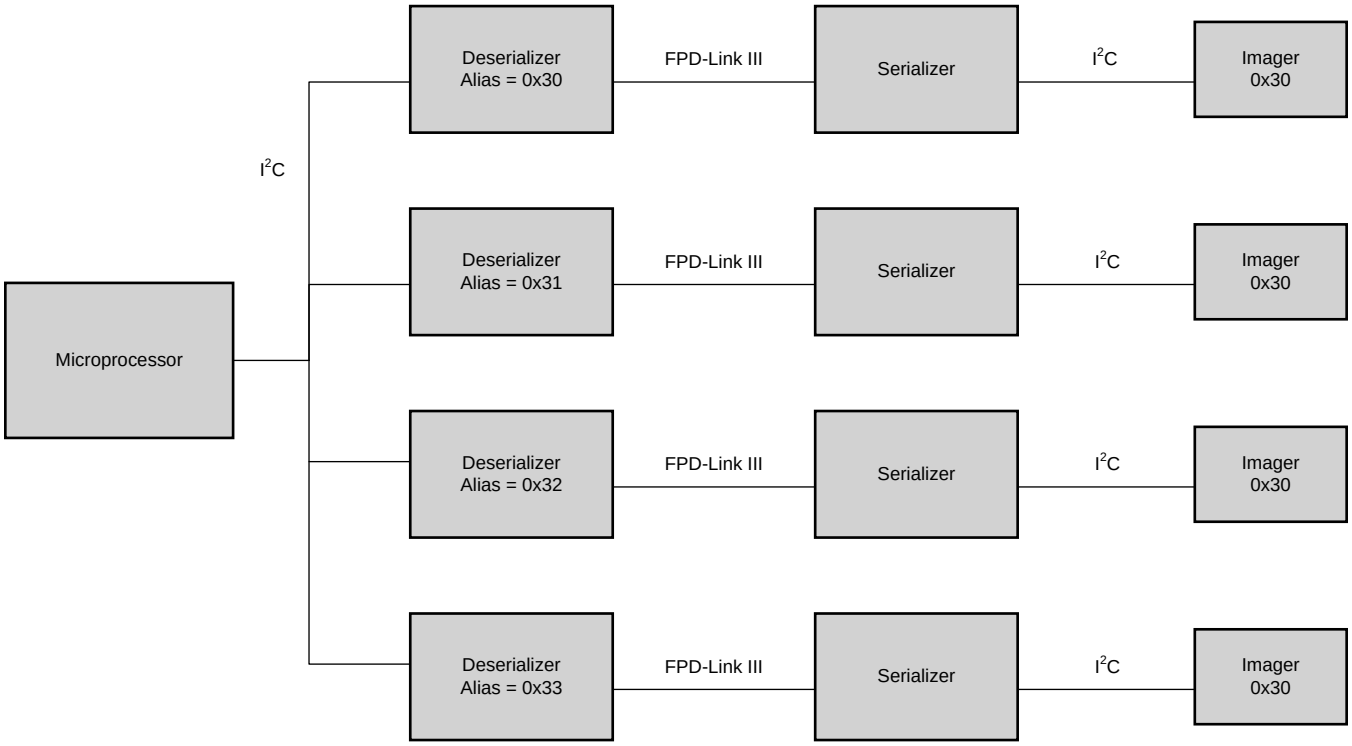


图 **12. I²C Address Aliasing**

3.2.2.3 I²C Communications

With the supplies up and running, check the FPD-Link connection, the I²C aliasing, and the state of the OV10640 imager in one step. 图 13 shows a reset of logic. This reset occurs after the microprocessor configures the deserializer on the other end of the link. Because this communication starts on the ECU board and is acknowledged by the camera, this shows that the communication through the FPD-Link III is functioning properly.

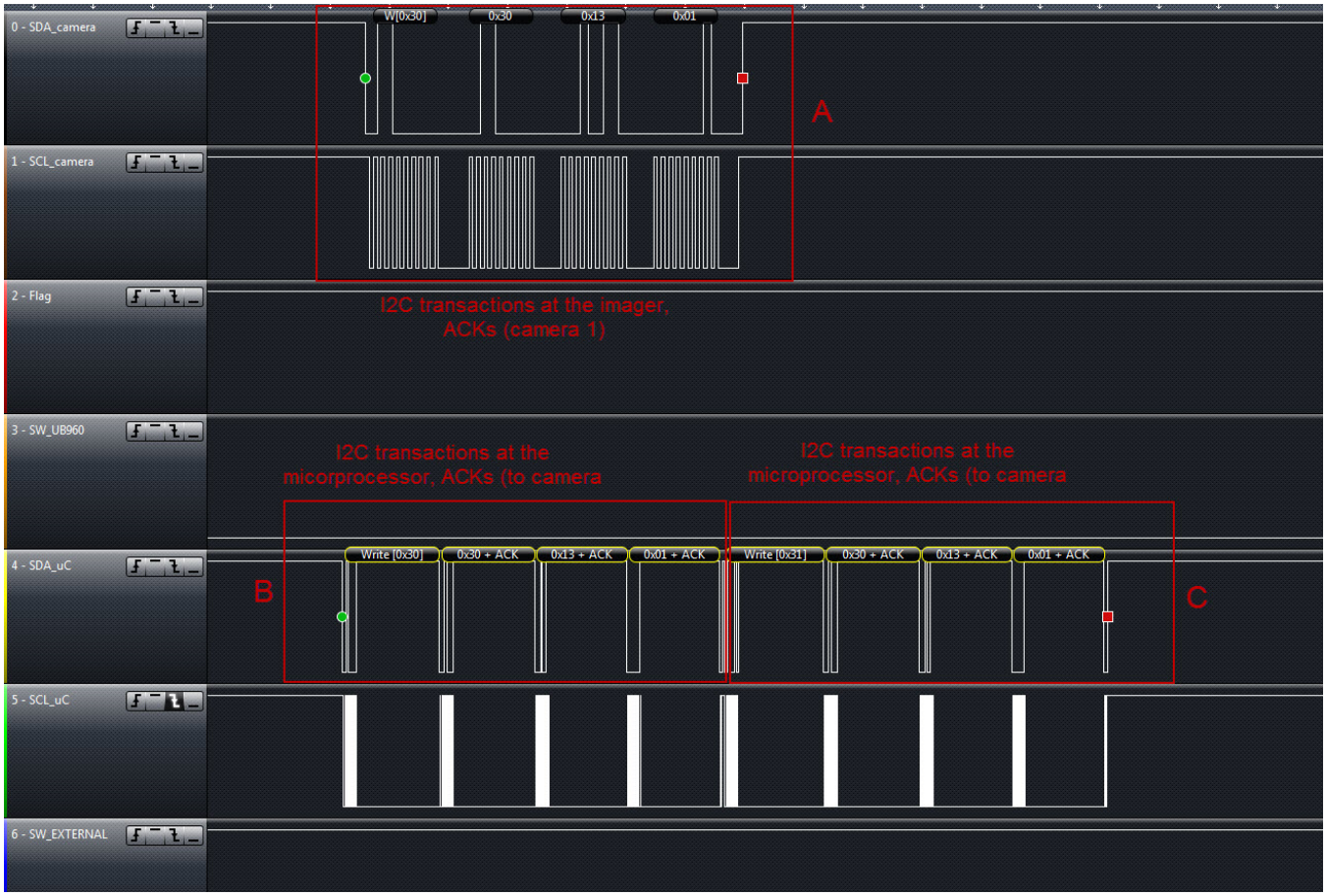


图 **13. I²C Transactions**

The box labeled B contains the first write from the microprocessor. This box is addressed to address 0x30, the register address as 0x3013, and the data to be written as 0x1. Because the address is 0x30, the deserializer passes this transaction to the first camera in the system. The transaction is routed to the imager, and the address is aliased to 0x30.

In box A, the same communication is slightly delayed. This shows that the communication is present on the camera one I²C bus, measured at the imager.

The write to address 0x31 in box C is for camera two (see 图 13). The deserializer on the ECU board passes this transaction to camera two, and the address is aliased to 0x30. This transaction is not present on the camera one I²C bus because the transaction is not intended for this camera.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01392.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01392.

4.3 PCB Layout Recommendations

4.3.1 Switching DC/DC Converters

During part placement and routing, it is helpful to consider the path that the current will be taking through the circuit. The yellow line in 图 14 shows the current path in through the input filter, the switch in the converter, inductor L2, and then out to R2 across the output capacitor (C6). Any return currents from the input capacitor (C5) or the output capacitor (C6) are joined together on the top side of the board before they are connected to the ground (return) plane (inside the green circle in 图 14). This routing reduces the amount of return currents and voltage gradients in the ground plane. This reduction may not be noticeable in the performance of the converter, but it reduces its coupled noise into other devices.

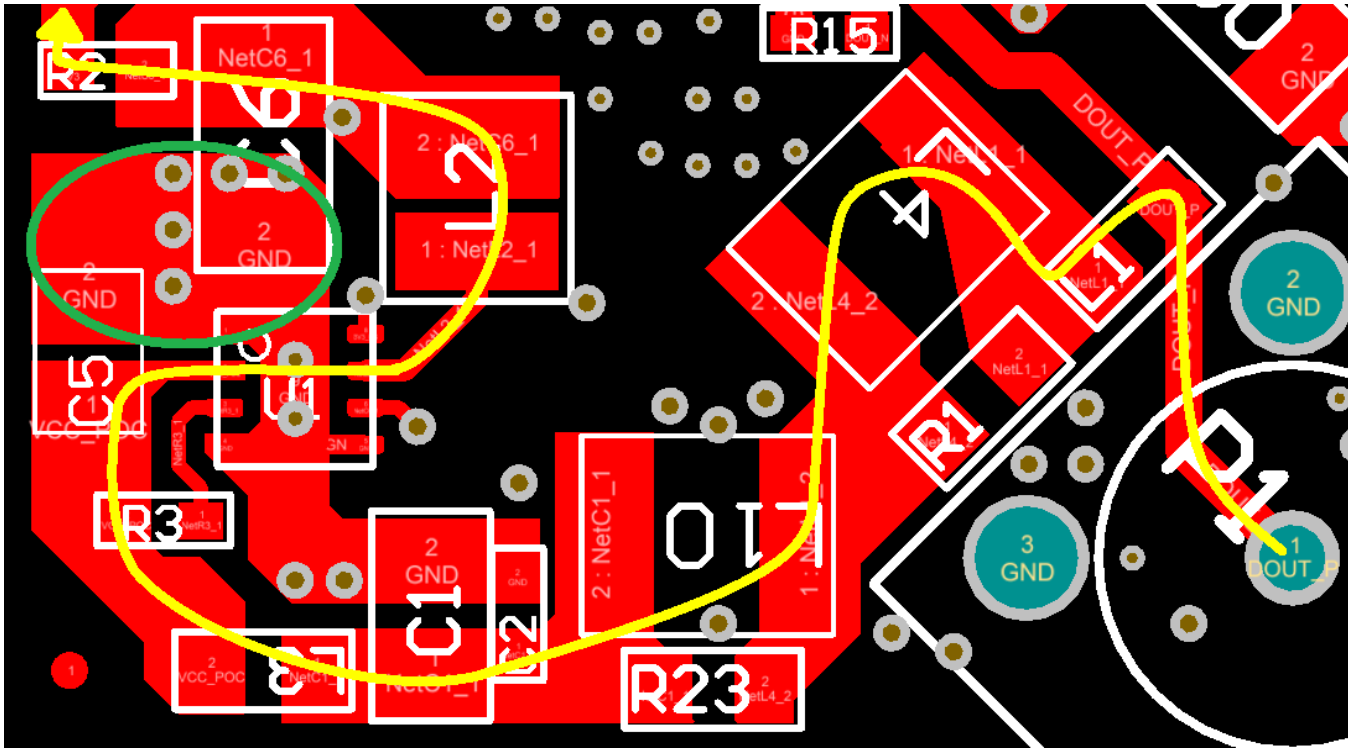


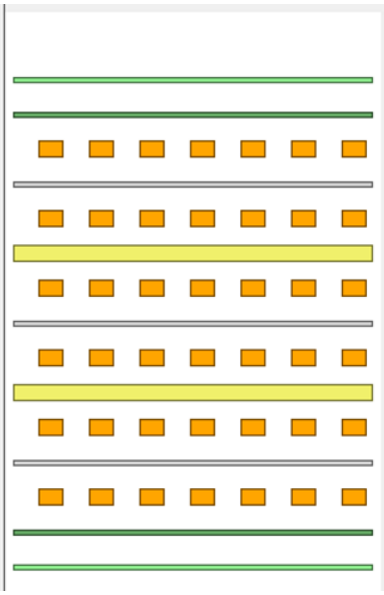
图 14. Routing FB Traces Around SW Nodes

4.3.2 PCB Layer Stackup Recommendations

The following are PCB layer stackup recommendations. Because automotive is the target space, there are a few extra measures and considerations to take, especially when dealing with high-speed signals and small PCBs.

- Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines.
- If using a four-layer board, layer two must be a ground plane. Because most of the components and switching currents are on the top layer, there is a reduction of the inductive effect of the vias when currents are returned through the plane.
- An additional two layers were used in this board to simplify BGA fan out and routing.

图 15 shows the stackup used in this board.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Lay...	Signal	Copper	1.4		
Dielectric 1	Dielectric	Prepreg	12.6	370HR	4.2
Layer 2 - GND	Signal	Copper	1.4		
Dielectric 2	Dielectric	Core	8	370HR	4.2
Layer 3 - Signal	Signal	Copper	1.417		
Dielectric 3	Dielectric	Prepreg	16.6	370HR	4.2
Layer 4 - Signal	Signal	Copper	1.417		
Dielectric 4	Dielectric	Core	8	370HR	4.2
Layer 5 - PWR	Signal	Copper	1.4		
Dielectric 5	Dielectric	Prepreg	12.6	370HR	4.2
Layer 6 - Bottom...	Signal	Copper	1.4		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

图 15. Layer Stackup

4.3.3 Serializer Layout Recommendations

Decoupling capacitors must be located very close to the supply pin on the serializer. Again, this placement requires that the user to consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. Smaller value capacitors that provide higher-frequency decoupling must be placed closest to the device.

图 16 shows the supply current from C32 in yellow. The green line is the return path. The cross-sectional area of this loop is very small. A similar sketch for C30 would show a larger loop.

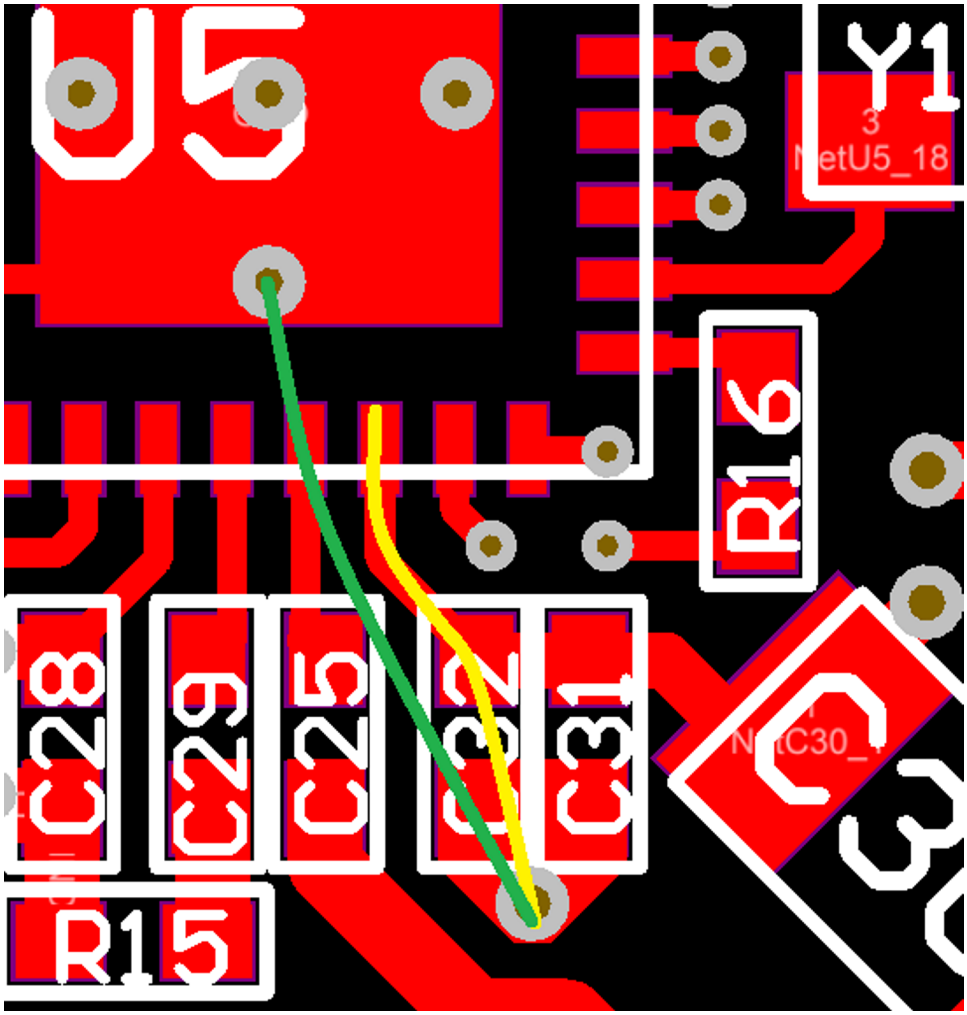


图 16. Decoupling Current Loop

For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Whenever possible, this connection must also be kept short. The routing of the high-speed serial line is shown in 图 17 and highlighted in white. The total length between the two yellow arrows is about ½ inch.

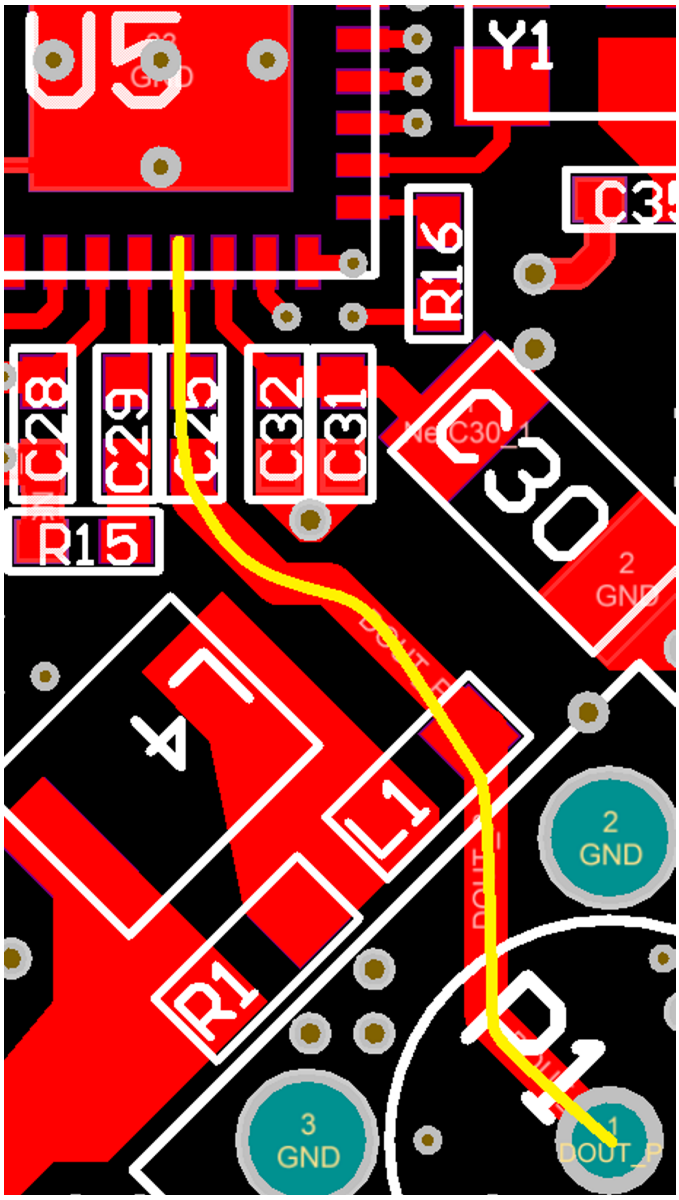


图 17. High-Speed Serial Trace

4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-01392.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01392.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01392.

5 Related Documentation

1. Texas Instruments, *DS90UB933-Q1 12-bit 100MHz FPD-Link III Serializer for 1MP/60fps and 2MP/30fps Cameras Data Sheet*
2. Texas Instruments, *TPS6217x-Q1 3-V to 17-V 0.5-A Step-Down Converters with DCS-Control™ Data Sheet*
3. Texas Instruments, *Automotive 300mA, Low Iq, Low-Dropout Regulator Data Sheet*
4. Texas Instruments, *Automotive 200mA, Low Iq, Low-Dropout Regulator Data Sheet*
5. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs Application Report*
6. Texas Instruments, *Cable Requirements for the DS90UB913A and DS90UB914A Application Report*
7. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 Output Filter Application Report*
8. Texas Instruments, *TPS6217x-Q1 3-V to 17-V 0.5-A Step-Down Converters with DCS-Control™ Data Sheet*

5.1 商标

修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (July 2017) to A Revision **Page**

- Updated Figure 1: *FPD-Link III Signal Path* 2
- Updated Figure 3: *PCB Top and Bottom Views*..... 4
- 已更改 backchannel carrier frequency from between 2 and 4 MHz to 2.5 MHz 5
- Updated Figure 14: *Routing FB Traces Around SW Nodes* 19

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