

TI 参考设计

适用于逆变器供电驱动器的效率为 98% 的 230V、900W PFC 参考设计



设计概述

TIDA-00443 是一款 900W 功率因数稳压器转换器，专为逆变器供电 BLDC/PMSM 电机设备而设计。该参考设计是连续导通模式升压转换器，通过使用 UCC28180 PFC 控制器实现，提供了所有必要的内置保护功能。硬件经过特别设计，已通过 EN55014 针对家用电器的传导发射、浪涌和 EFT 要求的测试。

此参考设计的突出亮点包括：

- 提供一个现成的前端 PFC 平台，可覆盖高达 900W 功率级别要求的各种电器
- 改进了逆变器供电电机驱动器的总体系统性能，具有更低的总线纹波、更低的总线电容、更低的均方根 (RMS) 电流以及前端保护
- 满足严格的电流总谐波失真 (THD) 和功率因数规定
- 稳健的输出电源，针对输出过流、输出过压和输出欠压现象提供保护

设计资源

TIDA-00443	包含设计文件的工具文件夹
UCC28180	产品文件夹
UCC27517A	产品文件夹



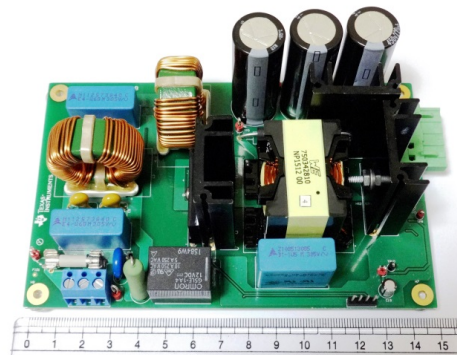
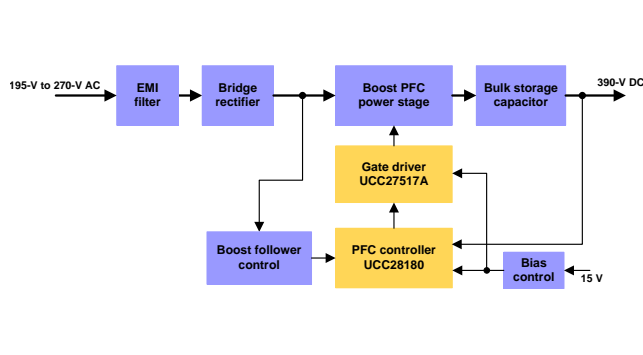
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设计特性

- 工作输入范围为 195V 到 270V 交流
- 旨在驱动功率高达 900W 的各类逆变器供电电机和下游直流/直流转换器
- 从中等负载到满负载（50% 到 100%），具有大于 0.99 的高功率因数和小于 5% 的 THD；10% 和 100% 负载时，均可满足 IEC 61000-3-2 A 类和 D 类要求的电流 THD 规定
- 在整个工作电压范围内，可在满负载情况下实现大于 97% 的高效率，因而在高达 55°C 的环境温度运行时也无需外部冷却
- 与具有可变交流输入的传统解决方案相比，内置升压跟随器输出选项提供了更高的效率（≈ 98%），提高了下游逆变器的效率，有效地降低了直流总线电容
- 符合传导发射标准 EN55011 A 类、EFT 规范 IEC6000-4-4 以及浪涌规范 IEC61000-4-5 的要求
- 简单易用的 PCB 封装 (149mm × 94mm)
- 经过完全验证，可驱动 900W 电机

特色应用

- 真空吸尘器
- HVAC
- 电动工具
- 在线式 UPS
- 洗衣机和烘干机
- 冰箱
- 电力存储和电池充电器



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1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage range	195- to 270-V AC (230-V nominal hi-line bus)
Input supply frequency	47 Hz to 63 Hz
Output voltage	390-V DC (with boost follower: 290 V to 390 V)
Output power	900 W, 390 V at 2.3 A
Efficiency	> 97 % with fixed output voltage ≅ 98 % with boost follower configuration
Power factor	> 0.99
Protection	Output overcurrent Output overvoltage Output undervoltage Open-loop detection
Stand by power	0.64 W at 230-V AC
Line and load regulation	< ± 1%
Operating ambient	-10°C to 55°C
Board form factor and specification	149 mm × 94 mm; PCB type: FR4, two-layer
Conducted emissions	As per EN55011 - class A
Power line harmonics	As per IEC 61000-3-2 class A and class D both at 10% and 100% loads
EFT	As per IEC-61000-4-4
Surge	As per IEC-61000-4-5

2 System Description

Home appliance equipment such as vacuum cleaners, refrigerators, air conditioners, washers, and kitchen hoods use three-phase, pulse-width modulated BLDC or PMSM drives. These motor drives typically have fractional or low horsepower ratings ranging from 0.25 HP (186 W) to 2 HP (1,500 W). An electronic drive is required to control the stator currents in a BLDC or PMSM motor. A typical electronic drive consists of:

- Power stage with a three-phase inverter with the required power capability
- Microcontroller unit (MCU) to implement the motor control algorithm
- Motor voltage and current sensing for closed-loop speed or torque control
- Gate driver for driving the three-phase inverter
- Power supply to power up the gate driver and MCU

These drives require a front-end power PFC regulator to shape the input current of the power supply and to meet the standards for power factor and current THD, such as IEC61000-2-3.

A PFC circuit shapes the input current of the power supply to be in phase with the mains voltage and helps to maximize the real power drawn from the mains. The front-end PFC also offers several benefits.

The following list highlights key benefits of the PFC circuit:

- **Reduces RMS input current**

For instance, a power circuit with a 230-V/5-A rating is limited to about 575 W of available power with a power factor (PF) of 0.5. Increasing the PF to 0.99 almost doubles the deliverable power to 1138 W, allowing the operation of higher power loads.

- **Facilitates power supply hold-up**

The active PFC circuit maintains a fixed, intermediate DC bus voltage that is independent of the input voltage so that the energy stored in the system does not decrease as the input voltage decreases. This maintenance allows the use of smaller, less expensive bulk capacitors.

- **Improves efficiency of downstream converters**

The PFC reduces the dynamic voltage range applied to the downstream inverters and converters. As a result, the voltage ratings of rectifiers can be reduced, resulting in lower forward drops. The operating duty-cycle can also be increased, resulting in lower current in the switches.

- **Increases the efficiency of the power distribution system**

A lower RMS current reduces distribution wiring losses.

- **Reduces the VA rating of standby power generators and stress on neutral conductors**

Reducing harmonics eliminates the risk of triplen harmonics (the third and multiples thereof) that can add up to dangerous levels in the neutral conductor of Y-connected three-phase systems.

This reference design is a boost power factor regulator implemented using the UCC28180 device as a PFC controller for use in all appliances that demand a power factor correction of up to 900 W. The design provides a ready platform of an active front-end to operate downstream inverters or DC-DC converters operating on a Hi-line AC voltage range from 195-V AC to 270-V AC.

Most appliances require a high efficiency over the entire operating voltage range and wide load variations from 50% to 100% of a load. This design demonstrates a high-performance power factor stage in a small form factor (149 mm x 94 mm) that operates from 195- to 270-V AC and delivers up to 900 W of continuous power output to drive inverters or converters at more than a 97% efficiency rate. The design also provides flexibility for the boost follower configuration, in which the boost voltage can be varied based

on AC input voltage, but only if the boosted voltage is above the peak input voltage. The boost follower configuration helps to reduce switching losses in the PFC regulator and the downstream inverter or converter. The design with boost follower configuration delivers an efficiency of approximately 98%. In comparison to fixed voltage operation, the boost follower configuration saves an additional 5.2 W of power at 230-V AC and a full load capacity.

The electromagnetic interference (EMI) filter at the front end of the circuit is designed to meet EN55011 class-A conducted emission levels. The design has a provision to disable the PFC power stage to achieve a very low level of standby power consumption. The design is fully tested and validated for various parameters such as regulation, efficiency, EMI signature, output ripple, start-up stresses, and switching stresses.

Above all, the design meets the key challenges of appliances to provide safe and reliable power with all protections built-in, while delivering a high performance with low power consumption and a low bill-of-material (BOM) cost.

3 Block Diagram

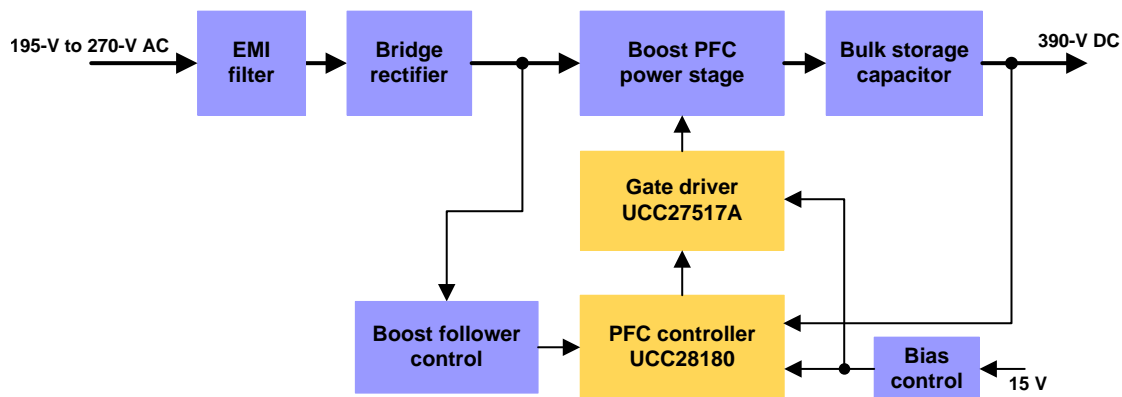


图 1. Block Diagram of PFC Regulator for Inverter Fed Drives

3.1 Highlighted Products and Key Advantages

The following subsections detail the highlighted products used in this reference design, including the key features for their selection. Refer to the respective product datasheet for complete details of any highlighted device.

3.1.1 UCC28180 – PFC Controller

To implement the high performance, small form factor PFC design at 900-W power, select the UCC28180 as the preferred controller, as it offers a series of benefits to address the next generation requirement of low THD standards for appliances.

The UCC28180 is a high performance, compact continuous conduction mode (CCM), 8-pin programmable frequency PFC controller. The wide and programmable operating frequency of the controller provides flexibility to design at a high frequency to optimize the components. The UCC28180 uses trimmed current loop circuits to achieve less than a 5% THD from a medium-to-full load (50% to 100%). A reduced current sense threshold enables the UCC28180 device to utilize a 50% smaller shunt resistor, resulting in lower power dissipation while maintaining low THD. The UCC28180 also consists of an integrated fast gate driver, with a drive of +2-A source current and -1.5-A sink current, which eliminates the requirement for an external gate driver.

The UCC28180 device also has a complete set of system protection features that greatly improve reliability and further simplify the design.

- Soft overcurrent
- Cycle-by-cycle peak current limit
- Output Overvoltage
- VCC undervoltage lockout (UVLO) protection
- Open pin protections (ISENSE and VSENSE pins)

3.1.2 UCC27517A – Low-Side Gate Driver

Obtaining a lower level of switching losses is important to achieve high efficiency. The switching losses of a MOSFET are a function of the drive current that is required to quickly pass through the Miller plateau region of the power-MOSFET's switching transition. Placing a high-current gate driver close to a FET allows for a faster turnon and turnoff by effectively charging and discharging voltage across the MOSFET's gate-to-drain parasitic capacitor (C_{GD}). This placement effectively reduces switching losses.

The UCC27517A is a simple, low-cost, low-side gate driver that offers a superior replacement for standard NPN and PNP discrete solutions, with a peak-source and sink current of 4 A. The UCC27517A is a single-channel, high-speed gate driver that has a symmetrical drive with the ability to handle negative input voltages (-5 V). The UCC27517A operates over a wide VDD range of 4.5 V to 18 V and a wide temperature range of -40°C to 140°C .

Other key features that make the device ideal for this application are:

- Fast propagation delays (13-ns typical)
- Outputs held low during VDD UVLO (to ensure glitch-free operation during power-up and power down)
- Logic thresholds with hysteresis for high noise immunity
- Output held low when input pins are floating
- 5-pin SOT-23 package to help optimize space

Using an additional gate driver is an optional means to further reduce the switching losses because the UCC28180 controller has an integrated fast gate driver of +2-A source current and -1.5 -A sink current, which is sufficient for the requirements of most applications.

4 System Design Theory

This reference design is a 900-W boost PFC regulator that operates in continuous conduction mode and is implemented using the UCC28180 PFC controller. The design is specifically tailored for inverter fed drives for use in home appliances, such as vacuum cleaners. This design serves as a simple and superior alternative to existing bulk, passive PFC circuits that are used to meet the power harmonic standards. This design is intended for operation at country-specific line voltages between 195- to 265-V AC. The system efficiency is greater than 97% over the wide input operating voltage range from 195- to 270-V AC, under full load conditions. Additionally, this design includes several embedded protections, that including output overvoltage protection and output short circuit protection.

The main focus of this design is a low EMI, high efficiency, high power factor, and protected DC power rail for targeted applications.

4.1 PFC Regulator Operating Mode

Power factor correction shapes the input current of the power supply to maximize the real power available from the mains. In addition, the use of PFC is important to comply with low harmonic (low THD) regulatory requirements, such as IEC61000-3-2. At the time of this writing, two modes of operation are widely utilized for PFC implementations: continuous conduction mode (CCM) and critical conduction mode (CrM). For higher power circuits, the topology of choice is the boost converter operating in continuous conduction mode (CCM) and with an average current mode control. For lower power applications, the critical conduction mode (CrM) boost topology is typically utilized.

For high power levels such as 900 W, utilizing CCM operation is preferable because it has lower peak and RMS currents. Lower peak currents significantly reduce the stress in the power MOSFET, diode, and inductor. Additionally, the filtering process is easier because the current moving through the boost inductor is more continuous. The switching frequency remains constant for the CCM operation, allowing for an easier design of the boost inductor and EMI filter.

4.2 PFC Circuit Component Design

The UCC28180 device operates at a fixed frequency in CCM mode and requires minimal external components for the implementation of a high wattage PFC regulator. The following subsections detail the design process and component selection for this design. All design calculations are available in the [TIDA-00443 Design Calculator](#).

4.2.1 Design Goal Parameters

The following [表 2](#) shows the design goal parameters for this design. These parameters are used in further calculations for the selection of components.

表 2. Design Goal Parameters

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{IN}	Input voltage	195		270	V-AC
f_{LINE}	Input frequency	47		63	Hz
OUTPUT					
V_{OUT}	Output voltage		390		V-DC
P_{OUT}	Output power			900	W
REGULATION					

表 2. Design Goal Parameters (continued)

PARAMETER		MIN	TYP	MAX	UNIT
	Line regulation			5%	
	Load regulation			5%	
PF	Targeted power factor		0.99		
η	Targeted efficiency		96%		

4.2.2 Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based upon the input current calculations. First, determine the maximum average output current, $I_{OUT(max)}$, as 公式 1 shows:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}}$$

$$I_{OUT(max)} = \frac{900 \text{ W}}{390 \text{ V}} = 2.31 \text{ A} \quad (1)$$

Calculate the maximum input RMS line current, $I_{IN_RMS(max)}$, in 公式 2 using the parameters from 表 2 and the efficiency and power factor:

$$I_{IN_RMS(max)} = \frac{P_{OUT(max)}}{\eta \times V_{IN(min)} \times PF}$$

$$I_{IN_RMS(max)} = \frac{900 \text{ W}}{0.96 \times 195 \text{ V} \times 0.99} = 4.86 \text{ A} \quad (2)$$

Based upon the calculated RMS values the maximum input current, $I_{IN(max)}$, and the maximum average input current, $I_{IN_AVG(max)}$ can be determined assuming the waveform is sinusoidal, as the following 公式 3 and 公式 4 show.

$$I_{IN(max)} = \sqrt{2} \times I_{IN_RMS(max)}$$

$$I_{IN(max)} = \sqrt{2} \times 4.86 \text{ A} = 6.87 \text{ A} \quad (3)$$

$$I_{IN_AVG(max)} = \frac{2}{\pi} \times I_{IN(max)}$$

$$I_{IN_AVG(max)} = \frac{2}{\pi} \times 6.87 \text{ A} = 4.34 \text{ A} \quad (4)$$

4.2.3 Switching Frequency

The UCC28180 switching frequency is user programmable with a single resistor on the FREQ pin to GND. This design uses a 100-KHz switching frequency, f_{sw} . Calculate the suitable resistor value to program the switching frequency using the following 公式 5:

$$R_{FREQ} = \frac{f_{TYP} \times R_{TYP} \times R_{INT}}{(f_{SW} \times R_{INT}) + (R_{TYP} \times f_{SW}) - (R_{TYP} \times f_{TYP})}$$

where

- f_{TYP} , R_{TYP} , and R_{INT} are constants internally fixed to the controller that are based on the UCC28180 control logic
 - $f_{TYP} = 65 \text{ KHz}$
 - $R_{TYP} = 32.7 \text{ k}\Omega$
 - $R_{INT} = 1 \text{ M}\Omega$
- (5)

Applying these constants in the preceding [公式 5](#) yields the appropriate resistor that must be placed between the FREQ and GND pins (see [公式 6](#)):

$$R_{\text{FREQ}} = \frac{65 \text{ kHz} \times 32.7 \text{ k}\Omega \times 1 \text{ M}\Omega}{(100 \text{ kHz} \times 1 \text{ M}\Omega) + (100 \text{ kHz} \times 32.7 \text{ k}\Omega) - (65 \text{ kHz} \times 32.7 \text{ k}\Omega)} = 21 \text{ k}\Omega \quad (6)$$

A typical value of 21.5 k Ω for the FREQ resistor results in a switching frequency of 98 kHz.

4.2.4 Bridge Rectifier

The maximum input AC voltage is 270-V AC, so the DC voltage can reach voltage levels of up to 385-V DC. Considering a safety factor of 30%, TI recommends to select a component with a voltage rating greater than 500-V DC. The input bridge rectifier must have an average current capability that exceeds the input average current ($I_{IN_AVG(max)}$). To optimize the power loss due to diode forward-voltage drop, use a higher-current bridge rectifier.

This design uses a 1000-V, 15-A, diode GBJ1508 for input rectification.

The forward voltage drop of the bridge rectifier diode, $V_{F_BRIDGE} = 0.85$ V.

Use the following 公式 7 to calculate the power loss in the input bridge, P_{BRIDGE} :

$$P_{BRIDGE} = 2 \times V_{F_BRIDGE} \times I_{IN_AVG(max)} = 2 \times 0.85 \text{ V} \times 4.34 \text{ A} = 7.38 \text{ W} \quad (7)$$

Be sure to select a heat sink of an appropriate size to maintain the operation within the safe operation area of the bridge rectifier.

4.2.5 Inductor Ripple Current

The UCC28180 is a CCM controller; however, if the chosen inductor allows relatively high-ripple current, the converter becomes forced to operate in discontinuous mode (DCM) at light loads and at the higher input voltage range. High-inductor ripple current affects the CCM/DCM boundary and results in a higher light-load THD. This type of current also affects the choices for the input capacitor, R_{SENSE} , and C_{ICOMP} values. Allowing an inductor ripple current, ΔI_{RIPPLE} , of 20% or less enables CCM operation over the majority of the operating range. However, this low inductor ripple current requires a boost inductor that has a higher inductance value, and the inductor itself is physically large. This design takes certain measures to optimize performance with size and cost. The inductor is sized to have a 40% peak-to-peak ripple current, with a focus on minimizing space and the knowledge that the converter operates in DCM at the higher input voltages and at light loads; however, the converter is well optimized for a nominal input voltage of 230-V AC at the full load.

4.2.6 Input Capacitor

The input capacitor must be selected based upon the input ripple current and an acceptable high frequency input voltage ripple. Allowing an inductor ripple current, ΔI_{RIPPLE} , of 40% and a high frequency voltage ripple factor, ΔV_{RIPPLE_IN} , of 2%, the maximum input capacitor value, C_{IN} , is calculated by first determining the input ripple current, I_{RIPPLE} , and the input voltage ripple, V_{IN_RIPPLE} , as the following 公式 8 shows:

$$\begin{aligned} I_{RIPPLE} &= \Delta I_{RIPPLE} \times I_{IN(max)} \\ I_{RIPPLE} &= 0.4 \times (\sqrt{2} \times 4.86 \text{ A}) = 2.75 \text{ A} \\ V_{IN_RIPPLE} &= \Delta V_{RIPPLE_IN} \times V_{IN_RECTIFIED(min)} \\ V_{IN_RIPPLE} &= 0.02 \times (\sqrt{2} \times 195 \text{ V}) = 5.52 \text{ V} \end{aligned} \quad (8)$$

The recommended value for the input X-capacitor can now be calculated in the following 公式 9:

$$\begin{aligned} C_{IN} &= \frac{I_{RIPPLE}}{8 \times f_{SW} \times V_{IN_RIPPLE}} \\ C_{IN} &= \frac{2.75 \text{ A}}{8 \times 98 \text{ kHz} \times 5.52 \text{ V}} = 0.635 \text{ } \mu\text{F} \end{aligned} \quad (9)$$

This design uses a standard value 0.68- μ F X2 film capacitor.

4.2.7 Boost Inductor

Based upon the allowable inductor ripple current that the preceding 节 4.2.5 details, the boost inductor, L_{BST} , is selected after determining the maximum inductor peak current, I_{L_PEAK} , as 公式 10 shows:

$$I_{L_PEAK(max)} = I_{IN(max)} + \frac{I_{RIPPLE}}{2}$$

$$I_{L_PEAK(max)} = 6.87 \text{ A} + \frac{2.75 \text{ A}}{2} = 8.245 \text{ A} \quad (10)$$

Calculate the minimum value of the boost inductor based upon the acceptable ripple current, I_{RIPPLE} , at a worst case duty cycle of 0.5, as 公式 11 shows:

$$L_{BST(min)} \geq \frac{V_{OUT} \times D \times (1-D)}{f_{SW} \times I_{RIPPLE}}$$

$$L_{BST(min)} \geq \frac{390 \text{ V} \times 0.5 \times (1-0.5)}{(98 \text{ kHz} \times 2.75 \text{ A})} \geq 360 \mu\text{H} \quad (11)$$

The actual value of the boost inductor used is $L_{BST} = 360 \mu\text{H}$.

The duty cycle of operation is a function of the rectified input voltage and changes continuously over the half-line cycle. The duty cycle, $DUTY_{(max)}$, can be calculated at the peak of the minimum input voltage, as 公式 12 shows:

$$DUTY_{(max)} = \frac{V_{OUT} - V_{IN_RECTIFIED(min)}}{V_{OUT}}$$

$$DUTY_{(max)} = \frac{390 \text{ V} - (1.414 \times 195 \text{ V})}{390 \text{ V}} = 0.293 \quad (12)$$

4.2.8 Boost Diode

The output diode must have a blocking voltage that exceeds the output overvoltage of the converter and average current same as $I_{OUT(max)}$. The output diode selected for this diode is the BYV29FX-600, a 600-V, 9-A diode.

Estimate the diode losses based on the forward-voltage drop, V_F , at 125°C and the reverse recovery charge, Q_{RR} , of the diode, as the following 公式 13 shows:

$$P_{DIODE} = V_{F_125C} \times I_{OUT(max)} + 0.5 \times f_{SW} \times V_{OUT} \times Q_{RR}$$

$$P_{DIODE} = 1.5 \text{ V} \times 2.31 \text{ A} + 0.5 \times 98 \text{ kHz} \times 390 \text{ V} \times 13 \text{ nC} = 3.71 \text{ W} \quad (13)$$

Despite the slightly more expensive price, by using a silicon carbide Schottky diode the user essentially eliminates the reverse recovery losses, which result in less power dissipation. For this design, the board was tested with a C3D04060A, 600-V, 7.5-A SiC diode.

公式 14 shows the estimated power loss with an SiC diode:

$$P_{DIODE} = 1.25 \text{ V} \times 2.31 \text{ A} + 0.5 \times 98 \text{ kHz} \times 390 \text{ V} \times 0 \text{ nC} = 2.89 \text{ W} \quad (14)$$

Use a heat sink of the appropriate size for the boost diode.

4.2.9 Switching Element

The MOSFET switch is driven by a GATE output that is clamped at 15.2 V internally for VCC bias voltages greater than 15.2 V. An external gate drive resistor is recommended to limit the rise time and to dampen any ringing caused by the parasitic inductances and capacitances of the gate drive circuit. This resistor also helps by meeting any EMI requirements of the converter. This design uses a 5.0- Ω resistor; the final value of any design depends on the parasitic elements associated with the layout of the design. To facilitate a fast turnoff, place a standard 100-V, 1-A Schottky diode or switching diode anti-parallel with the gate drive resistor. A 10-k Ω resistor is placed between the gate of the MOSFET and ground to discharge the gate capacitance and protect from inadvertent dV/dT triggered turnon.

公式 15 shows the drain-to-source RMS current, I_{DS_RMS} , which is calculated through switching FET.

$$I_{DS_RMS} = \frac{P_{OUT(max)}}{V_{IN_RECTIFIED(min)}} \times \sqrt{2 - \frac{16 \times V_{IN_RECTIFIED(min)}}{3 \times \pi \times V_{OUT}}}$$

$$I_{DS_RMS} = \frac{900 \text{ W}}{275 \text{ V}} \times \sqrt{2 - \left(\frac{16 \times 275 \text{ V}}{3 \times \pi \times 390 \text{ V}} \right)} = 2.93 \text{ A} \quad (15)$$

The maximum voltage across the FET is the maximum output boost voltage (that is, 425 V), which is the overvoltage set point of the PFC converter used to shut down the output. Considering a voltage de-rating of 30%, the voltage rating of the MOSFET must be greater than 550-V DC.

The TIDA-00443 design uses an IPP60R190P6 MOSFET of 600 V with 25 A at 25°C and 12 A at 100°C.

Estimate the conduction losses of the switch MOSFET in this design using the $R_{DS(on)}$ at 125°C, which is available in the device data sheet (see 公式 16):

$$P_{COND} = I_{DS_RMS}^2 \times R_{DS(on)}$$

$$P_{COND} = 2.93 \text{ A}^2 \times (0.37 \Omega) = 3.176 \text{ W} \quad (16)$$

The switching losses are estimated using the rise time, t_r , and fall time, t_f , of the MOSFET gate and the output capacitance losses (C_{OSS}), as 公式 17 shows.

$$P_{SW} = f_{SW} \left[0.5 \times V_{OUT} \times I_{IN(max)} \times (t_r + t_f) + 0.5 \times C_{OSS} \times V_{OUT}^2 \right]$$

$$P_{SW} = 98 \text{ kHz} \left[0.5 \times 390 \text{ V} \times 6.87 \text{ A} \times (12 \text{ ns} + 9 \text{ ns}) + 0.5 \times 61 \text{ pF} \times 390 \text{ V}^2 \right] = 3.212 \text{ W} \quad (17)$$

In 公式 18 the total FET losses calculate to:

$$P_{COND} + P_{SW} = 3.176 + 3.212 = 6.388 \text{ W} \quad (18)$$

Use a heat sink of the appropriate size for the MOSFET.

4.2.10 Sense Resistor

To accommodate the gain of the non-linear power limit, the sense resistor, R_{SENSE} , is sized such that it triggers the soft overcurrent at 10% higher than the maximum peak inductor current using the minimum soft overcurrent threshold of the ISENSE pin, V_{SOC} , where ISENSE is equal to 0.265 V. 公式 19 shows the calculations for R_{SENSE} considering the overload conditions:

$$R_{SENSE} = \frac{V_{SOC(min)}}{I_{L_PEAK(max)} \times 1.1}$$

$$R_{SENSE} = \frac{0.259 \text{ V}}{8.245 \text{ A} \times 1.1} = 0.0286 \Omega \quad (19)$$

The value selected for R_{SENSE} is 0.020 Ω .

A lower value of current sense is required to have normal full-load operation over the entire operating voltage range during the boost follower configuration.

The power dissipated across the sense resistor, P_{RSENSE} , must be calculated, as 公式 20 shows:

$$P_{RSENSE} = I_{IN_RMS(max)}^2 \times R_{SENSE}$$

$$P_{RSENSE} = 4.86 \text{ A}^2 \times 0.02 = 0.472 \text{ W} \quad (20)$$

The peak current limit, PCL, protection feature triggers when the current traveling through the sense resistor causes the voltage across R_{SENSE} to be equal to the V_{PCL} threshold. For a worst-case analysis, the maximum V_{PCL} threshold is used, as the following 公式 21 shows:

$$I_{PCL} = \frac{V_{PCL(max)}}{R_{SENSE}}$$

$$I_{PCL} = \frac{0.438 \text{ V}}{0.02} = 21.9 \text{ A} \quad (21)$$

To protect the ISENSE pin from inrush-surge current, the user can place a 220-Ω resistor, in series with the ISENSE pin. A 1000-pF capacitor is placed close to the device to improve noise immunity on the ISENSE pin.

4.2.11 Output Capacitor

The output capacitor, C_{OUT} , is sized to meet the hold-up requirements of the converter. Considering that the downstream converters require the output of the PFC stage to never fall below 290-V DC, $V_{OUT_HOLDUP(min)}$, during one line cycle of AC power loss ($t_{HOLDUP} = 1 / f_{LINE(min)}$), 公式 22 shows the minimum value for the output capacitor required to hold the voltage at 290-V DC for the t_{HOLDUP} time:

$$C_{OUT(min)} \geq \frac{2 \times P_{OUT(max)} \times t_{HOLDUP}}{V_{OUT}^2 - V_{OUT_HOLDUP(min)}^2}$$

$$C_{OUT(min)} \geq \frac{2 \times 900 \text{ W} \times 21.3 \text{ ms}}{(390 \text{ V}^2 - 290 \text{ V}^2)} = 564 \text{ } \mu\text{F} \quad (22)$$

TI recommends de-rating this capacitor value by 10% because the actual capacitor used is 660 μF.

Verifying that the maximum peak-to-peak output ripple voltage is less than 5% of the output voltage ensures that the ripple voltage does not trigger the output overvoltage or output undervoltage protection features of the controller. If the output ripple voltage is greater than 5% of the regulated output voltage, a larger output capacitor is required. The following 公式 23 calculates the maximum peak-to-peak ripple voltage (occurring at twice the line frequency), and the ripple current of the output capacitor:

$$V_{OUT_RIPPLE(pp)} < 0.05 \times V_{OUT}$$

$$V_{OUT_RIPPLE(pp)} < 0.05 \times 390 \text{ V} = 19.5 \text{ V}_{PP}$$

$$V_{OUT_RIPPLE(pp)} = \frac{I_{OUT(max)}}{2\pi \times 2 \times f_{LINE(min)} \times C_{OUT}}$$

$$V_{OUT_RIPPLE(pp)} = \frac{2.31 \text{ A}}{2\pi \times 2 \times 47 \text{ Hz} \times 660 \text{ } \mu\text{F}} = 5.925 \text{ V} \quad (23)$$

In 公式 24, the required ripple current rating at twice the line frequency, I_{COUT_2fline} , is equal to:

$$I_{COUT_2fline} = \frac{I_{OUT(max)}}{\sqrt{2}}$$

$$I_{COUT_2fline} = \frac{2.31 \text{ A}}{\sqrt{2}} = 1.634 \text{ A} \quad (24)$$

A high-frequency ripple current runs through the output capacitor, as 公式 25 shows:

$$I_{COUT_HF} = I_{OUT(max)} \times \sqrt{\frac{16 \times V_{OUT}}{3 \times \pi \times V_{IN_RECTIFIED(min)}} - 1.5}$$

$$I_{COUT_HF} = 2.31 \text{ A} \times \sqrt{\frac{16 \times 390 \text{ V}}{3 \times \pi \times 1.414 \times 195 \text{ V}} - 1.5} = 2.193 \text{ A} \quad (25)$$

In 公式 26, the total ripple current in the output capacitor, $I_{COUT_RMS(total)}$, is the combination of both I_{COUT_2fline} and I_{COUT_HF} . Select the output capacitor accordingly:

$$I_{\text{COUT_RMS(total)}} = \sqrt{(I_{\text{COUT_2fline}})^2 + (I_{\text{COUT_HF}})^2}$$
$$I_{\text{COUT_RMS(total)}} = \sqrt{(1.634)^2 + (2.193)^2} = 2.734 \text{ A} \quad (26)$$

4.2.12 Output Voltage Set Point

For low power dissipation and minimal contribution to the voltage set point, 9.96 M Ω is used for the top-voltage feedback divider resistor, R_{FB1} . Multiple resistors in series are used due to the maximum allowable voltage across each resistor. Using the internal 5-V reference, V_{REF} , the bottom divider resistor, R_{FB2} , is selected to meet the output voltage design goals, as 公式 27 shows.

$$R_{FB2} = \frac{V_{REF} \times R_{FB1}}{V_{OUT} - V_{REF}}$$

$$R_{FB2} = \frac{5 \text{ V} \times 1.0 \text{ M}\Omega}{390 \text{ V} - 5 \text{ V}} = 13.04 \text{ k}\Omega \quad (27)$$

A standard value 13-k Ω resistor for R_{FB2} results in a nominal output voltage set point of 391 V.

An output overvoltage is detected when the output voltage exceeds its nominal set-point level by 5%, as measured when the voltage at VSENSE is 105% of the reference voltage, V_{REF} (see 公式 28).

$$V_{OUT(ovd)} = V_{OVD} \times \left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right)$$

$$V_{OUT(ovd)} = (1.05 \times 5 \text{ V}) \times \frac{1.0 \text{ M}\Omega + 13 \text{ k}\Omega}{13 \text{ k}\Omega} = 410.7 \text{ V} \quad (28)$$

In the event of an extreme output overvoltage event, the GATE output is disabled if the output voltage exceeds its nominal set-point value by 9%. The output voltage, $V_{OUT(ovp)}$, at which this protection feature is triggered, calculates as the following 公式 29:

$$V_{OUT(ovp)} = 1.09 \times V_{REF} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} = 426.4 \text{ V} \quad (29)$$

An output undervoltage is detected when the output voltage falls below 5% of its nominal set-point as measured when the voltage at VSENSE is 95% of the reference voltage, V_{REF} (see 公式 30):

$$V_{OUT(uvp)} = V_{UVD} \times \left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right)$$

$$V_{OUT(uvp)} = (0.95 \times 5 \text{ V}) \times \frac{1.0 \text{ M}\Omega + 13 \text{ k}\Omega}{13 \text{ k}\Omega} = 371.6 \text{ V} \quad (30)$$

The user must add a small capacitor on the VSENSE to filter out noise. Limit the value of the filter capacitor such that the RC time constant is limited to approximately 10 μ s, so as not to significantly reduce the control response time to output voltage deviations (see 公式 31).

$$C_{VSENSE} = \frac{10 \mu\text{s}}{R_{FB2}} = 769 \text{ pF} \quad (31)$$

In this design, the closest standard value of 820 pF was used on the VSENSE pin for a time constant of 10.66 μ s.

4.2.13 Control Loop Compensation

The UCC28180 controller requires two loops to accomplish regulation. The inner current loop shapes the average input current to match the sinusoidal input voltage under continuous inductor current conditions. The outer voltage loop regulates the PFC output voltage by generating a voltage on V_{COMP} (depending on the line and load conditions), which determines the internal gain parameters for maintaining a low-distortion, steady-state, input-current wave shape.

For compensation of the current loop, first determining the product of the internal loop variables, $M_{1,2}$, using the internal controller constants K_1 and K_{FQ} . Compensation is optimized for a maximum load and nominal input voltage. This design uses a 230-V AC for the nominal line voltage:

$$M_{1,2} = \frac{I_{OUT(max)} \times V_{OUT}^2 \times 2.5 \times R_{SENSE} \times K_1}{\eta \times V_{IN_RMS}^2 \times K_{FQ}} \quad (32)$$

where

$$K_{FQ} = \frac{1}{f_{SW}} = \frac{1}{98 \text{ kHz}} = 10.2 \mu\text{s}$$

$$K_1 = 7$$

The $M_{1,2}$ calculates to the following 公式 33:

$$M_{1,2} = \frac{2.31 \text{ A} \times 390 \text{ V}^2 \times 2.5 \times 0.02 \Omega \times 7}{0.96 \times 230 \text{ V}^2 \times 10.2 \mu\text{s}} = 0.238 \frac{\text{V}}{\mu\text{s}} \quad (33)$$

The following 图 2 shows the V_{COMP} operating point. After obtaining the $M_{1,2}$ result from the preceding 公式 33, find the resultant V_{COMP} voltage at that operating point to calculate the individual M_1 and M_2 components.

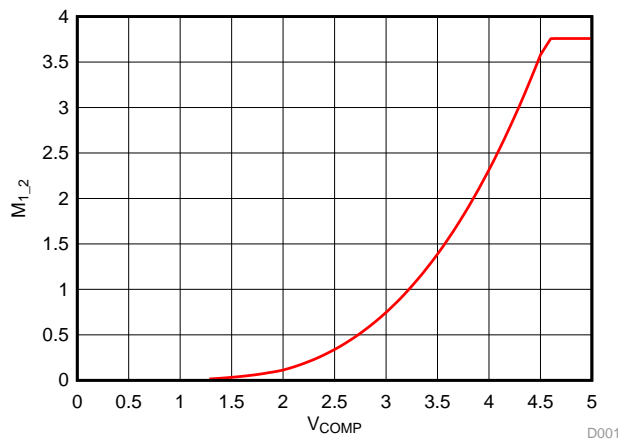


图 2. $M_{1,2}$ Versus V_{COMP}

For the given $M_{1,2}$ of 0.238 V/μs, the V_{COMP} is approximately equal to 2.4 V, as the preceding 图 2 shows. The individual loop factors, M_1 (current loop gain factor) and M_2 (voltage loop PWM ramp slope), are calculated using the conditions in 公式 34.

The M_1 non-linear current loop gain factor has the following characteristics:

$$\begin{aligned}
 &\text{If } (V_{\text{COMP}} < 1 \text{ V}), \text{ then } (M_1 = 0.068) \\
 &\text{If } (1 \text{ V} < V_{\text{COMP}} < 2 \text{ V}), \text{ then } (M_1 = 0.156 \times V_{\text{COMP}} - 0.088) \\
 &\text{If } (2 \text{ V} < V_{\text{COMP}} < 4.5 \text{ V}), \text{ then } (M_1 = 0.313 \times V_{\text{COMP}} - 0.401) \\
 &\text{If } (4.5 \text{ V} < V_{\text{COMP}} < 5 \text{ V}), \text{ then } (M_1 = 1.007)
 \end{aligned} \tag{34}$$

According to the graph in 图 2, in this design the V_{COMP} is approximately equal to 2.58 V, so M_1 is calculated to be approximately equal to 0.407 in the following 公式 35:

$$M_1 = 0.313 \times 2.4 \text{ V} - 0.401 = 0.35 \tag{35}$$

The M_2 non-linear PWM ramp slope complies with the relationships in the following 公式 36:

$$\begin{aligned}
 &\text{If } (V_{\text{COMP}} \leq 0.5 \text{ V}), \text{ then } \left(M_2 = 0 \frac{\text{V}}{\mu\text{s}} \right) \\
 &\text{If } (0.5 \text{ V} \leq V_{\text{COMP}} \leq 4.6 \text{ V}), \text{ then } \left(M_2 = \frac{f_{\text{SW}}}{65 \text{ kHz}} \times 0.1223 \times [V_{\text{COMP}} - 0.5]^2 \frac{\text{V}}{\mu\text{s}} \right) \\
 &\text{If } (4.6 \text{ V} \leq V_{\text{COMP}} \leq 5 \text{ V}), \text{ then } \left(M_2 = \frac{f_{\text{SW}}}{65 \text{ kHz}} \times 2.056 \frac{\text{V}}{\mu\text{s}} \right)
 \end{aligned} \tag{36}$$

In this TIDA-00443 design, with the V_{COMP} approximately equal to 2.58 V, the M_2 equals 0.665 V/ μ s as the following 公式 37 shows:

$$M_2 = \frac{98 \text{ kHz}}{65 \text{ kHz}} \times 0.1223 \times (2.4 - 0.5)^2 \frac{\text{V}}{\mu\text{s}} = 0.665 \frac{\text{V}}{\mu\text{s}} \tag{37}$$

Verify that the product of the individual gain factors, M_1 and M_2 , is approximately equal to the $M_{1,2}$ factor from the preceding 公式 32. If these values are not approximately equal, iterate the V_{COMP} value and recalculate $M_{1,2}$, as the following 公式 38 shows:

$$M_1 \times M_2 = 0.35 \times 0.665 \frac{\text{V}}{\mu\text{s}} = 0.232 \frac{\text{V}}{\mu\text{s}} \tag{38}$$

公式 39 shows that the product of M_1 and M_2 is within 1% of the $M_{1,2}$ factor previously calculated in 公式 32.

$$\begin{aligned}
 &M_1 \times M_2 \cong M_{1,2} \\
 &0.232 \frac{\text{V}}{\mu\text{s}} \cong 0.238 \frac{\text{V}}{\mu\text{s}}
 \end{aligned} \tag{39}$$

Now the non-linear gain variable, M_3 , can be calculated, as 公式 40 shows:

$$\begin{aligned}
 &\text{If } (V_{\text{COMP}} < 0.5 \text{ V}), \text{ then } (M_3 = 0) \\
 &\text{If } (0.5 \text{ V} < V_{\text{COMP}} < 1 \text{ V}), \text{ then } \left(M_3 = \frac{f_{\text{SW}}}{65 \text{ kHz}} \times \frac{\text{V}}{\mu\text{s}} \times [0.0166 \times V_{\text{COMP}} - 0.0083] \right) \\
 &\text{If } (1 \text{ V} < V_{\text{COMP}} < 2 \text{ V}), \text{ then } \left(M_3 = \frac{f_{\text{SW}}}{65 \text{ kHz}} \times \frac{\text{V}}{\mu\text{s}} \times [0.0572 \times V_{\text{COMP}}^2 - 0.0597 \times V_{\text{COMP}} + 0.0155] \right) \\
 &\text{If } (2 \text{ V} < V_{\text{COMP}} < 4.5 \text{ V}), \text{ then } \left(M_3 = \frac{f_{\text{SW}}}{65 \text{ kHz}} \times \frac{\text{V}}{\mu\text{s}} \times [0.1148 \times V_{\text{COMP}}^2 - 0.1746 \times V_{\text{COMP}} + 0.0586] \right) \\
 &\text{If } (4.5 \text{ V} < V_{\text{COMP}} < 4.6 \text{ V}), \text{ then } \left(M_3 = \frac{f_{\text{SW}}}{65 \text{ kHz}} \times \frac{\text{V}}{\mu\text{s}} \times [0.1148 \times V_{\text{COMP}}^2 - 0.1746 \times V_{\text{COMP}} + 0.0586] \right) \\
 &\text{If } (4.6 \text{ V} < V_{\text{COMP}} < 5 \text{ V}), \text{ then } (M_3 = 0)
 \end{aligned} \tag{40}$$

In this design, using 2.58 V for the V_{COMP} , M_3 calculates to 1.035 V/ μ s in the following 公式 41:

$$M_3 = \frac{98 \text{ kHz}}{65 \text{ kHz}} \times \frac{\text{V}}{\mu\text{s}} \times (0.1148 \times 2.4^2 - 0.1746 \times 2.4 + 0.0586) = 0.453 \frac{\text{V}}{\mu\text{s}} \quad (41)$$

For designs with high inductor ripple current, the current averaging pole, which functions to flatten out the ripple current on the input of the PWM comparator, must be placed at least a decade before the converter switching frequency. The completed converter may require an analysis to determine the ideal compensation pole for the current averaging circuit, because having too large of a capacitor on the ICOMP adds phase lag and increases i_{THD} . However, having too small of an ICOMP capacitor results in inadequate averaging and an unstable current averaging loop. This design uses an approximate 3.5 KHz for the frequency of the current averaging pole, f_{IAVG} , because the current ripple factor, ΔI_{RIPPLE} , is selected to be 40% at the onset of the design process, which can be large enough to force DCM operation and result in relatively-high inductor ripple current. As 公式 42 shows, determine the required capacitor on the ICOMP pin, C_{ICOMP} , using the transconductance gain, g_{mi} , of the internal current amplifier:

$$C_{ICOMP} = \frac{g_{mi} \times M_1}{2\pi \times K_1 \times f_{IAVG}}$$

$$C_{ICOMP} = \frac{0.95 \text{ ms} \times 0.35}{2\pi \times 7 \times 3.5 \text{ kHz}} = 2161 \text{ pF} \quad (42)$$

A standard value 2700-pF capacitor for C_{ICOMP} results in a current averaging pole frequency of 3.26 KHz, as the following 公式 43 shows:

$$f_{IAVG} = \frac{0.95 \text{ ms} \times 0.35}{2\pi \times 7 \times 2700 \text{ pF}} = 2.803 \text{ kHz} \quad (43)$$

图 3 shows the plot of the transfer function of the current loop (see 公式 44).

$$G_{CL}(f) = \frac{V_{OUT} \times 2.5 \times R_{SENSE} \times K_1}{M_1 \times M_2 \times K_{FQ} \times L_{BST}} \times \frac{1}{s(f) + \frac{s(f)^2 \times K_1 \times C_{ICOMP}}{g_{mi} \times M_1}}$$

$$G_{CLdB}(f) = 20 \log(|G_{CL}(f)|) \quad (44)$$

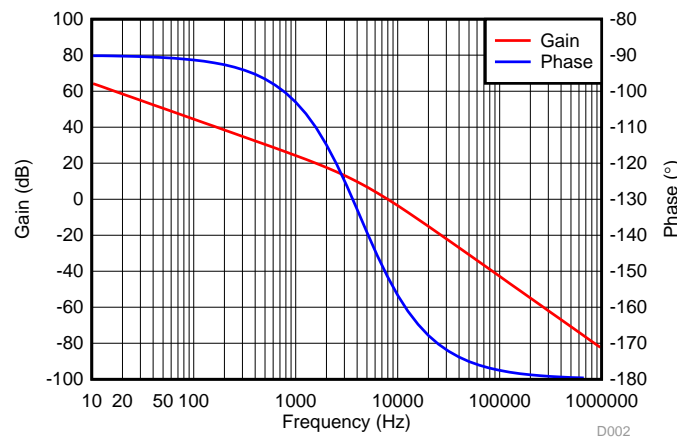


图 3. Bode Plot of Current Averaging Circuit

The voltage transfer function, $G_{VL}(f)$ contains the product of the voltage feedback gain, G_{FB} , and the gain from the PWM to the power stage, G_{PWM_PS} , which includes the PWM to the power stage pole, f_{PWM_PS} (see 公式 45, 公式 46, and 公式 47). 图 4 shows the plotted result.

$$G_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$

$$G_{FB} = \frac{13 \text{ k}\Omega}{1 \text{ M}\Omega + 13 \text{ k}\Omega} = 0.013 \quad (45)$$

$$f_{PWM_PS} = \frac{1}{2\pi \times \frac{C_{OUT} \times V_{OUT}^3 \times 2.5 \times R_{SENSE} \times K_1}{M_1 \times M_2 \times K_{FQ} \times V_{IN(nom)}^2}}$$

$$f_{PWM_PS} = \frac{1}{2\pi \times \frac{660 \mu\text{F} \times 390 \text{ V}^3 \times 2.5 \times 0.027 \Omega \times 7}{0.407 \times 0.798 \frac{\text{V}}{\mu\text{s}} \times 10.2 \mu\text{s} \times 230 \text{ V}^2}} = 1.48 \text{ Hz} \quad (46)$$

$$G_{PWM_PS}(f) = \frac{\left(\frac{M_3 \times V_{OUT}}{M_1 \times M_2 \times 1 \text{ V}} \right)}{1 + \frac{s(f)}{2\pi \times f_{PWM_PS}}}$$

$$G_{VL}(f) = G_{FB} \times G_{PWM_PS}(f)$$

$$G_{VLdB}(f) = 20 \log(|G_{VL}(f)|) \quad (47)$$

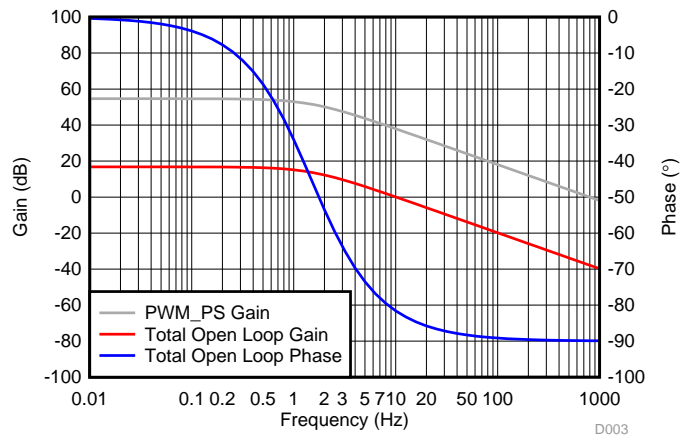


图 4. Bode Plot of Open Voltage Loop Without Error Amplifier

The voltage error amplifier is compensated with a zero, f_{ZERO} , at the f_{PWM_PS} pole. Place a pole, f_{POLE} , at 20 Hz to reject high frequency noise and roll off the gain amplitude. The desired value for the overall voltage loop crossover, f_V , is 10 Hz. Select the compensation components of the voltage error amplifier according to the calculations in 公式 48:

$$f_{ZERO} = \frac{1}{2\pi \times R_{VCOMP} \times C_{VCOMP}}$$

$$f_{POLE} = \frac{1}{2\pi \times \frac{R_{VCOMP} \times C_{VCOMP} \times C_{VCOMP_P}}{C_{VCOMP} + C_{VCOMP_P}}}$$

$$G_{EA}(f) = \left[\frac{1 + s(f) \times R_{VCOMP} \times C_{VCOMP}}{(C_{VCOMP} + C_{VCOMP_P}) \times s(f) \times \left[1 + s(f) \times \left(\frac{R_{VCOMP} \times C_{VCOMP} \times C_{VCOMP_P}}{C_{VCOMP} + C_{VCOMP_P}} \right) \right]} \right] \quad (48)$$

From the previous 图 4, the gain of the voltage transfer function at 10 Hz is approximately -0.387 dB. Estimating that the parallel capacitor, C_{VCOMP_P} , is much smaller than the series capacitor, C_{VCOMP} , the unity gain is at f_V , and the zero is at f_{PWM_PS} , the user can determine the series compensation capacitor in 公式 49:

$$f_V = 10 \text{ Hz}$$

$$C_{VCOMP} = \frac{g_{mv} \times \frac{f_V}{f_{PWM_PS}}}{2\pi \times f_V \times \left(10^{\frac{0 - G_{VLdB}(f)}{20}} \right)}$$

$$C_{VCOMP} = \frac{56 \mu\text{s} \times \frac{10 \text{ Hz}}{1.48 \text{ Hz}}}{2\pi \times 10 \text{ Hz} \times \left(10^{\frac{0.387 \text{ dB}}{20}} \right)} = 5.76 \mu\text{F} \quad (49)$$

The capacitor for V_{COMP} must have a voltage rating that is greater than the absolute maximum voltage rating of the V_{COMP} pin, which is 7 V. The readily-available standard value capacitor has a value of 4.7 μF , which is the value used for C_{VCOMP} in this design. This capacitor is rated for at least 10 V and is in the package size that fits the application.

Calculate the R_{VCOMP} in 公式 51 using the actual C_{VCOMP} capacitor value in the following 公式 50:

$$C_{VCOMP} = 4.7 \mu\text{F} \quad (50)$$

$$R_{VCOMP} = \frac{1}{2\pi \times f_{ZERO} \times C_{VCOMP}}$$

$$R_{VCOMP} = \frac{1}{2\pi \times 1.5 \text{ Hz} \times 4.7 \mu\text{F}} = 22.6 \text{ k}\Omega \quad (51)$$

The R_{VCOMP} uses a 23.7-k Ω resistor, as 公式 52 shows:

$$C_{VCOMP_P} = \frac{C_{VCOMP}}{2\pi \times f_{POLE} \times R_{VCOMP} \times C_{VCOMP} - 1}$$

$$C_{VCOMP_P} = \frac{4.7 \mu\text{F}}{2\pi \times 20 \text{ Hz} \times 23.7 \text{ k}\Omega \times 4.7 \mu\text{F} - 1} = 0.362 \mu\text{F} \quad (52)$$

The C_{VCOMP_P} uses a 0.39- μ F capacitor.

The total closed-loop transfer function, G_{VL_total} , contains the combined stages (see 公式 53); see the plot in 图 5.

$$G_{VL_total}(f) = G_{FB}(f) \times G_{PWM_PS}(f) \times G_{EA}(f)$$

$$G_{VL_totaldB}(f) = 20 \log(|G_{VL_total}(f)|) \tag{53}$$

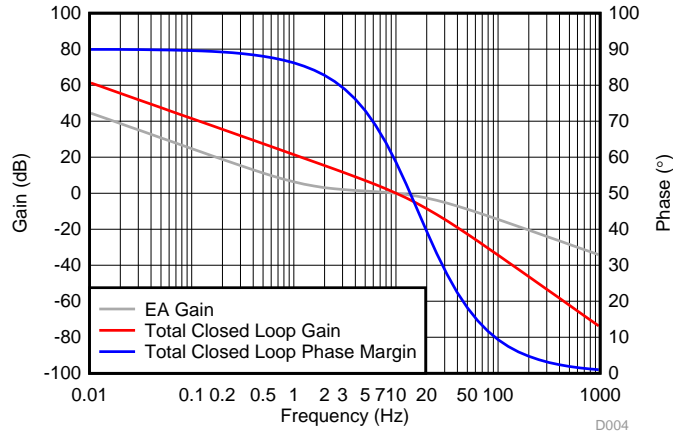


图 5. Closed-Loop Voltage Bode Plot

4.3 Boost Follower Control Circuit

The traditional design of PFC boost converters consists of a fixed output voltage greater than the maximum peak line voltage to maintain boost operation and be able to shape the input current waveform of the power supply. The boost voltage does not have to be fixed, but can be varied based on the AC input voltage provided that the boosted voltage is above the peak input voltage. The boost follower control circuit aids in setting the output voltage based on the peak input voltage. 图 6 shows how a boost follower and the output voltage of a conventional PFC boost regulator respond with changes in input voltage $V_{IN}(t)$.

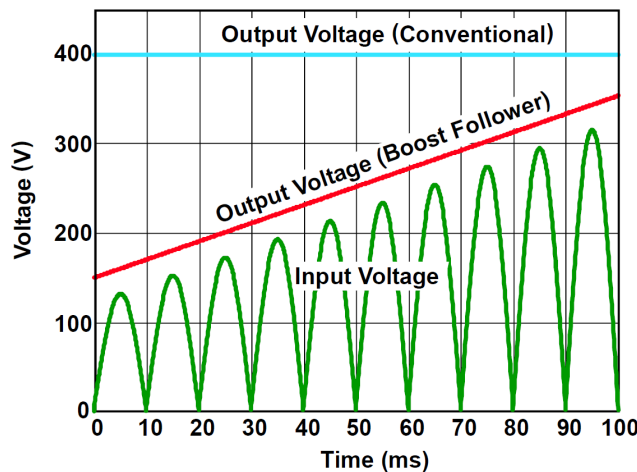


图 6. Variations of Tradition PFC Boost and PFC Boost Follower With Input Voltage

Varying the output voltage with variations in the peak line voltage provides several benefits.

- **Reduced boost inductor**

The boost inductor is selected based on the maximum allowed ripple current, at maximum duty cycle, at minimum line voltage, and at minimum output voltage. A decrease in V_{OUT} results in a decrease in the maximum duty cycle, which causes the boost inductor to decrease.


- **Reduced boost switch losses at low line operation**

In an offline PFC converter, a large amount of converter power loss is due to the switching losses of the boost FET). The boost follower PFC has a much lower output voltage at the low-input line voltage than a traditional PFC boost, which reduces the switching losses.

- **Reduced switching losses in the downstream inverter stage and isolated DC-DC converter stage**

The switching losses in a three-phase inverter drive or isolated DC-DC converter stage are proportional to the boost regulated voltage. A lower output voltage results in lower switching losses, increasing the overall efficiency of the system, which is more noticeable in the light-load efficiency of the power stage.

4.3.1 Boost Follower Circuit Description

Designing a boost follower PFC configuration with a UCC28180 PFC controller is simple and only requires five additional components. The following  shows the required additional circuitry.

The additional components R₃, R₄, R₅, C₁, Q₁, and D₁ are used to sink additional current out of the voltage amplifier's inverting signal in the voltage feedback loop. R₁ and R₂ are part of the voltage feedback circuit of the UCC28180 controller. As the rectified line voltage increases or decreases, Q₁ draws a proportional output current through R₁, causing the output voltage to change proportionately to the line voltage changes. The diode D₁ is used to offset the temperature variations in the base emitter junction (V_{be}) of Q₁. Capacitors C₁ and R₄ form a low-pass filter that removes the ripple voltage caused by the rectified line voltage.

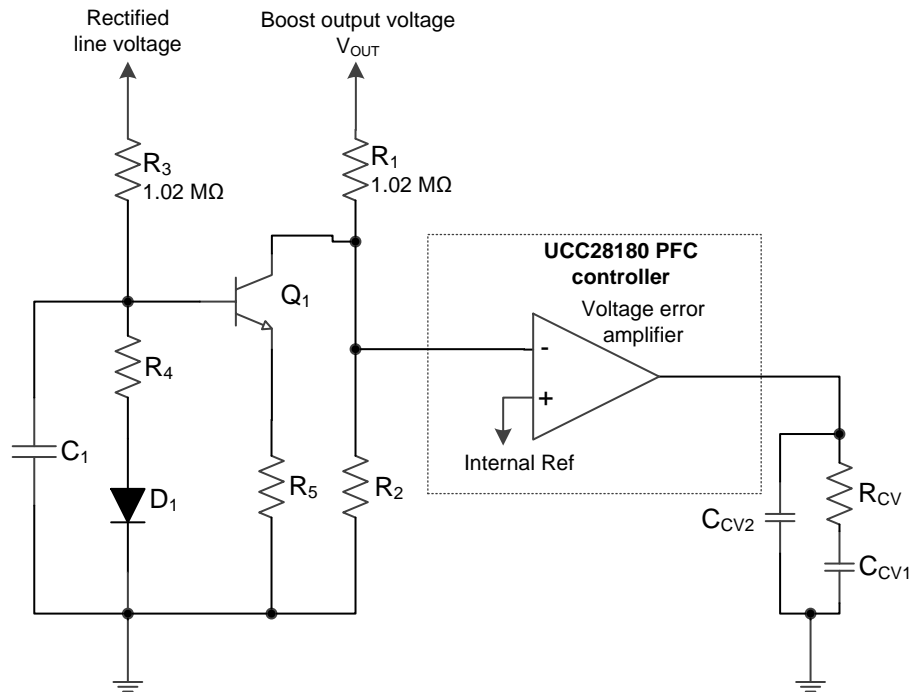


图 7. Five Additional Components for Boost Follower Circuit Implementation

4.3.2 Component Design for Boost Follower Control Circuit

The design of the boost follower control circuit is made to vary the output voltage 290-V DC to 400-V DC for an AC input voltage range of 195-V AC ($V_{IN(min)}$) to 270-V AC ($V_{IN(max)}$). The first step in designing this circuit is setting up the voltage divider network R_1 and R_2 .

Considering $R_1 = 1.02 \text{ M}\Omega$, $V_{OUT(min)} = 290 \text{ V}$, and $V_{REF} = 5.0 \text{ V}$ (internal voltage reference of controller) the $R_{dwn} = R_2 + R_5$ in 公式 54 is calculated as:

$$R_2 = \frac{2 \times R_1 \times V_{REF}}{V_{OUT(min)} - V_{REF}}$$

$$R_2 = \frac{2 \times 1.02 \text{ M}\Omega \times 5}{290 \text{ V} - 5 \text{ V}} = 35.8 \text{ k}\Omega \quad (54)$$

R_2 is divided between R_5 and R_2 in a 1:2 ratio, which means that R_2 can be simplified in the following 公式 55:

$$R_2 = \frac{35.8 \text{ k}\Omega}{3} \times 2 = 23.8 \text{ k}\Omega$$

$$R_5 = \frac{36.8 \text{ k}\Omega}{2} = 11.93 \text{ k}\Omega \quad (55)$$

The voltage divider formed by R_3 and R_4 is used in the setup to vary the voltage at the base of Q_1 from 2.0 V to 3.0 V. Take care to avoid saturating the transistor. The following 公式 56 is used to calculate R_4 :

$$R_4 = \frac{R_3 \times (V_{QB(\min)} - V_D)}{V_{IN(\min)} \times 0.9}$$

where

- $V_{QB(\min)}$ is the voltage at the base of Q_1 when the input voltage is minimized at 195-V AC RMS
 - V_D is the forward diode drop of D_1
- (56)

$$R_4 = \frac{1.02 \text{ M}\Omega \times (2.0 \text{ V} - 0.3 \text{ V})}{195 \text{ V} \times 0.9} = 9.88 \text{ k}\Omega$$

This design uses a standard resistor of 10 k Ω .

The capacitor C_1 is used to filter the voltage ripple on the rectified line. To limit the third harmonic current distortion, the filter is set up to attenuate the line frequency to 1.5% of the maximum voltage at the base of Q_1 . In the following 公式 57, C_1 is calculated as:

$$C_1 = \left[\left(\frac{R_4}{R_3 + R_4} \right) \times \left(\frac{V_{IN(\max)} \times 0.9}{V_{QB(\max)} \times 0.015} - 1 \right) \right] \times \left[\frac{1}{2\pi \times 2 \times f_{\text{line}} \times R_4} \right]$$

$$C_1 = \left[\left(\frac{10 \text{ k}\Omega}{1.02 \text{ M}\Omega + 10 \text{ k}\Omega} \right) \times \left(\frac{270 \text{ V} \times 0.9}{3.0 \text{ V} \times 0.015} - 1 \right) \right] \times \left[\frac{1}{2\pi \times 47 \times 2 \times 10 \text{ k}\Omega} \right] = 8.88 \text{ }\mu\text{F}$$
(57)

This design uses a standard capacitor value of 10 μF for C_1 .

The preceding values were tested on the board; see the improvement in efficiency in the plot of 图 8.

4.4 Bias Power

The TIDA-00443 design requires an external bias supply to power the UCC28180 PFC controller UCC27517A gate driver, and relay, which is used to shunt the inrush current limiting resistor.

TI recommends powering these devices from a regulated auxiliary supply. These devices are not intended to be used from a bootstrap bias supply. A bootstrap bias supply is fed from the input high voltage through a resistor with sufficient capacitance on the VCC pin to hold the voltage on the VCC pin until the current can be supplied from a bias winding on the boost inductor.

The auxiliary power supply is usually generated as a part of the main system by using a high-voltage buck converter power stage. The buck converter power stage can be implemented using an independent, low-cost PWM controller such as the UCC28722 (see the [TIDU850](#) user's guide). The bias supply voltage must be higher than the UVLO of the controllers used on board. The UCC28180 device has a UVLO of 11.5 V and the UCC27517A device has a UVLO of 4.5 V, whereas the minimum voltage required to turn on the relay is 9.6 V (for a 12-V relay), so the bias voltage for board operation must be ≥ 12 V. The total current required for these devices is approximately 55 mA.

TI recommends the use of an external bias power supply of 12 V to 16 V per 60 mA to power the board independently. The board has been tested and validated with a 15-V bias supply.

5 Getting Started Hardware

5.1 Test Conditions

For the input, the power supply source (V_{IN}) must range from 195- to 270-V AC. Set the input current limit of the input AC source to 7.5 A.

For the output, use an electronic variable load or a variable resistive load, which must be rated for ≥ 400 V and must vary the load current from 0 mA to 2.8 A.

5.2 Required Equipment

1. Isolated AC source
2. Single-phase power analyzer
3. Digital oscilloscope
4. Multimeters
5. Electronic load or resistive load

5.3 Procedure

1. Connect input terminals (pin-1 and pin-3 of connector J1) of the reference board to the AC power source
2. Connect output terminals (pin-1 and pin-3 of connector J2) to the electronic load, maintaining correct polarity (pin-1 is the VDC output and pin-3 is the GND terminal)
3. Set and maintain a minimum load of about 10 mA
4. Connect an auxiliary supply of 15 V between pin-1 and pin-2 of connector J3, maintaining correct polarity (pin-1 is the bias supply positive input and pin-2 is the GND terminal)
5. For independent testing of the board, short pin-1 and pin-3 of connector J3
6. Turn on the auxiliary supply and set a voltage of 15 V
7. Gradually increase the input voltage from 0 V to turn on the voltage of 195-V AC
8. Turn on the load to draw current from the output terminals of the PFC
9. Observe the startup conditions for smooth-switching waveforms

6 Test Results

The test results are divided in multiple sections that cover the steady-state performance measurements, functional performance waveforms and test data, transient performance waveforms, thermal measurements, conducted emission measurements, surge measurements, and EFT measurements.

6.1 Performance Data

6.1.1 Efficiency and Regulation With Load Variation

The following 表 3 and 表 4 show the data at a 230-V AC input.

表 3. Performance Data With SiC Diode-C3D04060A for Boost Diode (D1)

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	i_{THD} (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)	% REG
230	0.18	0.56	22.7	23.21	390.8	0.05	19.5	85.9	-0.02
230	0.25	0.75	43.0	32.98	390.8	0.10	39.6	92.2	-0.01
230	0.49	0.92	103.4	21.00	390.9	0.25	98.9	95.6	0.00
230	0.91	0.97	203.3	15.16	390.9	0.50	197.0	96.9	0.01
230	1.32	0.99	301.9	8.33	390.9	0.75	293.6	97.2	0.02
230	1.76	0.99	402.0	1.95	391.0	1.00	391.4	97.4	0.02
230	2.19	1.00	502.2	1.60	391.0	1.25	489.5	97.5	0.02
230	2.62	1.00	602.1	1.85	390.9	1.50	587.2	97.5	0.02
230	3.06	1.00	702.7	2.30	390.9	1.75	684.9	97.5	0.01
230	3.49	1.00	803.0	2.60	390.9	2.00	782.5	97.4	0.00
230	4.04	1.00	927.5	2.93	390.7	2.31	903.3	97.4	-0.04

表 4. Performance Data With Ultra-Fast Power Diode-BYV29FX-600 for Boost Diode (D1)

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	i_{THD} (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFFICIENCY (%)	% REG
230	0.18	0.58	23.4	23.50	390.1	0.05	19.4	82.95	-0.04
230	0.24	0.77	42.8	28.90	390.1	0.10	39.1	91.37	-0.03
230	0.49	0.92	103.8	22.47	390.1	0.25	98.5	94.93	-0.03
230	0.91	0.97	203.8	13.00	390.1	0.50	196.4	96.36	-0.03
230	1.34	0.99	304.2	3.48	390.1	0.75	294.2	96.70	-0.02
230	1.78	0.99	405.6	1.62	390.2	1.01	392.9	96.87	-0.01
230	2.21	1.00	505.5	1.59	390.2	1.26	489.8	96.88	0.01
230	2.65	1.00	606.2	1.84	390.3	1.50	587.1	96.84	0.03
230	3.09	1.00	707.7	2.16	390.4	1.75	684.8	96.77	0.06
230	3.53	1.00	809.2	2.56	390.4	2.00	782.4	96.68	0.05
230	4.06	1.00	933.8	2.80	390.3	2.31	902.3	96.63	0.02

6.1.2 Efficiency and Regulation With Line Variation (AC Input)

The following 表 5 shows the data for the efficiency and line regulation of the output with AC input voltage variation.

表 5. With Fixed Output Voltage Set to 390-V DC

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	i_{THD} (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	POWER LOSS (W)	EFFICIENCY (%)	% REG
195	4.787	0.999	933.50	3.086	390.39	2.31	901.80	31.7	96.6	-0.08
215	4.341	0.998	930.50	3.034	390.54	2.31	902.15	28.4	97.0	-0.04
230	4.030	0.998	927.90	2.879	390.65	2.31	902.40	25.5	97.3	-0.01
245	3.784	0.997	926.10	3.004	390.78	2.31	902.70	23.4	97.5	0.02
260	3.561	0.997	924.50	2.913	390.86	2.31	902.89	21.6	97.7	0.04
270	3.432	0.997	923.60	3.060	390.90	2.31	902.98	20.6	97.8	0.05

The output voltage varies with the variation of input voltage, so the output power is fixed to 900 W at each of the below measurements in 表 6.

表 6. With Boost Follower Configuration

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	i_{THD} (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	POWER LOSS (W)	EFFICIENCY (%)	POWER SAVING
195	4.831	0.974	911.50	22.490	338.97	2.62	886	25.1	97.2	6.61
215	4.331	0.992	924.10	11.700	353.68	2.55	902	22.6	97.6	5.78
230	4.007	0.997	919.90	4.320	362.29	2.48	900	20.3	97.8	5.16
245	3.762	0.997	919.50	3.067	372.28	2.42	901	18.6	98.0	4.82
260	3.523	0.997	914.60	2.913	382.61	2.34	896	18.1	98.0	3.47
270	3.398	0.996	915.70	2.720	389.32	2.30	897	19.1	97.9	1.52

6.1.3 Stand-By Power

The stand-by power was noted at multiple AC input voltages with a 900-k Ω load on the output DC bus and with the PFC controller disabled. The following 表 7 shows the tabulated results.

表 7. No-Load Power Measurement

V_{INAC} (V-AC)	I_{INAC} (mA)	P_{INAC} (W)	V_{OUT} (V)	I_{OUT} (mA) ($R_L = 900\text{ k}\Omega$)	P_{OUT} (W)	NO LOAD POWER (W)
195	72.6	0.51	274	0.30	0.08	0.43
230	85.8	0.75	324	0.36	0.12	0.64
270	100.4	1.05	378	0.42	0.16	0.89

The no load power is contributed by three main branches:

- Resistors used to discharge input X-capacitors to less than 35 V in 60 seconds
- Output voltage feedback to controller
- Input voltage sensing for boost follower circuit

6.2 Performance Curves

6.2.1 Efficiency Curves With Load and Line Variation

The following 图 8, 图 9, 图 10, and 图 11 show the measured efficiency and power loss in the system with AC input voltage variation with and without boost follower configurations. These graphs also compare the efficiency improvement between using an SiC diode and using an ultra-fast power diode.

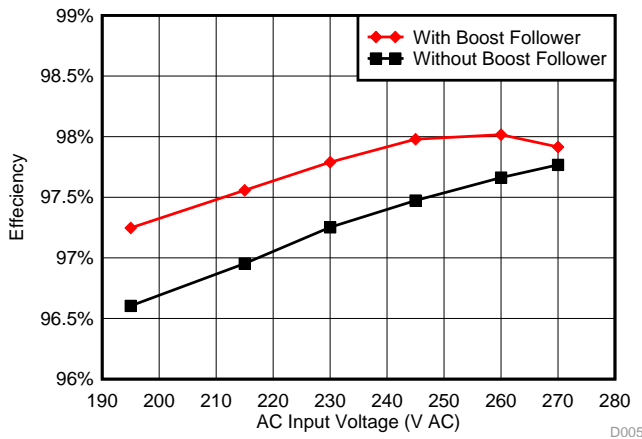


图 8. Efficiency Versus AC Input Voltage (195-V AC to 270-V AC)

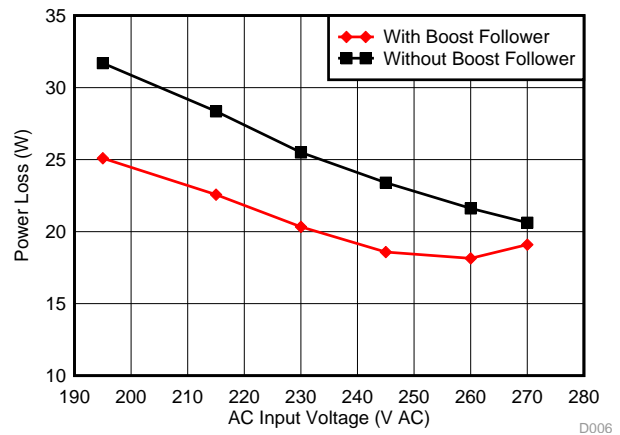


图 9. Power Loss Versus AC Input Voltage (195-V AC to 270-V AC)

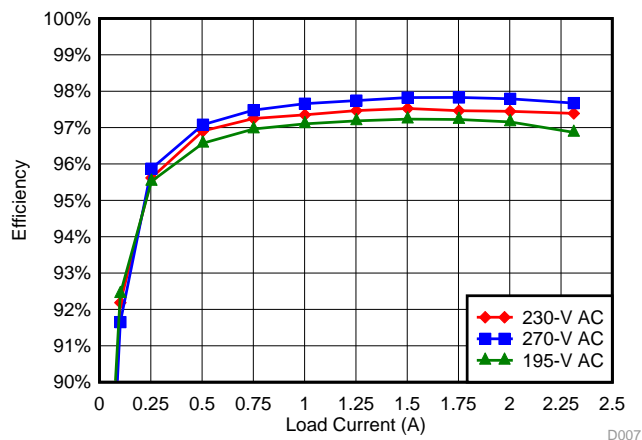


图 10. Efficiency Versus Output Load Current (I_{OUT}) With SiC Diode for D1

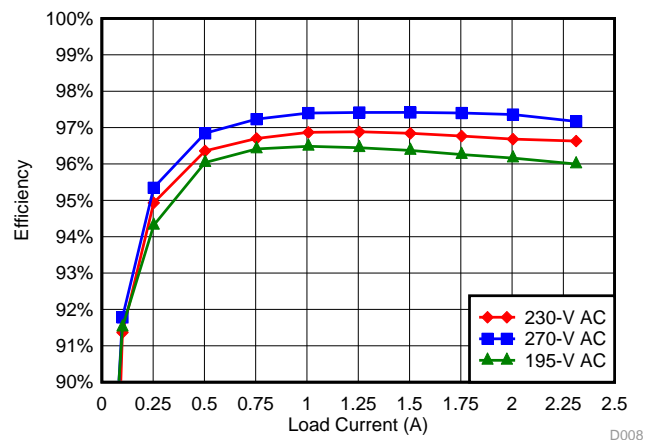


图 11. Efficiency Versus Output Load Current (I_{OUT}) With Ultra-Fast Power Diode for D1

6.2.2 Load and Line Regulation

The following 图 12 and 图 13 show the measured line and load regulation of the output with AC input voltage variation.

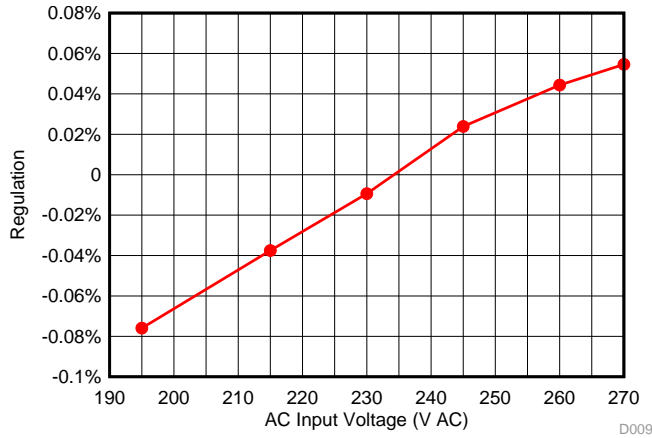


图 12. Output Voltage Variation With Input Voltage

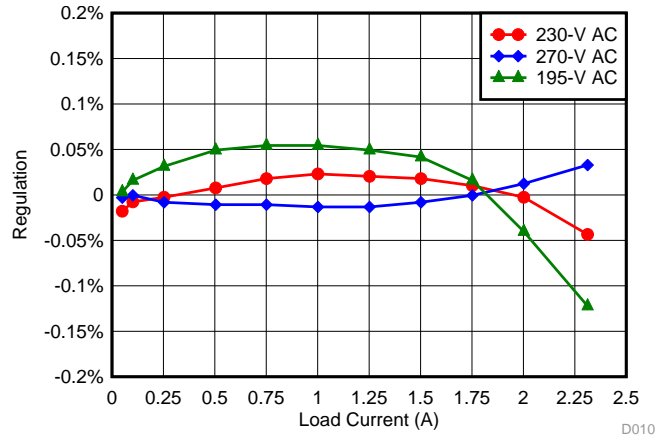


图 13. Output Voltage Variation With Load Current

6.2.3 Harmonic Current Measurements

The harmonic currents have been measured for any odd harmonic values and compared with the IEC-61000-3-2 class D standard as required for the targeted applications. The magnitude of harmonic currents are lower than the defined limit values set in the IEC-61000-3-2 class D standard, at both 100-W and 900-W loads.

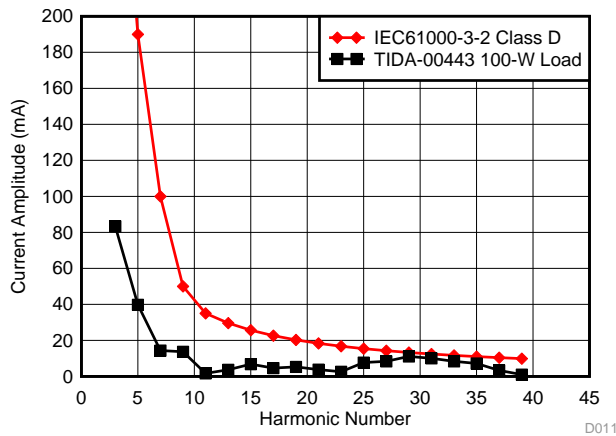


图 14. Harmonic Currents and Comparison With IEC-61000-3-2 Class D at 100-W Output Load

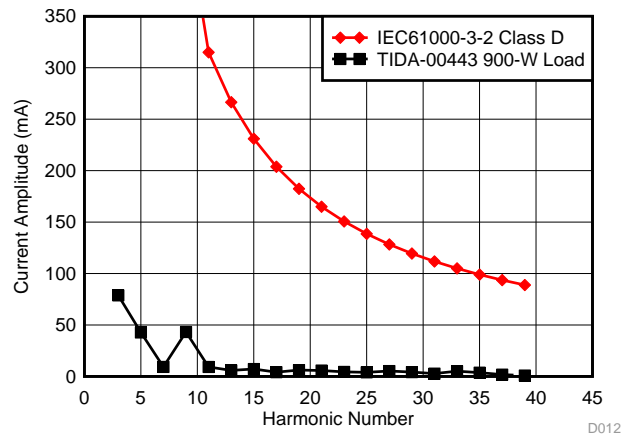


图 15. Harmonic Currents and Comparison With IEC-61000-3-2 Class D at 900-W Output Load

6.3 Functional Waveforms

6.3.1 Switching Node Waveforms

图 16 和 图 17 显示在开关节点 (SW) 处的波形，这些波形是在 MOSFET 电流为 195-V AC 和 270-V AC 满载 (2.31-A) 条件下观察到的。

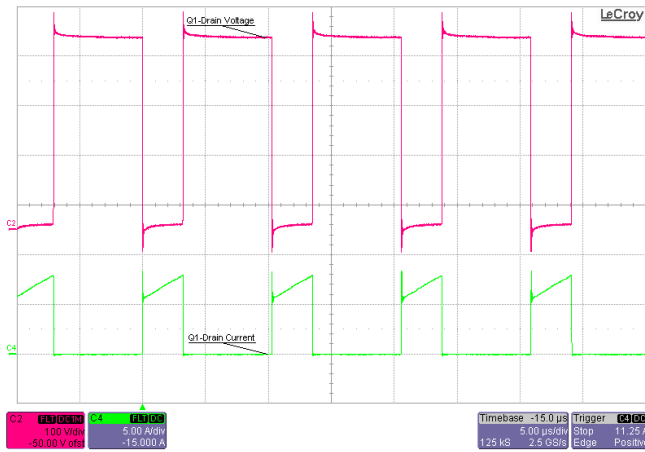


图 16. SW Node Waveform and MOSFET Current at V_{INAC} = 195-V AC, Full Load

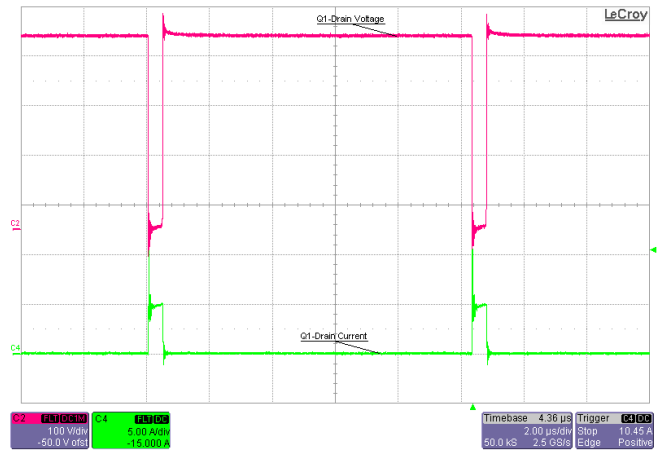


图 17. SW Node Waveform and MOSFET Current at V_{INAC} = 270-V AC, Full Load

6.3.2 Input Voltage and Current Waveform

图 18 显示在 230-V AC 满载条件下的输入电流波形。

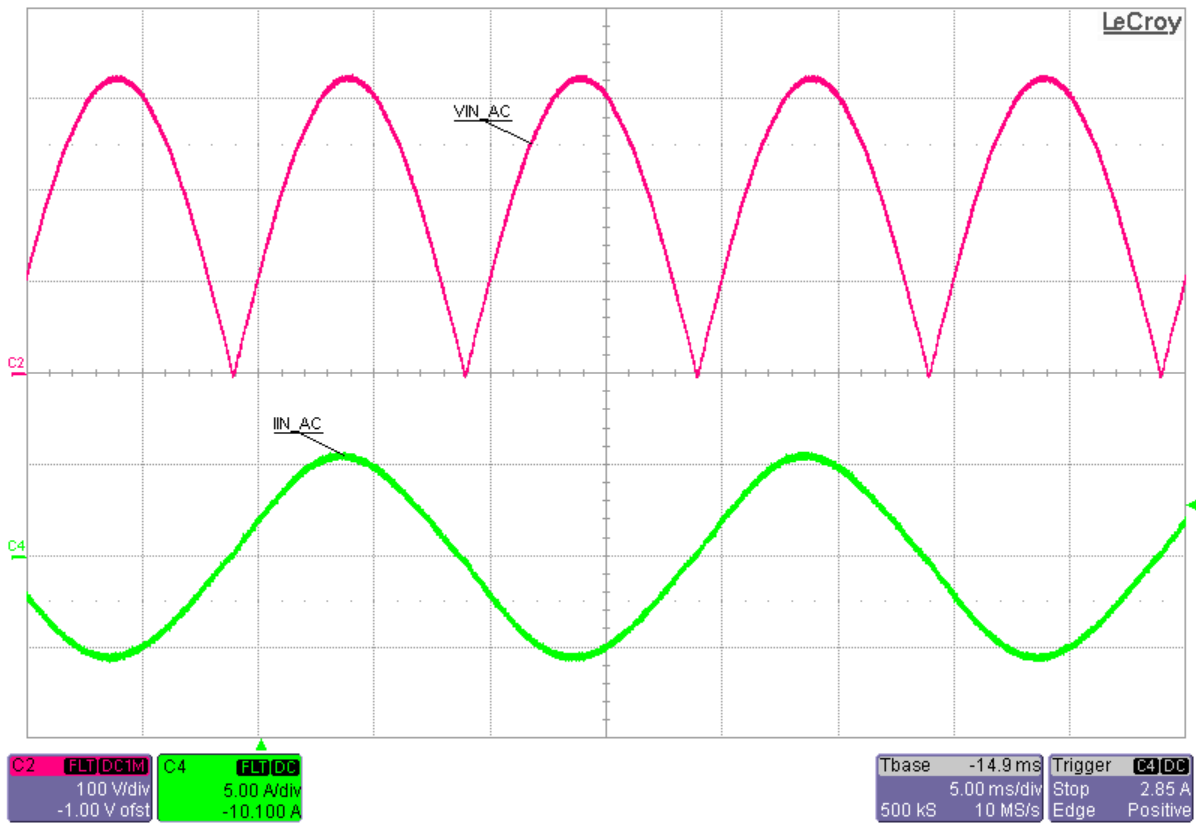


图 18. Input Voltage and Input Current at $V_{INAC} = 230\text{-V AC}$, Full Load

6.3.3 Inrush Current Waveform

图 19 shows the inrush current drawn by the system. The inrush current was observed and recorded at a maximum input voltage of 270-V AC.

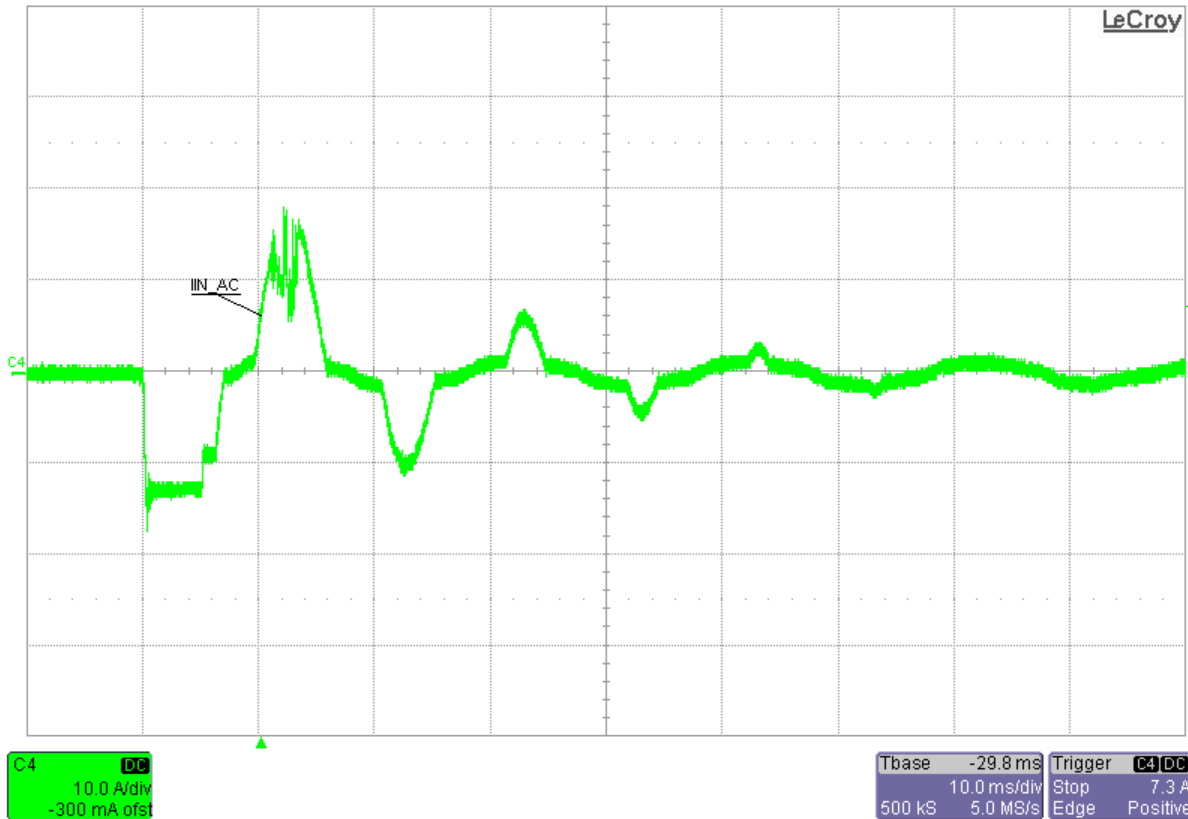


图 19. Output Voltage and Input Inrush Current at $V_{INAC} = 270\text{ V}$, Full Load

6.3.4 Output Ripple

As 图 20 and 图 21 show, the ripple was observed at a 390-V DC output loaded to 2.31 A at 230-V AC and 270-V AC.

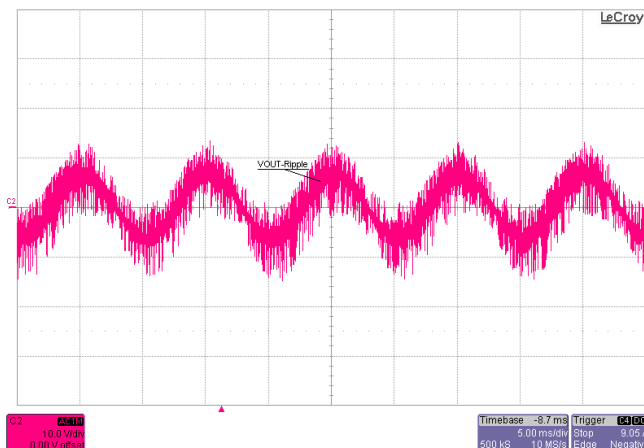


图 20. Output Voltage Ripple at $V_{INAC} = 230\text{ V}$ With Full Load

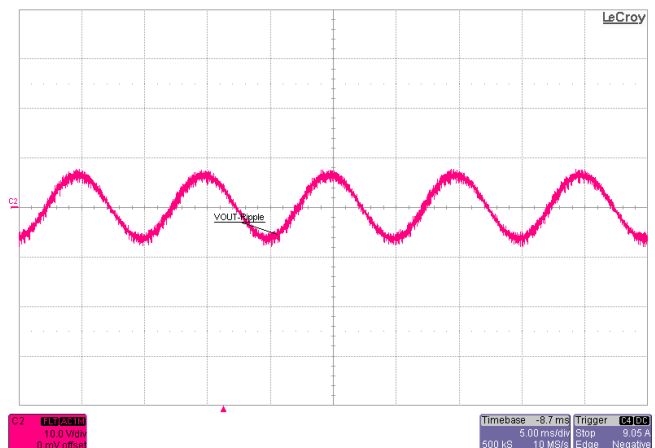


图 21. Output Voltage Ripple at $V_{INAC} = 230\text{ V}$ With Full Load, Only 50-Hz Component

6.3.5 Turnon Characteristics

图 22 和 图 23 显示 390-V 输出在满载容量 (2.31 A) 下的启动特性，该记录是在 230-V AC 输入下进行的。

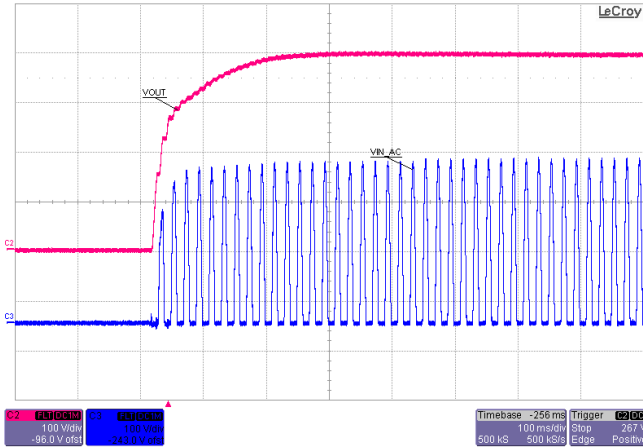


图 22. Output Turnon Waveform at $V_{INAC} = 230\text{ V}$ With Light Load of 0.3 A

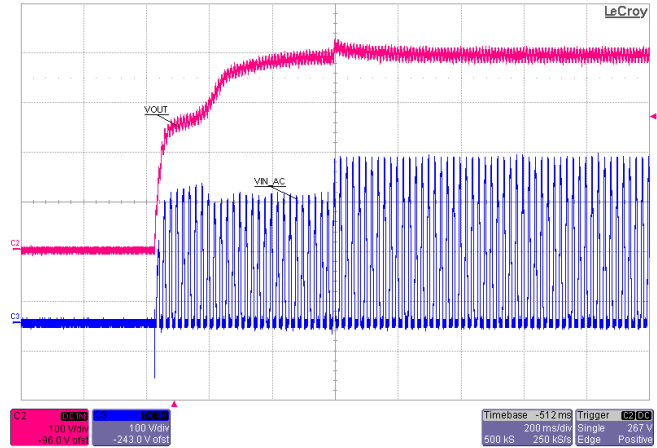


图 23. Output Turnon Waveform at $V_{INAC} = 230\text{ V}$ With Full Load of 2.31 A

6.4 Transient Waveforms

6.4.1 Transient Load Response

负载瞬态性能是在负载切换在 0.2-米导线长度下观察到的。输出负载使用电子负载进行切换。

图 24 和 图 25 显示 $V_{IN} = 230\text{-V AC}$ 和负载瞬态从 0.3 A 到 2.31 A。图 24 显示从 0.3 A 到 2.31 A 的阶跃变化，图 25 显示从 2.31 A 到 0.3 A 的负载阶跃。

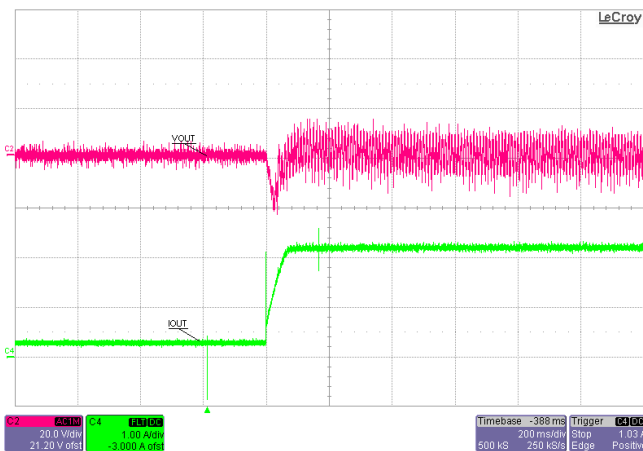


图 24. Output Voltage Waveform at $V_{INAC} = 230\text{ V}$, Load Transient from 0.3 A to 2.31 A

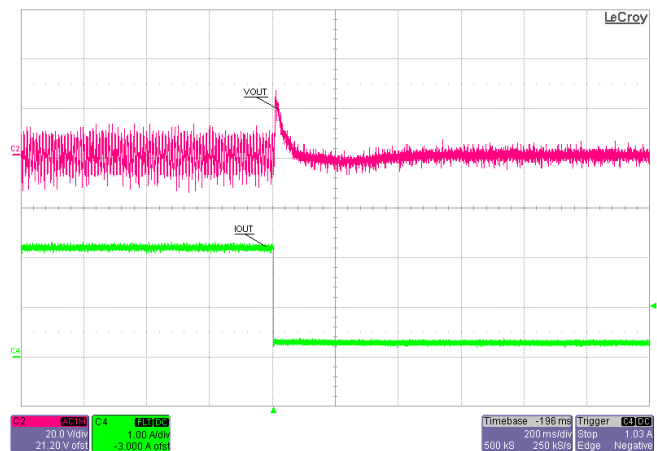


图 25. Output Voltage Waveform at $V_{INAC} = 230\text{ V}$, Load Transient from 2.31 A to 0.3 A

6.4.2 Overcurrent Limiting Protection

The overcurrent performance was observed with the load at a 0.2-meter wire length (see 图 26). The output is set at 125% of the load using an electronic load.

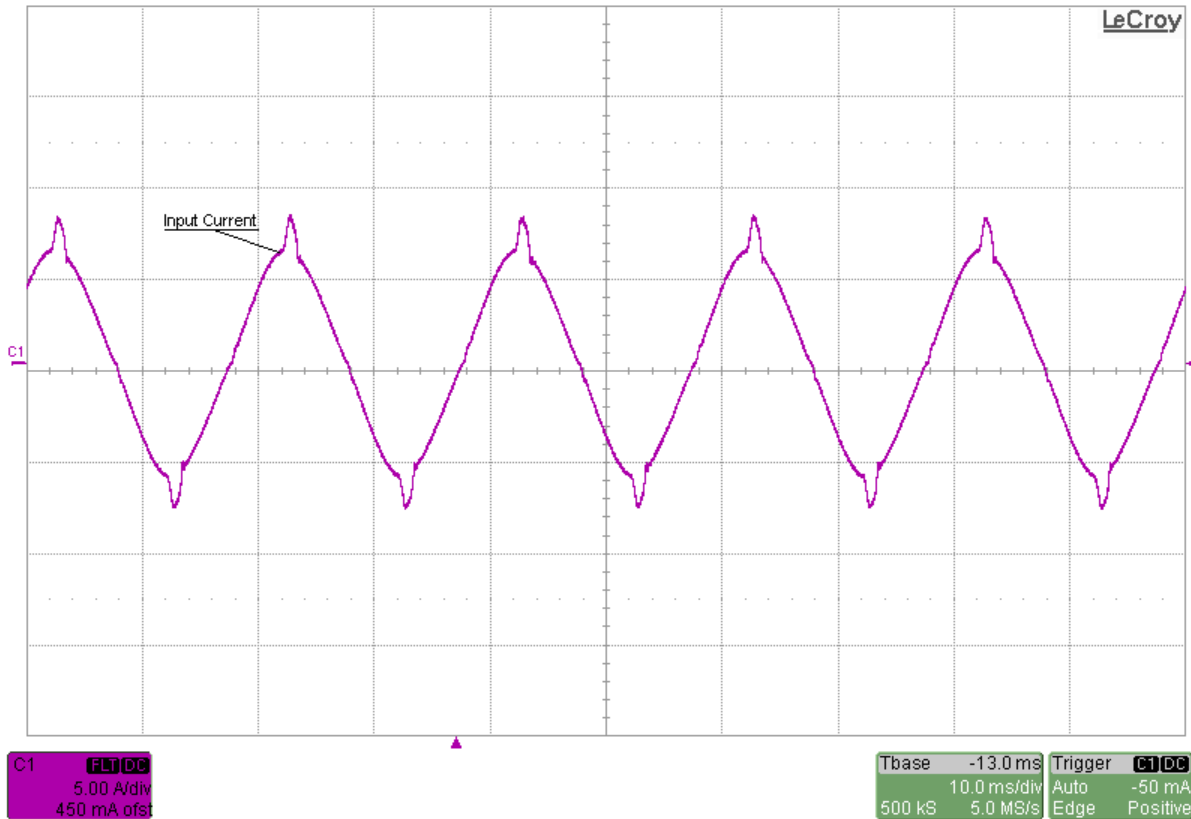


图 26. Input Current Waveform at $V_{INAC} = 230\text{ V}$ and Output Load = 2.65 A (114% Load)

6.5 Functional Performance With Inverter Load Driving Motor

The board was tested with an inverter load driving a BLDC motor using a companion inverter board. The functional performance was observed by measuring the parameters in the following subsections.

6.5.1 Input Current Waveform

图 27 和 图 28 显示在轻载条件和满载条件下从 AC 电源吸取的电流。

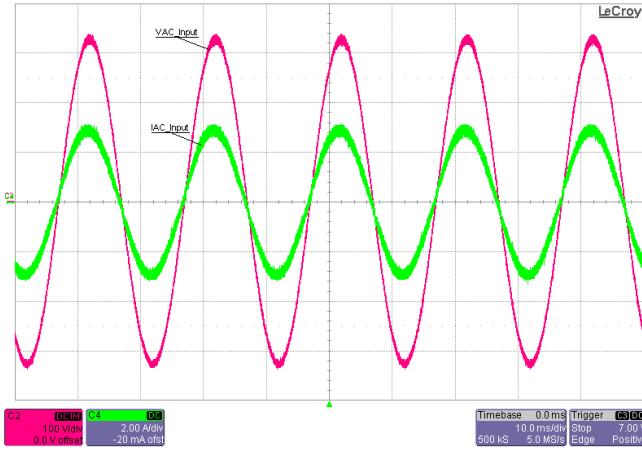


图 27. Input Current Waveform at $V_{INAC} = 230\text{ V}$ and Motor Load = 450 W

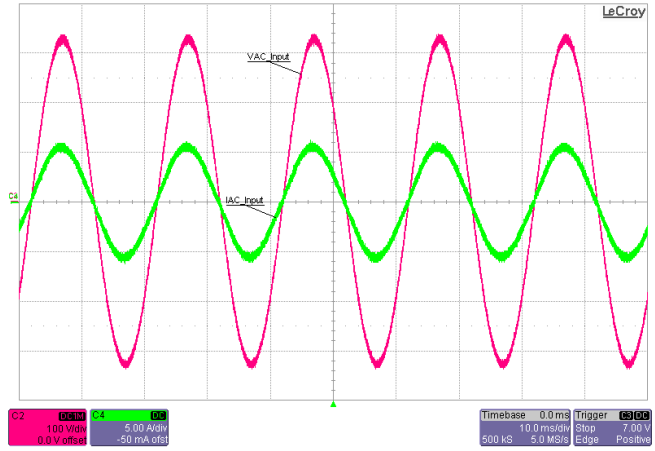


图 28. Input Current Waveform at $V_{INAC} = 230\text{ V}$ and Motor Load = 900 W

6.5.2 Ripple Voltage Waveform at Full Load

图 29 显示了在逆变器驱动电机负载时 DC 输出总线上的纹波电压。

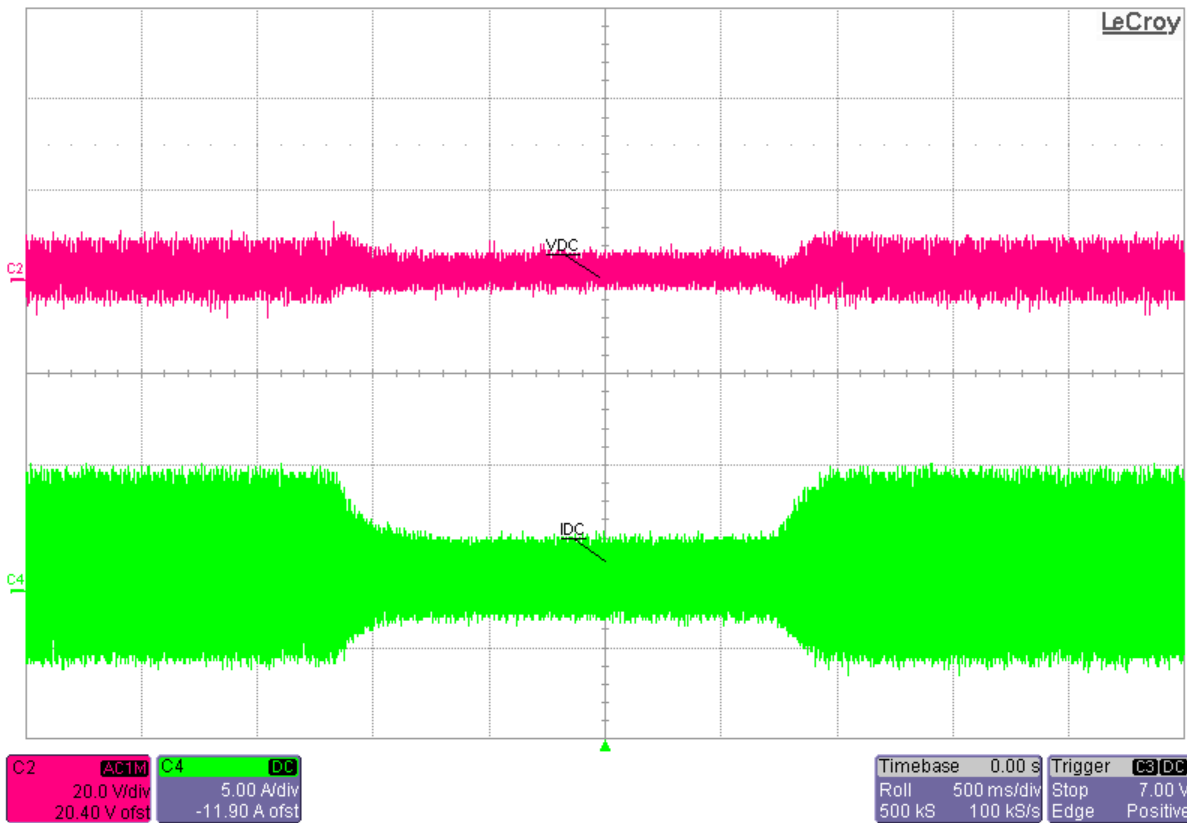


图 29. Output Voltage Ripple at $V_{INAC} = 230\text{ V}$ and Motor Load = 900 W

6.5.3 Start-up and Shut Down Performance With Inverter Load Driving Motor

图 30 和 图 31 显示了一个驱动电机负载的系统在 AC 输入开启和关闭时的启动和关闭性能。

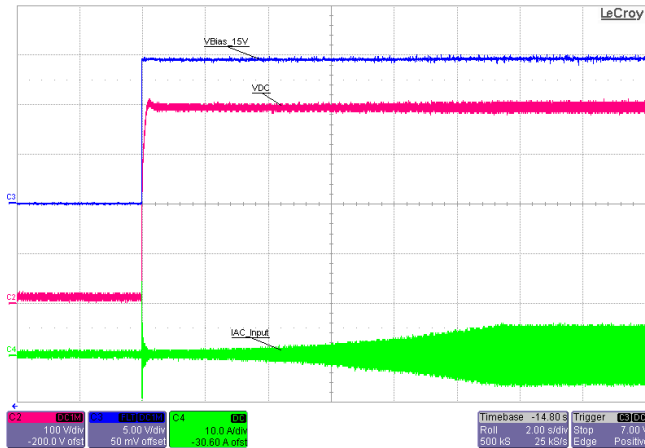


图 30. Motor Start-Up Performance Waveform at $V_{INAC} = 230\text{ V}$ With Full Load of 2.31 A

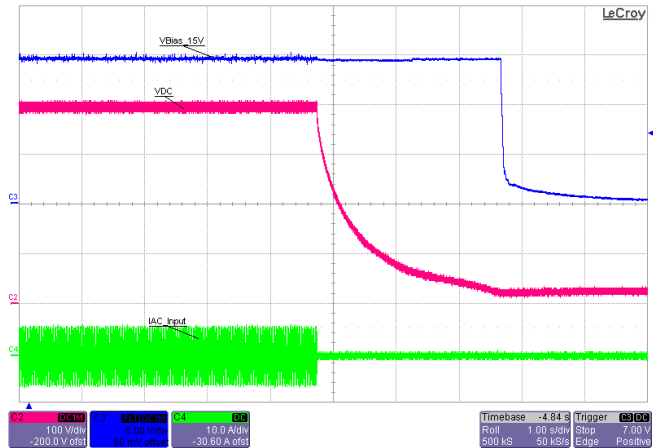


图 31. Motor Shut-Down Performance Waveform at $V_{INAC} = 230\text{ V}$ With Full Load of 2.31 A

6.5.4 Transient Load Response

对于 TIDA-00443 设计，负载瞬态性能是在负载通过阻塞真空吸尘器的吸力泵而切换时观察到的（参见图 32）。

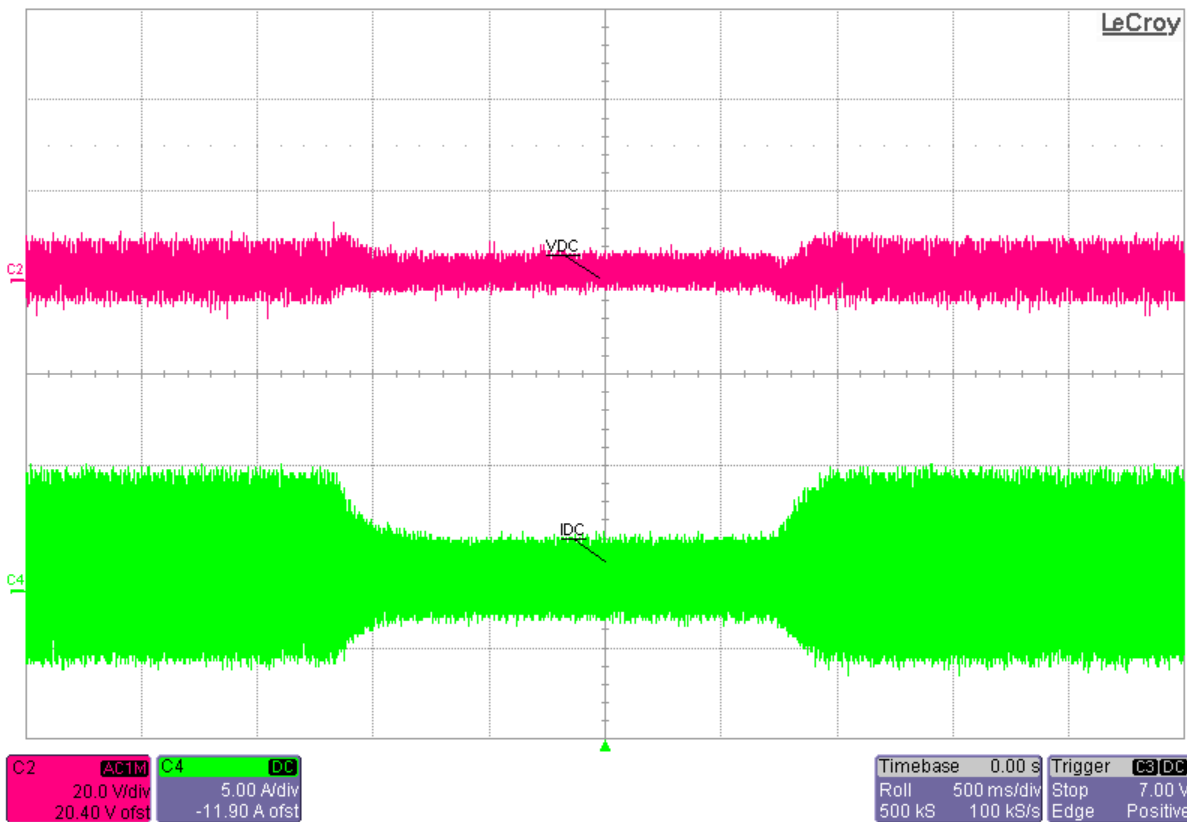


图 32. Output Voltage Waveform at $V_{INAC} = 230\text{ V}$, Load Transient From 900 W to 400 W and Back

6.6 Conducted Emissions

Conducted emissions are generally high at full-load capacity. As a result, the operating point was selected for measuring the conducted EMI.

6.6.1 With Resistive Load at Output

图 33 shows a plot of the resistive load with a 230-V AC input, 2.31-A resistive load connected to a power supply unit (PSU) with short leads. A comparison of the results from conducted emissions in a pre-compliance test setup against EN55011 class A limits shows that the conducted emissions meet these specified standards with ease.

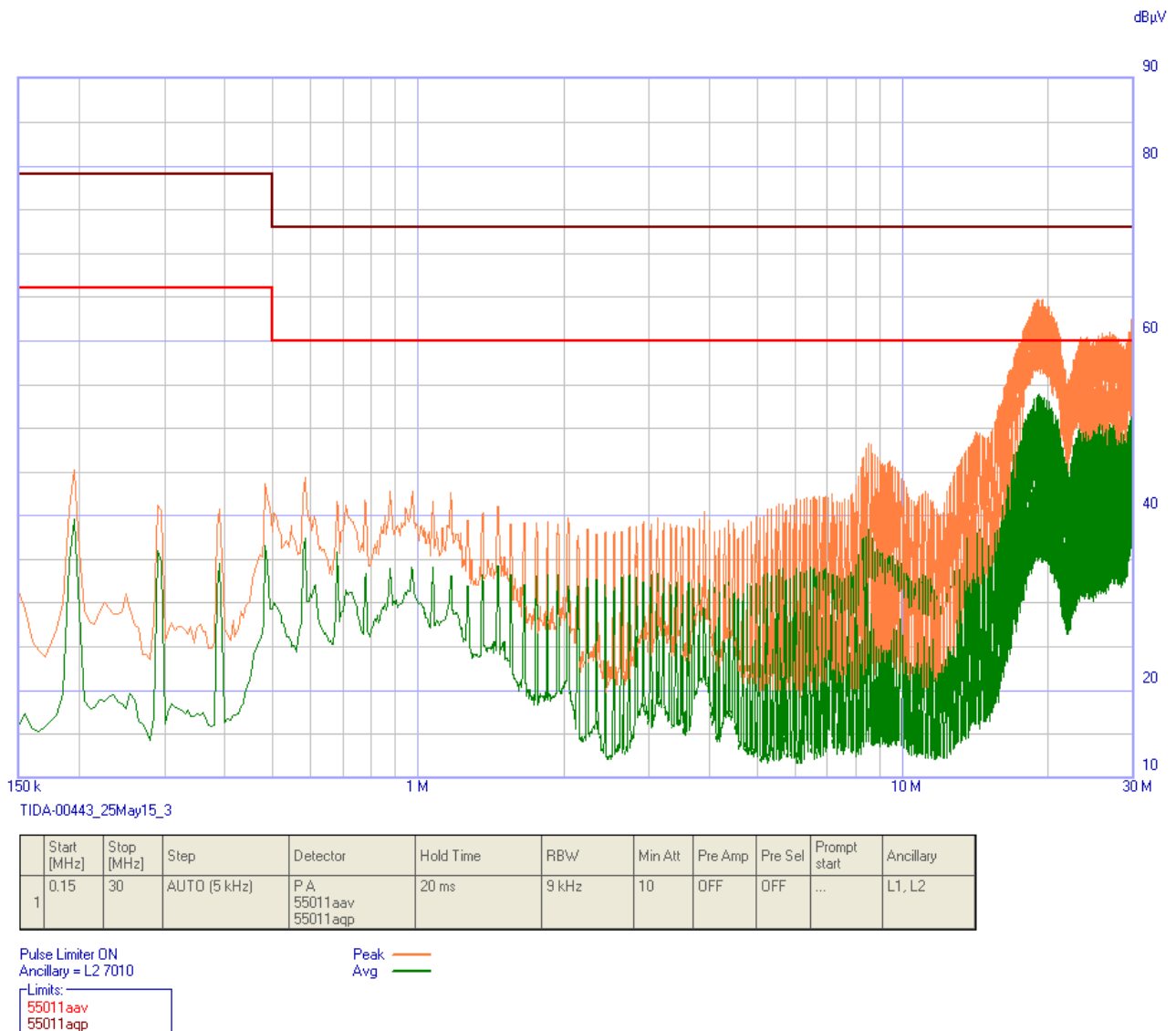


图 33. Conducted Emissions as per EN55011 Class B With Resistive Load

6.6.2 With Inverter Load Driving Motor at Full Load

The CE test was performed with a motor load to better understand the performance of front-end, PFC-driving inverter fed motors. 图 34 shows the conducted emissions plot at the 230-V AC input. The BLDC motor was run at a full-load capacity of 900-W output power using the companion inverter board switching at 10 KHz. The conducted emissions were compared in a pre-compliance test setup against the EN55011 class A limits and were found to meet the class A limits with ease.

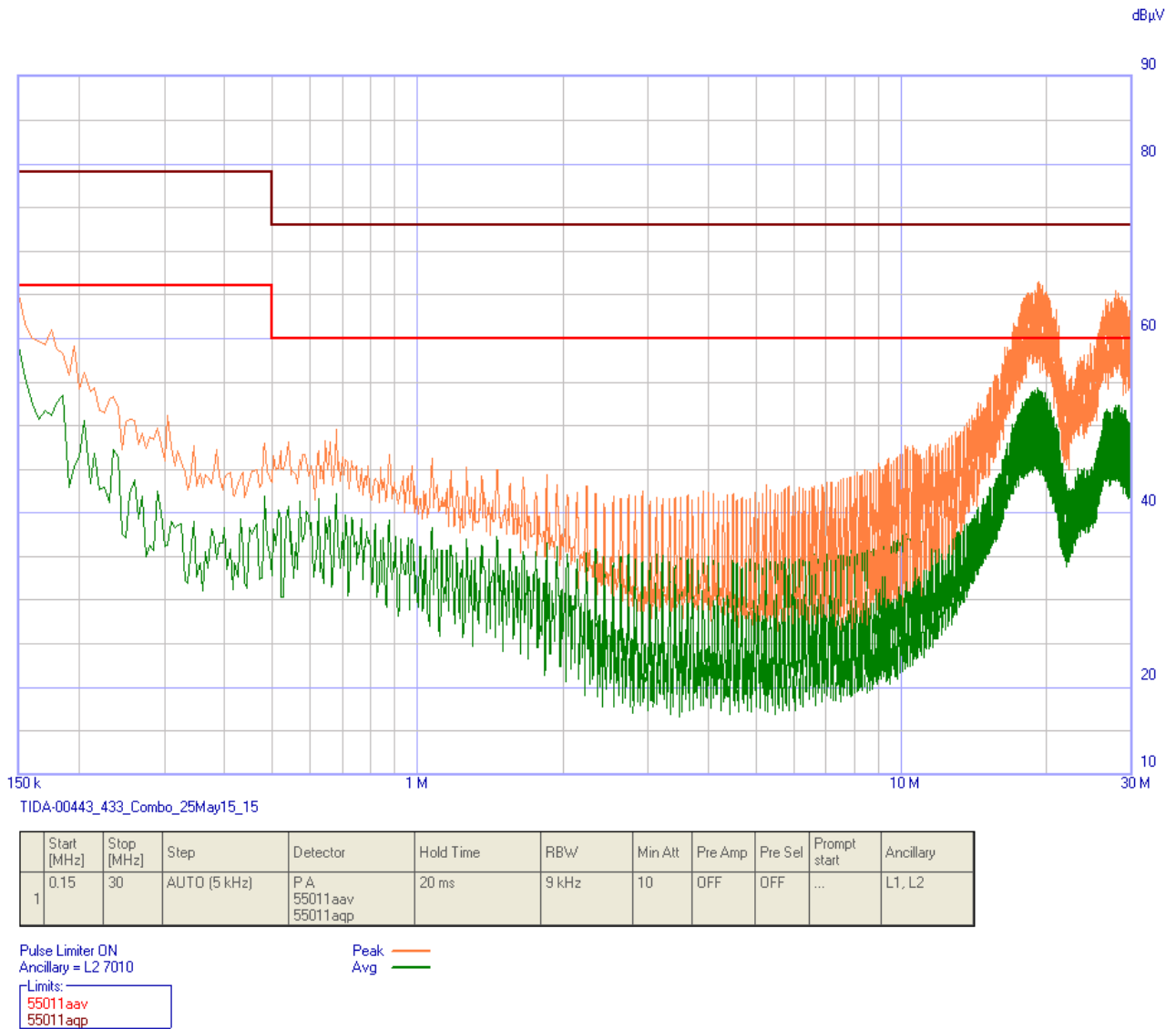


图 34. Conducted Emissions as per EN55011 Class B With 900-W Motor

6.7 Surge and Fast Transients Test

The surge and EFT testing was conducted on the boards as per the EN55014 testing standards. 表 8 shows the test condition and test results.

表 8. Surge and EFT Test Results

BASIC STANDARD	PORT	REQUIREMENTS FOR RESIDENTIAL, COMMERCIAL, AND LIGHT-INDUSTRIAL ENVIRONMENTS	REQUIRED PERFORMANCE CRITERION	TEST RESULT
IEC/EN 61000-4-4: Fast transients (burst)	AC input	± 1 kV, 5 kHz	B	Passed with performance criterion A
IEC/EN 61000-4-5: Surges	AC input	± 2 kV line to earth	B	Passed with performance criterion A
		± 1 kV line to line		

注: **Regarding the definition of "Performance Criteria":**

1. Normal performance within limits specified by the design or manufacturer
2. Temporary loss of function or degradation of performance that ceases after the disturbance ceases

6.8 Thermal Measurements

To better understand the temperature of power components and maximum possible operating temperature, the thermal images were plotted at room temperature (25°C) with a closed enclosure, no airflow, and at full-load conditions. The board was allowed to run for 30 minutes before capturing a thermal image.

Test setting – 1: Boost follower configuration

The following 图 35 shows the temperature of power components at input voltage of 230-V AC, with the load ON. The 362-V DC bus is a 2.5-A, 900-W power output.

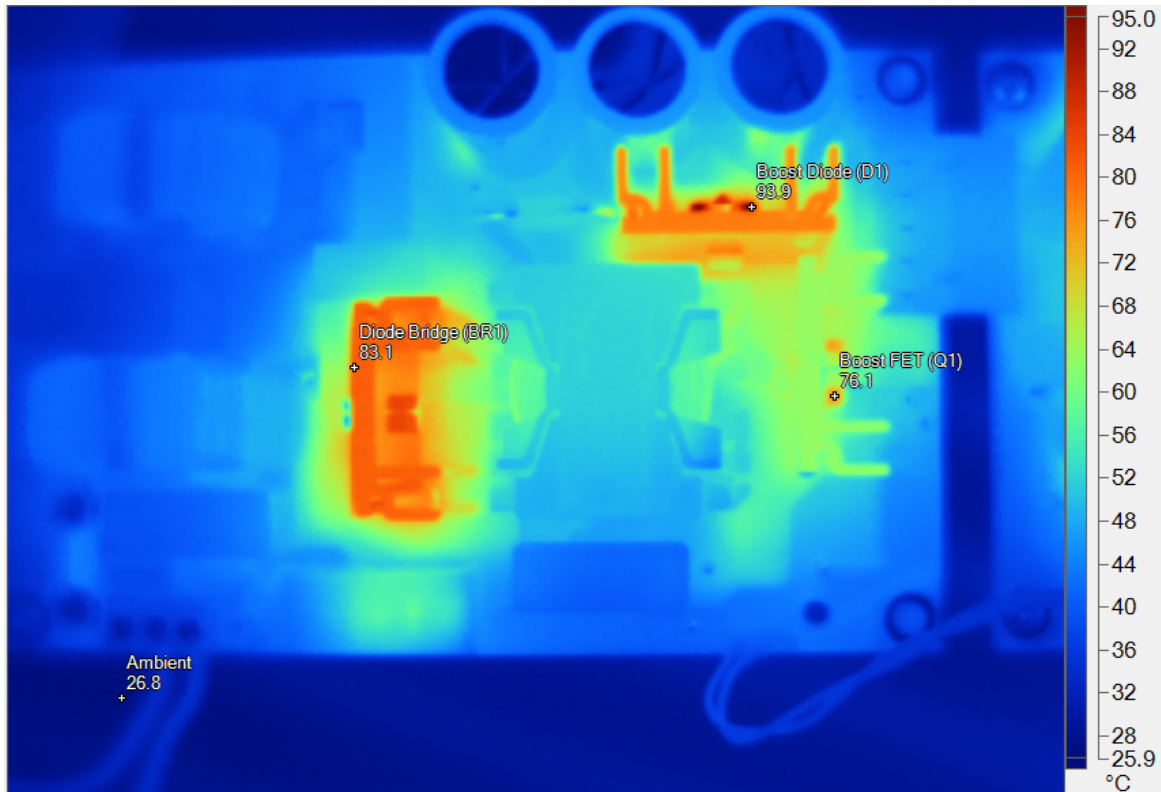



图 35. Top-Side Temperatures at 230-V AC Input and 900-W Output

表 9. Highlighted Image Markers

NAME	TEMPERATURE
Ambient	26.8°C
Boost FET (Q1)	76.1°C
Boost diode (D1)	93.9°C
Diode-bridge (BR1)	83.1°C

By implementing a boost follower configuration, the temperatures maintain at low values and have higher margins from the respective device junction temperatures.

Test setting – 2: Fixed boost output voltage

The following  shows the temperature of power components at an input voltage of 230-V AC with the load ON. The 390-V-DC bus is a 2.31-A, 900-W power output.

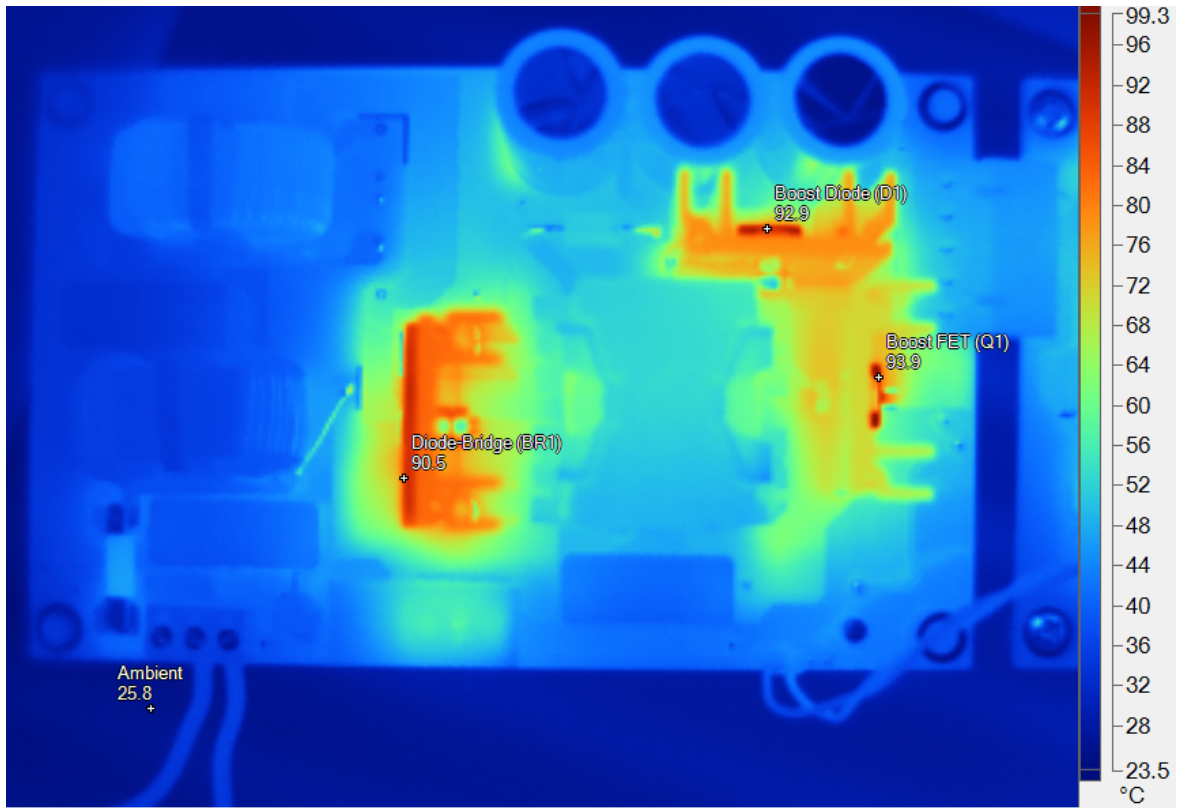


图 36. Top-Side Temperatures at 230-V AC Input and 900-W Output

表 10. Highlighted Image Markers

NAME	TEMPERATURE
Ambient	25.8°C
Boost FET (Q1)	93.9°C
Boost diode (D1)	92.9°C
Diode-bridge (BR1)	90.5°C

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00443.

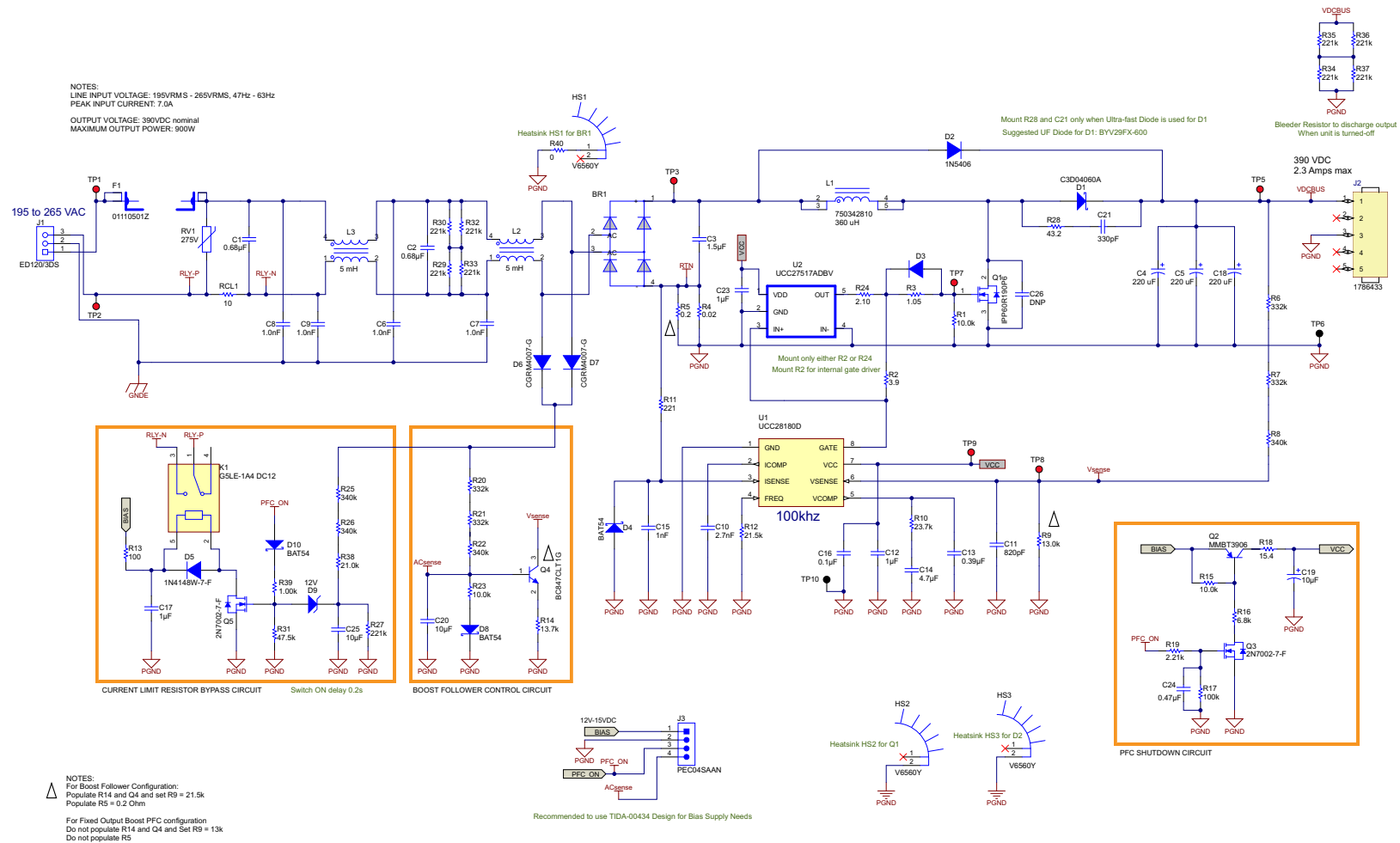


图 37. TIDA-00443 Schematic

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00443](#).

表 11. BOM

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER	NOTE
1	PCB	Printed Circuit Board	Any	TIDA-00443	Fitted
1	BR1	Diode, Bridge Rectifier, GPP 15A 800V GBJ	Micro Commercial Co	GBJ1508-BP	Fitted
2	C1, C2	CAP, Film, 0.68 μ F, 630 V, +/- 20%, TH	EPCOS Inc	B32923C3684M	Fitted
1	C3	CAP, Film, 1.5 μ F, 630 V, +/- 20%, 0.017 ohm, TH	EPCOS Inc	B32923C3155M	Fitted
3	C4, C5, C18	CAP, ALUMINIUM, RADIAL, 220 μ F, 450 V, 20%, TH	RUBYCON	450QXW220MEFC18X50	Fitted
4	C6, C7, C8, C9	CAP CER 1000PF 300VAC 20% RADIAL DISC 7mm Dia	TDK	CS65ZU2GA102MYNKA	Fitted
1	C10	CAP, CERM, 2700 pF, 100 V, +/- 5%, X7R, 0603	AVX	06031C272JAT2A	Fitted
1	C11	CAP, CERM, 820 pF, 50 V, +/- 10%, X7R, 0603	Kemet	C0603C821K5RACTU	Fitted
3	C12, C17, C23	CAP, CERM, 1 μ F, 25 V, +/- 10%, X7R, 0603	TDK	C1608X7R1E105K080AB	Fitted
1	C13	CAP, CERM, 0.39 μ F, 16 V, +/- 10%, X7R, 0603	Kemet	C0603C394K4RACTU	Fitted
1	C14	CAP, CERM, 4.7 μ F, 16 V, +/- 10%, X5R, 0603	MuRata	GRM188R61C475KAAJ	Fitted
1	C15	CAP, CERM, 1000 pF, 100 V, +/- 10%, X7R, 0603	AVX	06031C102KAT2A	Fitted
1	C16	CAP, CERM, 0.1 μ F, 50 V, +/- 10%, X7R, 0603	AVX	06035C104KAT2A	Fitted
1	C19	CAP, AL, 10 μ F, 35V, +/-20%, 0.95 ohm, TH	Nichicon	UPW1V100MDD6	Fitted
1	C20	CAP, CERM, 10 μ F, 25 V, +/- 10%, X5R, 0805	TDK	C2012X5R1E106K125AB	Fitted
1	C21	CAP, CERM, 330 pF, 1000 V, +/- 5%, U2J, 1206	MuRata	GRM31A7U3A331JW31D	Not-Fitted
1	C24	CAP, CERM, 0.47 μ F, 16 V, +/- 10%, X7R, 0603	Kemet	C0603C474K4RACTU	Fitted
1	C25	CAP CER 10UF 50V 20% X5R 1206	Taiyo Yuden	UMK316BBJ106ML-T	Fitted
1	C26	CAP, CERM, 100 pF, 1000 V, +/- 5%, U2J, 1206	MuRata	GRM31A7U3A101JW31D	Not-Fitted
1	D1	Diode, Schottky, 600 V, 4 A, TH	Cree	C3D04060A	Fitted
1	D2	Diode, Switching-Bridge, 600 V, 3 A, TH	Vishay-Semiconductor	1N5406	Fitted
1	D3	Diode, Switching, 100 V, 0.2 A, SOD-323	Micro Commercial Components	MMDL914-TP	Fitted
3	D4, D8, D10	Diode, Schottky, 30V, 0.2A, SOD-323	Fairchild	BAT54HT1G	Fitted
1	D5	Diode, Ultrafast, 100V, 0.15A, SOD-123	Diodes Inc.	1N4148W-7-F	Fitted
2	D6, D7	Diode, P-N, 1000 V, 1 A, 3.9x1.7x1.8mm	Comchip Technology	CGRM4007-G	Fitted
1	D9	Diode, Zener, 12V, 300mW, SOD-323	NXP Semiconductor	BZX384-C12,115	Fitted
1	F1	FUSE CLIP, CARTRIDGE, 250V, 10A, PCB	LITTELFUSE	01110501Z	Fitted
4	FID1, FID2, FID3, FID4	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fitted
4	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	Fitted
4	H7, H8, H9, H10	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	Fitted

表 11. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER	NOTE
3	HS1, HS2, HS3	HEATSINK ALUM Black Anodized, Board Mount	Assmann	V6560Y	Fitted
1	J1	TERMINAL BLOCK 5.08MM VERT 3POS, TH	On-Shore Technology	ED120/3DS	Fitted
1	J2	TERM BLOCK HDR 5POS R/A 5.08MM	PHOENIX CONTACT	1786433	Fitted
1	J3	Header, 100mil, 4x1, Tin, TH	Sullins Connector Solutions	PEC04SAAN	Fitted
1	K1	Relay, SPST-NO (1 Form A), 10A, 12 VDC, TH	Omron Electronic Components	G5LE-1A4 DC12	Fitted
1	L1	INDUCTOR, 360 uH, 8.3 A, 10%, TH	Würth Elektronik	750342810	Fitted
2	L2, L3	INDUCTOR, CHOKE, COMMON MODE, 5 mH, 8.9 A, 22 mOHM, TH	Bourns Inc	8113-RC	Fitted
1	Q1	MOSFET, N-CH, 600 V, 20.2 A, TO-220	Infineon Technologies	IPP60R190P6	Fitted
1	Q2	Transistor, PNP, 40V, 0.2A, SOT-23	Fairchild Semiconductor	MMBT3906	Fitted
2	Q3, Q5	MOSFET, N-CH, 60V, 0.17A, SOT-23	Diodes Inc.	2N7002-7-F	Fitted
1	Q4	Transistor, NPN, 45 V, 0.1 A, SOT-23	ON Semiconductor	BC847CLT1G	Fitted
3	R1, R15, R23	RES, 10.0 k, 1%, 0.1 W, 0603, RES, 10.0k ohm, 1%, 0.1W, 0603, RES, 10.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	Fitted
1	R2	RES, 3.9, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12063R90JNEA	Fitted
1	R3	RES, 1.05, 1%, 0.25 W, 1206	Vishay-Dale	CRCW12061R05FKEA	Fitted
1	R4	RES, 0.02, 1%, 3 W, 2512	Bourns	CRA2512-FZ-R020ELF	Fitted
1	R5	RES, 0.2, 1%, 2 W, 2512	Bourns	CRM2512-JW-201ELF	Fitted
4	R6, R7, R20, R21	RES, 332 k, 1%, 0.25 W, 1206	Vishay-Dale	CRCW1206332KFKEA	Fitted
4	R8, R22, R25, R26	RES, 340 k, 1%, 0.25 W, 1206	Vishay-Dale	CRCW1206340KFKEA	Fitted
1	R9	RES, 13.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060313K0FKEA	Fitted
1	R10	RES, 23.7 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060323K7FKEA	Fitted
1	R11	RES, 221 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603221RFKEA	Fitted
1	R12	RES, 21.5 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060321K5FKEA	Fitted
1	R13	RES, 100, 1%, 0.25 W, 1206	Vishay-Dale	CRCW1206100RFKEA	Fitted
1	R14	RES, 13.7 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060313K7FKEA	Fitted
1	R16	RES, 6.8 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06036K80JNEA	Fitted
1	R17	RES, 100 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KFKEA	Fitted
1	R18	RES, 15.4, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060315R4FKEA	Fitted
1	R19	RES, 2.21 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K21FKEA	Fitted
1	R24	RES, 2.10, 1%, 0.25 W, 1206	Vishay-Dale	CRCW12062R10FKEA	Not-Fitted
1	R27	RES, 221 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603221KFKEA	Fitted
1	R28	RES, 100, 1%, 1 W, 2512	Vishay-Dale	CRM2512-FX-43R2ELF	Not-Fitted
8	R29, R30, R32, R33, R34, R35, R36, R37	RES, 221 k, 1%, 0.25 W, 1206	Vishay-Dale	CRCW1206221KFKEA	Fitted

表 11. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER	NOTE
1	R31	RES, 47.5 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060347K5FKEA	Fitted
1	R38	RES, 21.0 k, 1%, 0.25 W, 1206	Vishay-Dale	CRCW120621K0FKEA	Fitted
1	R39	RES, 1.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	Fitted
1	R40	RES, 0, 5%, 0.125 W, 0805	Vishay-Dale	CRCW08050000Z0EA	Fitted
1	RCL1	RES 10 OHM 7W 5% AXIAL	Vishay-Dale	AC07000002009JAC00	Fitted
1	RV1	Varistor 275V RMS 10MM Radial, TH	EPCOS Inc	S10K275E2	Fitted
7	TP1, TP2, TP3, TP5, TP7, TP8, TP9	Test Point, Miniature, Red, TH	Keystone	5000	Fitted
2	TP6, TP10	Test Point, Miniature, Black, TH	Keystone	5001	Fitted
1	U1	8-PIN Continous Conduction Mode (CCM) PFC Controller	Texas Instruments	UCC28180D	Fitted
1	U2	IC, 4A Single Channel High-Speed Low-Side Gate Drivers	Texas Instruments	UCC27517ADBV	Fitted
3	MK1-MK3	Mounting Kit TO-220	Aavid Thermalloy	4880G	Fitted

7.3 Layout Guidelines

A careful PCB layout is critical and extremely important in a high-current fast-switching circuit to provide the appropriate device operation and design robustness. As with all switching power supplies, paying attention to the detail in the layout can save much time later on to avoid troubleshooting. The following subsections highlight the key guidelines to follow.

7.3.1 Power Stage Specific Guidelines

The following lists the key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This action helps to reduce EMI and improve the overall converter performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dv/dt potential and high di/dt capability away from or shielded from sensitive signal traces, with adequate clearance and ground shielding.
- For each power supply stage, keep power ground and control ground separated. Tie them together (if they are electrically connected) at one point near the DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, layout must be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower-series trace impedance experiences higher peak currents and becomes hotter (increased temperatures), i^2R .
- The heat sinks of all the power switching components must be tied to their respective power grounds.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These devices must also be routed with short traces to reduce inductance.
- The width of PCB traces must be chosen based on an acceptable temperature rise at the rated current, as per IPC2152, as well as acceptable DC and AC impedances. Also, the traces must withstand the fault currents (such as short circuit current) before the activation of electronic protections such as a fuse or circuit breaker.
- The distances between various traces of the circuit must be determined according to the requirements of applicable standards. This design follows the UL 60950-1 safety standard to maintain the creepage and clearance from live line to neutral line and to safety ground, as this standard defines in Tables 2K through 2N (standards are viewable with purchase from UL: <http://bit.ly/1K16UZL>).
- Thermal management must be adapted to fit the end-equipment requirements.

7.3.2 Controller Specific Guidelines

The following are key guidelines for the routing of controller components and signal circuits:

- The optimum placement for a decoupling capacitor is close to the VCC and GND terminals of the device. Take care to minimize the loop area formed by the bypass-capacitor connection and the GND terminal of the IC.
- The reference ground for the control device is a low-current signal ground (SGND), which must be a copper plane or island.
- Locate all of the controller support components at specific signal pins (VSENSE, VCOMP, ISENSE, ICOMP, and FREQ) close to their connection pin. Connect the other end of the component to the

SGND with the shortest trace length.

- The trace routing for the voltage sensing and current sensing circuit components to the device must be as short as possible to reduce parasitic effects on the current limit, current monitoring accuracy, and voltage monitoring accuracy. These traces must not have any coupling-to-switching signals on the board.
- The SGND plane must be connected to the high current ground (main power ground) at a single point that is at the negative terminal of the DC input and output capacitor, respectively.

7.3.3 Gate Driver Specific Guidelines

The following are key guidelines for the routing of a high-frequency, high-current gate driver:

- Place the driver device as close as possible to the power device to minimize the length of high-current traces between the output pins of gate drive and the gate of the power device.
- Place the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering.
- The turnon and turnoff current-loop paths (driver device, power MOSFET, and VDD bypass capacitor) must be minimized as much as possible to keep the stray inductance to a minimum.
- Star-point grounding is an effective way to minimize noise coupling from one current loop to another. The GND of the driver must be connected to the other circuit nodes, such as the source pin of the switching MOSFET or the ground of a PWM controller at one single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.

7.3.4 Layout Prints

To download the layout prints for each board, see the design files at [TIDA-00443](#).

7.4 Altium Project

To download the Altium project files, see the design files at [TIDA-00443](#).

7.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-00443](#).

7.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-00443](#).

8 Software Files

To download the design calculator spreadsheet, see the design files at [TIDA-00443](#).

9 References

1. Texas Instruments, Marjanovic, Milan; Ulmann, Matthias; *A Design Review of a Full-Featured 350-W Offline Power Converter*, Unitrode Power Supply Design Seminar Topic-2 2012 ([TIDU186](#))
2. Texas Instruments, *Snubber Circuits: Theory, Design and Application*, Reference Guide ([SLUP100](#))
3. Texas Instruments, *Using the UCC28180EVM-573, 360-W Power Factor Correction Module*, UCC28180EVM-573 User's Guide ([SLUUA73](#))
4. Texas Instruments, Mammano, Bob (TI); Bahra, Lal (Uderwriters Laboratories); *Safety Considerations in Power Supply Design*, Unitrode Power Supply Design Seminar Topic-1 2004/2005 ([SLUP224](#))

5. Texas Instruments, Cohen, Issac; Lu, Bing; *High Power Factor and High efficiency – You Can Have Both*, Unitrode Power Supply Design Seminar Topic-1 2008/2009 ([SEM1800](#))
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10 Terminology

EFT— Electrical fast transient

PWM— Pulse width modulation

FETs— Field-effect transistors

MOSFETs— Metal–oxide–semiconductor field-effect transistors

IGBT— Insulated gate bipolar transistor

ESD —Electrostatic discharge

RMS —Root mean square

BLDC —Brushless DC motor

PMSM— Permanent magnet synchronous motor

HVAC— Heating, ventilation, and air conditioning

11 About the Author

LATIF AMEER BABU is a Systems Architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Latif brings to this role his extensive experience in power electronics, high frequency DC-DC converter, and analog circuit design. Latif earned his Master of Technology in Power Electronics & Power Systems from Indian Institute of Technology, Mumbai; IN. Latif is a member of the Institute of Electrical and Electronics Engineers (IEEE).

修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (July 2015) to B Revision

Page

-
- 已更改 将标题从适用于逆变器供电驱动器和电器的 230V、900W 功率因数稳压器转换器 (PFC) 更改成了适用于逆变器供电驱动器的效率为 98% 的 230V、900W PFC 参考设计 1
-

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