

SN74AVC1T45 具有可配置电压转换和三态输出的 1 位双电源总线收发器

1 特性

- 采用德州仪器 (TI) NanoFree™ 封装
- 完全可配置的双轨设计, 支持各个端口在 1.2V 至 3.6V 的整个电源电压范围内运行
- V_{CC} 隔离特性 - 如果任何一个 V_{CC} 输入接地 (GND), 则两个端口均处于高阻抗状态
- DIR 输入电路以 V_{CCA} 为基准
- 3.3V 时, 输出驱动为 $\pm 12\text{mA}$
- I/O 可耐受 4.6V 电压
- I_{off} 支持局部省电模式运行
- 最大数据速率典型值
 - 500Mbps (1.8V 至 3.3V 转换)
 - 320Mbps (<1.8V 至 3.3V 转换)
 - 320Mbps (转换至 2.5V 或 1.8V)
 - 280Mbps (转换至 1.5V)
 - 240Mbps (转换至 1.2V)
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
 - $\pm 2000\text{V}$ 人体放电模型 (A114-A)
 - 200V 机器放电模型 (A115-A)
 - $\pm 1000\text{V}$ 充电器件模型 (C101)

2 应用

- 个人电子产品
- 工业
- 企业
- 电信

3 说明

这款 1 位同相总线收发器使用两个独立的可配置电源轨。SN74AVC1T45 经过优化, 可在 V_{CCA}/V_{CCB} 设置

为 1.4V 至 3.6V 的范围内正常运行。该器件可在 V_{CCA}/V_{CCB} 低至 1.2V 的情况下正常运行, A 端口旨在跟踪 V_{CCA} , V_{CCA} 电源电压为 1.2V 至 3.6V。B 端口旨在用于跟踪 V_{CCB} , V_{CCB} 电源电压为 1.2V 至 3.6V。因此可在 1.2V、1.5V、1.8V、2.5V 和 3.3V 电压节点之间进行通用的低电压双向转换。

SN74AVC1T45 旨在实现两条数据总线间的异步通信。方向控制 (DIR) 输入的逻辑电平将会激活 B 端口或 A 端口输出。当 B 端口输出被激活时, 此器件将数据从 A 总线发送到 B 总线, 而当 A 端口输出被激活时, 此器件将数据从 B 总线发送到 A 总线。A 端口和 B 端口上的输入电路一直处于激活状态并且必须施加一个逻辑高或低电平, 从而防止过大的 I_{CC} 和 I_{CCZ} 。

SN74AVC1T45 旨在实现通过 V_{CCA} 对 DIR 输入供电。

该器件专用于使用 I_{off} 的局部断电应用。 I_{off} 电路可禁用输出, 以防在器件断电时电流回流对器件造成损坏。

V_{CC} 隔离特性可确保任一 V_{CC} 输入接地时, 两个端口都处于高阻抗状态。

NanoFree 封装技术是 IC 封装概念的一项重大突破, 它将硅晶片用作封装。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SN74AVC1T45	DCK (SOT, 6)	2mm × 2.1mm
	DBV (SOT-23, 6)	2.9mm × 2.8mm
	DRL (SOT-5X3, 6)	1.6mm × 1.6mm
	YZP (DSBGA, 6)	1.75mm × 1.25mm

(1) 有关更多信息, 请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



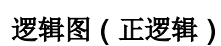


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4 Pin Configuration and Functions

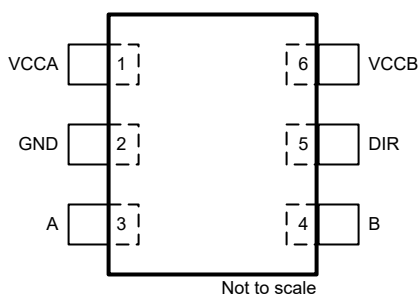


图 4-1. DBV Package,
6-Pin SOT-23 (Top View)

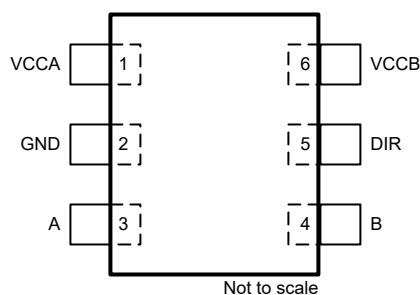


图 4-2. DCK Package,
6-Pin SOT-SC70 (Top View)

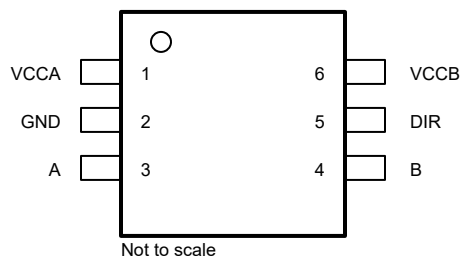


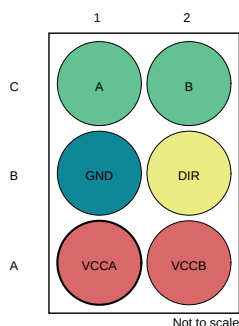
图 4-3. DRL Package, 6-Pin SOT-5X3 (Top View)

See mechanical drawings in 节 11 for dimensions.

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
V _{CCA}	1	P	A-port supply voltage. $1.2V \leq V_{CCA} \leq 3.6V$
GND	2	G	Ground
A	3	I/O	Input/output A. Referenced to V _{CCA} .
B	4	I/O	Input/output B. Referenced to V _{CCB} .
DIR	5	I	Direction control signal
V _{CCB}	6	P	B-port supply voltage. $1.2V \leq V_{CCB} \leq 3.6V$.

(1) I =input, O = output, P = power, G = ground

图 4-4. YZP Package,
6-Pin DSBGA (Bottom View)

Legend	
Power	Input or Output
Ground	Input

表 4-2. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
A1	V _{CCA}	P	A-port supply voltage. $1.2V \leq V_{CCA} \leq 3.6V$
A2	V _{CCB}	P	B-port supply voltage. $1.2V \leq V_{CCB} \leq 3.6V$.
B1	GND	G	Ground
B2	DIR	I	Direction control signal
C1	A	I/O	Input/output A. Referenced to V _{CCA} .
C2	B	I/O	Input/output B. Referenced to V _{CCB} .

(1) I =input, O = output, P = power, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V_{CCA}, V_{CCB}	Supply voltage	- 0.5	4.6	V
V_I	Input voltage ⁽²⁾	I/O ports (A port)	- 0.5	4.6
		I/O ports (B port)	- 0.5	4.6
		Control inputs	- 0.5	4.6
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A port	- 0.5	4.6
		B port	- 0.5	4.6
V_O	Voltage applied to any output in the high or low state ^{(2) (3)}	A port	- 0.5	$V_{CCA} + 0.5$
		B port	- 0.5	$V_{CCB} + 0.5$
I_{IK}	Input clamp current	$V_I < 0$	- 50	mA
I_{OK}	Output clamp current	$V_O < 0$	- 50	mA
I_O	Continuous output current		- 50	50
	Continuous current through V_{CCA}, V_{CCB} , or GND		- 100	100
T_{stg}	Storage temperature		- 65	150
				°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		Machine model, per A115-A	200

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.2	3.6	V
V _{CCB}	Supply voltage				1.2	3.6	V
V _{IH}	High-level input voltage	Data inputs	1.2V to 1.95V		V _{CCI} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		
V _{IL}	Low-level input voltage	Data inputs	1.2V to 1.95V		V _{CCI} × 0.35		V
			1.95V to 2.7V		0.7		
			2.7V to 3.6V		0.8		
V _{IH}	High-level input voltage	DIR (referenced to V _{CCA})	1.2V to 1.95V		V _{CCA} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		
V _{IL}	Low-level input voltage	DIR (referenced to V _{CCA})	1.2V to 1.95V		V _{CCA} × 0.35		V
			1.95V to 2.7V		0.7		
			2.7V to 3.6V		0.8		
V _I	Input voltage				0	3.6	V
V _O	Output voltage	Active state			0	V _{CCO}	V
		3-state			0	3.6	
I _{OH}	High-level output current			1.2V	− 3		mA
				1.4V to 1.6V	− 6		
				1.65V to 1.95V	− 8		
				2.3V to 2.7V	− 9		
				3V to 3.6V	− 12		
I _{OL}	Low-level output current			1.2V	3		mA
				1.4V to 1.6V	6		
				1.65V to 1.95V	8		
				2.3V to 2.7V	9		
				3V to 3.6V	12		
Δ t/ Δ v	Input transition rise or fall rate				5		ns/V
T _A	Operating free-air temperature				− 40	85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AVC1T45				UNIT
		DBV	DCK	DRL	YZP	
		6 PINS				
R _{θJA}	Junction-to-ambient thermal resistance	183.4	211.4	236.2	130	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	102.5	145.2	135.2	54	
R _{θJB}	Junction-to-board thermal resistance	92.6	65.7	111.7	51	
ψ _{JT}	Junction-to-top characterization parameter	39.5	47.0	16.5	1	
ψ _{JB}	Junction-to-board characterization parameter	63.4	65.4	111.0	50	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			– 40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V _{OH}		I _{OH} = – 100 μA	1.2V to 3.6V	1.2V to 3.6V				V _{CCO} – 0.2		V
		I _{OH} = – 3mA	1.2V	1.2V		0.95				
		I _{OH} = – 6mA	1.4V	1.4V				1.05		
		I _{OH} = – 8mA	1.65V	1.65V				1.2		
		I _{OH} = – 9mA	2.3V	2.3V				1.75		
		I _{OH} = – 12mA	3V	3V				2.3		
V _{OL}		I _{OL} = 100 μA	1.2V to 3.6V	1.2V to 3.6V				0.2		V
		I _{OL} = 3mA	1.2V	1.2V		0.15				
		I _{OL} = 6mA	1.4V	1.4V				0.35		
		I _{OL} = 8mA	1.65V	1.65V				0.45		
		I _{OL} = 9mA	2.3V	2.3V				0.55		
		I _{OL} = 12mA	3V	3V				0.7		
I _I	DIR	V _I = V _{CCA} or GND	1.2V to 3.6V	1.2V to 3.6V	– 0.25	±0.025	0.25	– 1	1	μA
I _{off}	A port	V _I or V _O = 0 to 3.6V	0V	0 to 3.6V	– 1	±0.1	1	– 5	5	μA
	B port		0 to 3.6V	0V	– 1	±0.1	1	– 5	5	
I _{OZ}	B port	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	0V	3.6V	– 2.5	±0.5	2.5	– 5	5	μA
	A port		3.6V	0V	– 2.5	±0.5	2.5	– 5	5	
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0	1.2V to 3.6V	1.2V to 3.6V				10		μA
			0V	3.6V				– 2		
			3.6V	0V				10		
I _{CCB}		V _I = V _{CCI} or GND, I _O = 0	1.2V to 3.6V	1.2V to 3.6V				10		μA
			0V	3.6V				10		
			3.6V	0V				– 2		
I _{CCA} + I _{CCB} (see 表 8-3)		V _I = V _{CCI} or GND, I _O = 0	1.2V to 3.6V	1.2V to 3.6V				20		μA
C _i	Control inputs	V _I = 3.3V or GND	3.3V	3.3V		2.5				pF
C _{io}	A or B port	V _O = 3.3V or GND	3.3V	3.3V		6				pF

- (1) V_{CCI} is the V_{CC} associated with the input port.
- (2) V_{CCO} is the V_{CC} associated with the output port.
- (3) All unused data inputs of the device must be held at V_{CCI} or GND for proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

5.6 Switching Characteristics: $V_{CCA} = 1.2V$

over recommended operating free-air temperature range, $V_{CCA} = 1.2V$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2V$	$V_{CCB} = 1.5V$	$V_{CCB} = 1.8V$	$V_{CCB} = 2.5V$	$V_{CCB} = 3.3V$	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.3	2.7	2.4	2.3	2.4	ns
t_{PHL}			3.3	2.7	2.4	2.3	2.4	
t_{PLH}	B	A	3.3	3.1	2.9	2.8	2.7	ns
t_{PHL}			3.3	3.1	2.9	2.8	2.7	
t_{PHZ}	DIR	A	5.1	5.2	5.3	5.2	3.7	ns
t_{PLZ}			5.1	5.2	5.3	5.2	3.7	
t_{PHZ}	DIR	B	5.3	4.3	4	3.3	3.7	ns
t_{PLZ}			5.3	4.3	4	3.3	3.7	
$t_{PZH}^{(1)}$	DIR	A	8.6	7.3	6.8	6.1	6.4	ns
$t_{PZL}^{(1)}$			8.6	7.3	6.8	6.1	6.4	
$t_{PZH}^{(1)}$	DIR	B	8.3	7.8	7.7	7.5	5.8	ns
$t_{PZL}^{(1)}$			8.3	7.8	7.7	7.5	5.8	

(1) The enable time is a calculated value, derived using the formula shown in the 节 8.1.1 section.

5.7 Switching Characteristics: $V_{CCA} = 1.5V \pm 0.1V$

over recommended operating free-air temperature range, $V_{CCA} = 1.5V \pm 0.1V$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2V$	$V_{CCB} = 1.5V \pm 0.1V$		$V_{CCB} = 1.8V \pm 0.15V$		$V_{CCB} = 2.5V \pm 0.2V$		$V_{CCB} = 3.3V \pm 0.3V$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	ns
t_{PHL}			2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	
t_{PLH}	B	A	2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	ns
t_{PHL}			2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	
t_{PHZ}	DIR	A	3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	ns
t_{PLZ}			3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	
t_{PHZ}	DIR	B	5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	ns
t_{PLZ}			5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	
$t_{PZH}^{(1)}$	DIR	A	7.7		13.6		12.4		9.6		9.3	ns
$t_{PZL}^{(1)}$			7.7		13.6		12.4		9.6		9.3	
$t_{PZH}^{(1)}$	DIR	B	6.7		12.3		12		11.1		10.7	ns
$t_{PZL}^{(1)}$			6.7		12.3		12		11.1		10.7	

(1) The enable time is a calculated value, derived using the formula shown in the 节 8.1.1 section.

5.8 Switching Characteristics: $V_{CCA} = 1.8V \pm 0.15V$

over recommended operating free-air temperature range, $V_{CCA} = 1.8V \pm 0.15V$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2V$	$V_{CCB} = 1.5V \pm 0.1V$		$V_{CCB} = 1.8V \pm 0.15V$		$V_{CCB} = 2.5V \pm 0.2V$		$V_{CCB} = 3.3V \pm 0.3V$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.7	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	ns
t_{PHL}			2.7	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	
t_{PLH}	B	A	2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	ns
t_{PHL}			2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	
t_{PHZ}	DIR	A	3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	ns
t_{PLZ}			3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	
t_{PHZ}	DIR	B	5	1.8	7.7	1.4	6.8	1	4.4	1.4	5.3	ns
t_{PLZ}			5	1.8	7.7	1.4	6.8	1	4.4	1.4	5.3	
$t_{PZH}^{(1)}$	DIR	A	7.3		12.9		11.8		9		8.7	ns
$t_{PZL}^{(1)}$			7.3		12.9		11.8		9		8.7	
$t_{PZH}^{(1)}$	DIR	B	6.5		11.2		10.9		9.8		9.4	ns
$t_{PZL}^{(1)}$			6.5		11.2		10.9		9.8		9.4	

(1) The enable time is a calculated value, derived using the formula shown in the 节 8.1.1 section.

5.9 Switching Characteristics: $V_{CCA} = 2.5V \pm 0.2V$

over recommended operating free-air temperature range, $V_{CCA} = 2.5V \pm 0.2V$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2V$	$V_{CCB} = 1.5V \pm 0.1V$		$V_{CCB} = 1.8V \pm 0.15V$		$V_{CCB} = 2.5V \pm 0.2V$		$V_{CCB} = 3.3V \pm 0.3V$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	ns
t_{PHL}			2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	
t_{PLH}	B	A	2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	ns
t_{PHL}			2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	
t_{PHZ}	DIR	A	2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	ns
t_{PLZ}			2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	
t_{PHZ}	DIR	B	4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	ns
t_{PLZ}			4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	
$t_{PZH}^{(1)}$	DIR	A	7.1		11.8		10.3		7.5		7.3	ns
$t_{PZL}^{(1)}$			7.1		11.8		10.3		7.5		7.3	
$t_{PZH}^{(1)}$	DIR	B	5.4		8.6		8.1		7		6.6	ns
$t_{PZL}^{(1)}$			5.4		8.6		8.1		7		6.6	

(1) The enable time is a calculated value, derived using the formula shown in the 节 8.1.1 section.

5.10 Switching Characteristics: $V_{CCA} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CCA} = 3.3V \pm 0.3V$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2V$	$V_{CCB} = 1.5V \pm 0.1V$		$V_{CCB} = 1.8V \pm 0.15V$		$V_{CCB} = 2.5V \pm 0.2V$		$V_{CCB} = 3.3V \pm 0.3V$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	ns
t_{PHL}			2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	
t_{PLH}	B	A	2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	ns
t_{PHL}			2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	
t_{PHZ}	DIR	A	3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	ns
t_{PLZ}			3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	
t_{PHZ}	DIR	B	4	0.7	7.4	0.6	6.5	0.7	4	1.5	4.9	ns
t_{PLZ}			4	0.7	7.4	0.6	6.5	0.7	4	1.5	4.9	
$t_{PZH}^{(1)}$	DIR	A	6.2		11.2		9.9		7		6.7	ns
$t_{PZL}^{(1)}$			6.2		11.2		9.9		7		6.7	
$t_{PZH}^{(1)}$	DIR	B	5.7		8.9		8.5		7.2		6.8	ns
$t_{PZL}^{(1)}$			5.7		8.9		8.5		7.2		6.8	

(1) The enable time is a calculated value, derived using the formula shown in the 节 8.1.1 section.

5.11 Operating Characteristics

$T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.2V$	$V_{CCA} = V_{CCB} = 1.5V$	$V_{CCA} = V_{CCB} = 1.8V$	$V_{CCA} = V_{CCB} = 2.5V$	$V_{CCA} = V_{CCB} = 3.3V$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$C_{pdA}^{(1)}$	A-port input, B-port output	$C_L = 0pF$, $f = 10MHz$, $t_r = t_f = 1ns$	3	3	3	3	4	pF
	B-port input, A-port output		13	13	14	15	15	
$C_{pdB}^{(1)}$	A-port input, B-port output	$C_L = 0pF$, $f = 10MHz$, $t_r = t_f = 1ns$	13	13	14	15	15	pF
	B-port input, A-port output		3	3	3	3	3	

(1) Power dissipation capacitance per transceiver

5.12 Typical Characteristics

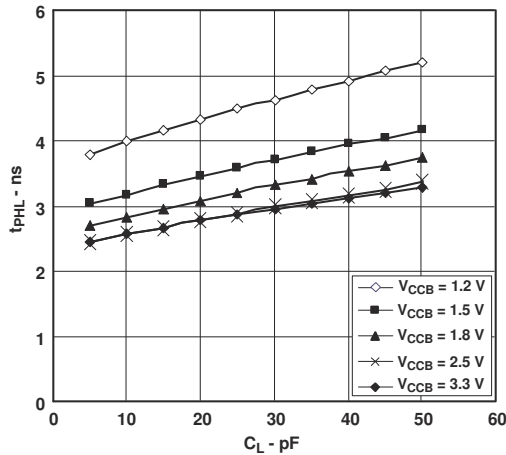


图 5-1. Typical Propagation Delay
of High-to-Low (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2\text{V}$

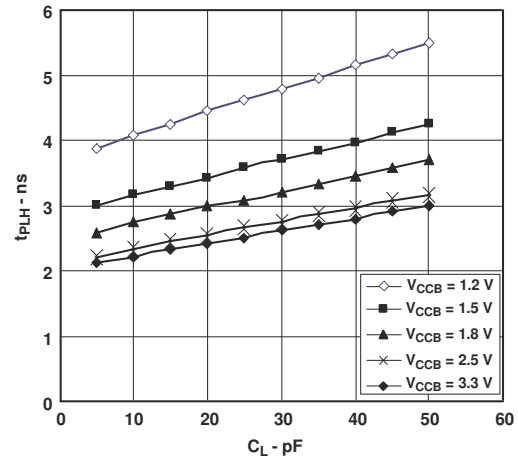


图 5-2. Typical Propagation Delay
of Low-to-High (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2\text{V}$

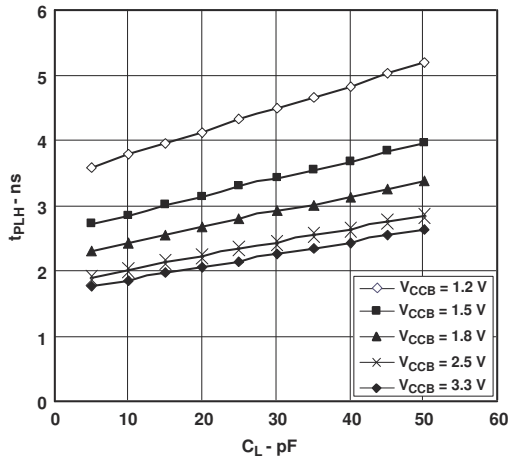


图 5-3. Typical Propagation Delay
of High-to-Low (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.5\text{V}$

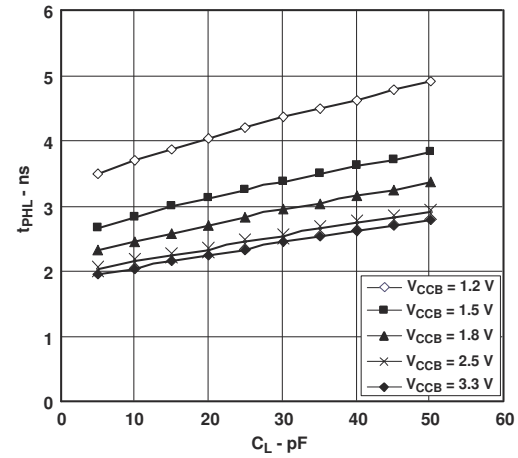


图 5-4. Typical Propagation Delay
of Low-to-High (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.5\text{V}$

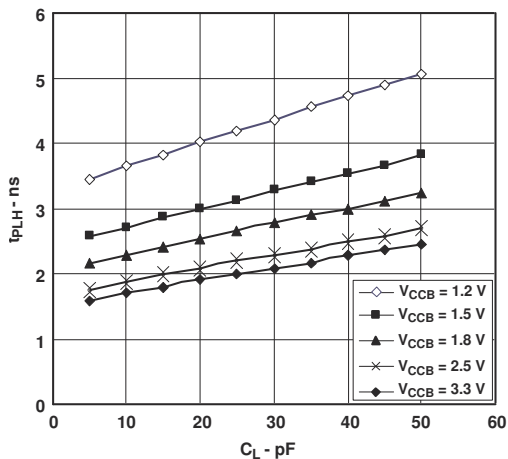


图 5-5. Typical Propagation Delay
of High-to-Low (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{V}$

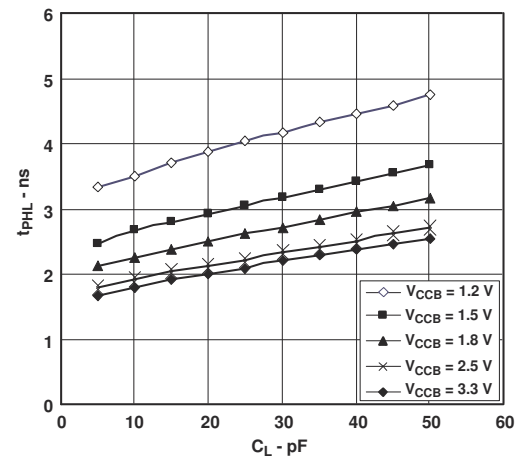


图 5-6. Typical Propagation Delay
of Low-to-High (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{V}$

5.12 Typical Characteristics (continued)

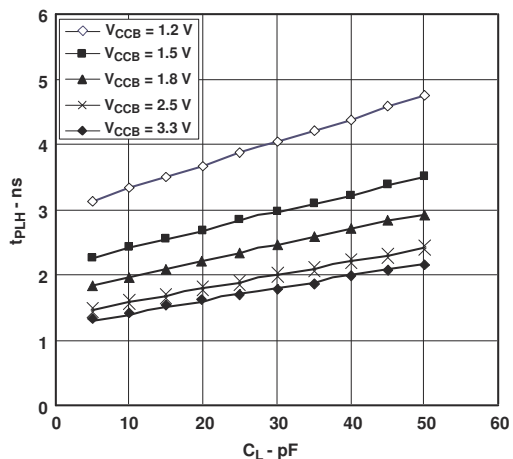


图 5-7. Typical Propagation Delay
of High-to-Low (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{V}$

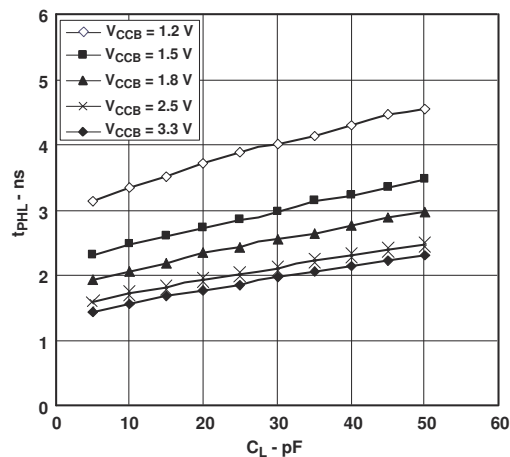


图 5-8. Typical Propagation Delay
of Low-to-High (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{V}$

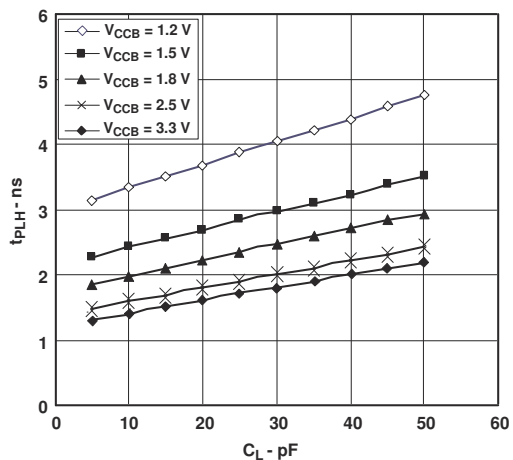


图 5-9. Typical Propagation Delay
of High-to-Low (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{V}$

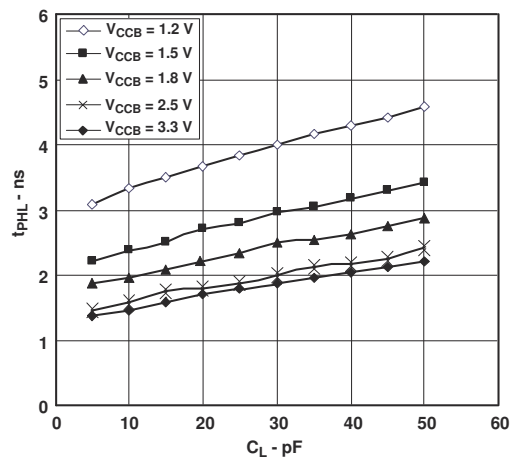
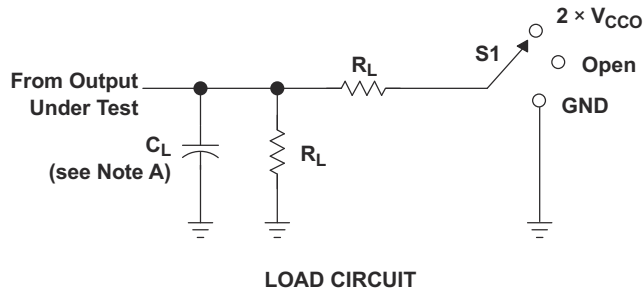


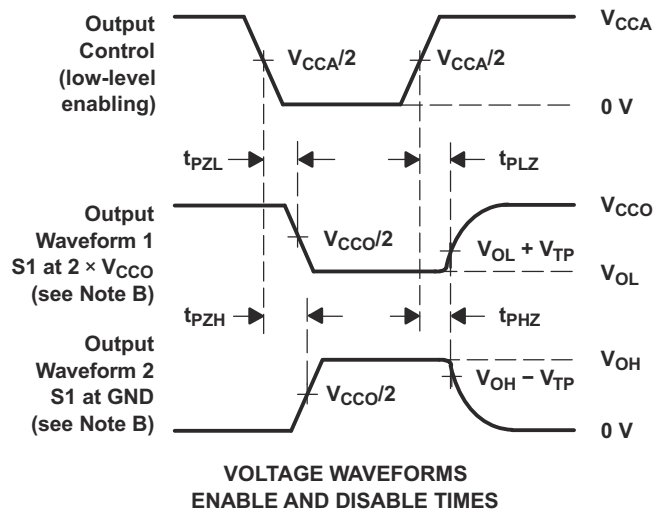
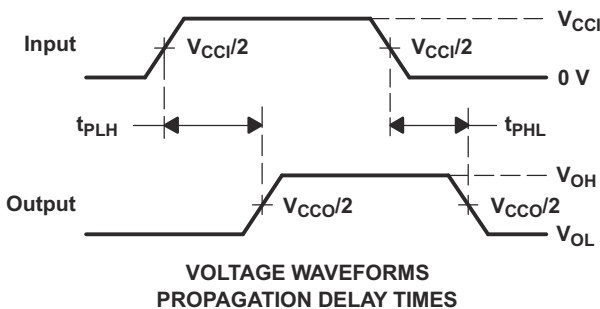
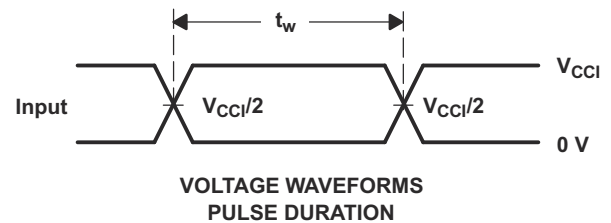
图 5-10. Typical Propagation Delay
of Low-to-High (A to B) vs Load Capacitance
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{V}$

6 Parameter Measurement Information



V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kW	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 kW	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 kW	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 kW	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 kW	0.3 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CCI} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.

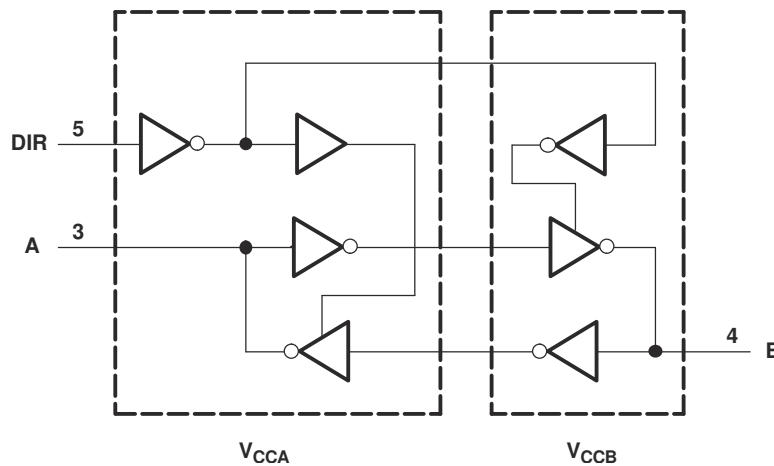
图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AVC1T45 is single-bit, dual-supply, noninverting voltage level translation. V_{CCA} supports pin A and the direction control pin, and V_{CCB} supports pin B. The A port can accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.2 to 3.6V. The high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fully Configurable

The fully configurable dual-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range. Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2V and 3.6V making the device an excellent choice for translating between any of the voltage nodes (1.2V, 1.8V, 2.5V, and 3.3V).

7.3.2 Support High-Speed Translation

SN74AVC1T45 can support high data-rate application. The translated signal data rate can be up to 500Mbps when signal is translated from 1.8V to 3.3V.

7.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

7.4 Device Functional Modes

表 7-1. Function Table

INPUT DIR ⁽¹⁾	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74AVC1T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum data rate can be up to 500Mbps when device translate signal from 1.8V to 3.3V.

8.1.1 Enable Times

Calculate the enable times for the SN74AVC1T45 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

8.2 Typical Applications

8.2.1 Unidirectional Logic Level-Shifting Application

图 8-1 shows an example of the SN74AVC1T45 being used in a unidirectional logic level-shifting application.

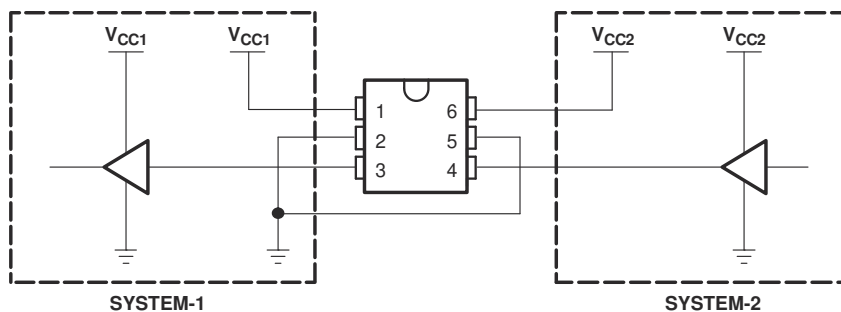


图 8-1. Unidirectional Logic Level-Shifting Application

PIN	NAME	FUNCTION	DESCRIPTION
1	V _{CCA}	V _{CC1}	SYSTEM-1 supply voltage (1.2V to 3.6V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V _{CC1} voltage.
4	B	IN	Input threshold value depends on V _{CC2} voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V _{CCB}	V _{CC2}	SYSTEM-2 supply voltage (1.2V to 3.6V)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.2V to 3.6V
Output voltage range	1.2V to 3.6V

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the SN74AVC1T45 device to determine the input voltage range. For a valid logic-high, the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.
- Output voltage range
 - Use the supply voltage of the device that the SN74AVC1T45 device is driving to determine the output voltage range.

8.2.1.3 Application Curve

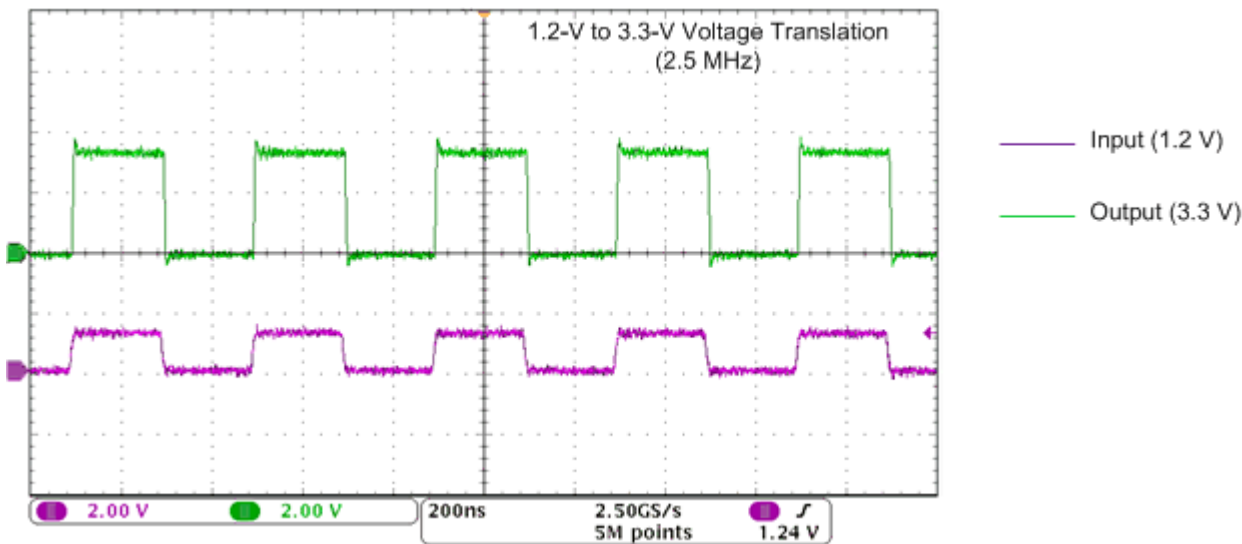


图 8-2. Translation Up (1.2V to 3.3V) at 2.5MHz

8.2.2 Bidirectional Logic Level-Shifting Application

图 8-3 shows the SN74AVC1T45 being used in a bidirectional logic level-shifting application. Because the SN74AVC1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

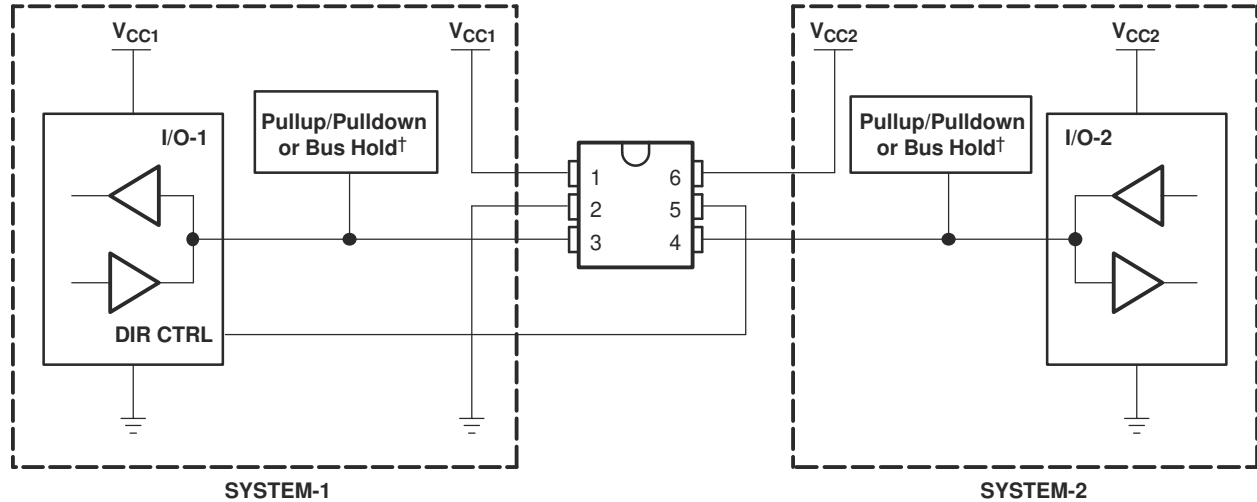


图 8-3. Bidirectional Logic Level-Shifting Application

The following table provides data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

表 8-2. Data Transmission: SYSTEM-1 and SYSTEM-2

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions (for example, both pullup or both pulldown).

8.2.2.1 Design Requirements

Refer to 节 8.2.1.1.

8.2.2.2 Detailed Design Procedure

Refer to 节 8.2.1.2.

8.2.2.3 Application Curve

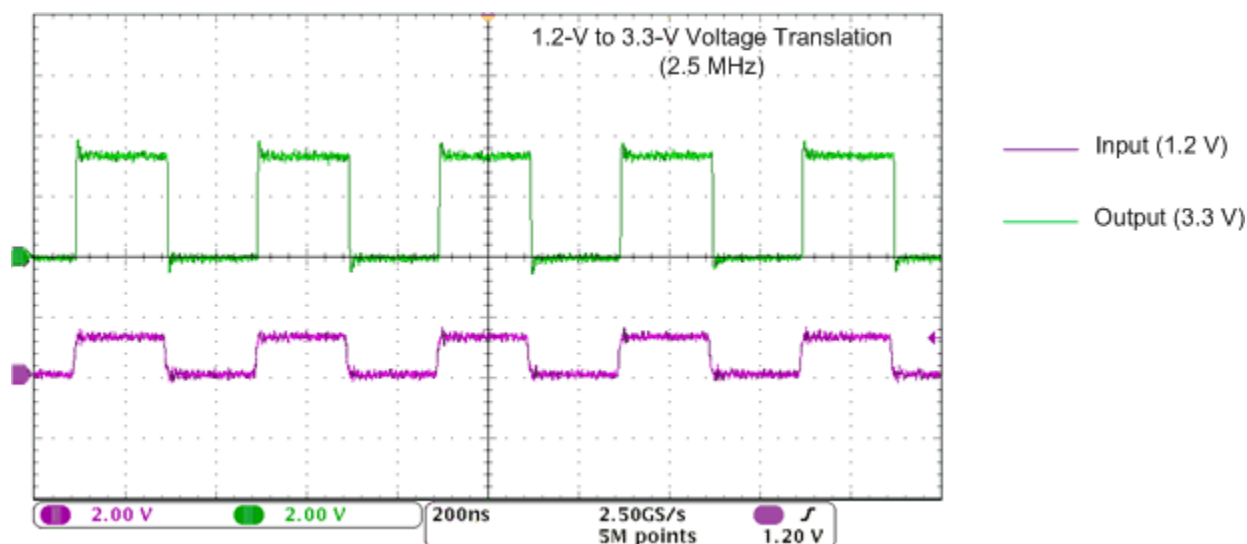


图 8-4. Translation Up (1.2V to 3.3V) at 2.5MHz

8.3 Power Supply Recommendations

The SN74AVC1T45 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB} . V_{CCA} accepts any supply voltage from 1.2V to 3.6V, and V_{CCB} accepts any supply voltage from 1.2V to 3.6V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage, bidirectional translation between any of the 1.2V, 1.5 -V, 1.8V, and 3.3V voltage nodes.

8.3.1 Power-Up Considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA} .
3. V_{CCB} can be ramped up along with or after V_{CCA} .

表 8-3. Typical Total Static Power Consumption ($I_{CCA} + I_{CCB}$)

V_{CCB}	V_{CCA}						UNIT
	0V	1.2V	1.5V	1.8V	2.5V	3.3V	
0V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2V	<0.5	<1	<1	<1	<1	1	
1.5V	<0.5	<1	<1	<1	<1	1	
1.8V	<0.5	<1	<1	<1	<1	<1	
2.5V	<0.5	1	<1	<1	<1	<1	
3.3V	<0.5	1	<1	<1	<1	<1	

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

8.4.2 Layout Example

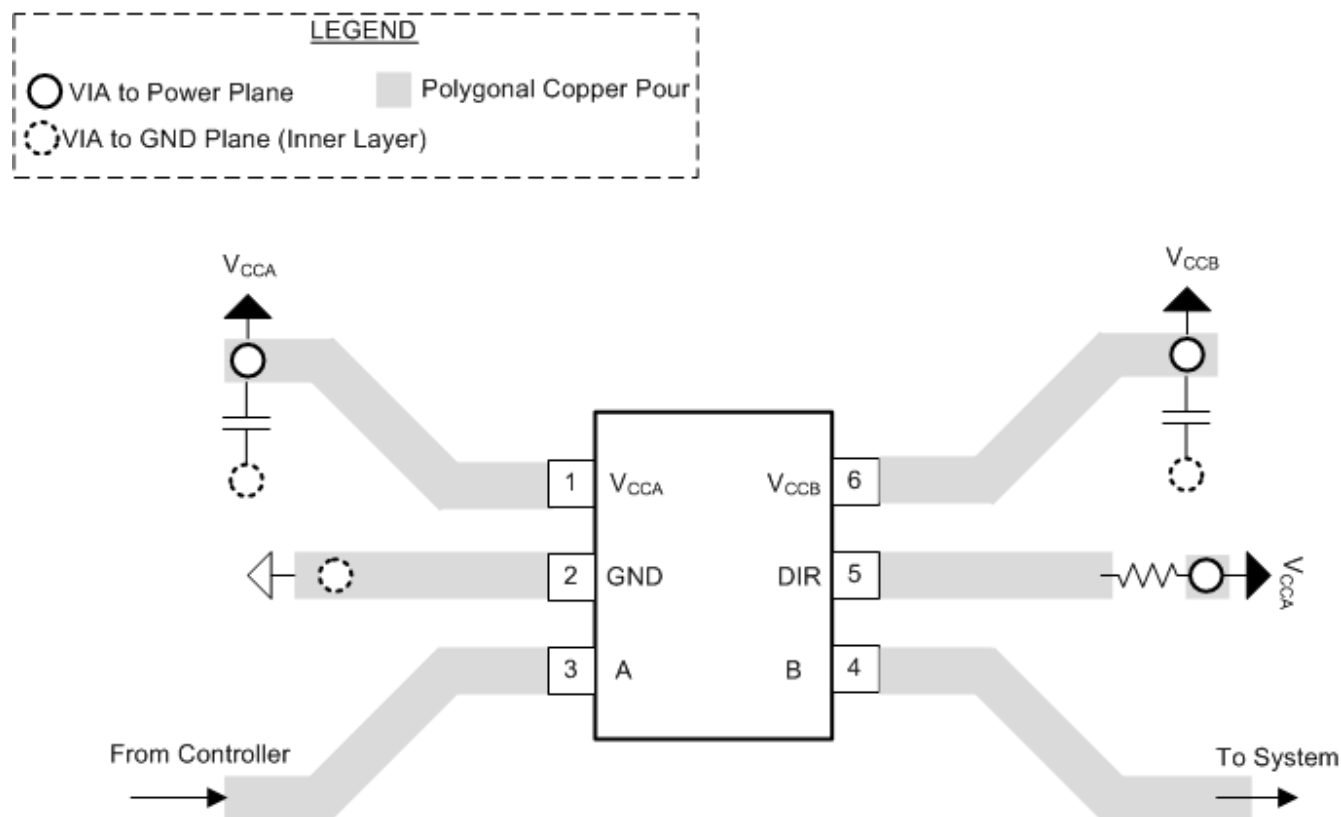


图 8-5. PCB Layout Example

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.3 Trademarks

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9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (October 2014) to Revision I (March 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 更新了封装信息表以包含封装引线尺寸.....	1
• Added Tjmax to the <i>Absolute Maximum Ratings</i> section.....	5

Changes from Revision G (January 2008) to Revision H (October 2014)	Page
• 添加了 引脚配置和功能 部分、 ESD 等级表 、 特性说明 部分、 器件功能模式 、 应用和 实施 部分、 电源相关建议 部分、 布局 部分、 器件和文档支持 部分以及 机械 、 封装和可订购信息 部分.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC1T45DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(DT1F, DT1R) (DT1H, DT1P)	Samples
SN74AVC1T45DBVRE4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	(DT1F, DT1R) (DT1H, DT1P)	Samples
SN74AVC1T45DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	(DT1F, DT1R) (DT1H, DT1P)	Samples
SN74AVC1T45DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT1R DT1H	Samples
SN74AVC1T45DBVTE4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT1R DT1H	Samples
SN74AVC1T45DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DCKRE4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DCKTG4	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(1JW, TCR) TCH	Samples
SN74AVC1T45DRLRG4	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1JW, TCR) TCH	Samples
SN74AVC1T45YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TC2, TCN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

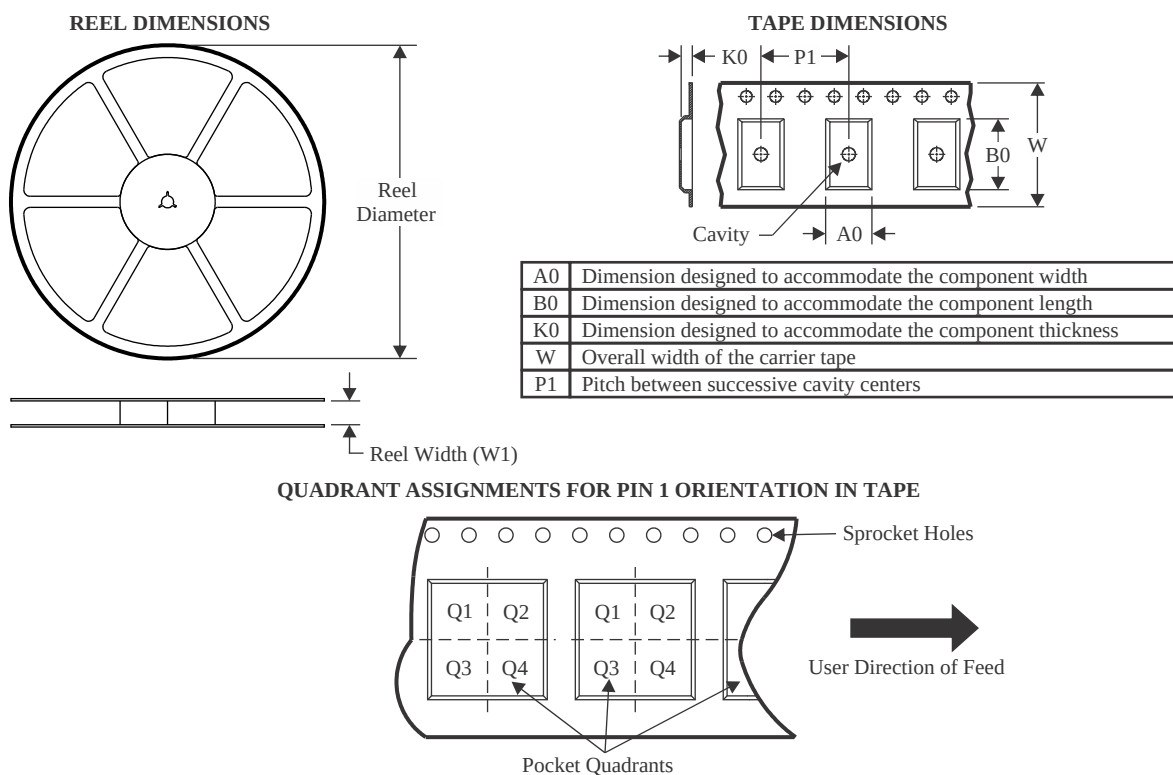
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

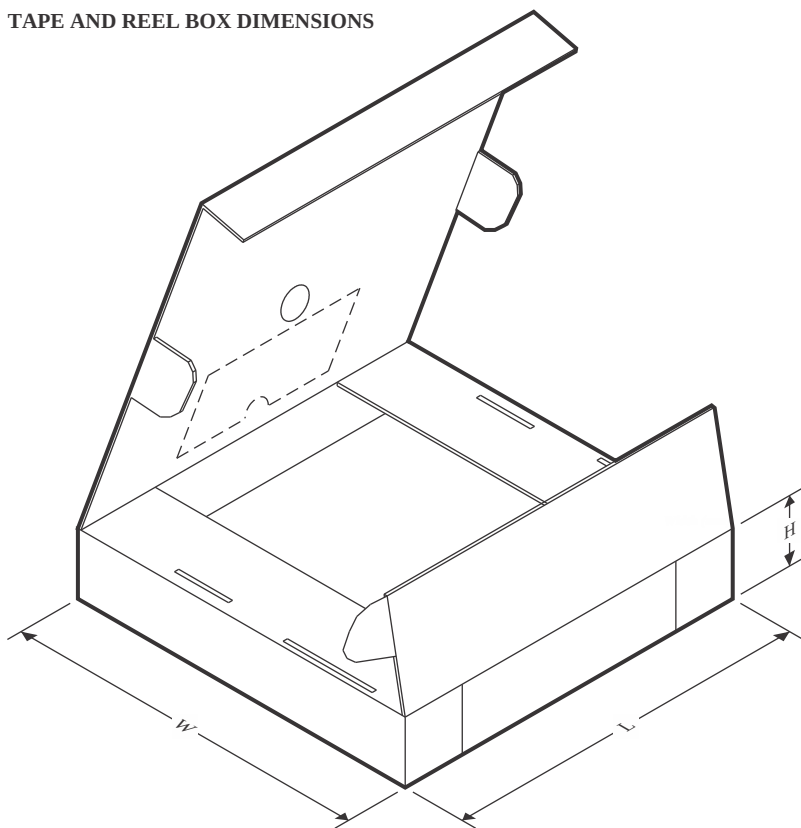
TAPE AND REEL INFORMATION



*All dimensions are nominal

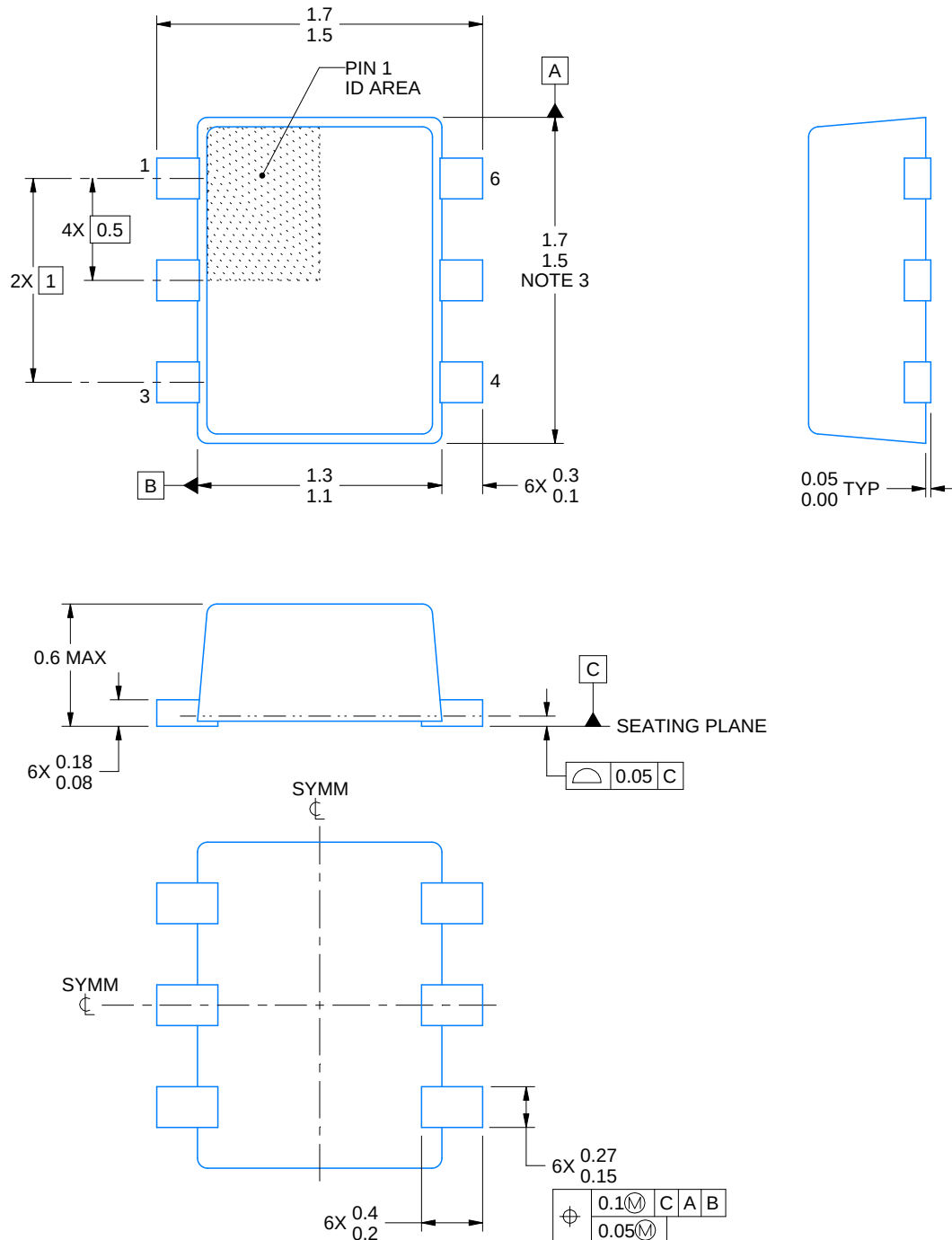
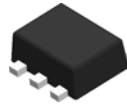
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVC1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AVC1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AVC1T45DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74AVC1T45YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC1T45DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AVC1T45DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AVC1T45DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AVC1T45DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74AVC1T45YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0



4223266/C 12/2021

NOTES:

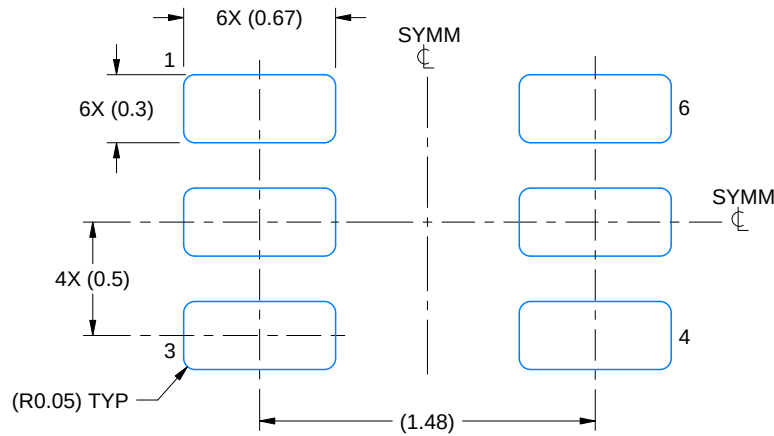
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

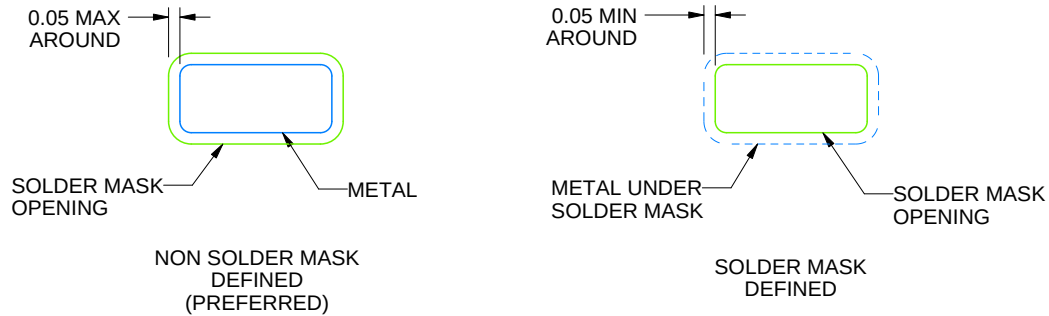
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

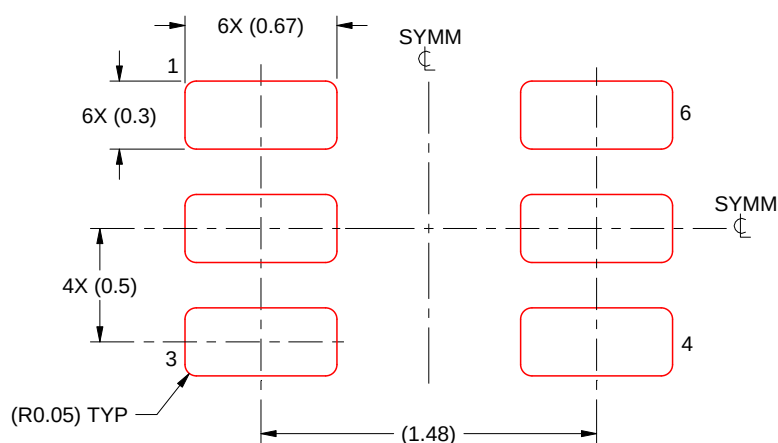
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

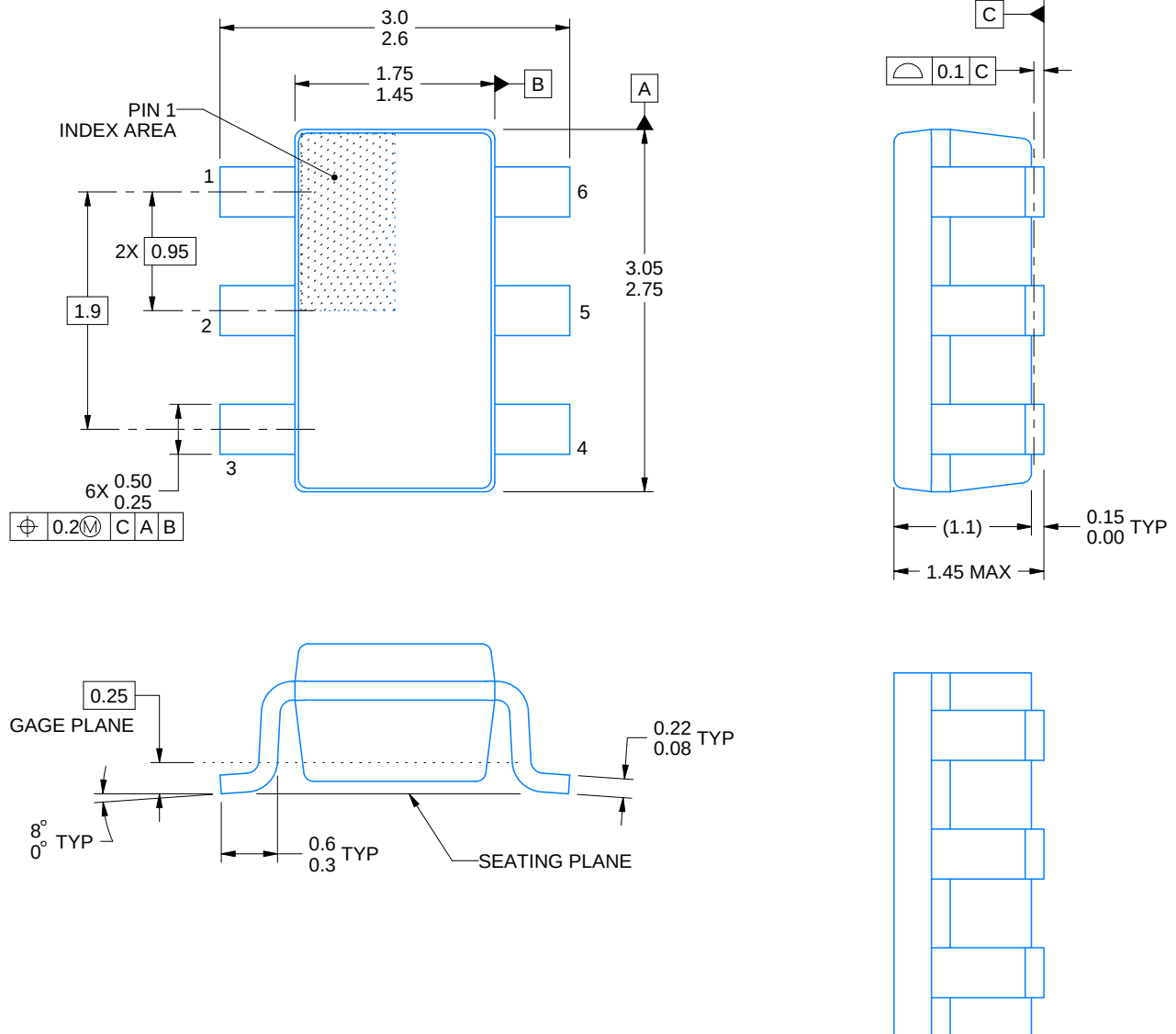
DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214840/E 02/2024

NOTES:

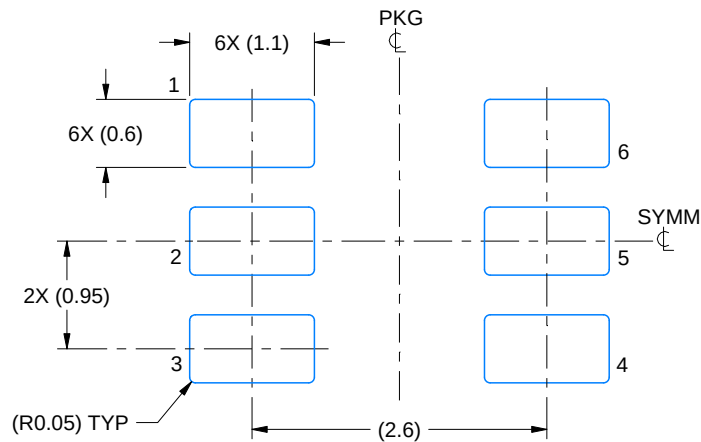
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

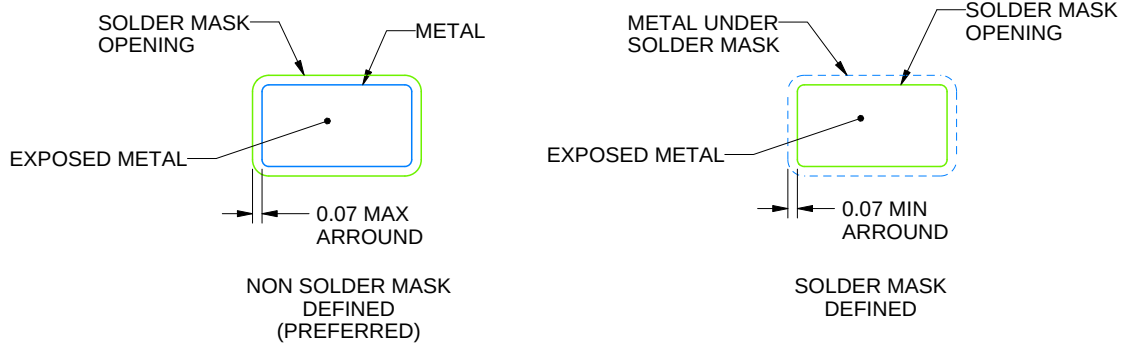
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

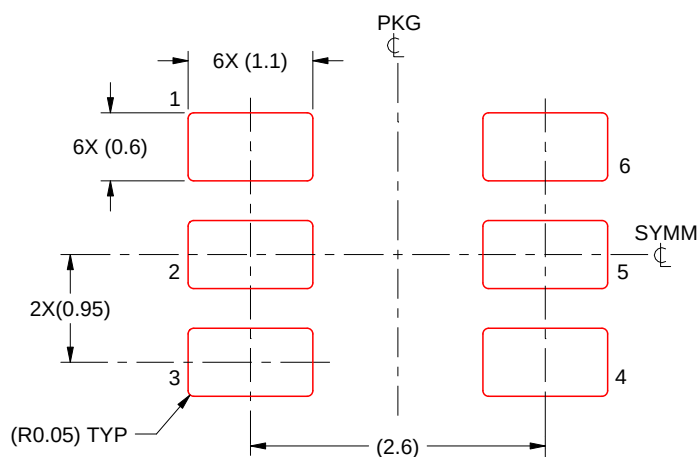
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

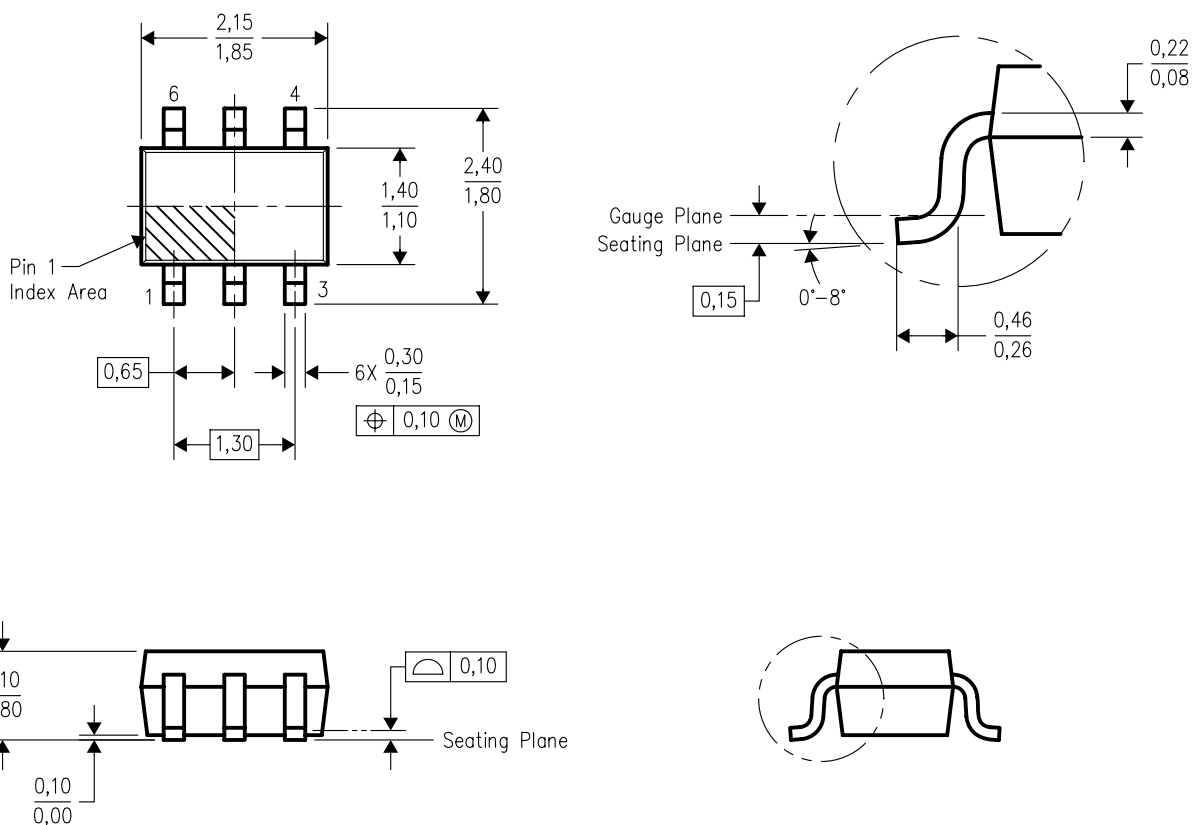
4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

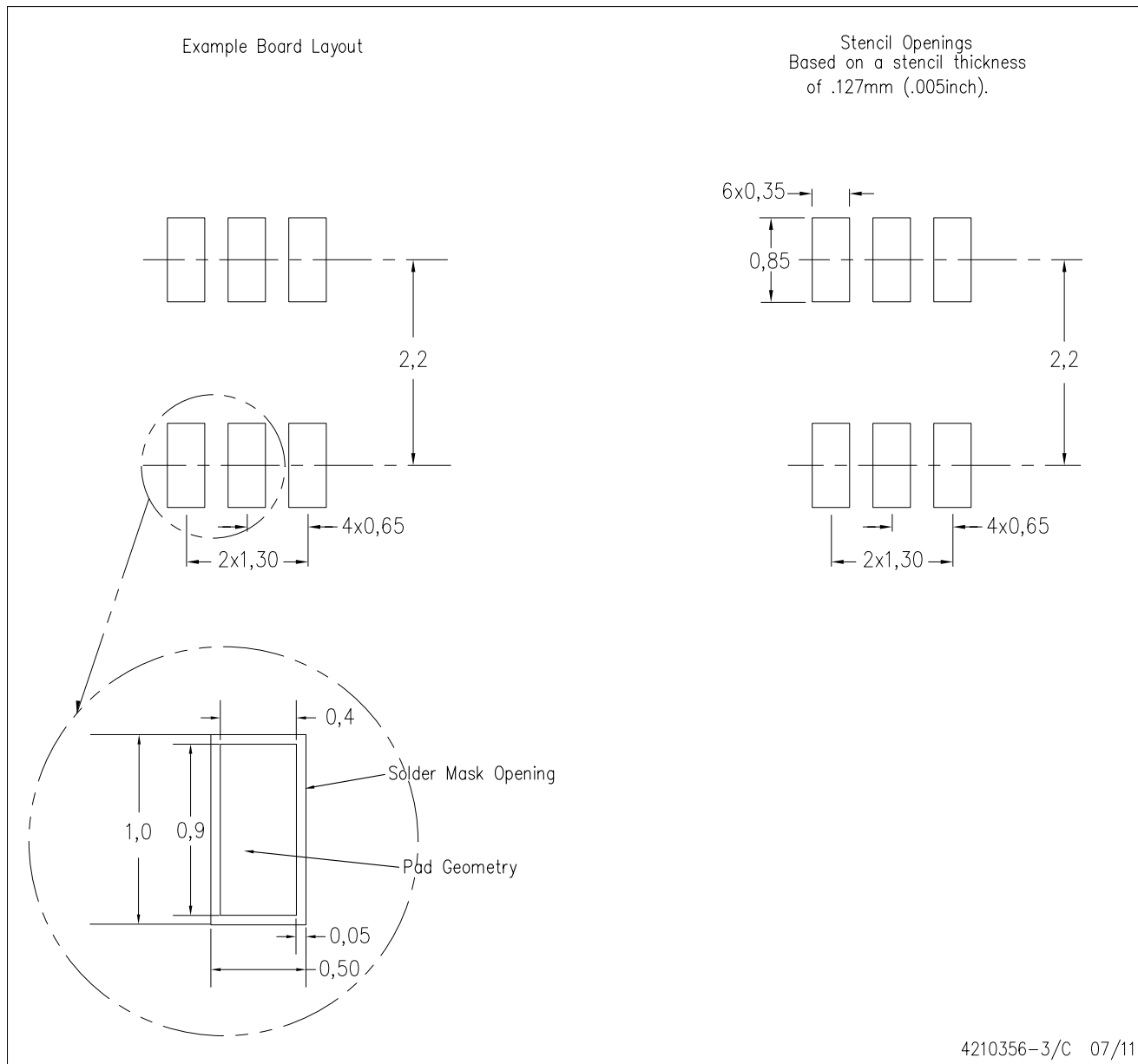


4093553-4/G 01/2007

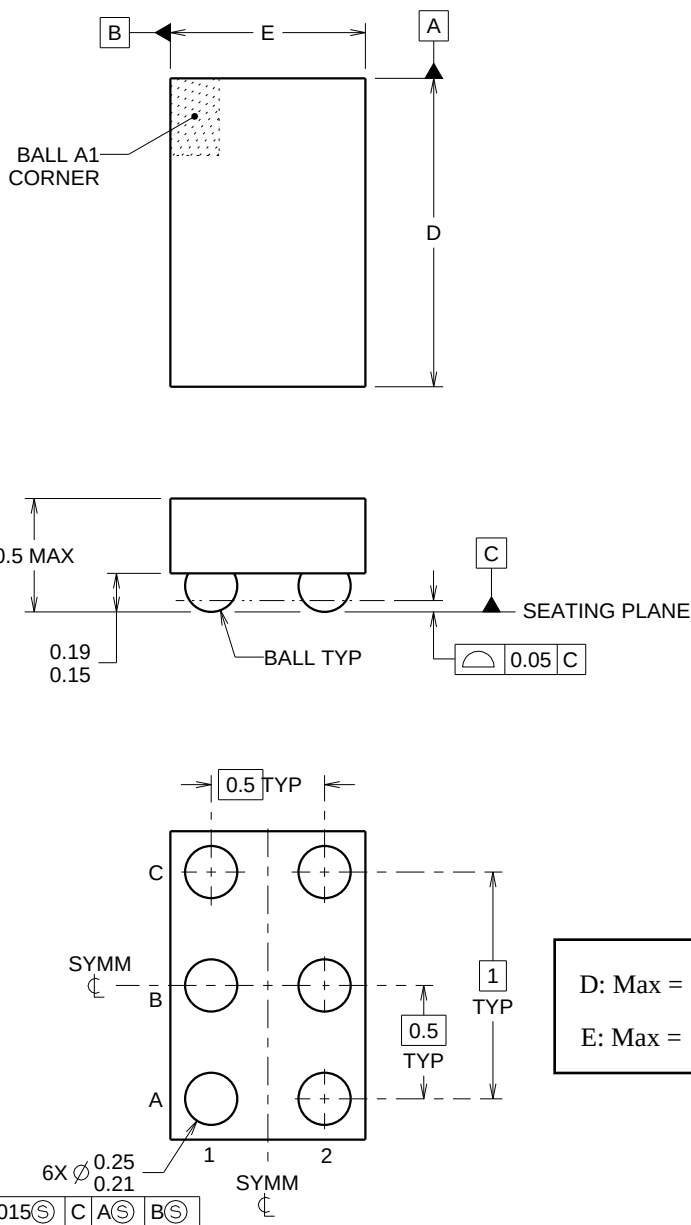
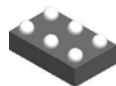
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



4219524/A 06/2014

NOTES:

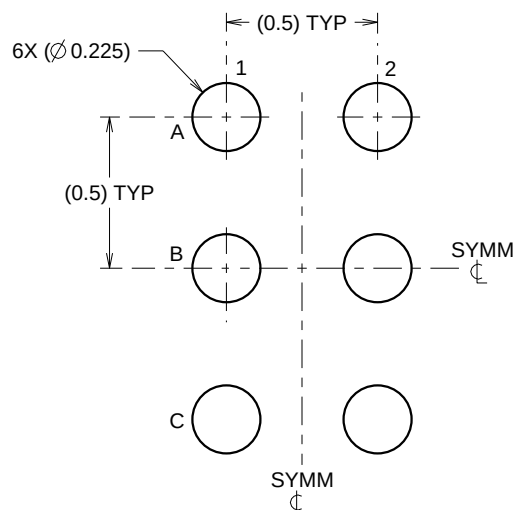
NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

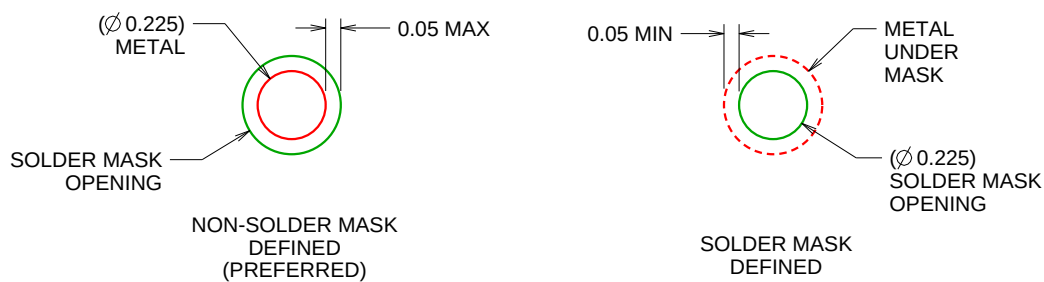
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

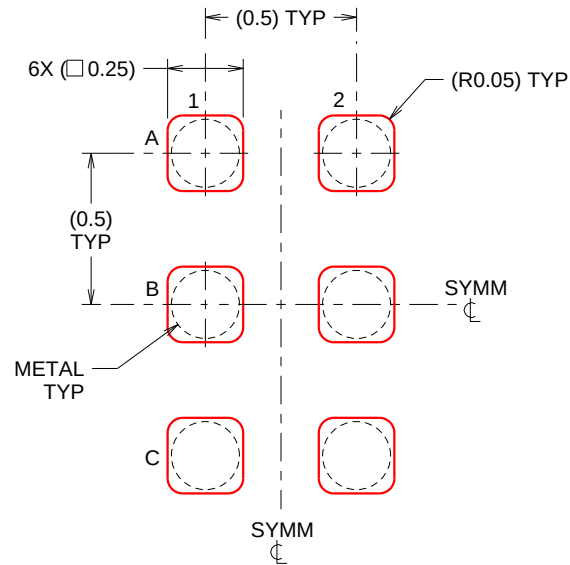
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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