

INA183 2.7V 至 26V、高精度电流检测放大器

1 特性

- 宽共模范围：2.7V 至 26V
- 失调电压： $\pm 170\mu\text{V}$ (最大值)
(支持 10mV 满量程分流压降)
- 精度：
 - 增益误差 $\pm 0.4\%$ (最高过热温度)：
 - $0.5\mu\text{V}/^\circ\text{C}$ 偏移漂移 (最大值)
 - $10\text{ppm}/^\circ\text{C}$ 增益漂移 (最大值)
- 增益选择：
 - INA183A1：50V/V
 - INA183A2：100V/V
 - INA183A3：200V/V
- 静态电流：130 μA (最大值)
- 封装：5 引脚 SOT-23

2 应用

- 服务器
- 电源
- 电池管理
- 电信设备

3 说明

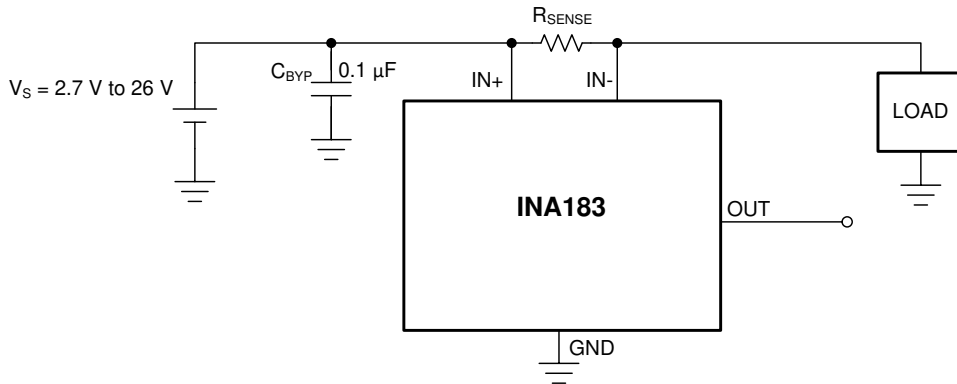
INA183 是一款高精度电压输出、电流分流监控器 (也称为电流检测放大器)，常用于过流保护、针对系统优化的精密电流测量或闭环反馈电路。该器件可在独立于电源电压的 2.7V 至 26V 共模电压下感应分流电阻器上的电压降。50 V/V、100V/V 和 200 V/V。零漂移架构的低偏移使得该器件能够在分流器上的最大压降低至 10mV (满量程) 的情况下进行电流感应。

该器件通过从 IN+ 引脚获取功率而运行，消耗的最大电源电流为 130 μA 。所有版本的额定工作温度范围为 -40°C 至 125°C ，并且采用 5 引脚的 SOT-23 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
INA183	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用



Table of Contents

1 特性	1	8.4 Device Functional Modes.....	11
2 应用	1	9 Application and Implementation	12
3 说明	1	9.1 Application Information.....	12
4 Revision History	2	9.2 Typical Application.....	13
5 Device Comparison	3	10 Power Supply Recommendations	15
6 Pin Configuration and Functions	3	11 Layout	15
7 Specifications	4	11.1 Layout Guidelines.....	15
7.1 Absolute Maximum Ratings	4	11.2 Layout Example.....	15
7.2 ESD Ratings	4	12 Device and Documentation Support	16
7.3 Recommended Operating Conditions	4	12.1 Documentation Support.....	16
7.4 Thermal Information	4	12.2 接收文档更新通知.....	16
7.5 Electrical Characteristics	5	12.3 支持资源.....	16
7.6 Typical Characteristics.....	6	12.4 Trademarks.....	16
8 Detailed Description	10	12.5 静电放电警告.....	16
8.1 Overview.....	10	12.6 术语表.....	16
8.2 Functional Block Diagram.....	10	13 Mechanical, Packaging, and Orderable Information	16
8.3 Feature Description.....	10		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	VERSION	NOTES
February 2021	*	Initial Release.

5 Device Comparison

表 5-1. Device Comparison

PRODUCT	GAIN
INA183A1	50
INA183A2	100
INA183A3	200

6 Pin Configuration and Functions

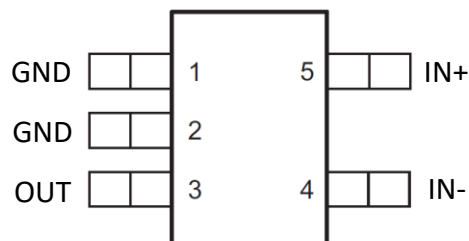


图 6-1. DBV Package 5-Pin SOT-23 Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOT-23		
GND	1, 2	Analog	Device ground. Both pins must be connected to ground.
IN -	4	Analog input	Connect to load side of shunt resistor.
IN+	5	Analog input	Connect to supply side of shunt resistor.
OUT	3	Analog output	Output voltage.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Analog inputs, V_{IN+} , V_{IN-} ⁽¹⁾	Differential ($V_{IN+} - V_{IN-}$)	GND – 0.3	26	V
	Common-mode ⁽²⁾	GND – 0.3	26	V
Output ⁽²⁾		GND – 0.3	(V_{IN+}) + 0.3	V
Operating temperature		– 55	150	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) V_{IN+} and V_{IN-} are the voltages at the $IN+$ and $IN-$ terminals, respectively.

(2) Input voltage at any terminal may exceed the voltage shown if the current at that terminal is limited to 5 mA.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage range, voltage at $IN+$ pin	2.7	12	26	V
T_A	Operating free-air temperature	– 40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA183	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	164.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

at $T_A = 25\text{ }^{\circ}\text{C}$, $V_{\text{SENSE}} = V_{\text{IN}+} - V_{\text{IN}-}$, and $V_{\text{IN}+} = 12\text{ V}$, unless otherwise noted.

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V _{CM}	Common-mode input range		T _A = - 40 °C to +125 °C	2.7		26	V
CMRR	Common-mode rejection ratio		V _{IN+} = 2.7 V to 26 V, V _{SENSE} = 10 mV, T _A = - 40 °C to +125 °C	100	120		dB
V _{OS}	Offset voltage, RTI ⁽¹⁾		V _{CM} = 12 V		±25	±170	μ V
dV _{OS} /dT	RTI vs temperature		T _A = - 40 °C to +125 °C		0.1	0.5	μ V/°C
I _{IB}	Input bias current (IB-)		V _{SENSE} = 0 mV		30	40	μ A
OUTPUT							
G	Gain	A1 devices			50		V/V
		A2 devices			100		V/V
		A3 devices			200		V/V
E _G	Gain error		V _{OUT} = 0.5 V to V _{IN+} - 0.5 V, T _A = - 40 °C to +125 °C		±0.1%	±0.4%	
	Gain error vs temperature		T _A = - 40 °C to +125 °C		3	10	ppm/°C
	Nonlinearity error		V _{OUT} = 0.5 V to V _{IN+} - 0.5 V		±0.01%		
	Maximum capacitive load		No sustained oscillation		1		nF
VOLTAGE OUTPUT							
V _{SP}	Swing to IN+		R _L = 10 kΩ to GND, T _A = - 40 °C to +125 °C		(V _{IN+}) - 0.05	(V _{IN+}) - 0.2	V
V _{SN}	Swing to GND		R _L = 10 kΩ to GND, V _{IN+} - V _{IN-} = -10 mV, T _A = - 40 °C to +125 °C		(V _{GND}) + 0.005	(V _{GND}) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	A1 devices	C _{LOAD} = 10 pF		80		kHz
		A2 devices	C _{LOAD} = 10 pF		30		kHz
		A3 devices	C _{LOAD} = 10 pF		14		kHz
SR	Slew rate				0.4		V/ μ s
NOISE, RTI ⁽¹⁾							
	Voltage noise density				25		nV/ √ Hz
POWER SUPPLY							
I _Q	Quiescent current, (IN+)		V _{SENSE} = 0 mV		83	130	μ A
	I _Q over temperature		T _A = - 40 °C to +125 °C			140	μ A

(1) RTI = referred-to-input.

7.6 Typical Characteristics

$T_A = 25\text{ }^{\circ}\text{C}$, $V_S = V_{IN+} = 12\text{ V}$ (unless otherwise noted)

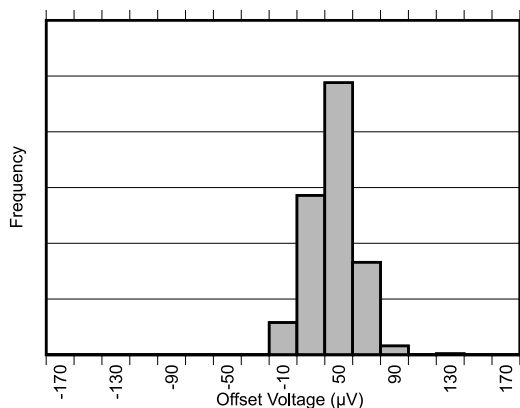


图 7-1. Input Offset Voltage Production Distribution

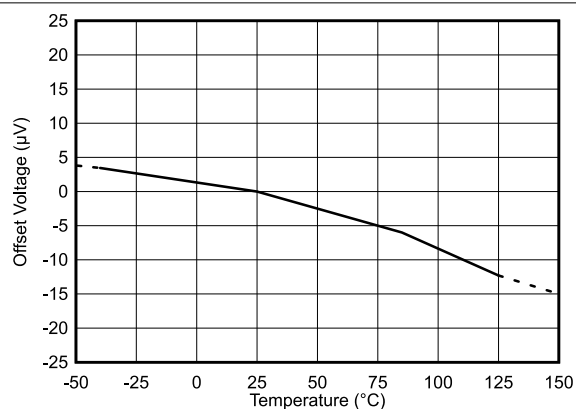


图 7-2. Offset Voltage vs. Temperature

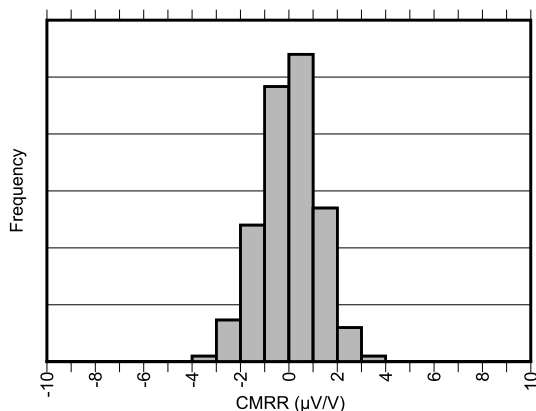


图 7-3. Common-Mode Rejection Production Distribution (A1 Devices)

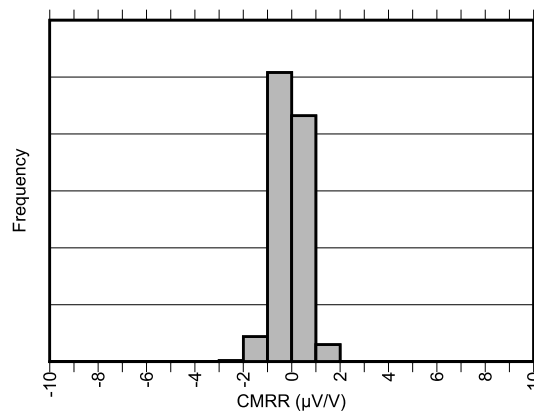


图 7-4. Common-Mode Rejection Production Distribution (A2 Devices)

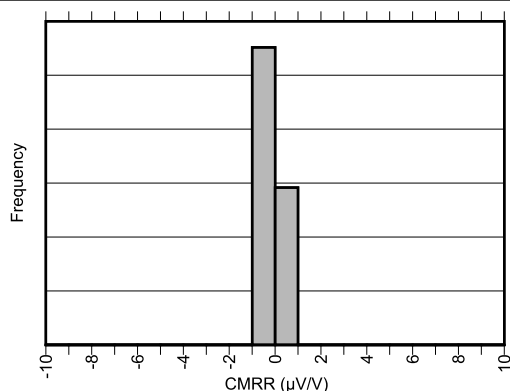


图 7-5. Common-Mode Rejection Production Distribution (A3 Devices)

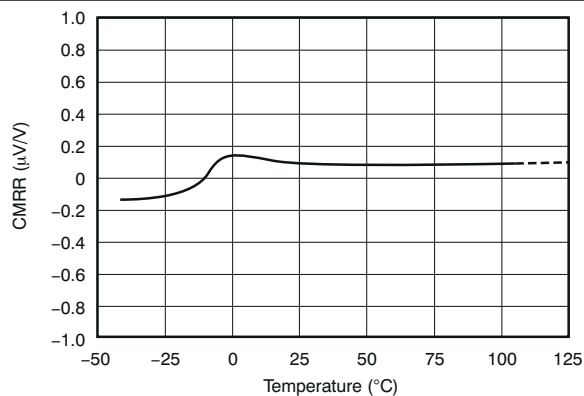


图 7-6. Common-Mode Rejection Ratio vs. Temperature

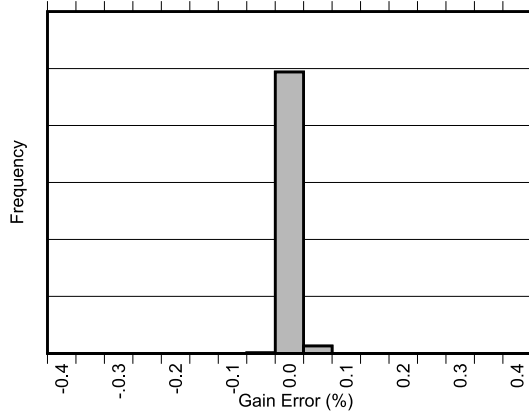


图 7-7. Gain Error Production Distribution (A1 Devices)

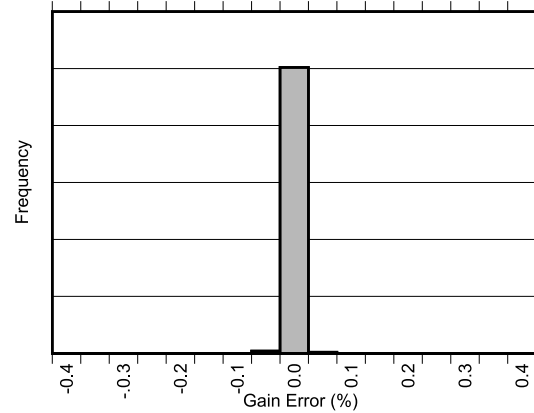


图 7-8. Gain Error Production Distribution (A2 Devices)

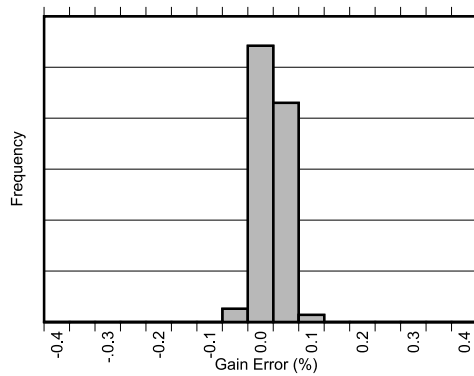


图 7-9. Gain Error Production Distribution (A3 Devices)

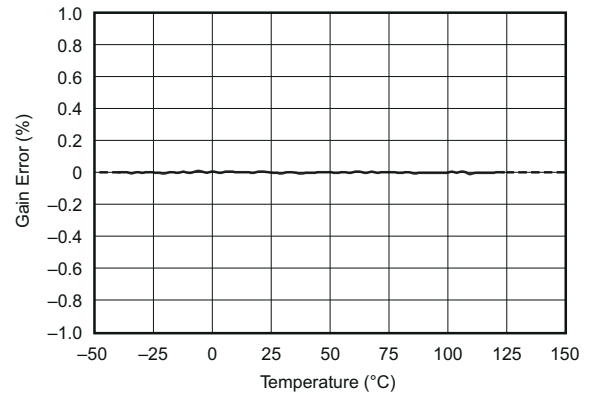


图 7-10. Gain Error vs. Temperature

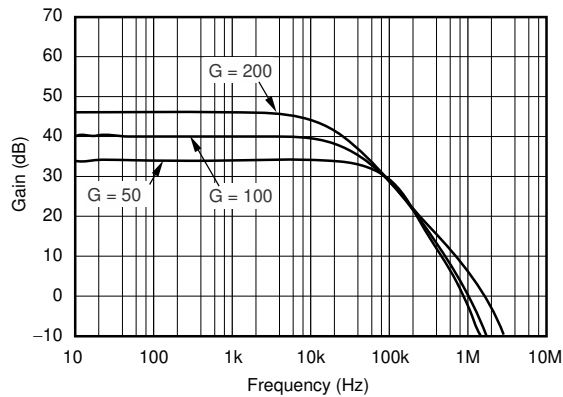


图 7-11. Gain vs. Frequency

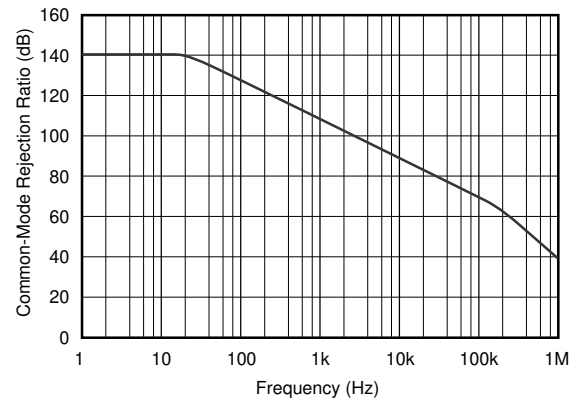


图 7-12. Common-Mode Rejection Ratio vs. Frequency

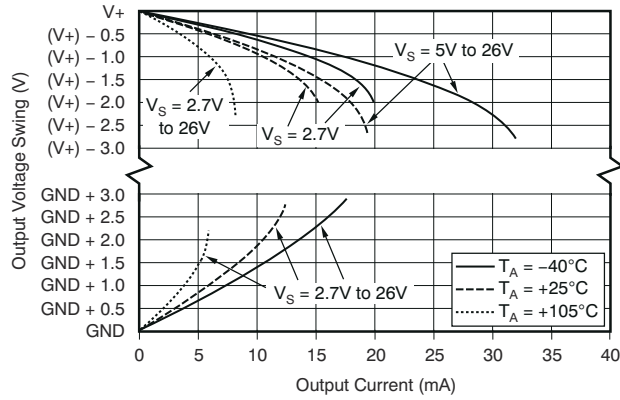


图 7-13. Output Voltage Swing vs. Output Current

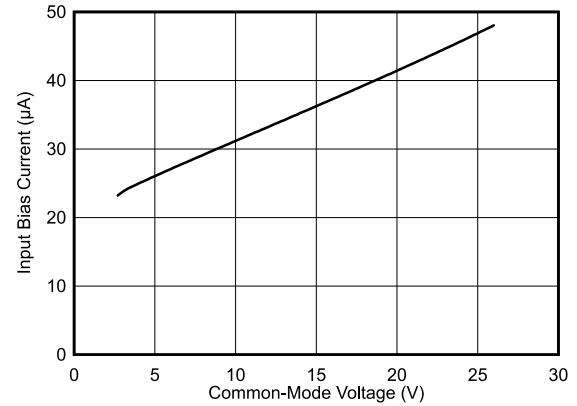


图 7-14. Input Bias Current vs. Common-Mode Voltage

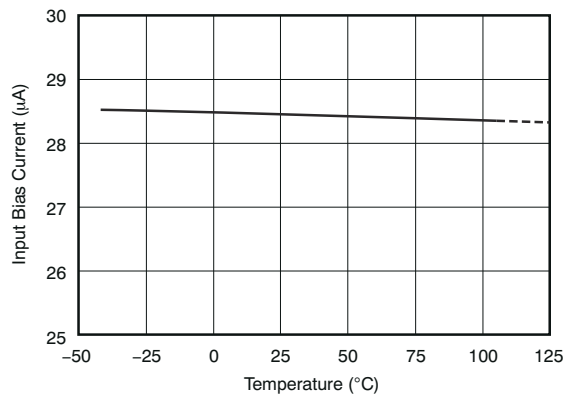


图 7-15. Input Bias Current vs. Temperature

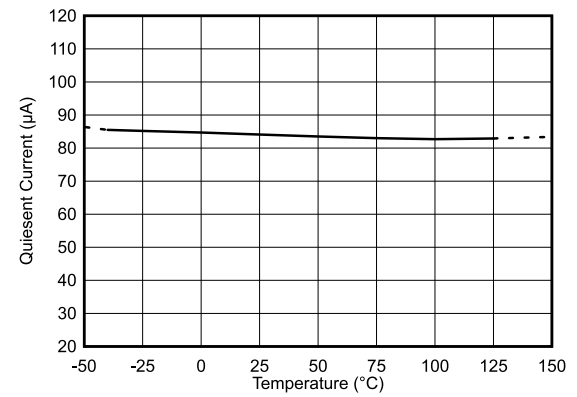


图 7-16. Quiescent Current vs. Temperature

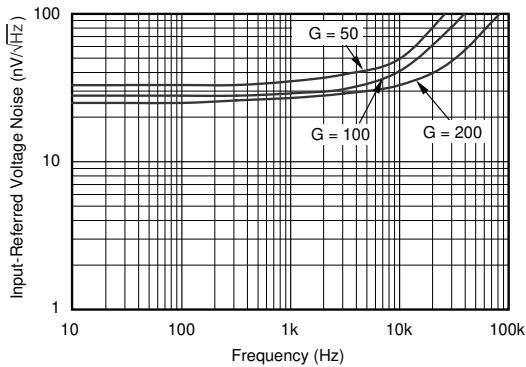


图 7-17. Input-Referred Voltage Noise vs. Frequency

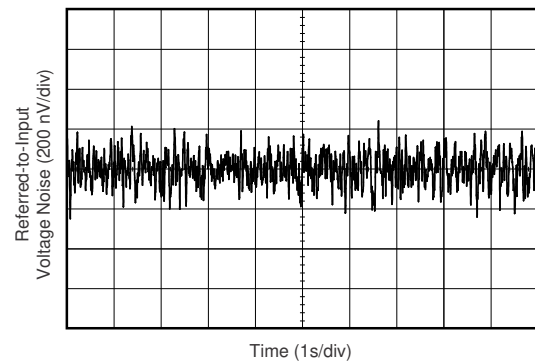


图 7-18. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

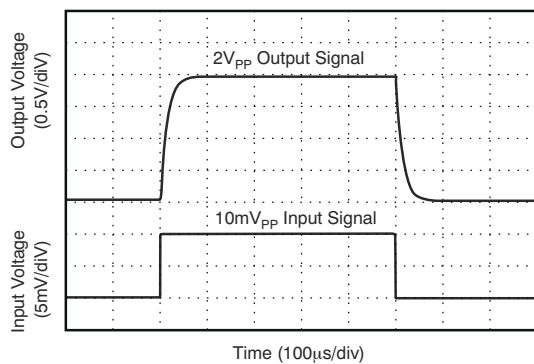


图 7-19. Step Response (10-mV_{PP} Input Step)

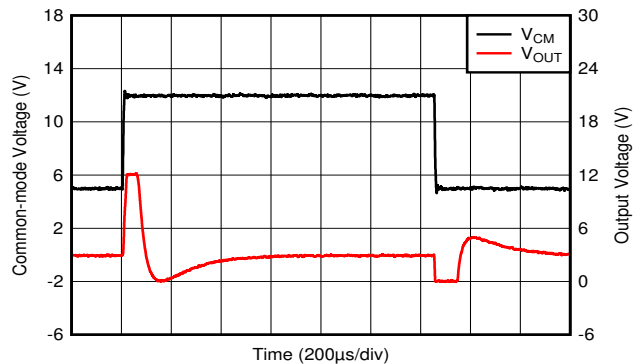


图 7-20. Common-Mode Voltage Transient Response

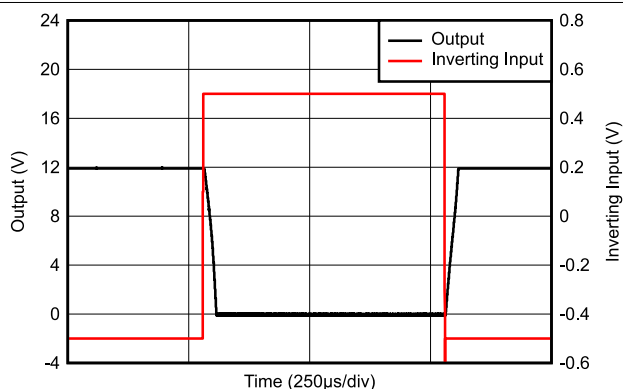
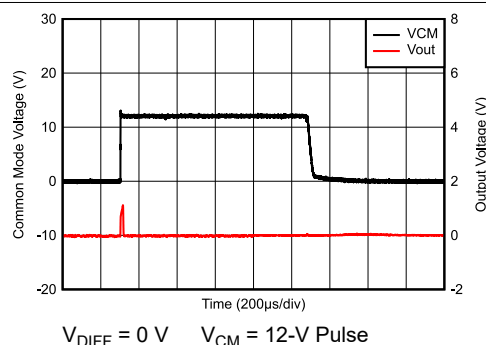


图 7-21. Inverting Differential Input Overload



$V_{DIFF} = 0 \text{ V}$ $V_{CM} = 12\text{-V Pulse}$

图 7-22. Start-Up Response

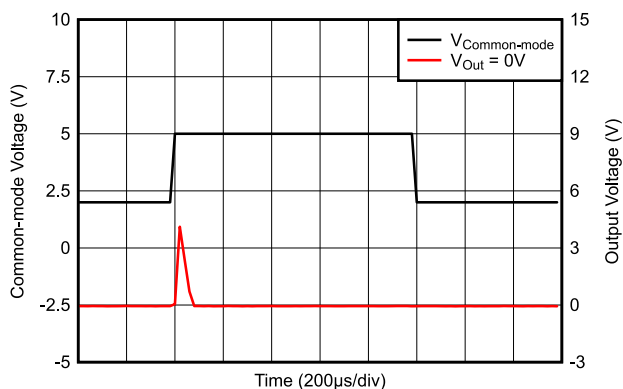


图 7-23. Brownout Recovery

8 Detailed Description

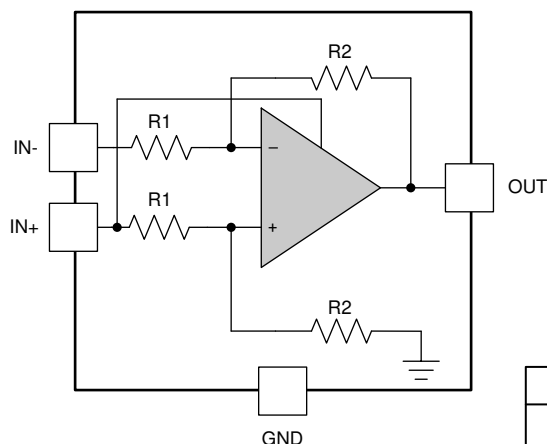
8.1 Overview

The INA183 is a 26-V common-mode, zero-drift topology, current-sensing amplifier meant for high-side, current-sensing applications. The device is a specially-designed, current-sensing amplifier that can accurately measure voltages developed across a current-sensing resistor. The device is capable of measuring current on input voltage rails as high as 26 V and as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 170 μV with a maximum temperature contribution of 0.5 $\mu\text{V}/^\circ\text{C}$ over the full temperature range of -40°C to $+125^\circ\text{C}$.

8.2 Functional Block Diagram

The simplified functional diagram below shows the device power is provided by the voltage on the IN+ pin. This diagram also shows the nominal values for the internal gain set resistors. The nominal value of these resistors can vary by 20% or more; however, the matching between these resistors is tightly controlled. The matching of these internal resistors results in a precise fixed gain that varies very little over temperature.



DEVICE	GAIN	R1	R2
INA183A1	50	20 k Ω	1 M Ω
INA183A2	100	10 k Ω	1 M Ω
INA183A3	200	5 k Ω	1 M Ω

8.3 Feature Description

8.3.1 Single-Supply Operation from IN+

The INA183 does not have a dedicated power-supply. Instead, an internal connection to the IN+ pin serves as the power supply for this device. This allows the device to be used in applications where lower voltage or sub-regulated supply rails are not present. The operational voltage range on this pin is 2.7 V to 26 V and is designed for power-supply applications. The maximum current drawn from the IN+ pin is 130 μA , when the current sense voltage is zero.

8.3.2 Low Gain Error and Offset Voltage

The maximum gain error of the INA183 is 0.4% and is specified over the full operational temperature range. The low gain error allows for accurate measurements as the sense voltage increases, and is designed for applications that need to detect overcurrent conditions accurately. The offset voltage of the INA183 is specified to be $\pm 170 \mu\text{V}$ for all gain options. The low offset voltage allows for increased accuracy when the sense voltage is small or allows for reduction in the size of the current sense resistor with less impact on the total measurement accuracy. Smaller value resistors reduce the power loss in the application which allows the use of lower wattage resistors that are generally lower cost.

8.3.3 Low Drift Architecture

The INA183 features low drift for both the gain error and offset voltage specifications. The low gain error drift of 10 PPM/ $^\circ\text{C}$ results from the well matched internal resistor network that sets the device gain. The low offset drift

is due to the internal chopping architecture of the amplifier. Input chopping reduces both the offset and offset drift since any change in offset is canceled with each chopping cycle. The maximum input offset drift of the INA183 is $0.5 \mu\text{V}/^\circ\text{C}$. The low drift of the gain error and offset voltage provides accurate current measurement over the operational temperature range of -40°C to 125°C that exceeds the performance of most discrete current sensing implementations.

8.4 Device Functional Modes

8.4.1 Normal Operation

The INA183 is in normal operation when the following conditions are met:

- The voltage at the IN+ pin is between 2.7 V and 26 V.
- The maximum differential input signal times the gain is less than $V_{\text{IN}+}$ minus the output voltage swing to $V_{\text{IN}+}$.
- The minimum differential input signal times the gain is greater than the swing to GND.

During normal operation, this device produces an output voltage that is the *amplified* representation of the difference voltage from IN+ to IN-.

8.4.2 Unidirectional, High-Side Operation

The INA183 measures the differential voltage developed by current flowing through a resistor that is commonly referred to as a current shunt resistor or current-sensing resistor. The INA183 operates in high-side, unidirectional mode only, meaning it only senses current sourced from a power supply to a system load as shown in 图 8-1.

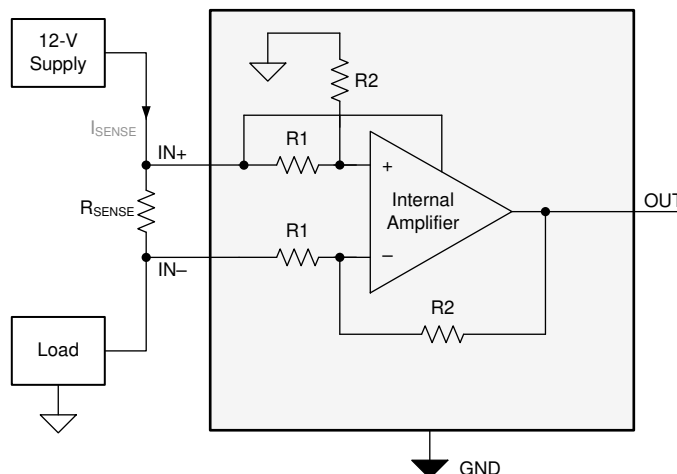


图 8-1. High-Side Unidirectional Application

8.4.3 Input Differential Overload

If the differential input voltage ($V_{\text{IN}+} - V_{\text{IN}-}$) times gain exceeds the voltage swing specification, the INA183 drives the output as close as possible to the IN+ pin or ground, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the INA183 returns to the expected value approximately 30 μs after removal of the fault condition. When the input differential voltage is overloaded the bias currents will increase by a significant amount. The increase in bias currents will occur even with the device is powered down. Input differential overloads less than the absolute maximum voltage rating do not damage the device or result in an output inversion.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The INA183 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

9.1.1 R_{SENSE} and Device Gain Selection

Choosing the largest possible shunt resistor will maximize the accuracy of any current-sense amplifier. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application because of the resistor size and maximum allowable power dissipation. 方程式 1 gives the maximum value for the current-sense resistor for a given power dissipation budget:

$$R_{\text{SENSE}} < \frac{PD_{\text{MAX}}}{I_{\text{MAX}}^2} \quad (1)$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE} .
- I_{MAX} is the maximum current expected to flow through R_{SENSE} .

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage at the IN+ pin, and device swing-to-rail limitations. To ensure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. 方程式 2 provides the maximum values of R_{SENSE} and GAIN to keep the device from exceeding the positive swing limitation.

$$I_{\text{MAX}} \times R_{\text{SENSE}} \times \text{GAIN} < V_{\text{SP}} \quad (2)$$

where:

- I_{MAX} is the maximum current that will flow through R_{SENSE} .
- GAIN is the gain of the current-sense amplifier.
- V_{SP} is the positive output swing as specified in the data sheet.

Positive output swing limitations should be considered when selecting the value of R_{SENSE} . There is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device to avoid positive swing limitations.

The negative swing specification limits how small the sense resistor value can be for a given application. 方程式 3 provides the limit on the minimum value of the sense resistor.

$$I_{\text{MIN}} \times R_{\text{SENSE}} \times \text{GAIN} > V_{\text{SN}} \quad (3)$$

where:

- I_{MIN} is the minimum current that will flow through R_{SENSE} .
- GAIN is the gain of the current-sense amplifier.
- V_{SN} is the negative output swing of the device.

9.2 Typical Application

图 9-1 shows the basic connections for the INA183. The input pins, IN+ and IN−, must be connected as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

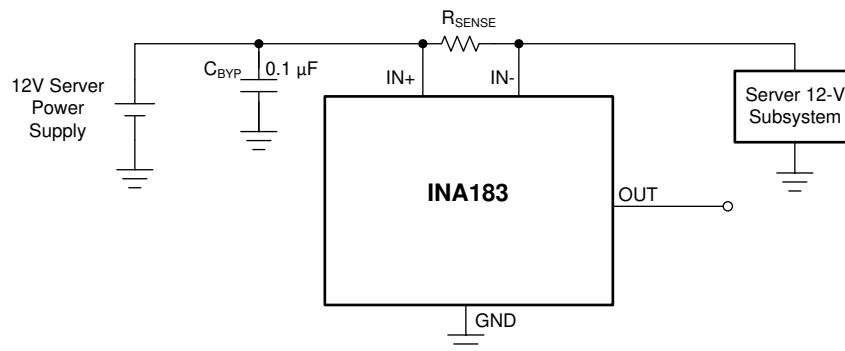


图 9-1. Typical Server Application

A power-supply bypass capacitor is required on the IN+ pin. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

In server applications, the INA183 typically monitors the current on the 12-V bus that is distributed to various server sub-systems like memory, storage, or CPU power. The monitored current can be used by the server for fault detection or sub-system power optimization.

9.2.1 Design Requirements

表 9-1 lists the design setup for this application.

表 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
High-side supply voltage ($V_{\text{IN+}}$)	12 V
Maximum sense current (I_{MAX})	5 A
Gain option	50 V/V

9.2.2 Detailed Design Procedure

The maximum value of the current-sense resistor is calculated based on choice of gain, the value of the maximum current to be sensed (I_{MAX}), and the power-supply voltage ($V_{\text{IN+}}$). When operating at the maximum current, the output voltage must not exceed the positive output swing specification, V_{SP} . Under the given design parameters, 方程式 4 calculates the maximum value for R_{SENSE} as 47.2 mΩ.

$$R_{\text{SENSE}} < \frac{V_{\text{SP}}}{I_{\text{MAX}} \times \text{GAIN}} \quad (4)$$

For this design example, a value of $40.2\text{ m}\Omega$ is selected because, while the $40.2\text{ m}\Omega$ is less than the maximum value calculated, $40.2\text{ m}\Omega$ is still large enough to give an adequate signal at the current-sense amplifier output. To reduce resistor power losses or to operate over a reduced output range, smaller value resistors can be used as the expense of dynamic range and low current accuracy.

9.2.3 Application Curve

图 9-2 shows the output response of the device to a sinusoidal current.

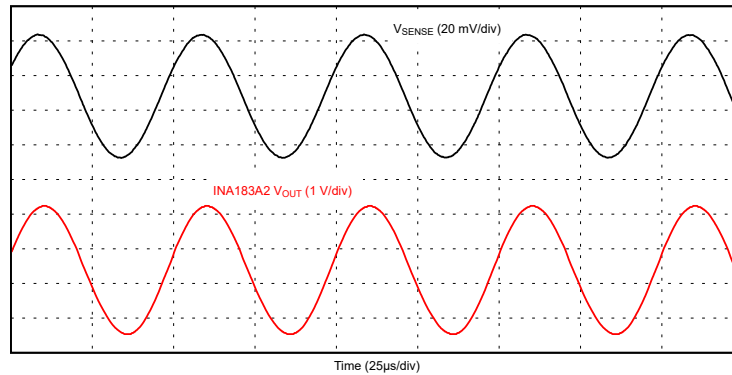


图 9-2. INA183 Output Response

10 Power Supply Recommendations

The device is powered from the IN+ pin with a voltage from 2.7 V to 26 V. The voltage at the output will also be limited by this voltage during overload or fault conditions. Also, the INA183 can withstand the full input signal range up to 26 V on the IN – pin, regardless of whether the device has power applied or not.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the IN+ pin and ground pins. TI recommends using a bypass capacitor with a value of 0.1 μ F. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.2 Layout Example

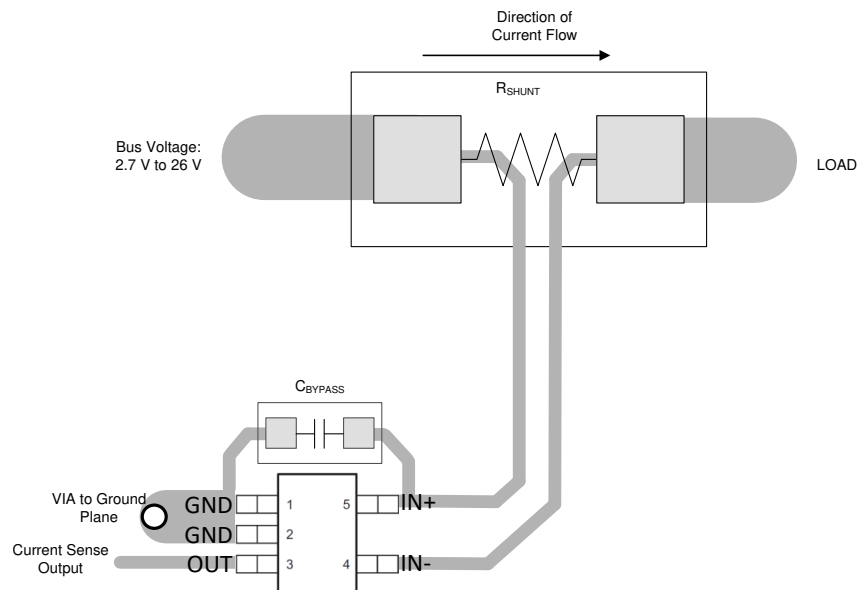


图 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [INA183A1-A3EVM User's Guide](#)
- [TIDA-00302 Transient Robustness for Current Shunt Monitor](#)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA183A1IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BRQ	Samples
INA183A1IDBVT	NRND	SOT-23	DBV	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BRQ	
INA183A2IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BSQ	Samples
INA183A3IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BTQ	Samples
INA183A3IDBVT	NRND	SOT-23	DBV	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BTQ	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

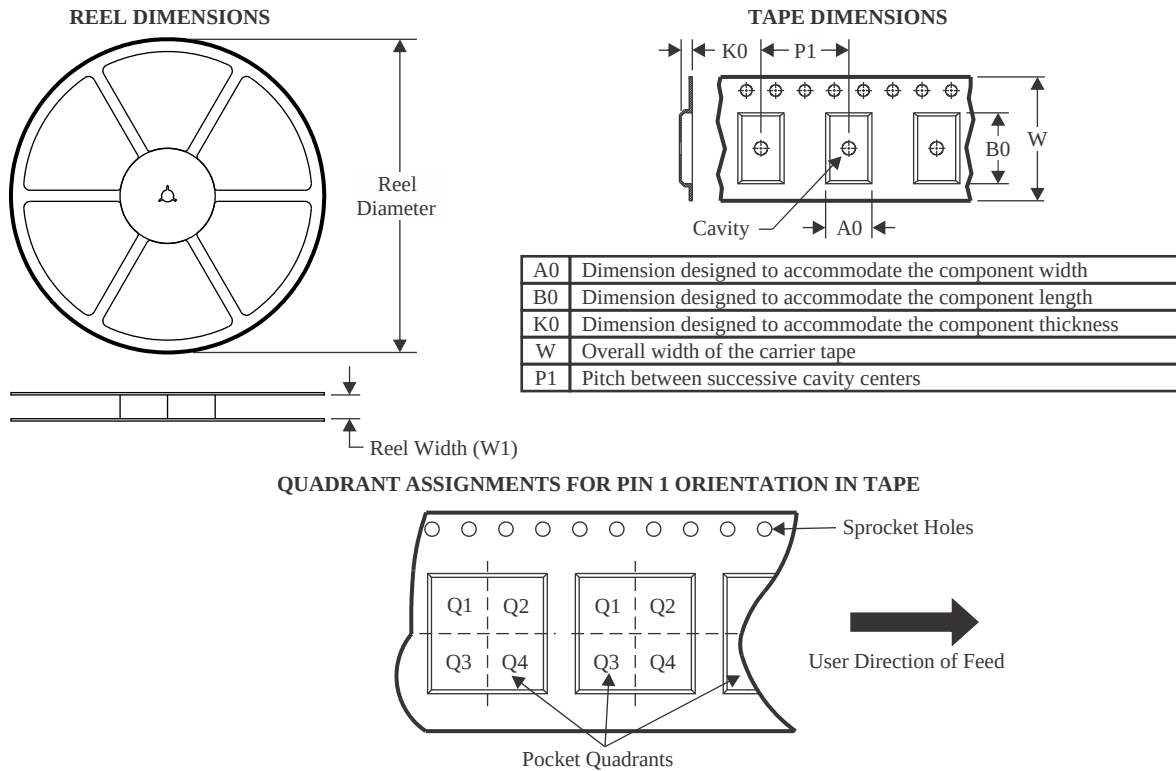
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

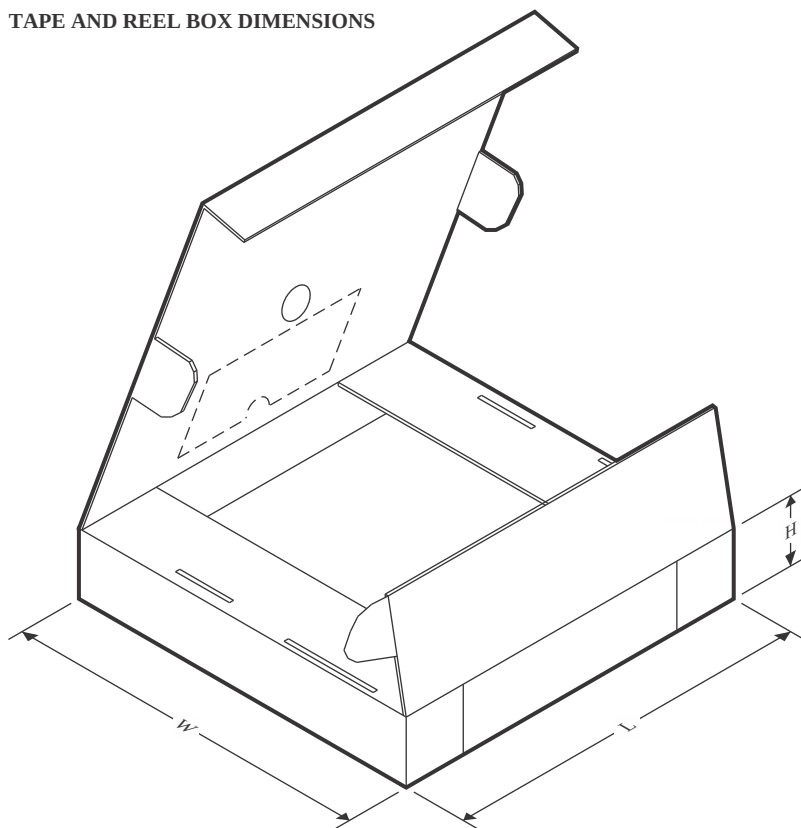
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA183A1IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A1IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A2IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A3IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A3IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA183A1IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
INA183A1IDBVT	SOT-23	DBV	5	250	190.0	190.0	30.0
INA183A2IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
INA183A3IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
INA183A3IDBVT	SOT-23	DBV	5	250	190.0	190.0	30.0



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



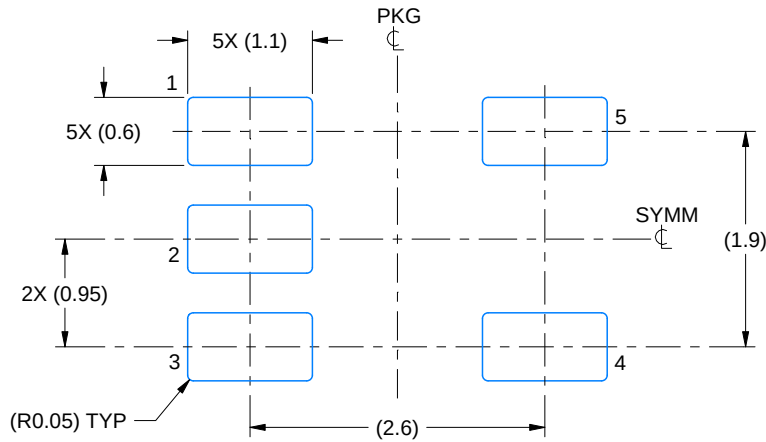
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

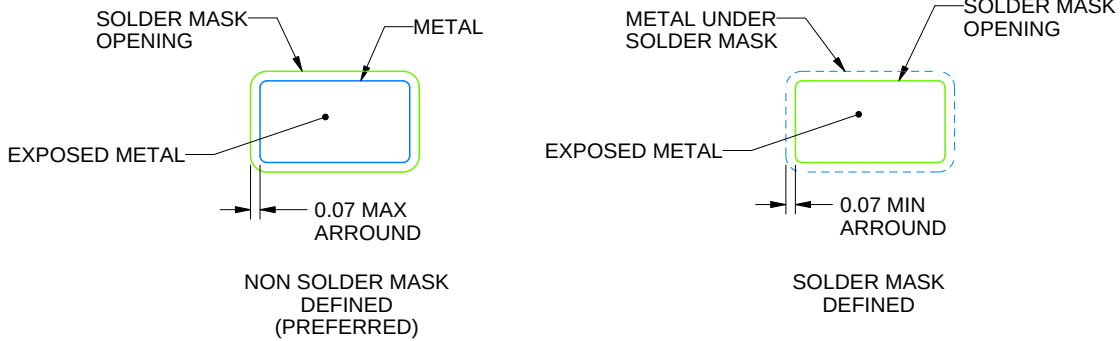
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

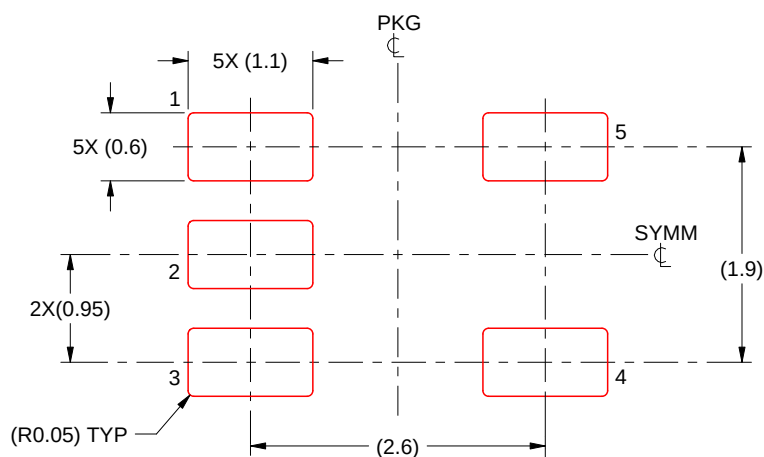
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024，德州仪器 (TI) 公司