# TUSB1210 独立 USB 收发器硅芯片

## 1 特性

- USB2.0 PHY 收发器芯片，可通过 ULPI 接口连接 USB 控制器，完全符合：
  - *通用串行总线规范* 2.0 版
  - *USB 2.0 规范移动附录* 1.3 版
  - *UTMI+ 低引脚接口 (ULPI) 规范* 1.1 版
  - *ULPI 12 引脚 SDR 接口*
- DP/DM 线路外部元件补偿（专利号 US7965100 B1）
- 具有连接主机、外设和 OTG 器件内核的接口；针对便携式设备或具有内置 USB OTG 器件内核的系统 ASIC 进行了优化
- 完整的 USB OTG 物理前端，支持主机协商协议 (HNP) 和会话请求协议 (SRP)
- $V_{BUS}$ 过压保护电路系统可在 –2V 至 20V 的电压范围内保护 $V_{BUS}$ 引脚
- 内部 5V 短路保护功能，可防止 DP、DM 和 ID 引脚通过电缆短接至 $V_{BUS}$ 引脚
- ULPI 接口：
  - I/O 接口 (1.8V) 针对无端接 50Ω 线路阻抗进行了优化
  - ULPI 时钟引脚 (60MHz) 支持输入和输出时钟配置
  - 符合 ULPI 标准的完全可编程寄存器集
- 完全工业级工作温度范围：–40°C 至 85°C
- 采用 32 引脚 Quad Flat No Lead [QFN (RHB)] 封装

## 2 应用

- 手机
- 便携式计算机
- 平板电脑设备
- 视频游戏机
- 台式机
- 便携式音乐播放器

## 3 说明

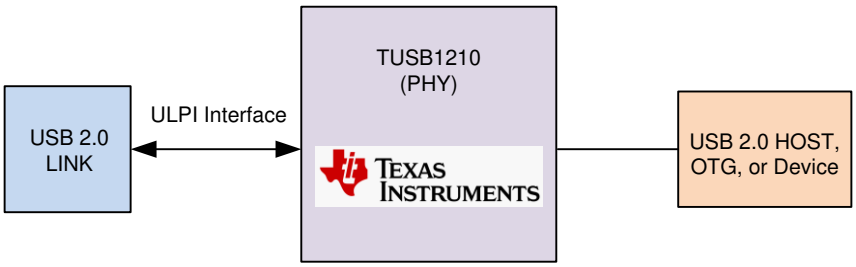
TUSB1210 是一款 USB2.0 收发器芯片，可通过 ULPI 接口连接到 USB 控制器。该器件支持所有 USB2.0 数据速率（高速 480Mbps、全速 12Mbps 以及低速 1.5Mbps），且兼容主机和外设模式。该器件还支持 UART 模式和传统的 ULPI 串行模式。TUSB1210 还支持 USB2.0 规范的 OTG（1.3 版）可选附录，包括 HNP 和 SRP。

发送器中的 DP/DM 外部元件补偿可对串联阻抗中的变化进行补偿，以匹配数据线路阻抗和接收器输入端阻抗，限制数据反射，从而改善眼图。

**器件信息**(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TUSB1210 | VQFN (32) | 5.00mm × 5.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




图

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## 4 Revision History

**Changes from Revision I (December 2019) to Revision J (July 2021)** — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 ..... 1
- Changed the $t_{DC}$, $t_{DD}$ OUTPUT CLOCK delay value From: MAX = 9 ns To: MAX = 5 ns in the *Timing Requirements* ..... 13
- Changed the $t_{DC}$, $t_{DD}$ OUTPUT CLOCK delay value From: MIN = blank To: MIN = 1.2 ns in the *Timing Requirements* ..... 13
- Added the *Related Documentation* section ..... 63

**Changes from Revision H (June 2015) to Revision I (December 2019)** — **Page**

- 将文档从数据手册格式更改为 TI 数据表格式 ..... 1
- Changed RHB Package 32-Pin OFN To: RHB Package 32-Pin VQFN in *Pin Configuration and Functions* ..... 4
- Changed the HBM value From: ±2 V To : ±2000 V in the *ESD Ratings* ..... 6
- Changed the $t_{SC}$, $t_{SD}$ INPUT CLOCK value From: MAX = 3 ns To: MIN = 3 ns in the *Timing Requirements* ..... 13
- Changed the $t_{SC}$, $t_{SD}$ OUTPUT CLOCK value From: MAX = 6 ns To: MIN = 6 ns in the *Timing Requirements* ..... 13
- Deleted section Via Channel from the *Mechanical Packaging and Orderable Information* section ..... 63

**Changes from Revision G (October 2014) to Revision H (June 2015)** — **Page**

- Move Storage Temperature From: *ESD Ratings* To: *Absolute Maximum Ratings* ..... 6
- Changed the *Handling Ratings* table To: *ESD Ratings* ..... 6

**Changes from Revision F (July 2013) to Revision G (October 2014)** **Page**

- 添加了*引脚配置和功能*部分、*ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ..... 1

# 5 Pin Configuration and Functions

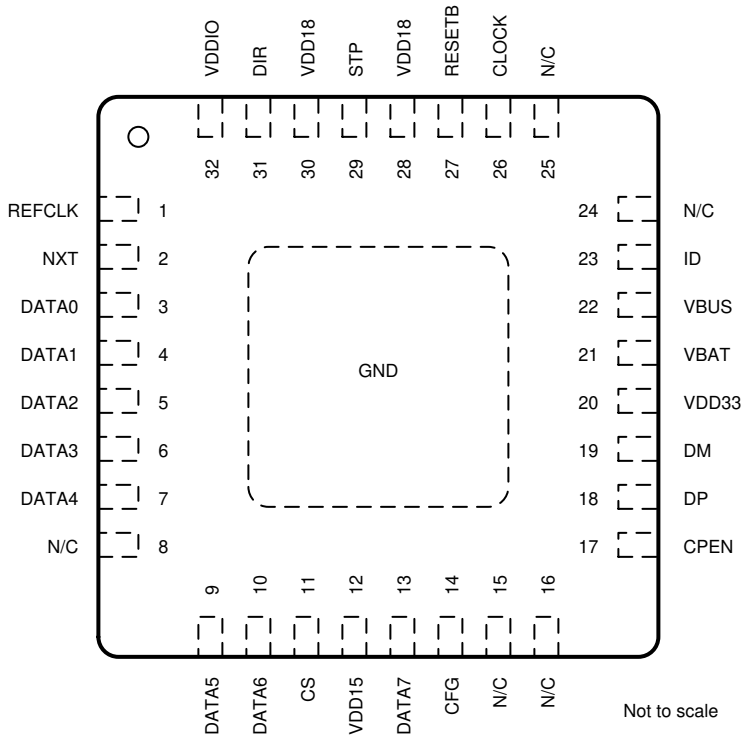



**图 5-1. RHB Package Top View**

**表 5-1. Pin Functions**

| PIN | | A/D | TYPE | LEVEL | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| CFG | 14 | D | I | $V_{DDIO}$ | REFCLK clock frequency configuration pin. Two frequencies are supported: 19.2 MHz when 0, or 26 MHz when 1. |
| CLOCK | 26 | D | O | $V_{DDIO}$ | ULPI 60 MHz clock on which ULPI data is synchronized.<br>Two modes are possible:<br>Input Mode: CLOCK defaults as an input.<br>Output Mode: When an input clock is detected on REFCLK pin (after 4 rising edges) then CLOCK will change to an output. |
| CPEN | 17 | D | O | $V_{DD33}$ | CMOS active-high digital output control of external 5 V VBUS supply |
| CS | 11 | D | I | $V_{DDIO}$ | Active-high chip select pin. When low the IC is in power down and ULPI bus is tri-stated. When high normal operation. Tie to $V_{DDIO}$ if unused. |
| DATA0 | 3 | D | I/O | $V_{DDIO}$ | ULPI DATA input or output signal 0 synchronized to CLOCK |
| DATA1 | 4 | D | I/O | $V_{DDIO}$ | ULPI DATA input or output signal 1 synchronized to CLOCK |
| DATA2 | 5 | D | I/O | $V_{DDIO}$ | ULPI DATA input or output signal 2 synchronized to CLOCK |
| DATA3 | 6 | D | I/O | $V_{DDIO}$ | ULPI DATA input or output signal 3 synchronized to CLOCK |
| DATA4 | 7 | D | I/O | $V_{DDIO}$ | ULPI DATA input or output signal 4 synchronized to CLOCK |
| DATA5 | 9 | D | I/O | $V_{DDIO}$ | ULPI DATA input or output signal 5 synchronized to CLOCK |
| DATA6 | 10 | D | I/O | $V_{DDIO}$ | ULPI DATA input or output signal 6 synchronized to CLOCK |
| DATA7 | 13 | D | I/O | $V_{DDIO}$ | ULPI DATA input or output signal 7 synchronized to CLOCK |
| DIR | 31 | D | O | $V_{DDIO}$ | ULPI DIR output signal |
| DM | 19 | A | I/O | $V_{DD33}$ | DM pin of the USB connector |
| DP | 18 | A | I/O | $V_{DD33}$ | DP pin of the USB connector |
| ID | 23 | A | I/O | $V_{DD33}$ | Identification (ID) pin of the USB connector |
| N/C | 8, 15,16, 24, 25 | — | — | — | No connection |

表 5-1. Pin Functions (continued)

| PIN | | A/D | TYPE | LEVEL | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| NXT | 2 | D | O | $V_{DDIO}$ | ULPI NXT output signal |
| REFCLK | 1 | A | I | 3.3 V | $V_{DD33}$ Reference clock input (square-wave only). Tie to GND when pin 26 (CLOCK) is required to be Input mode. Connect to square-wave reference clock of amplitude in the range of 3 V to 3.6 V when Pin 26 (CLOCK) is required to be Output mode. See pin 14 (CFG) description for REFCLK input frequency settings. |
| RESETB | 27 | D | I | $V_{DDIO}$ | When low, all digital logic (except 32 kHz logic required for power up sequencing) including registers are reset to their default values, and ULPI bus is tri-stated. When high, normal USB operation. |
| STP | 29 | D | I | $V_{DDIO}$ | ULPI STP input signal |
| $V_{BAT}$ | 21 | A | power | $V_{BAT}$ | Input supply voltage or battery source |
| $V_{BUS}$ | 22 | A | power | $V_{BUS}$ | $V_{BUS}$ pin of the USB connector |
| $V_{DD15}$ | 12 | A | power | | 1.5 V internal LDO output. Connect to external filtering capacitor. |
| $V_{DD18}$ | 28, 30 | A | power | $V_{DD18}$ | External 1.8 V supply input. Connect to external filtering capacitor. |
| $V_{DD33}$ | 20 | A | power | $V_{DD33}$ | 3.3 V internal LDO output. Connect to external filtering capacitor. |
| $V_{DDIO}$ | 32 | A | I | $V_{DDIO}$ | External 1.8 V supply input for digital I/Os. Connect to external filtering capacitor. |
| GND | Thermal Pad | A | power | — | Reference Ground |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Main battery supply voltage(2) | | 0 | 5 | V |
| | Voltage on any input(3) | Where supply represents the voltage applied to the power supply pin associated with the input | –0.3 | 1 × $V_{CC}$ +0.3 | V |
| | $V_{BUS}$ input | | –2 | 20 | V |
| | ID, DP, DM inputs | Stress condition guaranteed 24h | –0.3 | 5.25 | V |
| $V_{DDIO}$ | IO supply voltage | Continuous | | 1.98 | V |
| $T_A$ | Ambient temperature range | | –40 | 85 | °C |
| $T_J$ | Ambient temperature range | Absolute maximum rating | –40 | 150 | °C |
| | | For parametric compliance | –40 | 125 | |
| | Ambient temperature for parametric compliance | With max 125°C as junction temperature | –40 | 85 | °C |
| | DP, DM, ID high voltage short circuit | DP, DM or ID pins short circuited to $V_{BUS}$ supply, in any mode of TUSB1210 operation, continuously for 24 hours | | 5.25 | V |
| | DP, DM, ID low voltage short circuit | DP, DM or ID pins short circuited to GND in any mode of TUSB1210 operation, continuously for 24 hours | 0 | | V |
| $T_{stg}$ | Storage temperature range | | –55 | 125 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The product will have negligible reliability impact if voltage spikes of 5.5 V occur for a total (cumulative over lifetime) duration of 5 milliseconds.
(3) Except $V_{BAT}$ input, $V_{BUS}$, ID, DP, and DM pads

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge (ESD) performance: | Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1) | ±2000 | V |
| | | Charged device model (CDM), per JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | Battery supply voltage | | 2.7 | 3.6 | 4.8 | V |
| $V_{BAT\ CERT}$ | Battery supply voltage for USB 2.0 compliancy (USB 2.0 certification) | When $V_{DD33}$ is supplied internally | 3.15 | | | V |
| | | When $V_{DD33}$ is shorted to $V_{BAT}$ externally | 3.05 | | | |
| $V_{DDIO}$ | Digital IO pin supply | | 1.71 | | 1.98 | V |
| $T_A$ | Ambient temperature range | | –40 | | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | RHB (16 Pins) | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 34.72 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 37.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 10.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 10.5 | °C/W |
| $R_{\theta JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | 3.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Analog I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CPEN Output Pin** | | | | | | |
| $V_{OL}$ | CPEN low-level output voltage | $I_{OL}$ = 3 mA | | | 0.3 | V |
| $V_{OH}$ | CPEN high-level output voltage | $I_{OH}$ = – 3 mA | $V_{DD33}$ – 0.3 | | | V |

## 6.6 Digital I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CLOCK** | | | | | | |
| $V_{OL}$ | Low-level output voltage | Frequency = 60 MHz, Load = 10 pF | | | 0.45 | V |
| $V_{OH}$ | High-level output voltage | | $V_{DDIO}$ - 0.45 | | | V |
| **STP, DIR, NXT, DATA0 to DATA7** | | | | | | |
| $V_{OL}$ | Low-level output voltage | Frequency = 30 MHz, Load = 10 pF | | | 0.45 | V |
| $V_{OH}$ | High-level output voltage | | $V_{DDIO}$ - 0.45 | | | V |

## 6.7 Digital IO Pins (Non-ULPI)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CS, CFG, RESETB Input Pins** | | | | | | |
| $V_{IL}$ | Maximum low-level input voltage | | | | 0.35 x $V_{DDIO}$ | V |
| $V_{IH}$ | Minimum high-level input voltage | | 0.65 x $V_{DDIO}$ | | | V |
| **RESETB Input Pin Timing Spec** | | | | | | |
| $t_{w(POR)}$ | Internal power-on reset pulse width | | 0.2 | | | µs |
| $t_{w(RESET)}$ | External RESETB pulse width | Applied to external RESETB pin when CLOCK is toggling. | 8 | | | CLOCK cycles |

## 6.8 PHY Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **LS/FS Single-Ended Receivers** | | | | | | | |
| | USB single-ended receivers | | | | | | |
| $SK_{WVP\_VM}$ | Skew between VP and VM | | Driver outputs unloaded | –2 | 0 | 2 | ns |
| $V_{SE\_HYS}$ | Single-ended hysteresis | | | 50 | | | mV |
| $V_{IH}$ | High (driven) | | | 2 | | | V |
| $V_{IL}$ | Low | | | | | 0.8 | V |
| $V_{TH}$ | Switching threshold | | | 0.8 | | 2 | V |
| **LS/FS Differential Receiver** | | | | | | | |
| $V_{DI}$ | Differential input sensitivity | | Ref. USB2.0 | 200 | | | mV |
| $V_{CM}$ | Differential Common mode range | | Ref. USB2.0 | 0.8 | | 2.5 | V |
| **LS Transmitter** | | | | | | | |
| $V_{OL}$ | Low | | Ref. USB2.0 | 0 | | 300 | mV |
| $V_{OH}$ | High (driven) | | Ref. USB2.0 | 2.8 | | 3.6 | V |
| $V_{CRS}$ | Output signal crossover voltage | | Ref. USB2.0, covered by eye diagram | 1.3 | | 2 | V |
| $t_r$ | Rise time | | Ref. USB2.0, covered by eye diagram | 75 | | 300 | ns |
| $t_f$ | Fall time | | | 75 | | 300 | ns |
| $t_{FRFM}$ | Differential rise and fall time matching | | | 80% | | 125% | |
| $t_{FDRATE}$ | Low-speed data rate | | Ref. USB2.0, covered by eye diagram | 1.4775 | | 1.5225 | Mb/s |
| $t_{DJ1}$ | Source jitter total (including frequency tolerance) | To next transition | Ref. USB2.0, covered by eye diagram | –25 | | 25 | ns |
| $t_{DJ2}$ | | For paired transitions | | –10 | | 10 | |
| $t_{FEOPT}$ | Source SE0 interval of EOP | | Ref. USB2.0, covered by eye diagram | 1.25 | | 1.5 | µs |
| | Downstream eye diagram | | Ref. USB2.0, covered by eye diagram | | | | |
| $V_{CM}$ | Differential common mode range | | Ref. USB2.0 | 0.8 | | 2.5 | V |
| **FS Transmitter** | | | | | | | |
| $V_{OL}$ | Low | | Ref. USB2.0 | 0 | | 300 | mV |
| $V_{OH}$ | High (driven) | | Ref. USB2.0 | 2.8 | | 3.6 | V |
| VCRS | Output signal crossover voltage | | Ref. USB2.0, covered by eye diagram | 1.3 | | 2 | V |
| $t_{FR}$ | Rise time | | Ref. USB2.0 | 4 | | 20 | ns |
| $t_{FF}$ | Fall time | | Ref. USB2.0 | 4 | | 20 | ns |
| $t_{FRFM}$ | Differential rise and fall time matching | | Ref. USB2.0, covered by eye diagram | 90% | | 111.11% | |
| $Z_{DRV}$ | Driver output resistance | | Ref. USB2.0 | 28 | | 44 | Ω |
| TFDRATE | Full-speed data rate | | Ref. USB2.0, covered by eye diagram | 11.97 | | 12.03 | Mb/s |
| $t_{DJ1}$ | Source jitter total (including frequency tolerance) | To next transition | Ref. USB2.0, covered by eye diagram | –2 | | 2 | ns |
| $t_{DJ2}$ | | For paired transitions | | –1 | | 1 | |
| TFEOPT | Source SE0 interval of EOP | | Ref. USB2.0, covered by eye diagram | 160 | | 175 | ns |
| | Downstream eye diagram | | Ref. USB2.0, covered by eye diagram | | | | |
| | Upstream eye diagram | | | | | | |

## 6.8 PHY Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **HS Differential Receiver** | | | | | | |
| VHSSQ | High-speed squelch detection threshold (differential signal amplitude) | Ref. USB2.0 | 100 | | 150 | mV |
| VHSDSC | High-speed disconnect detection threshold (differential signal amplitude) | Ref. USB2.0 | 525 | | 625 | mV |
| | High-speed differential input signaling levels | Ref. USB2.0, specified by eye pattern templates | | | | mV |
| VHSCM | High-speed data signaling common mode voltage range (guidelines for receiver) | Ref. USB2.0 | –50 | | 500 | mV |
| | Receiver jitter tolerance | Ref. USB2.0, specified by eye pattern templates | | | 150 | ps |
| **HS Transmitter** | | | | | | |
| $V_{HSOI}$ | High-speed idle level | Ref. USB2.0 | –10 | | 10 | mV |
| $V_{HSOH}$ | High-speed data signaling high | Ref. USB2.0 | 360 | | 440 | mV |
| $V_{HSOL}$ | High-speed data signaling low | Ref. USB2.0 | –10 | | 10 | mV |
| VCHIRPJ | Chirp J level (differential voltage) | Ref. USB2.0 | 700 | | 1100 | mV |
| VCHIRPK | Chirp K level (differential voltage) | Ref. USB2.0 | -900 | | -500 | mV |
| $t_r$ | Rise Time (10% - 90%) | Ref. USB2.0, covered by eye diagram | 500 | | | ps |
| $t_f$ | Fall time (10% - 90%) | Ref. USB2.0, covered by eye diagram | 500 | | | ps |
| ZHSDRV | Driver output resistance (which also serves as high-speed termination) | Ref. USB2.0 | 40.5 | | 49.5 | Ω |
| THSDRAT | High-speed data range | Ref. USB2.0, covered by eye diagram | 479.76 | | 480.24 | Mb/s |
| | Data source jitter | Ref. USB2.0, covered by eye diagram | | | | |
| | Downstream eye diagram | Ref. USB2.0, covered by eye diagram | | | | |
| | Upstream eye diagram | Ref. USB2.0, covered by eye diagram | | | | |
| **CEA-2011/UART Transceiver** | | | | | | |
| | UART Transmitter CEA-2011 | | | | | |
| $t_{PH\_UART\_EDGE}$ | Phone UART edge rates | DP_PULLDOWN asserted | | | 1 | μs |
| $V_{OH\_SER}$ | Serial interface output high | ISOURCE = 4 mA | 2.4 | 3.3 | 3.6 | V |
| $V_{OL\_SER}$ | Serial interface output low | ISINK = –4 mA | 0 | 0.1 | 0.4 | V |
| | UART Receiver CEA-2011 | | | | | |
| $VI_{H\_SER}$ | Serial interface input high | DP_PULLDOWN asserted | 2 | | | V |
| $V_{IL\_SER}$ | Serial interface input low | DP_PULLDOWN asserted | | | 0.8 | V |
| $V_{TH}$ | Switching threshold | | 0.8 | | 2 | V |

## 6.9 Pullup/Pulldown Resistors

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| RPUI | Bus pullup resistor on upstream port (idle bus) | Bus idle | 0.9 | 1.1 | 1.575 | kΩ |
| RPUA | Bus pullup resistor on upstream port (receiving) | Bus driven/driver's outputs unloaded | 1.425 | 2.2 | 3.09 | |
| VIHZ | High (floating) | Pullups/pulldowns on both DP and DM lines | 2.7 | | 3.6 | V |
| VPH_DP_UP | Phone D+ pullup voltage | Driver's outputs unloaded | 3 | 3.3 | 3.6 | V |
| | Pulldown resistors | | | | | |
| RPH_DP_DWN | Phone D+/– pulldown | Driver's outputs unloaded | 14.25 | 18 | 24.8 | kΩ |
| RPH_DM_DWN | | | | | | |
| $V_{IHZ}$ | High (floating) | Pullups/pulldowns on both DP and DM lines | 2.7 | | 3.6 | V |
| | D+/– Data line | | | | | |
| $C_{INUB}$ | Upstream facing port | [1.0] | | 22 | 75 | pF |
| $V_{OTG\_DATA\_LKG}$ | On-the-go device leakage | [2] | | | 0.342 | V |
| $Z_{INP}$ | Input impedance exclusive of pullup/ pulldown | Driver's outputs unloaded | 300 | | | kΩ |

## 6.10 OTG Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | COMMENTS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| OTG $V_{BUS}$ Electrical | | | | | | | |
| **$V_{BUS}$ Comparators** | | | | | | | |
| VA_SESS_VLD | A-device session valid | | | 0.8 | 1.4 | 2.0 | V |
| VA_VBUS_VLD | A-device $V_{BUS}$ valid | | | 4.4 | 4.5 | 4.625 | V |
| VB_SESS_END | B-device session end | | | 0.2 | 0.5 | 0.8 | V |
| VB_SESS_VLD | B-device session valid | | | 2.1 | 2.4 | 2.7 | V |
| **$V_{BUS}$ Line** | | | | | | | |
| RA_BUS_IN | A-device $V_{BUS}$ input impedance to ground | SRP ($V_{BUS}$ pulsing) capable A-device not driving $V_{BUS}$ | | 40 | 70 | 100 | kΩ |
| RB_SRP_DWN | B-device $V_{BUS}$ SRP pulldown | 5.25 V / 8 mA, Pullup voltage = 3 V | | 0.656 | 10 | | kΩ |
| RB_SRP_UP | B-device $V_{BUS}$ SRP pullup | (5.25 V – 3 V) / 8 mA, Pullup voltage = 3 V | | 0.281 | 1 | 2 | kΩ |
| $t_{RISE\_SRP\_UP\_MAX}$ | B-device $V_{BUS}$ SRP rise time maximum for OTG-A communication | 0 to 2.1 V with < 13 µF load | $RV_{BUS}$ = 0 Ω and R1KSERIES = '0' | | | 31.4 | ms |
| | | | $RV_{BUS}$ = 1000 Ω ±10% and R1KSERIES = '1' | | | 57.8 | |
| | | | $RV_{BUS}$ = 1200 Ω ±10% and R1KSERIES = '1' | | | 64 | |
| | | | $RV_{BUS}$ = 1800 Ω ±10% and R1KSERIES = '1' | | | 85.4 | |

## 6.10 OTG Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | COMMENTS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{RISE\_SRP\_UP\_MIN}$ | B-device $V_{BUS}$ SRP rise time minimum for standard host connection | 0.8 to 2 V with > 97 µF load | $RV_{BUS}$ = 0 Ω and R1KSERIES = '0' | 46.2 | | | ms |
| | | | $RV_{BUS}$ = 1000 Ω ±10% and R1KSERIES = '1' | 96 | | | |
| | | | $RV_{BUS}$ = 1200 Ω ±10% and R1KSERIES = '1' | 100 | | | |
| | | | $RV_{BUS}$ = 1800 Ω ±10% and R1KSERIES = '1' | 100 | | | |

## 6.11 OTG ID Electrical

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ID Comparators — ID External Resistors Specifications** | | | | | | |
| $R_{ID\_GND}$ | ID ground comparator | ID_GND interrupt | 12 | 20 | 28 | kΩ |
| $R_{ID\_FLOAT}$ | ID Float comparator | ID_FLOAT interrupt | 200 | | 500 | kΩ |
| | ID Line | | | | | |
| $R_{PH\_ID\_UP}$ | Phone ID pullup to VPH_ID_UP | ID unloaded ($V_{RUSB}$) | 70 | 90 | 286 | kΩ |
| $VP_{H\_ID\_UP}$ | Phone ID pullup voltage | Connected to $V_{RUSB}$ | 2.5 | | 3.2 | V |
| | ID line maximum voltage | | | | 5.25 | V |

## 6.12 Power Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **$V_{DD33}$ Internal LDO Regulator Characteristics** | | | | | | | |
| $V_{INVDD33}$ | Input voltage | $V_{BAT}$ USB | | $V_{VDD33}$ typ + 0.2 | 3.6 | 4.5 | V |
| $V_{VDD33}$ | Output voltage | ON mode, | VUSB3V3_VSEL = '000 | 2.4 | 2.5 | 2.6 | V |
| | | | VUSB3V3_VSEL = '001 | 2.65 | 2.75 | 2.85 | |
| | | | VUSB3V3_VSEL = '010 | 2.9 | 3.0 | 3.1 | |
| | | | VUSB3V3_VSEL = '011 (default) | 3.0 | 3.1 | 3.2 | |
| | | | VUSB3V3_VSEL = '100 | 3.1 | 3.2 | 3.3 | |
| | | | VUSB3V3_VSEL = '101 | 3.2 | 3.3 | 3.4 | |
| | | | VUSB3V3_VSEL = '110 | 3.3 | 3.4 | 3.5 | |
| | | | VUSB3V3_VSEL = '111 | 3.4 | 3.5 | 3.6 | |
| $I_{VDD33}$ | Rated output current | $V_{BAT}$ USB | Active mode | | | 15 | mA |
| | | | Suspend/reset mode | | | 1 | |
| **$V_{DD15}$ Internal LDO Regulator Characteristics** | | | | | | | |
| $V_{IN\ VDD15}$ | Input voltage | | On mode, $V_{IN\ VDD15}$ = $V_{BAT}$ | 2.7 | 3.6 | 4.5 | V |
| $V_{VDD15}$ | Output voltage | | $V_{INVDD15\ min}$ – $V_{INVDD15\ max}$ | 1.45 | 1.56 | 1.65 | V |
| $I_{VDD15}$ | Rated output current | | On mode | | | 30 | mA |

## 6.13 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Electrical Characteristics: Clock Input** | | | | | | |
| | Clock input duty cycle | | 40 | | 60% | |
| $f_{CLK}$ | Clock nominal frequency | | | 60 | | MHz |
| | Clock input rise/fall time | In % of clock period $t_{CLK}$ ( = 1/$f_{CLK}$ ) | | | 10% | |
| | Clock input frequency accuracy | | | | 250 | ppm |
| | Clock input integrated jitter | | | | 600 | ps rms |
| **Electrical Characteristics: REFCLK** | | | | | | |
| | REFCLK input duty cycle | | 40 | | 60% | |
| $f_{REFCLK}$ | REFCLK nominal frequency | When CFG pin is tied to GND | | 19.2 | | MHz |
| | | When CFG pin is tied to $V_{DDIO}$ | | 26 | | |
| | REFCLK input rise/fall time | In % of clock period $t_{REFCLK}$ ( = 1/ $f_{REFCLK}$ ) | | | 20% | |
| | REFCLK input frequency accuracy | | | | 250 | ppm |
| | REFCLK input integrated jitter | | | | 600 | ps rms |
| | REFCLK HIZ Leakage current | | | | 3 | µA |
| | REFCLK HIZ Leakage current | | –3 | | | |
| **Digital IO Electrical Characteristics: CLOCK** | | | | | | |
| $t_r$ | Rise time | Frequency = 60 MHz, Load = 10 pF | | | 1 | ns |
| $t_f$ | Fall time | Frequency = 30 MHz, Load = 10 pF | | | 1 | ns |
| **Digital IO Electrical Characteristics: STP, DIR, NXT, DATA0 to DATA7** | | | | | | |
| $t_r$ | Rise time | Frequency = 30 MHz, Load = 10 pF | | | 1 | ns |
| $t_f$ | Fall time | | | | 1 | ns |

## 6.14 Timing Requirements

| PARAMETER | | INPUT CLOCK | | OUTPUT CLOCK | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| **ULPI Interface Timing** | | | | | | |
| $t_{SC}$, $t_{SD}$ | Set-up time (control in, 8-bit data in) | 3 | | 6 | | ns |
| $t_{SC}$, $t_{HD}$ | Hold time (control in, 8-bit data in) | 1.5 | | 0 | | ns |
| $t_{DC}$, $t_{DD}$ | Output delay (control out, 8-bit data out) | | 6 | 1.2 | 5 | ns |
| **USB UART Interface Timing** | | | | | | |
| $t_{PH\_DP\_CON}$ | Phone D+ connect time | 100 | | | | ms |
| $t_{PH\_DISC\_DET}$ | Phone D+ disconnect time | 150 | | | | ms |
| $f_{UART\_DFLT}$ | Default UART signaling rate (typical rate) | | 9600 | | | bps |

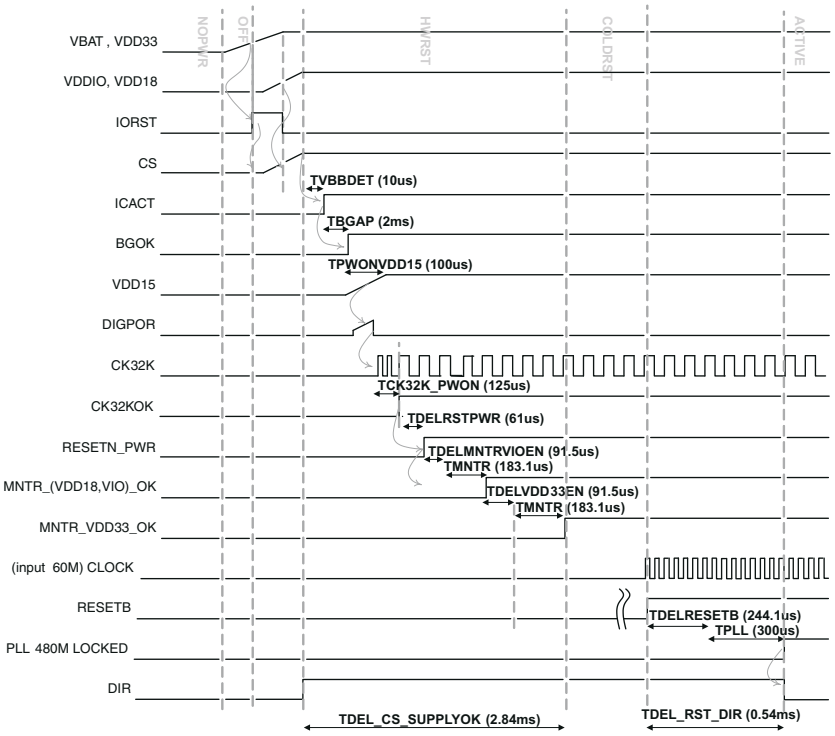



**图 6-1. TUSB1210 Power-Up Timing (ULPI Clock Input Mode)**

**表 6-1. Timers and Debounce**

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{DEL\_CS\_SUPPLYOK}$ | Chip-select-to-supplies OK delay | | | 2.84 | 4.10 | ms |
| $t_{DEL\_RST\_DIR}$ | RESETB to PHY PLL locked and DIR falling-edge delay | | | 0.54 | 0.647 | ms |
| $t_{VBBDET}$ | $V_{BAT}$ detection delay | | | 10 | | µs |
| $t_{BGAP}$ | Bandgap power-on delay | | | 2 | | ms |
| $t_{PWONVDD15}$ | $V_{DD15}$ power-on delay | | | 100 | | µs |
| $t_{PWONCK32K}$ | 32-KHz RC-OSC power-on delay | | | 125 | | µs |
| $t_{DELRSTPWR}$ | Power control reset delay | | | 61 | | µs |
| $t_{DELMNTRVIOEN}$ | Monitor enable delay | | | 91.5 | | µs |
| $t_{MNTR}$ | Supply monitoring debounce | | | 183.1 | | µs |
| $t_{DELVDD33EN}$ | $V_{DD33}$ LDO enable delay | | | 93.75 | | µs |
| $t_{DELRESETB}$ | RESETB internal delay | | | 244.1 | | µs |
| $t_{PLL}$ | PLL lock time | | | 300 | | µs |

### 6.14.1 Timing Parameter Definitions

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated as shown in 表 6-2.

**表 6-2. Timing Parameter Definitions**

| LOWERCASE SUBSCRIPTS | |
|---|---|
| **SYMBOL** | **PARAMETER** |
| C | Cycle time (period) |
| D | Delay time |
| Dis | Disable time |
| En | Enable time |
| H | Hold time |
| Su | Setup time |
| START | Start bit |
| T | Transition time |
| V | Valid time |
| W | Pulse duration (width) |
| X | Unknown, changing, or don't care level |
| H | High |
| L | Low |
| V | Valid |
| IV | Invalid |
| AE | Active edge |
| FE | First edge |
| LE | Last edge |
| Z | High impedance |

### 6.14.2 Interface Target Frequencies

表 6-3 assumes testing over the recommended operating conditions.

**表 6-3. TUSB1210 Interface Target Frequencies**

| IO INTERFACE | INTERFACE DESIGNATION | | TARGET FREQUENCY 1.5 V |
|---|---|---|---|
| USB | Universal serial bus | High speed | 480 Mbits/s |
| | | Full speed | 12 Mbits/s |
| | | Low speed | 1.5 Mbits/s |

## 6.15 Typical Characteristics

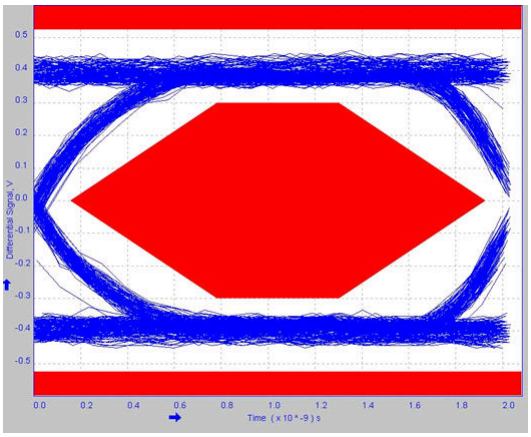



图 6-2. High-Speed Eye Diagram

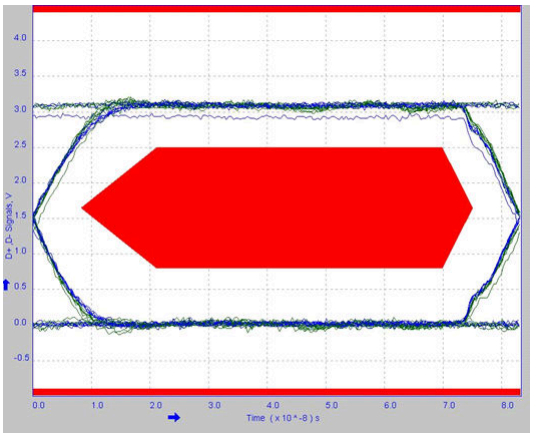



图 6-3. Full-Speed Eye Diagram

# 7 Detailed Description

## 7.1 Overview

The TUSB1210 is a USB2.0 transceiver chip, designed to interface with a USB controller through a ULPI interface. It supports all USB2.0 data rates High-Speed, Full-Speed, and Low-Speed. Compliant to Host and Peripheral (OTG) modes. It additionally supports a UART mode and legacy ULPI serial modes. TUSB1210 Integrates a 3.3-V LDO, which makes it flexible to work with either battery operated systems or pure 3.3 V supplied systems. Also, it has an integrated PLL Supporting 2 Clock Frequencies 19.2 MHz/26 MHz. The ULPI clock pin (60 MHz) supports input and output clock configurations. TUSB1210 has low power consumption, optimized for portable devices, and complete USB OTG Physical Front-End that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).

TUSB1210 is optimized to be interfaced through a 12-pin SDR UTMI Low Pin Interface (ULPI), supporting both input clock and output clock modes, with 1.8 V interface supply voltage.

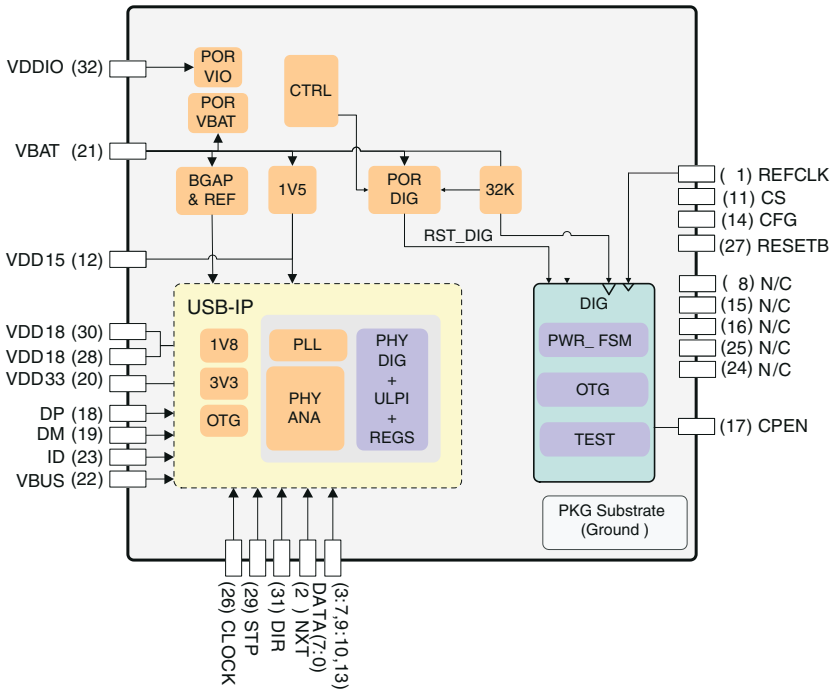
TUSB1210 integrates a 3.3 V LDO, which makes it flexible to work with either battery operated systems or pure 3.3 V supplied systems. Both the main supply and the 3.3 V power domain can be supplied through an external switched-mode converter for optimized power efficiency.

TUSB1210 includes a POR circuit to detect supply presence on $V_{BAT}$ and $V_{DDIO}$ pins. TUSB1210 can be disabled or configured in low power mode for energy saving.

TUSB1210 is protected against accidental shorts to 5 V or ground on its exposed interface (DP/DM/ID). It is also protected against up to 20 V surges on $V_{BUS}$.

TUSB1210 integrates a high-performance low-jitter 480 MHz PLL and supports two clock configurations. Depending on the required link configuration, TUSB1210 supports both ULPI input and output clock mode: input clock mode, in which case a square-wave 60 MHz clock is provided to TUSB1210-Q1 at the ULPI interface CLOCK pin; and output clock mode in which case TUSB1210 can accept a square-wave reference clock at REFCLK of either 19.2 MHz, 26 MHz. Frequency is indicated to TUSB1210 via the configuration pin CFG. This can be useful if a reference clock is already available in the system.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Processor Subsystem

#### *7.3.1.1 Clock Specifications*

##### 7.3.1.1.1 USB PLL Reference Clock

The USB PLL block generates the clocks used to synchronize:

- The ULPI interface (60 MHz clock)
- The USB interface (depending on the USB data rate, 480 Mbps, 12 Mbps, or 1.5 Mbps)

TUSB1210 requires an external reference clock which is used as an input to the 480 MHz USB PLL block. Depending on the clock configuration, this reference clock can be provided either at REFCLK pin or at CLOCK pin. By default CLK pin is configured as an input.

Two clock configurations are possible:

- Input clock configuration (see 节 7.3.1.1.2)
- Output clock configuration (see 节 7.3.1.1.3)

##### 7.3.1.1.2 ULPI Input Clock Configuration

In this mode, REFCLK must be externally tied to GND. CLOCK remains configured as an input.

When the ULPI interface is used in input clock configuration, that is, the 60 MHz ULPI clock is provided to TUSB1210 on Clock pin, then this is used as the reference clock for the 480 MHz USB PLL block. See *节 6.13*.

##### 7.3.1.1.3 ULPI Output Clock Configuration

In this mode, a reference clock must be externally provided on the REFCLK pin. When an input clock is detected on the REFCLK pin, then CLK is automatically changed to an output. For example, 60 MHz ULPI clock is the TUSB1210 devices output on the CLK pin.

Two reference clock input frequencies are supported. REFCLK input frequency is communicated to TUSB1210 through a configuration pin, CFG. See $f_{REFCLK}$ in 表 8-3 for frequency correspondence. TUSB1210 supports square-wave reference clock input only. Reference clock input must be square-wave of amplitude in the range 3 V to 3.6 V. See *节 6.13*.

##### 7.3.1.1.4 Clock 32 kHz

An internal clock generator running at 32 kHz has been implemented to provide a low-speed, low-power clock to the system See *节 7.3.1.1.4*.

##### 7.3.1.1.5 Reset

All logic is reset if CS = 0 or $V_{BAT}$ are not present.

All logic (except 32 kHz logic) is reset if $V_{DDIO}$ is not present.

PHY logic is reset when any supplies are not present ($V_{DDIO}$, $V_{DD15}$, $V_{DD18}$, and $V_{DD33}$) or if RESETB pin is low.

TUSB1210 may be reset manually by toggling the RESETB pin to GND for at least 200 ns.

If manual reset through RESETB is not required, then RESETB pin may be tied to $V_{DDIO}$ permanently.

#### *7.3.1.2 USB Transceiver*

The TUSB1210 device includes a universal serial bus (USB) on-the-go (OTG) transceiver that supports USB 480 Mb/s high-speed (HS), 12 Mb/s full-speed (FS), and USB 1.5 Mb/s low-speed (LS) through a 12-pin UTMI+ low pin interface (ULPI).

**Note**

LS device mode is not allowed by a USB2.0 HS capable PHY, therefore it is not supported by TUSB1210. This is stated in USB2.0 standard Chapter 7, page 119, second paragraph: *"A high-speed capable upstream facing transceiver must not support low-speed signaling mode.."* There is also some related commentary in Chapter 7.1.2.3.

#### 7.3.1.2.1 PHY Electrical Characteristics

The PHY is the physical signaling layer of the USB 2.0. It essentially contains all the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through a standard 12-pin digital interface called UTMI+ low pin interface (ULPI).

The transmitters and receivers inside the PHY are classified into two main classes.

- The full-speed (FS) and low-speed (LS) transceivers. These are the legacy USB1.x transceivers.
- The HS (HS) transceivers

To bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A DPLL which does a frequency multiplication to achieve the 480-MHz low-jitter lock necessary for USB and also the clock required for the switched capacitor resistance block.
- A switched capacitor resistance block which is used to replicate an external resistor on chip.

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry which protects it from accidental 5-V short on the DP and DM lines.

##### *7.3.1.2.1.1 LS/FS Single-Ended Receivers*

In addition to the differential receiver, there is a single-ended receiver (SE－, SE+) for each of the two data lines D+/－. The main purpose of the single-ended receivers is to qualify the D+ and D－ signals in the full-speed/low-speed modes of operation. See 节 6.8.

##### *7.3.1.2.1.2 LS/FS Differential Receiver*

A differential input receiver (Rx) retrieves the LS/FS differential data signaling. The differential voltage on the line is converted into digital data by a differential comparator on DP/DM. This data is then sent to a clock and data recovery circuit which recovers the clock from the data. An additional serial mode exists in which the differential data is directly output on the RXRCV pin. See 节 6.13.

##### *7.3.1.2.1.3 LS/FS Transmitter*

The USB transceiver (Tx) uses a differential output driver to drive the USB data signal D+/－ onto the USB cable. The driver's outputs support 3-state operation to achieve bidirectional half-duplex transactions. See 节 6.13.

##### *7.3.1.2.1.4 HS Differential Receiver*

The HS receiver consists of the following blocks:

A differential input comparator to receive the serial data

- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a NRZI decoder, bit unstuffing, and serial-to-parallel converter to generate the ULPI DATAOUT

  See 节 6.13.

#### *7.3.1.2.1.5 HS Differential Transmitter*

The HS transmitter is always operated via the ULPI parallel interface. The parallel data on the interface is serialized, bit stuffed, NRZI encoded, and transmitted as a dc output current on DP or DM depending on the data. Each line has an effective 22.5 Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double thereby doubling the differential amplitude seen on the DP/DM lines of 节 *6.13*.

#### *7.3.1.2.1.6 UART Transceiver*

In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver. See 节 *6.13*.

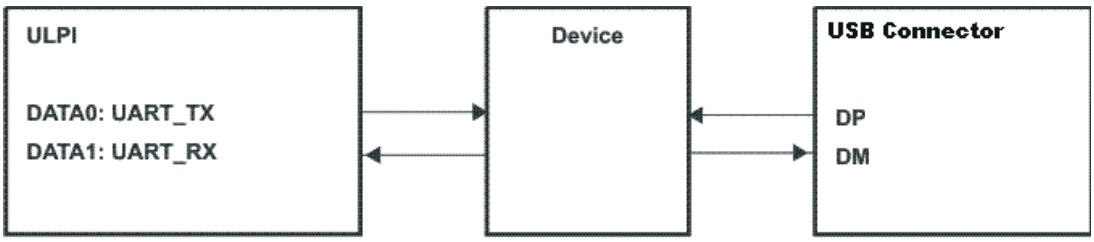



**图 7-1. USB UART Data Flow**

#### 7.3.1.2.2 OTG Characteristics

The on-the-go (OTG) block integrates three main functions:

- The USB plug detection function on $V_{BUS}$ and ID
- The ID resistor detection
- The $V_{BUS}$ level detection

See 节 *6.10*.

## 7.4 Device Functional Modes

### 7.4.1 TUSB1210 Modes vs ULPI Pin Status

表 7-1, 表 7-2, and 表 7-3 show the status of each of the 12 ULPI pins including input or output direction and whether output pins are driven to ‘0’ or to ‘1’, or pulled up or pulled down through the internal pullup or pulldown resistors.

Note that pullup or pulldown resistors are automatically replaced by driven ‘1’/’0’ levels respectively once internal IORST is released, with the exception of the pullup on STP which is maintained in all modes.

Pin assignment changes in ULPI 3-pin serial mode, ULPI 6-pin serial mode, and UART mode. Unused pins are tied low in these modes as shown below.

**表 7-1. TUSB1210 Modes vs ULPI Pin Status:ULPI Synchronous Mode Power-Up**

| | | ULPI SYNCHRONOUS MODE POWER-UP | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | UNTIL IORST RELEASE | | PLL OFF | | PLL ON + STP HIGH | | PLL ON + STP LOW | |
| PIN NO. | PIN NAME | DIR | PU/PD | DIR | PU/PD | DIR | PU/PD | DIR | PU/PD |
| 26 | CLOCK | Hiz | PD | I | PD | IO | — | IO | — |
| 31 | DIR | Hiz | PU | O, ( ‘1’ ) | — | O, ( ‘0’ ) | — | O | — |
| 2 | NXT | Hiz | PD | O, ( ‘0’ ) | — | O, ( ‘0’ ) | — | O | — |
| 29 | STP | Hiz | PU | I | PU | I | PU | I | PU |
| 3 | DATA0 | Hiz | PD | O, ( ‘0’ ) | — | I | PD | IO | — |
| 4 | DATA1 | Hiz | PD | O, ( ‘0’ ) | — | I | PD | IO | — |
| 5 | DATA2 | Hiz | PD | O, ( ‘0’ ) | — | I | PD | IO | — |
| 6 | DATA3 | Hiz | PD | O, ( ‘0’ ) | — | I | PD | IO | — |
| 7 | DATA4 | Hiz | PD | O, ( ‘0’ ) | — | I | PD | IO | — |
| 9 | DATA5 | Hiz | PD | O, ( ‘0’ ) | — | I | PD | IO | — |
| 10 | DATA6 | Hiz | PD | O, ( ‘0’ ) | — | I | PD | IO | — |
| 13 | DATA7 | Hiz | PD | O, ( ‘0’ ) | — | I | PD | IO | — |

**表 7-2. TUSB1210 Modes vs ULPI Pin Status: USB Suspend Mode**

| | | SUSPEND MODE | | LINK / EXTERNAL RECOMMENDED SETTING DURING SUSPEND MODE | |
|---|---|---|---|---|---|
| PIN NO. | PIN NAME | DIR | PU/PD | DIR | PU/PD |
| 26 | CLOCK | I | — | O | — |
| 31 | DIR | O, ( ‘1’ ) | — | I | — |
| 2 | NXT | O, ( ‘0’ ) | — | I | — |
| 29 | STP | I | PU(1) | O, ( ‘0’ ) | — |
| 3 | DATA0 | O, (LINESTATE0) | — | I | — |
| 4 | DATA1 | O, (LINESTATE1) | — | I | — |
| 5 | DATA2 | O, ( ‘0’ ) | — | I | — |
| 6 | DATA3 | O, (INT) | — | I | — |
| 7 | DATA4 | O, ( ‘0’ ) | — | I | — |
| 9 | DATA5 | O, ( ‘0’ ) | — | I | — |
| 10 | DATA6 | O, ( ‘0’ ) | — | I | — |
| 13 | DATA7 | O, ( ‘0’ ) | — | I | — |

(1) Can be disabled by software before entering Suspend Mode to reduce current consumption

**表 7-3. TUSB1210 Modes vs ULPI Pin Status: ULPI 6-Pin Serial Mode and UART Mode**

| | ULPI 6-PIN SERIAL MODE | | | ULPI 3-PIN SERIAL MODE | | | UART MODE | | |
|---|---|---|---|---|---|---|---|---|---|
| PIN NO. | PIN NAME | DIR | PU/PD | PIN NAME | DIR | PU/PD | PIN NAME | DIR | PU/PD |
| 26 | CLOCK (1) | IO | — | CLOCK (1) | IO | — | CLOCK (1) | IO | — |
| 31 | DIR | O | — | DIR | O | — | DIR | O | — |
| 2 | NXT | O | — | NXT | O | — | NXT | O | — |
| 29 | STP | I | PU | STP | I | PU | STP | I | PU |
| 3 | TX_ENABLE | I | — | TX_ENABLE | I | — | TXD | I | — |
| 4 | TX_DAT | I | — | DAT | IO | — | RXD | IO | — |
| 5 | TX_SE0 | I | — | SE0 | IO | — | tie low | O | — |
| 6 | INT | O | — | INT | O | — | INT | O | — |
| 7 | RX_DP | O | — | tie low | O | — | tie low | O | — |
| 9 | RX_DM | O | — | tie low | O | — | tie low | O | — |
| 10 | RX_RCV | O | — | tie low | O | — | tie low | O | — |
| 13 | tie low | O | — | tie low | O | — | tie low | O | — |

## 7.5 Register Map

表 7-4. USB Register Summary

| REGISTER NAME | TYPE | REGISTER WIDTH (BITS) | PHYSICAL ADDRESS |
|---|---|---|---|
| VENDOR_ID_LO | R | 8 | 0x00 |
| VENDOR_ID_HI | R | 8 | 0x01 |
| PRODUCT_ID_LO | R | 8 | 0x02 |
| PRODUCT_ID_HI | R | 8 | 0x03 |
| FUNC_CTRL | RW | 8 | 0x04 |
| FUNC_CTRL_SET | RW | 8 | 0x05 |
| FUNC_CTRL_CLR | RW | 8 | 0x06 |
| IFC_CTRL | RW | 8 | 0x07 |
| IFC_CTRL_SET | RW | 8 | 0x08 |
| IFC_CTRL_CLR | RW | 8 | 0x09 |
| OTG_CTRL | RW | 8 | 0x0A |
| OTG_CTRL_SET | RW | 8 | 0x0B |
| OTG_CTRL_CLR | RW | 8 | 0x0C |
| USB_INT_EN_RISE | RW | 8 | 0x0D |
| USB_INT_EN_RISE_SET | RW | 8 | 0x0E |
| USB_INT_EN_RISE_CLR | RW | 8 | 0x0F |
| USB_INT_EN_FALL | RW | 8 | 0x10 |
| USB_INT_EN_FALL_SET | RW | 8 | 0x11 |
| USB_INT_EN_FALL_CLR | RW | 8 | 0x12 |
| USB_INT_STS | R | 8 | 0x13 |
| USB_INT_LATCH | R | 8 | 0x14 |
| DEBUG | R | 8 | 0x15 |
| SCRATCH_REG | RW | 8 | 0x16 |
| SCRATCH_REG_SET | RW | 8 | 0x17 |
| SCRATCH_REG_CLR | RW | 8 | 0x18 |
| Reserved | R | 8 | 0x19 0x2E |
| ACCESS_EXT_REG_SET | RW | 8 | 0x2F |
| Reserved | R | 8 | 0x30 0x3C |
| VENDOR_SPECIFIC1 | RW | 8 | 0x3D |
| VENDOR_SPECIFIC1_SET | RW | 8 | 0x3E |
| VENDOR_SPECIFIC1_CLR | RW | 8 | 0x3F |
| VENDOR_SPECIFIC2 | RW | 8 | 0x80 |
| VENDOR_SPECIFIC2_SET | RW | 8 | 0x81 |
| VENDOR_SPECIFIC2_CLR | RW | 8 | 0x82 |
| VENDOR_SPECIFIC1_STS | R | 8 | 0x83 |
| VENDOR_SPECIFIC1_LATCH | R | 8 | 0x84 |
| VENDOR_SPECIFIC3 | RW | 8 | 0x85 |
| VENDOR_SPECIFIC3_SET | RW | 8 | 0x86 |
| VENDOR_SPECIFIC3_CLR | RW | 8 | 0x87 |

### 7.5.1 VENDOR_ID_LO

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x00 | | |
| **PHYSICAL ADDRESS** | 0x00 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Lower byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451) | | |
| **TYPE** | R | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VENDOR_ID | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7:00 | VENDOR_ID | | R | 0x51 |

### 7.5.2 VENDOR_ID_HI

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x01 | | |
| **PHYSICAL ADDRESS** | 0x01 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Upper byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451) | | |
| **TYPE** | R | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VENDOR_ID | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7:00 | VEN DOR_ID | | R | 0x04 |

### 7.5.3 PRODUCT_ID_LO

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x02 | | |
| **PHYSICAL ADDRESS** | 0x02 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Lower byte of Product ID supplied by Vendor (TUSB1210 Product ID is 0x1507). | | |
| **TYPE** | R | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PRODUCT_ID | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7:00 | PRODUCT_ID | R | 0x07 | |

### 7.5.4 PRODUCT_ID_HI

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x03 | | |
| **PHYSICAL ADDRESS** | 0x03 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Upper byte of Product ID supplied by Vendor (TUSB1210 Product ID is 0x1507). | | |
| **TYPE** | R | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PRODUCT_ID | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7:00 | PRODUCT_ID | R | 0x15 | |

### 7.5.5 FUNC_CTRL

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x04 | | |
| **PHYSICAL ADDRESS** | 0x04 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Controls UTMI function settings of the PHY. | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SUSPENDM | RESET | OPMODE | | TERMSELECT | XCVRSELECT | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | SUSPENDM | Active low PHY suspend. Put PHY into Low Power Mode. In Low Power Mode the PHY power down all blocks except the full speed receiver, OTG comparators, and the ULPI interface pins. The PHY automatically set this bit to '1' when Low Power Mode is exited. | RW | 1 |
| 5 | RESET | Active high transceiver reset. Does not reset the ULPI interface or ULPI register set.<br>Once set, the PHY asserts the DIR signal and reset the UTMI core. When the reset is completed, the PHY de-asserts DIR and clears this bit. After de-asserting DIR, the PHY re-assert DIR and send an RX command update.<br>Note: This bit is auto-cleared, this explain why it can't be read at '1'. | RW | 0 |
| 4:03 | OPMODE | Select the required bit encoding style during transmit<br>0x0: Normal operation<br>0x1: Non-driving<br>0x2: Disable bit-stuff and NRZI encoding<br>0x3: Reserved (No SYNC and EOP generation feature not supported) | RW | 0x0 |
| 2 | TERMSELECT | Controls the internal 1.5KΩs pull-up resistor and 45Ωs HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. | RW | 0 |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 1:00 | XCVRSELECT | Select the required transceiver speed.<br>0x0: Enable HS transceiver<br>0x1: Enable FS transceiver<br>0x2: Enable LS transceiver<br>0x3: Enable FS transceiver for LS packets<br>(FS preamble is automatically pre-pended) | RW | 0x1 |

### 7.5.6 FUNC_CTRL_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x05 | | |
| **PHYSICAL ADDRESS** | 0x05 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SUSPENDM | RESET | OPMODE | TERMSELECT | XCVRSELECT | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | SUSPENDM | | RW | 1 |
| 5 | RESET | | RW | 0 |
| 4:03 | OPMODE | | RW | 0x0 |
| 2 | TERMSELECT | | RW | 0 |
| 1:00 | XCVRSELECT | | RW | 0x1 |

### 7.5.7 FUNC_CTRL_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x06 | | |
| **PHYSICAL ADDRESS** | 0x06 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SUSPENDM | RESET | OPMODE | TERMSELECT | XCVRSELECT | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | SUSPENDM | | RW | 1 |
| 5 | RESET | | RW | 0 |
| 4:03 | OPMODE | | RW | 0x0 |
| 2 | TERMSELECT | | RW | 0 |
| 1:00 | XCVRSELECT | | RW | 0x1 |

### 7.5.8 IFC_CTRL

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x07 | | |
| **PHYSICAL ADDRESS** | 0x07 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Enables alternative interfaces and PHY features. | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INTERFACE_PROTECT_DISABLE | INDICATORPASSTHRU | INDICATORCOMPLEMENT | AUTORESUME | CLOCKSUSPENDM | CARKITMODE | FSLSSERIALMODE_3PIN | FSLSSERIALMODE_6PIN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | INTERFACE_PROTECT_DISABLE | Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states stp and data.<br>0b: Enables the interface protect circuit<br>1b: Disables the interface protect circuit | RW | 0 |
| 6 | INDICATORPASSTHRU | Controls whether the complement output is qualified with the internal vbusvalid comparator before being used in the VBUS State in the RXCMD.<br>0b: Complement output signal is qualified with the internal VBUSVALID comparator.<br>1b: Complement output signal is not qualified with the internal VBUSVALID comparator. | RW | 0 |
| 5 | INDICATORCOMPLEMENT | Tells the PHY to invert EXTERNALVBUSINDICATOR input signal, generating the complement output.<br>0b: PHY will not invert signal EXTERNALVBUSINDICATOR (default)<br>1b: PHY will invert signal EXTERNALVBUSINDICATOR | RW | 0 |
| 4 | AUTORESUME | Enables the PHY to automatically transmit resume signaling.<br>Refer to USB specification 7.1.7.7 and 7.9 for more details.<br>0 = AutoResume disabled<br>1 = AutoResume enabled (default) | RW | 1 |
| 3 | CLOCKSUSPENDM | Active low clock suspend. Valid only in Serial Modes. Powers down the internal clock circuitry only. Valid only when SuspendM = 1b. The PHY must ignore ClockSuspend when SuspendM = 0b. By default, the clock will not be powered in Serial and Carkit Modes.<br>0b : Clock will not be powered in Serial and UART Modes.<br>1b : Clock will be powered in Serial and UART Modes. | RW | 0 |
| 2 | CARKITMODE | Changes the ULPI interface to UART interface. The PHY automatically clear this field when UART mode is exited.<br>0b: UART disabled.<br>1b: Enable serial UART mode. | RW | 0 |
| 1 | FSLSSERIALMODE_3PIN | Changes the ULPI interface to 3-pin Serial.<br>The PHY must automatically clear this field when serial mode is exited.<br>0b: FS/LS packets are sent using parallel interface<br>1b: FS/LS packets are sent using 4-pin serial interface | RW | 0 |
| 0 | FSLSSERIALMODE_6PIN | Changes the ULPI interface to 6-pin Serial.<br>The PHY must automatically clear this field when serial mode is exited.<br>0b: FS/LS packets are sent using parallel interface<br>1b: FS/LS packets are sent using 6-pin serial interface | RW | 0 |

### 7.5.9 IFC_CTRL_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x08 | | |
| **PHYSICAL ADDRESS** | 0x08 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the ifc_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INTERFACE_PROTECT_DISABLE | INDICATORPASSTHRU | INDICATORCOMPLEMENT | AUTORESUME | CLOCKSUSPENDM | CARKITMODE | FSLSSERIALMODE_3PIN | FSLSSERIALMODE_6PIN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | INTERFACE_PROTECT_DISABLE | | RW | 0 |
| 6 | INDICATORPASSTHRU | | RW | 0 |
| 5 | INDICATORCOMPLEMENT | | RW | 0 |
| 4 | AUTORESUME | | RW | 1 |
| 3 | CLOCKSUSPENDM | | RW | 0 |
| 2 | CARKITMODE | | RW | 0 |
| 1 | FSLSSERIALMODE_3PIN | | RW | 0 |
| 0 | FSLSSERIALMODE_6PIN | | R | 0 |

### 7.5.10 IFC_CTRL_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x09 | | |
| **PHYSICAL ADDRESS** | 0x09 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the ifc_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INTERFACE_PROTECT_DISABLE | INDICATORPASSTHRU | INDICATORCOMPLEMENT | AUTORESUME | CLOCKSUSPENDM | CARKITMODE | FSLSSERIALMODE_3PIN | FSLSSERIALMODE_6PIN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | INTERFACE_PROTECT_DISABLE | | RW | 0 |
| 6 | INDICATORPASSTHRU | | RW | 0 |
| 5 | INDICATORCOMPLEMENT | | RW | 0 |
| 4 | AUTORESUME | | RW | 1 |
| 3 | CLOCKSUSPENDM | | RW | 0 |
| 2 | CARKITMODE | | RW | 0 |
| 1 | FSLSSERIALMODE_3PIN | | RW | 0 |
| 0 | FSLSSERIALMODE_6PIN | | R | 0 |

### 7.5.11 OTG_CTRL

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x0A | | |
| **PHYSICAL ADDRESS** | 0x0A | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Controls UTMI+ OTG functions of the PHY. | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| USEEXTERNALVBUSINDICATOR | DRVVBUSEXTERNAL | DRVVBUS | CHRGVBUS | DISCHRGVBUS | DMPULLDOWN | DPPULLDOWN | IDPULLUP |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | USEEXTERNALVBUSINDICATOR | Tells the PHY to use an external VBUS over-current indicator.<br>0b: Use the internal OTG comparator (VA_VBUS_VLD) or internal VBUS valid indicator (default)<br>1b: Use external VBUS valid indicator signal. | RW | 0 |
| 6 | DRVVBUSEXTERNAL | Selects between the internal and the external 5 V VBUS supply.<br>0b: Pin17 (CPEN) is disabled (output GND level). TUSB1210 does not support internal VBUS supply.<br>1b: Pin17 (CPEN) is set to ‘1’ (output VDD33 voltage level) if DRVVBUS bit is ‘1’, else Pin17 (CPEN) is disabled (output GND level) if DRVVBUS bit is ‘0’ | RW | 0 |
| 5 | DRVVBUS | VBUS output control bit<br>0b : do not drive VBUS<br>1b : drive 5V on VBUS<br>Note: Both DRVVBUS and DRVVBUSEXTERNAL bits must be set to 1 in order to to set Pin17 (CPEN). CPEN pin can be used to enable an external VBUS supply | RW | 0 |
| 4 | CHRGVBUS | Charge VBUS through a resistor. Used for VBUS pulsing SRP. The Link must first check that VBUS has been discharged (see DischrgVbus register bit), and that both D+ and D- data lines have been low (SE0) for 2ms.<br>0b : do not charge VBUS<br>1b : charge VBUS | RW | 0 |
| 3 | DISCHRGVBUS | Discharge VBUS through a resistor. If the Link sets this bit to 1, it waits for an RX CMD indicating SessEnd has transitioned from 0 to 1, and then resets this bit to 0 to stop the discharge.<br>0b : do not discharge VBUS<br>1b : discharge VBUS | RW | 0 |
| 2 | DMPULLDOWN | Enables the 15k Ohm pull-down resistor on D-.<br>0b : Pull-down resistor not connected to D-.<br>1b : Pull-down resistor connected to D-. | RW | 1 |
| 1 | DPPULLDOWN | Enables the 15k Ohm pull-down resistor on D+.<br>0b : Pull-down resistor not connected to D+.<br>1b : Pull-down resistor connected to D+. | RW | 1 |
| 0 | IDPULLUP | Connects a pull-up to the ID line and enables sampling of the signal level.<br>0b : Disable sampling of ID line.<br>1b : Enable sampling of ID line. | RW | 0 |

### 7.5.12 OTG_CTRL_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x0B | | |
| **PHYSICAL ADDRESS** | 0x0B | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the otg_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| USEEXTERNALVBUSINDICATOR | DRVVBUSEXTERNAL | DRVVBUS | CHRGVBUS | DISCHRGVBUS | DMPULLDOWN | DPPULLDOWN | IDPULLUP |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | USEEXTERNALVBUSINDICATOR | | RW | 0 |
| 6 | DRVVBUSEXTERNAL | | RW | 0 |
| 5 | DRVVBUS | | RW | 0 |
| 4 | CHRGVBUS | | RW | 0 |
| 3 | DISCHRGVBUS | | RW | 0 |
| 2 | DMPULLDOWN | | RW | 1 |
| 1 | DPPULLDOWN | | RW | 1 |
| 0 | IDPULLUP | | RW | 0 |

### 7.5.13 OTG_CTRL_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x0C | | |
| **PHYSICAL ADDRESS** | 0x0C | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the otg_ctrl register with read/Clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| USEEXTERNALVBUSINDICATOR | DRVVBUSEXTERNAL | DRVVBUS | CHRGVBUS | DISCHRGVBUS | DMPULLDOWN | DPPULLDOWN | IDPULLUP |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | USEEXTERNALVBUSINDICATOR | | RW | 0 |
| 6 | DRVVBUSEXTERNAL | | RW | 0 |
| 5 | DRVVBUS | | RW | 0 |
| 4 | CHRGVBUS | | RW | 0 |
| 3 | DISCHRGVBUS | | RW | 0 |
| 2 | DMPULLDOWN | | RW | 1 |
| 1 | DPPULLDOWN | | RW | 1 |
| 0 | IDPULLUP | | RW | 0 |

### 7.5.14 USB_INT_EN_RISE

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x0D | | |
| **PHYSICAL ADDRESS** | 0x0D | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled. | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | IDGND_RISE | SESSEND_RISE | SESSVALID_RISE | VBUSVALID_RISE | HOSTDISCONNECT_RISE |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_RISE | Generate an interrupt event notification when IdGnd changes from low to high. | RW | 1 |
| | | Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1. | | |
| 3 | SESSEND_RISE | Generate an interrupt event notification when SessEnd changes from low to high. | RW | 1 |
| 2 | SESSVALID_RISE | Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. | RW | 1 |
| 1 | VBUSVALID_RISE | Generate an interrupt event notification when VbusValid changes from low to high. | RW | 1 |
| 0 | HOSTDISCONNECT_RISE | Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). | RW | 1 |

### 7.5.15 USB_INT_EN_RISE_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x0E | | |
| **PHYSICAL ADDRESS** | 0x0E | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the usb_int_en_rise register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | IDGND_RISE | SESSEND_RISE | SESSVALID_RISE | VBUSVALID_RISE | HOSTDISCONNECT_RISE |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_RISE | | RW | 1 |
| 3 | SESSEND_RISE | | RW | 1 |
| 2 | SESSVALID_RISE | | RW | 1 |
| 1 | VBUSVALID_RISE | | RW | 1 |
| 0 | HOSTDISCONNECT_RISE | | RW | 1 |

### 7.5.16 USB_INT_EN_RISE_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x0F | | |
| **PHYSICAL ADDRESS** | 0x0F | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the usb_int_en_rise register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | IDGND_RISE | SESSEND_RISE | SESSVALID_RISE | VBUSVALID_RISE | HOSTDISCONNECT_RISE |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_RISE | | RW | 1 |
| 3 | SESSEND_RISE | | RW | 1 |
| 2 | SESSVALID_RISE | | RW | 1 |
| 1 | VBUSVALID_RISE | | RW | 1 |
| 0 | HOSTDISCONNECT_RISE | | RW | 1 |

### 7.5.17 USB_INT_EN_FALL

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x10 | | |
| **PHYSICAL ADDRESS** | 0x10 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled. | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | IDGND_FALL | SESSEND_FALL | SESSVALID_FALL | VBUSVALID_FALL | HOSTDISCONNECT_FALL |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_FALL | Generate an interrupt event notification when IdGnd changes from high to low.<br>Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1. | RW | 1 |
| 3 | SESSEND_FALL | Generate an interrupt event notification when SessEnd changes from high to low. | RW | 1 |
| 2 | SESSVALID_FALL | Generate an interrupt event notification when SessValid changes from high to low. SessValid is the same as UTMI+ AValid. | RW | 1 |
| 1 | VBUSVALID_FALL | Generate an interrupt event notification when VbusValid changes from high to low. | RW | 1 |
| 0 | HOSTDISCONNECT_FALL | Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). | RW | 1 |

### 7.5.18 USB_INT_EN_FALL_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x11 | | |
| **PHYSICAL ADDRESS** | 0x11 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the usb_int_en_fall register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action) | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | IDGND_FALL | SESSEND_FALL | SESSVALID_FALL | VBUSVALID_FALL | HOSTDISCONNECT_FALL |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_FALL | | RW | 1 |
| 3 | SESSEND_FALL | | RW | 1 |
| 2 | SESSVALID_FALL | | RW | 1 |
| 1 | VBUSVALID_FALL | | RW | 1 |
| 0 | HOSTDISCONNECT_FALL | | RW | 1 |

### 7.5.19 USB_INT_EN_FALL_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x12 | | |
| **PHYSICAL ADDRESS** | 0x12 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the usb_int_en_fall register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | IDGND_FALL | SESSEND_FALL | SESSVALID_FALL | VBUSVALID_FALL | HOSTDISCONNECT_FALL |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_FALL | | RW | 1 |
| 3 | SESSEN D_FALL | | RW | 1 |
| 2 | SESSVALID_FALL | | RW | 1 |
| 1 | VBUSVALID_FALL | | RW | 1 |
| 0 | HOSTDISCONNECT_FALL | | RW | 1 |

### 7.5.20 USB_INT_STS

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x13 | | |
| **PHYSICAL ADDRESS** | 0x13 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Indicates the current value of the interrupt source signal. | | |
| **TYPE** | R | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | IDGND | SESSEND | SESSVALID | VBUSVALID | HOSTDISCONNECT |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND | Current value of UTMI+ IdGnd output.<br>This bit is not updated if IdPullup bit is reset to 0 and for 50 ms after IdPullup is set to 1. | R | 0 |
| 3 | SESSEND | Current value of UTMI+ SessEnd output. | R | 0 |
| 2 | SESSVALID | Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid. | R | 0 |
| 1 | VBUSVALID | Current value of UTMI+ VbusValid output. | R | 0 |
| 0 | HOSTDISCONNECT | Current value of UTMI+ Hostdisconnect output.<br>Applicable only in host mode.<br>Automatically reset to 0 when Low Power Mode is entered.<br>NOTE: Reset value is '0' when host is connected.<br>Reset value is '1' when host is disconnected. | R | 0 |

### 7.5.21 USB_INT_LATCH

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x14 | | |
| **PHYSICAL ADDRESS** | 0x14 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial Mode or Carkit Mode is entered regardless of the value of ClockSuspendM.<br>The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit. It is important to note that if register read data is returned to the Link in the same cycle that a USB Interrupt Latch bit is to be set, the interrupt condition is given immediately in the register read data and the Latch bit is not set.<br>Note that it is optional for the Link to read the USB Interrupt Latch register in Synchronous Mode because the RX CMD byte already indicates the interrupt source directly | | |
| **TYPE** | R | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | IDGND_LATCH | SESSEND_LATCH | SESSVALID_LATCH | VBUSVALID_LATCH | HOSTDISCONNECT_LATCH |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_LATCH | Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read. | R | 0 |
| 3 | SESSEND_LATCH | Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read. | R | 0 |
| 2 | SESSVALID_LATCH | Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid. | R | 0 |
| 1 | VBUSVALID_LATCH | Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read. | R | 0 |
| 0 | HOSTDISCONNECT_LATCH | Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode.<br>NOTE: As this IT is enabled by default, the reset value depends on the host status<br>Reset value is '0' when host is connected.<br>Reset value is '1' when host is disconnected. | R | 0 |

### 7.5.22 DEBUG

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x15 | | |
| **PHYSICAL ADDRESS** | 0x15 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Indicates the current value of various signals useful for debugging. | | |
| **TYPE** | R | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | LINESTATE | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | Reserved | | R | 0 |
| 3 | Reserved | | R | 0 |
| 2 | Reserved | | R | 0 |
| 1:00 | LINESTATE | These signals reflect the current state of the single ended receivers. They directly reflect the current state of the DP (LineState[0]) and DM (LineState[1]) signals.<br>• Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp)<br>• Read 0x1:<br>– LS: 'K' State,<br>– FS: 'J' State,<br>– HS: !Squelch,<br>– Chirp: !Squelch & HS_Differential_Receiver_Output<br>• Read 0x2:<br>– LS: 'K' State,<br>– FS: 'J' State,<br>– HS: !Squelch,<br>– Chirp: !Squelch & HS_Differential_Receiver_Output<br>• Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp) | R | 0x0 |

### 7.5.23 SCRATCH_REG

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x16 | | |
| **PHYSICAL ADDRESS** | 0x16 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected. | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCRATCH | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7:00 | SCRATCH | Scratch data. | RW | 0x00 |

### 7.5.24 SCRATCH_REG_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x17 | | |
| **PHYSICAL ADDRESS** | 0x17 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the scratch_reg register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCRATCH | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7:00 | SCRATCH | | RW | 0x00 |

### 7.5.25 SCRATCH_REG_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x18 | | |
| **PHYSICAL ADDRESS** | 0x18 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the scratch_reg with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCRATCH | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7:00 | SCRATCH | | RW | 0x00 |

### 7.5.26 VENDOR_SPECIFIC1

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x3D | | |
| **PHYSICAL ADDRESS** | 0x3D | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Power Control register. | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SPARE | MNTR_VUSBIN_OK_EN | ID_FLOAT_EN | ID_RES_EN | BVALID_FALL | BVALID_RISE | SPARE | ABNORMALSTRESS_EN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | SPARE | Reserved. The link must never write a 1b to this bit. | RW | 0 |
| 6 | MNTR_VUSBIN_OK_EN | When set to 1, it enables RX CMDs for high to low or low to high transitions on MNTR_VUSBIN_OK. This bit is provided for debugging purposes. | RW | 0 |
| 5 | ID_FLOAT_EN | When set to 1, it enables RX CMDs for high to low or low to high transitions on ID_FLOAT. This bit is provided for debugging purposes. | RW | 0 |
| 4 | ID_RES_EN | When set to 1, it enables RX CMDs for high to low or low to high transitions on ID_RESA, ID_RESB and ID_RESC. This bit is provided for debugging purposes. | RW | 0 |
| 3 | BVALID_FALL | Enables RX CMDs for high to low transitions on BVALID. When BVALID changes from high to low, the USB TRANS will send an RX CMD to the link with the alt_int bit set to 1b.<br>This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default. | RW | 0 |
| 2 | BVALID_RISE | Enables RX CMDs for low to high transitions on BVALID. When BVALID changes from low to high, the USB Trans will send an RX CMD to the link with the alt_int bit set to 1b.<br>This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default. | RW | 0 |
| 1 | SPARE | Reserved. The link must never write a 1b to this bit. | RW | 0 |
| 0 | ABNORMALSTRESS_EN | When set to 1, it enables RX CMDs for low to high and high to low transitions on ABNORMALSTRESS. This bit is provided for debugging purposes. | RW | 0 |

### 7.5.27 VENDOR_SPECIFIC1_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x3E | | |
| **PHYSICAL ADDRESS** | 0x3E | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATEN CY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SPARE | MNTR_VUSBIN_OK_EN | ID_FLOAT_EN | ID_RES_EN | BVALID_FALL | BVALID_RISE | SPARE | ABNORMALSTRESS_EN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | SPARE | | RW | 0 |
| 6 | MNTR_VUSBIN_OK_EN | | RW | 0 |
| 5 | ID_FLOAT_EN | | RW | 0 |
| 4 | ID_RES_EN | | RW | 0 |
| 3 | BVALID_FALL | | RW | 0 |
| 2 | BVALID_RISE | | RW | 0 |
| 1 | SPARE | | RW | 0 |
| 0 | ABNORMALSTRESS_EN | | RW | 0 |

### 7.5.28 VENDOR_SPECIFIC1_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x3F | | |
| **PHYSICAL ADDRESS** | 0x3F | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SPARE | MNTR_VUSBIN_OK_EN | ID_FLOAT_EN | ID_RES_EN | BVALID_FALL | BVALID_RISE | SPARE | ABNORMALSTRESS_EN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | SPARE | | RW | 0 |
| 6 | MNTR_VUSBIN_OK_EN | | RW | 0 |
| 5 | ID_FLOAT_EN | | RW | 0 |
| 4 | ID_RES_EN | | RW | 0 |
| 3 | BVALID_FALL | | RW | 0 |
| 2 | BVALID_RISE | | RW | 0 |
| 1 | SPARE | | RW | 0 |
| 0 | ABNORMALSTRESS_EN | | RW | 0 |

### 7.5.29 VENDOR_SPECIFIC2

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x80 | | |
| **PHYSICAL ADDRESS** | 0x80 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Eye diagram programmability and DP/DM swap control . | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SPARE | DATAPOLARITY | ZHSDRV | IHSTX | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | SPARE | | RW | 0 |
| 6 | DATAPOLARITY | Control data polarity on dp/dm | RW | 1 |
| 5:04 | ZHSDRV | High speed output impedance configuration for eye diagram tuning :<br>00 45.455 Ω<br>01 43.779 Ω<br>10 42.793 Ω<br>11 42.411 Ω | RW | 0x0 |
| 3:00 | IHSTX | High speed output drive strength configuration for eye diagram tuning :<br>0000 17.928 mA<br>0001 18.117 mA<br>0010 18.306 mA<br>0011 18.495 mA<br>0100 18.683 mA<br>0101 18.872 mA<br>0110 19.061 mA<br>0111 19.249 mA<br>1000 19.438 mA<br>1001 19.627 mA<br>1010 19.816 mA<br>1011 20.004 mA<br>1100 20.193 mA<br>1101 20.382 mA<br>1110 20.570 mA<br>1111 20.759 mA<br>IHSTX[0] is also the AC BOOST enable<br>IHSTX[0] = 0 à AC BOOST is disabled<br>IHSTX[0] = 1 à AC BOOST is enabled | RW | 0x1 |

### 7.5.30 VENDOR_SPECIFIC2_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x81 | | |
| **PHYSICAL ADDRESS** | 0x81 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the VENDOR_SPECIFIC1 register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SPARE | DATAPOLARITY | ZHSDRV | IHSTX | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | SPARE | | RW | 0 |
| 6 | DATAPOLARITY | | RW | 1 |
| 5:04 | ZHSDRV | | RW | 0x0 |
| 3:00 | IHSTX | | RW | 0x1 |

### 7.5.31 VENDOR_SPECIFIC2_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x82 | | |
| **PHYSICAL ADDRESS** | 0x82 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | This register does not physically exist.<br>It is the same as the VENDOR_SPECIFIC1 register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SPARE | DATAPOLARITY | ZHSDRV | IHSTX | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | SPARE | | RW | 0 |
| 6 | DATAPOLARITY | | RW | 1 |
| 5:04 | ZHSDRV | | RW | 0x0 |
| 3:00 | IHSTX | | RW | 0x1 |

### 7.5.32 VENDOR_SPECIFIC1_STS

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x83 | | |
| **PHYSICAL ADDRESS** | 0x83 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | Indicates the current value of the interrupt source signal. | | |
| **TYPE** | R | | |
| **WRITE LATEN CY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | MNTR_VUSBIN_OK_STS | ABNORMALSTRESS_STS | ID_FLOAT_STS | ID_RESC_STS | ID_RESB_STS | ID_RESA_STS | BVALID_STS |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | MNTR_VUSBIN_OK_STS | Current value of MNTR_VUSBIN_OK output | R | 0 |
| 5 | ABNORMALSTRESS_STS | Current value of ABNORMALSTRESS output | R | 0 |
| 4 | ID_FLOAT_STS | Current value of ID_FLOAT output | R | 0 |
| 3 | ID_RESC_STS | Current value of ID_RESC output | R | 0 |
| 2 | ID_RESB_STS | Current value of ID_RESB output | R | 0 |
| 1 | ID_RESA_STS | Current value of ID_RESA output | R | 0 |
| 0 | BVALID_STS | Current value of VB_SESS_VLD output | R | 0 |

### 7.5.33 VENDOR_SPECIFIC1_LATCH

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x84 | | |
| **PHYSICAL ADDRESS** | 0x84 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial mode is entered regardless of the value of ClockSuspendM.<br>The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit. | | |
| **TYPE** | R | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | MNTR_VUSBIN_OK_LATCH | ABNORMALSTRESS_LATCH | ID_FLOAT_LATCH | ID_RESC_LATCH | ID_RESB_LATCH | ID_RESA_LATCH | BVALID_LATCH |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | R | 0 |
| 6 | MNTR_VUSBIN_OK_LATCH | Set to 1 when an unmasked event occurs on MNTR_VUSBIN_OK_LATCH. Clear on read register. | R | 0 |
| 5 | ABNORMALSTRESS_LATCH | Set to 1 when an unmasked event occurs on ABNORMALSTRESS. Clear on read register. | R | 0 |
| 4 | ID_FLOAT_LATCH | Set to 1 when an unmasked event occurs on ID_FLOAT. Clear on read register. | R | 0 |
| 3 | ID_RESC_LATCH | Set to 1 when an unmasked event occurs on ID_RESC. Clear on read register. | R | 0 |
| 2 | ID_RESB_LATCH | Set to 1 when an unmasked event occurs on ID_RESB. Clear on read register. | R | 0 |
| 1 | ID_RESA_LATCH | Set to 1 when an unmasked event occurs on ID_RESA. Clear on read register. | R | 0 |
| 0 | BVALID_LATCH | Set to 1 when an unmasked event occurs on VB_SESS_VLD. Clear on read register. | R | 0 |

### 7.5.34 VENDOR_SPECIFIC3

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x85 | | |
| **PHYSICAL ADDRESS** | 0x85 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | SOF_EN | CPEN_OD | CPEN_ODOS | IDGND_DRV | VUSB3V3_VSEL | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | RW | 0 |
| 6 | SOF_EN | 0: HS USB SOF detector disabled.<br>1: Enable HS USB SOF detection when PHY is set in device mode. SOF are output on CPEN pin. HS USB SOF (start-of-frame) output clock is available on CPEN pin when this bit is set. HS USB SOF packet rate is 8 kHz.<br>This bit is provided for debugging purpose only. It must never been write to ‘1’ in functional mode | RW | 0 |
| 5 | CPEN_OD | This bit has no effect when CPEN_ODOS = ‘0’, else :<br>0: CPEN pad is in OS (Open Source) mode.<br>In this case CPEN pin has an internal NMOS driver, and will be active LOW.<br>Externally there should be a pullup resistor on CPEN (min 1kΩ) to a supply voltage (max 3.6V).<br>1: CPEN pad is in OD (Open Drain) mode<br>In this case CPEN pin has an internal PMOS driver, and will be active HIGH.<br>Externally there should be a pull-down resistor on CPEN (min 1 kΩ to GND. | RW | 0 |
| 4 | CPEN_ODOS | Mode selection bit for CPEN pin.<br>0 : CPEN pad is in CMOS mode<br>1: CPEN pad is in OD (Open Drain) or OS (Open Source) mode (controlled by CPEN_OD bit) | RW | 0 |
| 3 | IDGND_DRV | Drives ID pin to ground | RW | 0x0 |
| 2:00 | VUSB3V3_VSEL | 000 VRUSB3P1V = 2.5 V<br>001 VRUSB3P1V = 2.75 V<br>010 VRUSB3P1V = 3.0 V<br>011 VRUSB3P1V = 3.10 V (default)<br>100 VRUSB3P1V = 3.20 V<br>101 VRUSB3P1V = 3.30 V<br>110 VRUSB3P1V = 3.40 V<br>111 VRUSB3P1V = 3.50 V | RW | 0x3 |

### 7.5.35 VENDOR_SPECIFIC3_SET

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x86 | | |
| **PHYSICAL ADDRESS** | 0x86 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | SOF_EN | CPEN_OD | CPEN_ODOS | IDGND_DRV | VUSB3V3_VSEL | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | RW | 0 |
| 6 | SOF_EN | | RW | 0 |
| 5 | CPEN_OD | | RW | 0 |
| 4 | CPEN _ODOS | | RW | 0 |
| 3 | IDGND_DRV | | RW | 0x0 |
| 2:00 | VUSB3V3_VSEL | | RW | 0x3 |

### 7.5.36 VENDOR_SPECIFIC3_CLR

| | | | |
|---|---|---|---|
| **ADDRESS OFFSET** | 0x87 | | |
| **PHYSICAL ADDRESS** | 0x87 | **INSTANCE** | USB_SCUSB |
| **DESCRIPTION** | | | |
| **TYPE** | RW | | |
| **WRITE LATENCY** | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | SOF_EN | CPEN_OD | CPEN_ODOS | IDGND_DRV | VUSB3V3_VSEL | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|---|---|---|---|---|
| 7 | Reserved | | RW | 0 |
| 6 | SOF_EN | | RW | 0 |
| 5 | CPEN_OD | | RW | 0 |
| 4 | CPEN_ODOS | | RW | 0 |
| 3 | IDGND_DRV | | RW | 0x0 |
| 2:00 | VUSB3V3_VSEL | | RW | 0x3 |

# 8 Application and Implementation

**Note**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

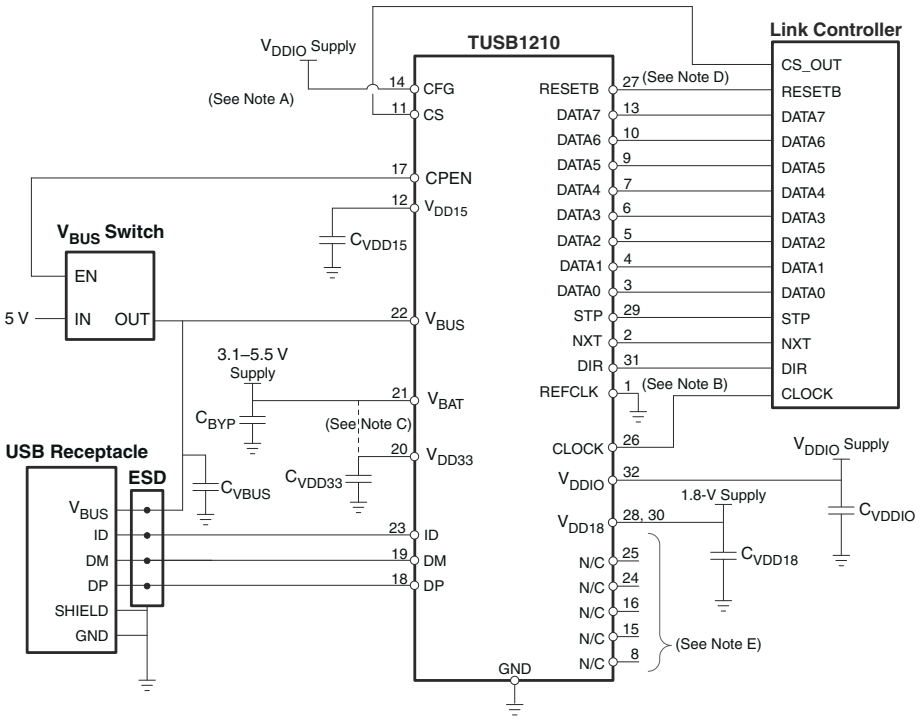
## 8.1 Application Information

*图 8-1* shows the suggested application diagram (Host or OTG, ULPI input-clock mode).

## 8.2 Typical Application

### 8.2.1 Host or OTG, ULPI Input Clock Mode Application

图 8-1 shows a suggested application diagram for TUSB1210 in the case of ULPI input-clock mode (60 MHz ULPI clock is provided by link processor), in Host or OTG application. Note: this is just one example, it is of course possible to operate as HOST or OTG while also in ULPI output-clock mode.




A. Pin 11 (CS): can be tied high to $VI_O$ if the CS_OUT pin is unavailable; Pin 14 (CFG): tie-high is *do not care* since the ULPI clock is used in input mode
B. Pin 1 (REFCLK): must be tied low
C. Ext 3 V supply supported
D. Pin 27 (RESETB) can be tied to $V_{DDIO}$ if unused.
E. Pins labeled N/C (no-connect) are truly no-connect, and can be tied or left floating.

**图 8-1. Host or OTG, ULPI Input Clock Mode Application Diagram**

### 8.2.1.1 Design Requirements

表 8-1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| $V_{BAT}$ | 3.3 V |
| $V_{DDIO}$ | 1.8 V |
| $V_{BUS}$ | 5.0 V |
| USB Support | HS, FS, LS |
| USB On the Go (OTG) | Yes |
| Clock Sources | 60 MHz Clock |

### 8.2.1.2 Detailed Design Procedure

Connect the TUSB1210 device as is shown in 图 8-1.

Follow the Board Guidelines in the TUSB121x USB2.0 Board Guidelines application report.

#### 8.2.1.2.1 Unused Pins Connection

- **VBUS:** Input. Recommended to tie to GND if unused. However, leaving $V_{BUS}$ floating is also acceptable since internally there is an 80 kΩ resistance to ground.
- **REFCLK:** Input. If REFCLK is unused and 60 MHz clock is provided by MODEM (60 MHz should be connected to CLOCK pin in this case), then tie REFCLK to GND.
- **CFG:** Tie to GND if REFCLK is 19.2 MHz, or tie to $V_{DDIO}$ if REFCLK is 26 MHz. Tie to either GND or $V_{DDIO}$ (does not matter which) if REFCLK is not used (for example, ULPI input clock configuration).

### 8.2.1.3 Application Curve

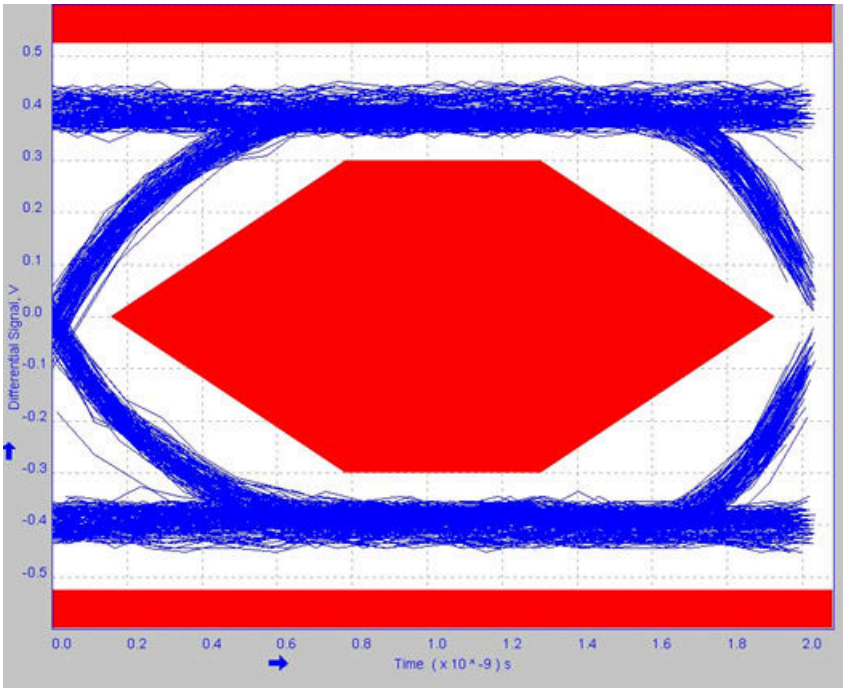
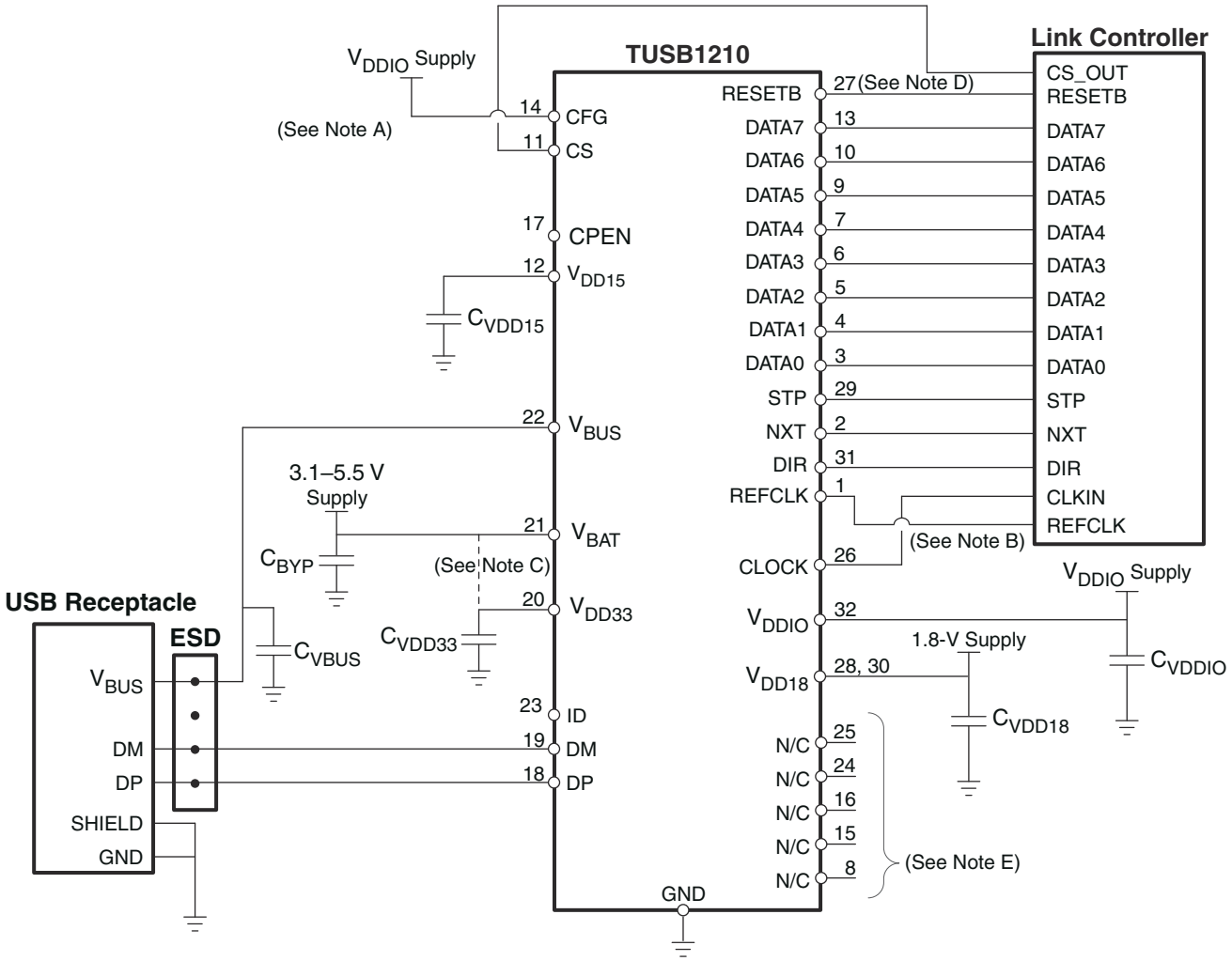



图 8-2. High-Speed Eye Diagram

### 8.2.2 Device, ULPI Output Clock Mode Application

图 8-3 shows a suggested application diagram for TUSB1210 in the case of ULPI output clock mode (60 MHz ULPI clock is provided by TUSB1210, while link processor or another external circuit provides REFCLK), in Device mode application. Note: this is just one example, it is of course possible to operate as Device while also in ULPI input-clock mode. Refer also to 图 8-1.




A. Pin 11 (CS): can be tied high to $V_{IO}$ if CS_OUT pin unavailable; Pin 14 (CFG): Tied to $V_{DDIO}$ for 26 MHz REFCLK mode here, tie to GND for 19.2 MHz mode.
B. Pin 1 (REFCLK): connect to external 3.3 V square-wave reference clock
C. Ext 3 V supply supported
D. Pin 27 (RESETB) can be tied to $V_{DDIO}$ if unused.
E. Pins labeled N/C (no-connect) are truly no-connect, and can be tied or left floating.

**图 8-3. Device, ULPI Output Clock Mode Application Diagram**

### 8.2.2.1 Design Requirements

表 8-2. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| $V_{BAT}$ | 3.3 V |
| $V_{DDIO}$ | 1.8 V |
| $V_{BUS}$ | 5.0 V |
| USB Support | HS, FS, LS |
| Clock Sources | 26 MHz or 19.2 MHz Oscillator |

### 8.2.2.2 Detailed Design Procedure

Connect the TUSB1210 device as is shown in 图 8-3.

Follow the Board Guidelines in the TUSB121x USB2.0 Board Guidelines application report.

#### 8.2.2.2.1 Unused Pins Connection

- **ID:** Input. Leave floating if unused or TUSB1210 is Device mode only. Tie to GND through RID < 1 kΩ if Host mode.
- **REFCLK:** Input. If REFCLK is unused, and 60 MHz clock is provided by MODEM (60 MHz should be connected to CLOCK pin in this case) then tie REFCLK to GND.
- **CFG:** Tie to GND if REFCLK is 19.2 MHz, or tie to $V_{DDIO}$ if REFCLK is 26 MHz. Tie to either GND or $V_{DDIO}$ (does not matter which) if REFCLK not used (for example, ULPI input clock configuration).

### 8.2.2.3 Application Curve

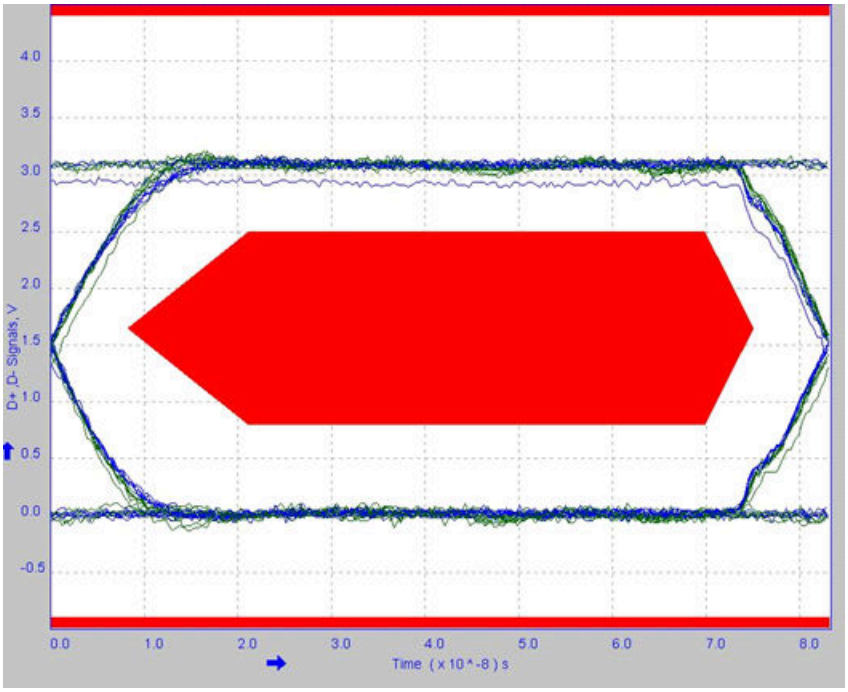



图 8-4. Full-Speed Eye Diagram

## 8.3 External Components

表 8-3. TUSB1210 External Components

| FUNCTION | COMPONENT | REFERENCE | VALUE | NOTE | LINK |
|---|---|---|---|---|---|
| $V_{DDIO}$ | Capacitor | CVDDIO | 100 nF | Suggested value, application dependent | 图 8-1 |
| $V_{DD33}$ | Capacitor | CVDD33 | 2.2 µF | Range: [0.45 µF: 6.5 µF] , ESR = [0: 600 mΩ] for f> 10 kHz | 图 8-1 |
| $V_{DD15}$ | Capacitor | CVDD15 | 2.2 µF | Range: [0.45 µF: 6.5 µF] , ESR = [0: 600 mΩ] for f> 10 kHz | 图 8-1 |
| $V_{DD18}$ | Capacitor | Ext 1.8V supply | 100 nF | Suggested value, application dependent | 图 8-1 |
| | | CVDD18 | | | |
| $V_{BAT}$ | Capacitor | CBYP | 100 nF(1) | Range: [0.45 µF: 6.5 µF] , ESR = [0: 600 mΩ] for f> 10 kHz | 图 8-1 |
| $V_{BUS}$ | Capacitor | CVBUS | See 表 8-4 | Place close to USB connector | 图 8-1 |

(1) Recommended value but 2.2 µF may be sufficient in some applications

表 8-4. TUSB1210 $V_{BUS}$ Capacitors

| FUNCTION | COMPONENT | REFERENCE | VALUE | NOTE | LINK |
|---|---|---|---|---|---|
| VBUS – HOST | Capacitor | CVBUS | >120 µF | | 图 8-1 |
| VBUS – DEVICE | Capacitor | CVBUS | 4.7 µF | Range: 1.0 µF to 10.0 µF | 图 8-1 |
| VBUS – OTG | Capacitor | CVBUS | 4.7 µF | Range: 1.0 µF to 6.5 µF | 图 8-1 |

# 9 Power Supply Recommendations

$V_{BUS}$, $V_{BAT}$, and $V_{DDIO}$ are needed to power the TUSB1210. Recommended operation is for $V_{BAT}$ to be present before $V_{DDIO}$. Applying $V_{DDIO}$ before $V_{BAT}$ to TUSB1210 is not recommended as there is a diode from $V_{DDIO}$ to $V_{BAT}$ which will be forward biased when $V_{DDIO}$ is present but $V_{BAT}$ is not present. TUSB1210 does not strictly require $V_{BUS}$ to function.

## 9.1 TUSB1210 Power Supply

- The $V_{DDIO}$ pins of the TUSB1210 supply 1.8 V (nominal) power to the core of the TUSB1210. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The $V_{BAT}$ pin of the TUSB1210 supply 3.3 V (nominal) power rail to the TUSB1210. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The $V_{BUS}$ pin of the TUSB1210 supply 5.0 V (nominal) power rail to the TUSB1210. This pin is normally connected to the $V_{BUS}$ pin of the USB connector.
- The $V_{BUS}$ pin of the TUSB1210 supply 5.0 V (nominal) power rail to the TUSB1210. This pin is normally connected to the $V_{BUS}$ pin of the USB connector.

## 9.2 Ground

It is recommended that almost one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

## 9.3 Power Providers

表 9-1 is a summary of TUSB1210 power providers.

**表 9-1. Power Providers(1)**

| NAME | USAGE | TYPE | TYPICAL VOLTAGE (V) | MAXIMUM CURRENT (mA) |
|---|---|---|---|---|
| $V_{DD15}$ | Internal | LDO | 1.5 | 50 |
| $V_{DD18}$ | External | LDO | 1.8 | 30 |
| $V_{DD33}$ | Internal | LDO | 3.1 | 15 |

(1) $V_{DD33}$ may be supplied externally or by shorting the $V_{DD33}$ pin to $V_{BAT}$ pin, provided $V_{BAT}$ minimum is in range [3.2 V: 3.6 V]. Note that the $V_{DD33}$ LDO will always power-on when the chip is enabled, irrespective of whether $V_{DD33}$ is supplied externally or not. In the case the $V_{DD33}$ pin is not supplied externally in the application, the electrical specifications for this LDO are provided below.

## 9.4 Power Modules

### 9.4.1 $V_{DD33}$ Regulator

The $V_{DD33}$ internal LDO regulator powers the USB PHY, charger detection, and OTG functions of the USB subchip inside TUSB1210. 节 6.12 describes the regulator characteristics.

$V_{DD33}$ regulator takes its power from $V_{BAT}$.

Since the USB2.0 standard requires data lines to be biased with pullups biased from a supply greater than 3 V, and since $V_{DD33}$ regulator has an inherent voltage drop from its input, $V_{BAT}$, to its regulated output, TUSB1210 will not meet USB 2.0 Standard if operated from a battery whose voltage is lower than 3.3 V.

### 9.4.2 $V_{DD18}$ Supply

The $V_{DD18}$ supply is powered externally at the $V_{DD18}$ pin. See 表 8-3 for external components.

### 9.4.3 $V_{DD15}$ Regulator

The $V_{DD15}$ internal LDO regulator powers the USB subchip inside TUSB1210. 节 6.12 describes the regulator characteristics.

## 9.5 Power Consumption

表 9-2 describes the power consumption depending on the use cases.

**Note**

The typical power consumption is obtained in the nominal operating conditions and with the TUSB1210 standalone.

**表 9-2. Power Consumption**

| MODE | CONDITIONS | SUPPLY | TYPICAL CONSUMPTION | UNIT |
|---|---|---|---|---|
| OFF Mode | $V_{BAT}$ = 3.6 V, $V_{DDIO}$ = 1.8 V, $V_{DD18}$ = 1.8 V, CS = 0 V | $I_{VBAT}$ | 8 | µA |
| | | $I_{VDDIO}$ | 3 | |
| | | $I_{VDD18}$ | 5 | |
| | | **$I_{TOTAL}$** | 16 | |
| Suspend Mode | $V_{BUS}$ = 5 V, $V_{BAT}$ = 3.6 V, $V_{DDIO}$ = 1.8 V, No clock | $I_{VBAT}$ | 204 | µA |
| | | $I_{VDDIO}$ | 3 | |
| | | $I_{VDD18}$ | 3 | |
| | | **$I_{TOTAL}$** | 210 | |
| HS USB Operation (Synchronous Mode) | $V_{BAT}$ = 3.6 V, $V_{DDIO}$ = 1.8 V, $V_{DD18}$ = 1.8 V, active USB transfer | $I_{VBAT}$ | 24.6 | mA |
| | | $I_{VDDIO}$ | 1.89 | |
| | | $I_{VDD18}$ | 21.5 | |
| | | **$I_{TOTAL}$** | 48 | |
| FS USB Operation (Synchronous Mode) | $V_{BAT}$ = 3.6 V, $V_{DDIO}$ = 1.8 V, active USB transfer | $I_{VBAT}$ | 25.8 | mA |
| | | $I_{VDDIO}$ | 1.81 | |
| | | $I_{VDD18}$ | 4.06 | |
| | | **$I_{TOTAL}$** | 31.7 | |
| Reset Mode | RESETB = 0 V, $V_{BUS}$ = 5 V, $V_{BAT}$ = 3.6 V, $V_{DDIO}$ = 1.8 V, No clock | $I_{VBAT}$ | 237 | µA |
| | | $I_{VDDIO}$ | 3 | |
| | | $I_{VDD18}$ | 3 | |
| | | **$I_{TOTAL}$** | 243 | |

# 10 Layout

## 10.1 TUSB121x USB2.0 Product Family Board Layout Recommendations

表 10-1. TUSB121x USB2.0 Product Family Board Layout Recommendations

| Item | USB General Considerations |
|---|---|
| 1.00 | USB design requires symmetrical termination and symmetrical component placement along the DP and DM paths. |
| 1.01 | Place the USB host controller and major components on the unrouted board first. |
| 1.02 | Place the USB host controller, as close as possible to the transceiver device, that is, ULPI interface traces as short as possible. |
| 1.03 | Route high-speed clock and high-speed USB. Route differential pairs first.<br>Since these signals are critical and long length traces are to be avoided, it is therefore recommended to route DP/DM before routing less critical signals on the board. A similar recommendation is true for CLK, and ULPI signals which should be routed with equalized trace length. |
| 1.04 | Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as I/O connectors, control, and signal headers or power connectors). |
| 1.05 | Place the USB receptacle at the board edge. |
| 1.06 | Maximum TI-recommended external capacitance on DP (or DM) lines is 4 pF<br>• This capacitance is the sum of all external discrete components, that is, the total capacitance on DP (or DM) lines including trace capacitance can be larger than 4 pF.<br>• All discrete components should be placed as close as possible to the USB receptacle. |
| 1.07 | Place the low-capacitance ESD protections as close as possible to the USB receptacle, with no other external devices in between. |
| 1.08 | Common mode chokes degrade signal quality, thus they should only be used if EMI performance enhancement is absolutely necessary. |
| 1.09 | Place the common mode choke (if required to improve EMI performance) as close as possible to the USB receptacle (but after one or more of the ESD devices). |
| | **USB Interface (DP, DM)** |
| 2.00 | Separate signal traces into similar categories and route similar signal traces together, that is, DP/DM and ULPI. |
| 2.01 | Route the USB receptacle ground pin to the analog ground plane of the device with multiple via connections. |
| 2.02 | Route the DP/DM trace pair together. |
| 2.03 | For HS-capable devices, route the DP/DM signals from the device to the USB receptacle with an optimum trace length of 5 cm. Maximum trace length 1-way delay of 0.5 ns (7.5 cm for 67 ps/cm in FR-3). |
| 2.04 | Match the DP/DM trace lengths. Maximum mismatch allowable is 150 mils (≈0.4 cm). |
| 2.05 | Route the DP/DM signals with 90 Ω differential impedance, and 22.5≈30-Ω common-mode impedance (objective is to have Zodd ≈ Z0 = Zdiff/2 = 45 Ω). |
| 2.06 | Use an impedance calculator to determine the trace width and spacing required for the specific board stack up being used. |
| 2.07 | Keep the maximum possible distance between DP and DM signals from the other platform clocks, power sources and digital or analog signals. |
| 2.08 | Do not route DP/DM signals over or under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use clocks. |
| 2.09 | Avoid changing the routing layer for DP/DM traces. If unavoidable, use multiple vias. |
| 2.10 | Minimize bends and corners on DP/DM traces. |
| 2.11 | When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities. |

**表 10-1. TUSB121x USB2.0 Product Family Board Layout Recommendations (continued)**

| Item | USB General Considerations |
|---|---|
| 2.12 | Avoid creating stubs on the DP/DM traces as stubs cause signal reflections and affect global signal quality. |
| 2.13 | If stubs are unavoidable, they must be less than 200 mils (≈0.5 cm). |
| 2.14 | Route DP/DM signals over continuous VCC or GND planes, without interruption, avoiding crossing anti-etch (plane splits), which increase both inductance and radiation levels by introducing a greater loop area. |
| 2.15 | Route DP/DM signals with at least 25 mils (≈0.65 mm) away from any plane splits. |
| 2.16 | Follow the 20×h thumb rule by keeping traces at least 20×(height above the plane) away from the edge of the plane ($V_{CC}$ or GND, depending on the plane the trace is over). |
| 2.17 | Changing signal layers is preferable to crossing plane splits if a choice must be made. |
| 2.18 | If crossing a plane split is completely unavoidable, proper placement of stitching capacitors can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. |
| 2.19 | Avoid anti-etch on the ground plane. |
| | **ULPI Interface (ULPIDATA<7:0>, ULPICLK, ULPINXT, ULPIDIR, ULPISTP)** |
| 3.00 | Route ULPI 12-pin bus as a 50 Ω single-ended adapted bus. |
| 3.01 | Route ULPI 12-pin bus with minimum trace lengths and a strict maximum of 90 mm, to ensure timing. (Timing budget 600 ps maximum 1-way delay assuming 66 ps/cm.) |
| 3.02 | Route ULPI 21-pin bus equalizing paths lengths as much as possible to have equal delays. |
| 3.03 | Route ULPI 12-pin bus as clock signals and set a minimum spacing of 3 times the trace width (S < 3W). |
| 3.04 | If the 3W minimum spacing is not respected, the minimum spacing for clock signals based on EMI testing experience is 50 mils (1.27 mm). |
| 3.05 | Route ULPI 12-pin bus with a dedicated ground plane. |
| 3.06 | Place and route the ULPI monitoring buffers as close as possible from the device ULPI bus (on test boards). |
| | **USB Clock (USBCLKIN, CLK_IN1, CLK_IN0)** |
| 4.00 | Route the USB clock with the minimum possible trace length. |
| 4.01 | Keep the maximum possible distance between the USB clock and the other platform clocks, power sources, and digital and analog signals. |
| 4.02 | Route the USBCLKIN, CLK_IN1 and CLK_IN0 inputs as 50 Ω single-ended signals. |
| | **USB Power Supply (VBUS, REG3V3, REG1V5, VBAT)** |
| 5.00 | VBUS must be a power plane from the device VBUS ball to the USB receptacle, or if a power plan is not possible, VBUS must be as large as possible. |
| 5.01 | Power signals must be wide to accommodate current level. |

## 10.2 Layout Guidelines

- The $V_{DDIO}$ pins of the TUSB1210 supply 1.8 V (nominal) power to the core of the TUSB1210. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The $V_{BAT}$ pin of the TUSB1210 supply 3.3 V (nominal) power rail to the TUSB1210. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The $V_{BUS}$ pin of the TUSB1210 supply 5 V (nominal) power rail to the TUSB1210. This pin is normally connected to the $V_{BUS}$ pin of the USB connector.
- All power rails require 0.1 μF decoupling capacitors for stability and noise immunity. The smaller decoupling capacitors should be placed as close to the TUSB1210 power pins as possible with an optimal grouping of two of differing values per pin.

## 10.3 Layout Example

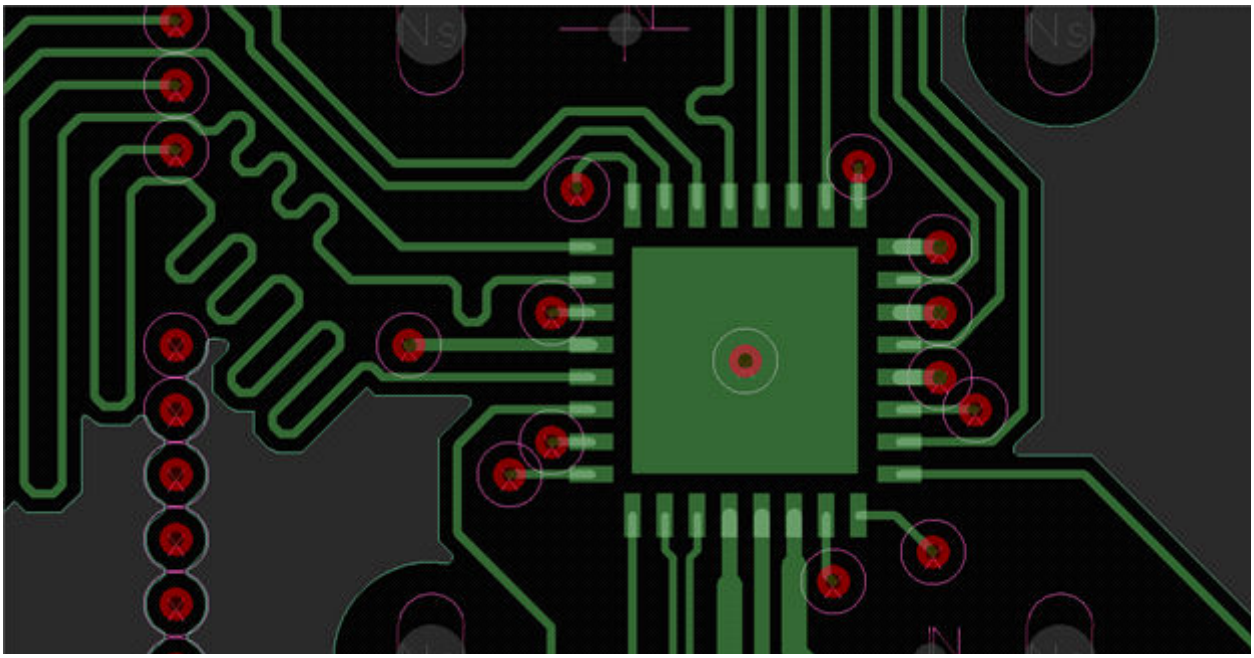


**图 10-1. TUSB1210 Layout Example**

# 11 Device and Documentation Support

## 11.1 Device Support

## 11.2 Documentation Support

SLLZ066 ***Silicon Errata.*** Describes the known exceptions to the functional specifications for the TUSB1210-Q1.

### 11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TUSB121x USB2.0 Board Guidelines* application report

## 11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TUSB1210BRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | T1210B | Samples |
| TUSB1210BRHBT | ACTIVE | VQFN | RHB | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | T1210B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF TUSB1210 :**

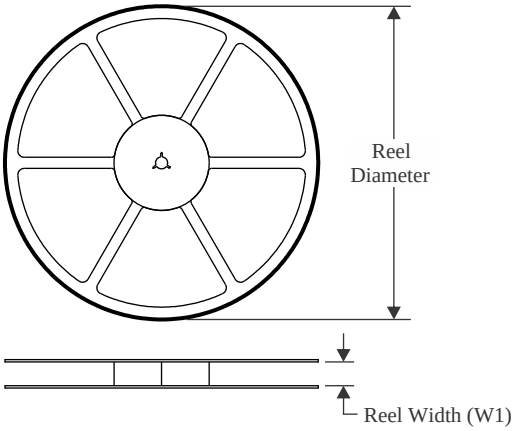
- Automotive : TUSB1210-Q1

NOTE: Qualified Version Definitions:

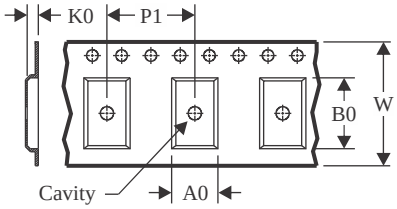
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

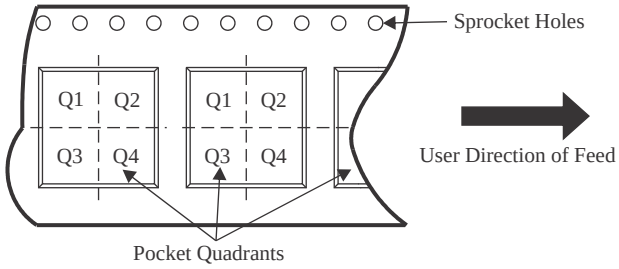



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

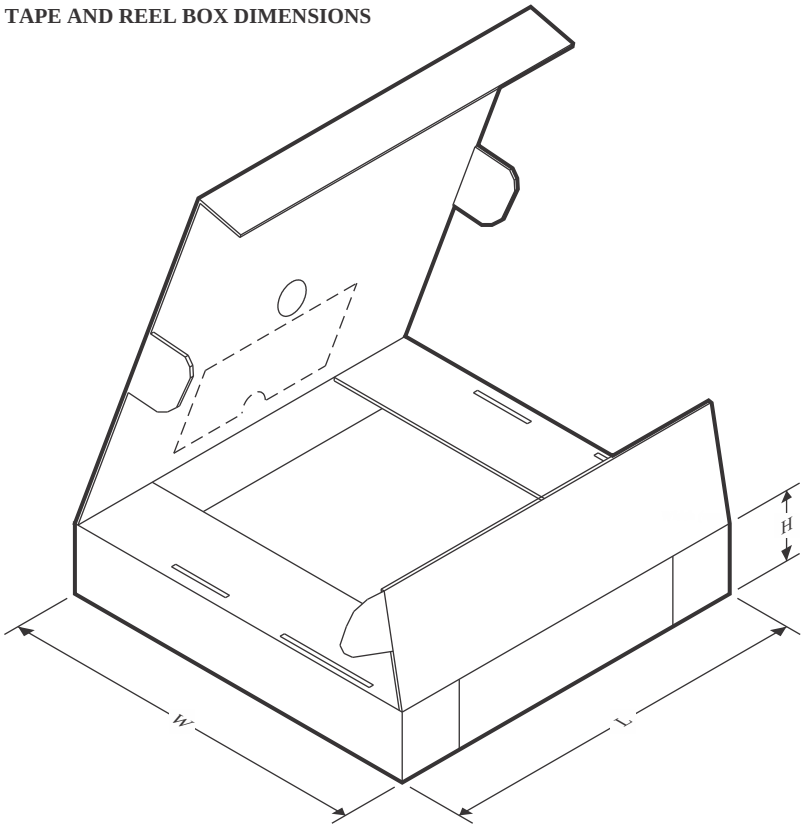
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TUSB1210BRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TUSB1210BRHBT | VQFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TUSB1210BRHBR | VQFN | RHB | 32 | 3000 | 346.0 | 346.0 | 33.0 |
| TUSB1210BRHBT | VQFN | RHB | 32 | 250 | 182.0 | 182.0 | 20.0 |

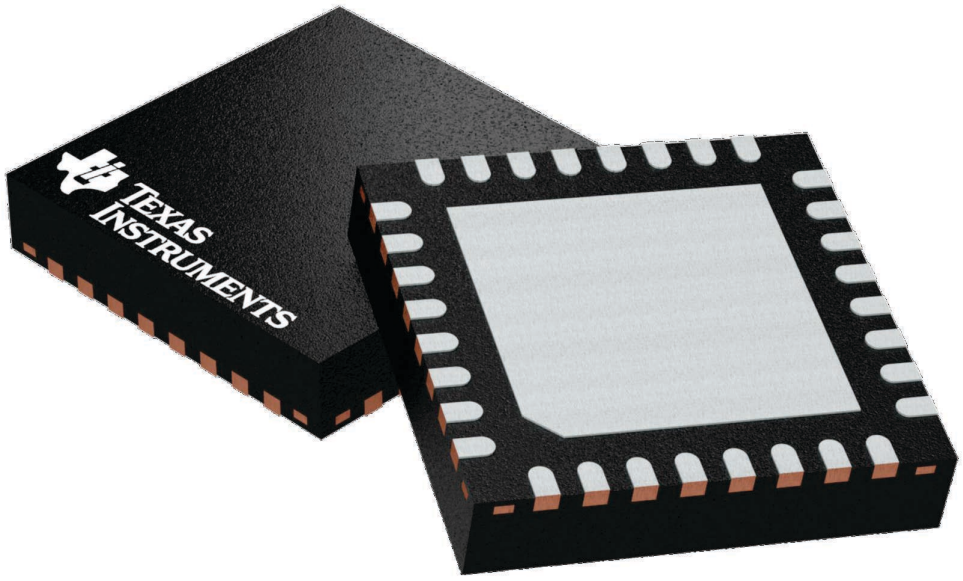
# GENERIC PACKAGE VIEW

## RHB 32

## VQFN - 1 mm max height

**5 x 5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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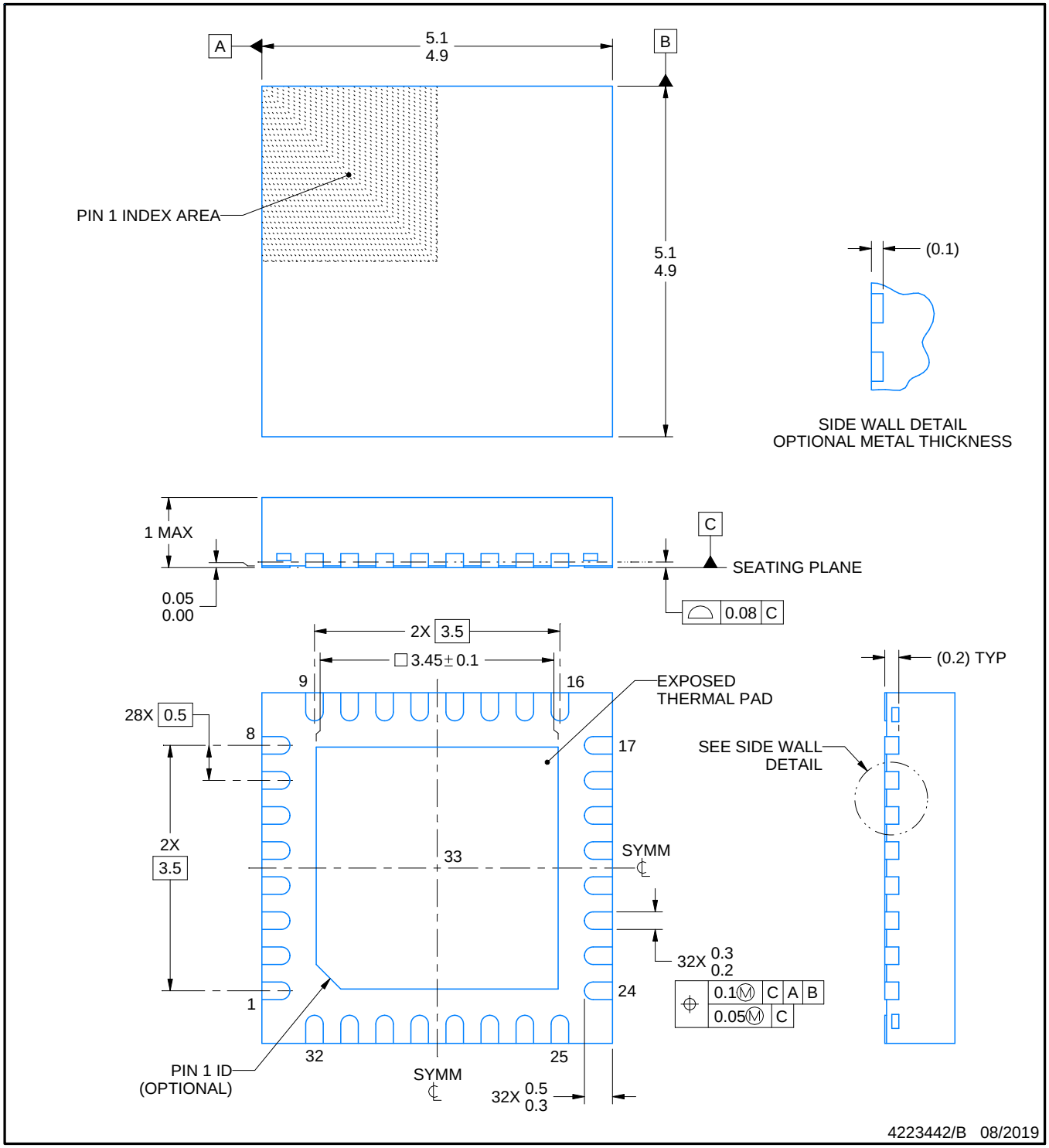
# RHB0032E

# PACKAGE OUTLINE

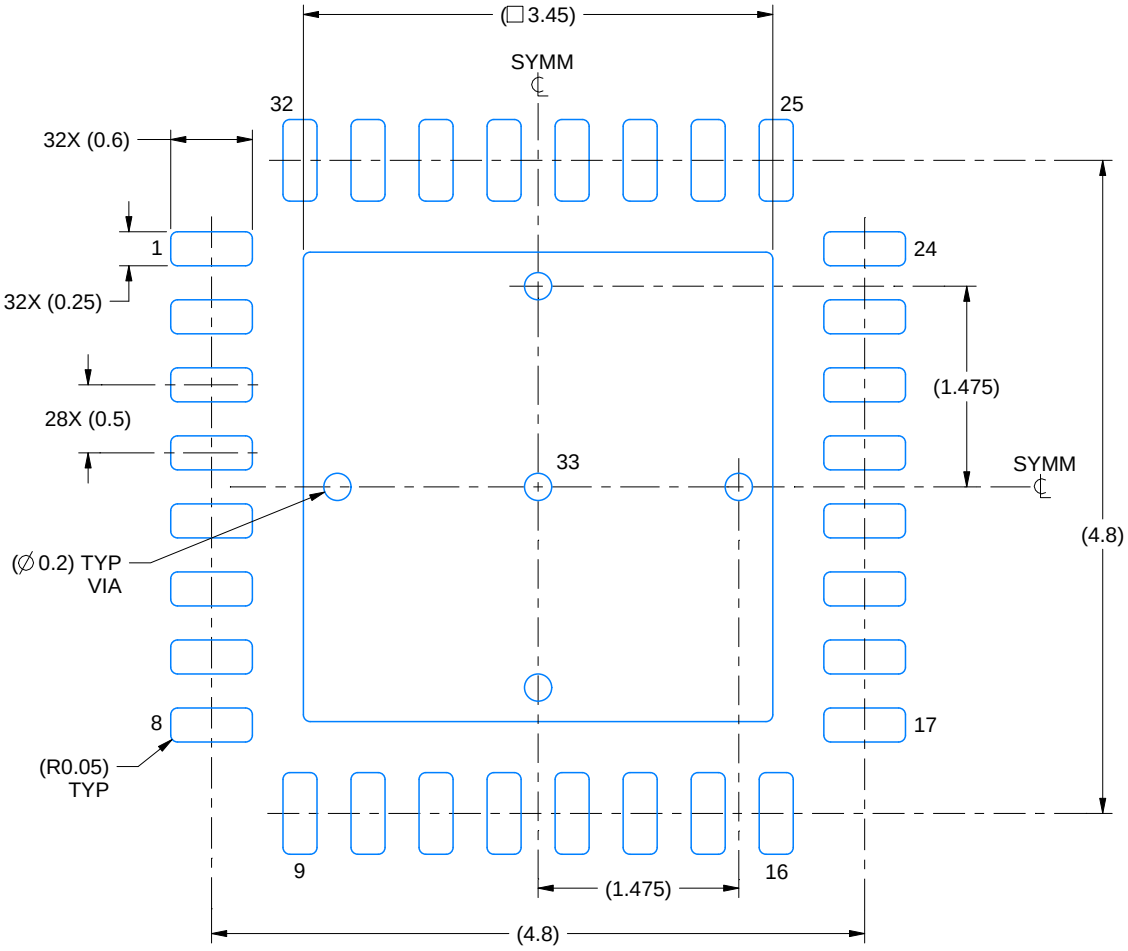
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

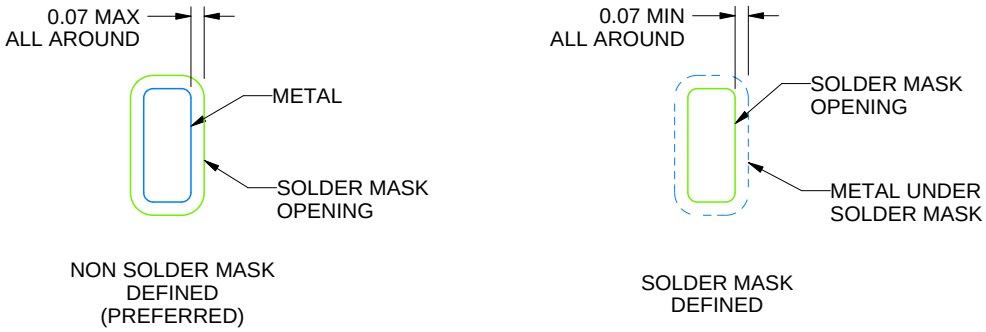



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:18X




SOLDER MASK DETAILS

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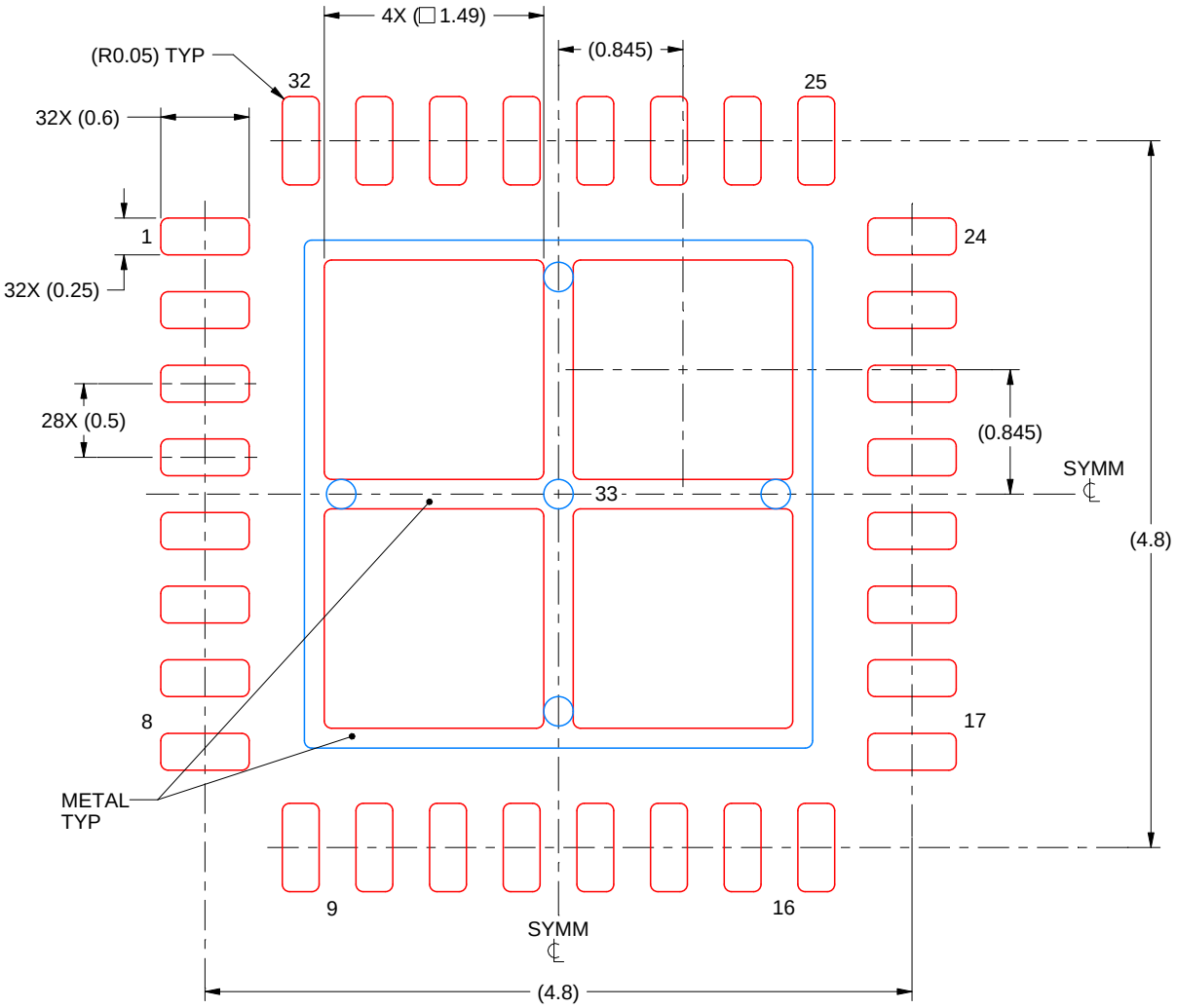
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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